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Average Model-Based Feedforward and Feedback Control for PUC5 Inverter

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ABSTRACT This paper proposes new average model based control strategies for a 5-level Packed U-cell (PUC5) inverter in both standalone and grid-connected modes of operation. First, a simple feedforward controller (FFC) is designed, using only two pulse width modulation (PWM) carrier signals, for the PUC5 inverter operating in standalone mode. This proposed control technique ensures self-balanced operation with high steady-state performance. Moreover, the employment of the proposed FFC leads to a decrease in the capacitor's value as well as the minimization of the Total Harmonic Distortion (THD). Then, a feedback linearizing control technique is designed to improve the transient and steady-state performances. In grid-connected mode, a reduced-sensor technique based on the FFC and the state feedback (FC) techniques was applied. Simulations and experimental results are presented to prove the high performance of the proposed solutions for standalone and grid-connected operating modes.

INDEX TERMS Packed U-cell inverter, PUC5, self-balancing, average model, feedback linearizing, feedforward control, power quality.

I. INTRODUCTION

Recently, multilevel inverters (MLIs) have become very popular in renewable energy applications due to their high conversion performance and low harmonics content [1]–[5]. This growth is mainly due to the latest developments of power semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) that are enabling a new generation of power semiconductor devices [6]. Several topologies have been proposed to achieve a good compromise between system performance and complexity. The mostly used MLIs in the literature are cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitors (FC) inverters [7]–[11]. The performance of these inverters is directly related to the number of generated output voltage levels. However, the increase of output voltage levels is generally associated with the increase in components count, which leads to a higher cost and implementation complexity.

Recently, the Packed U-cell (PUC) inverter has emerged as an alternative MLI topology showing additional advantages compared to the existing topologies, such as allowing the generation of higher numbers of output voltage levels with a relatively reduced number of components. The PUC topology consists of cascaded power cells, where each cell is composed of two bidirectional switches and one capacitor.

The PUC was firstly introduced with its 7-level version (PUC7), where the 7-level output voltage could be achieved by regulating the capacitor voltage at one-third of the DC source voltage ($V_c = E/3$) [12]–[14]. However, this configuration lacks of redundant switching states resulting in a loss of capacitor voltage controllability [15], [16]. This limitation could be overcome with the introduction of the 5-level version of the inverter (PUC5) in [16], [17], where the capacitor voltage is regulated at half of the DC source voltage $V_c = E/2$. Though this new configuration allows generating only five levels of output voltage, it gives the converter full controllability by taking advantage of the switching redundancies and proper control.

Several methodologies have been proposed in the literature to control the PUC5 inverter. Some of the proposed techniques have achieved the balancing of the capacitor voltage without the use of feedback loop (feedforward techniques). The first solution was proposed in [16] by applying a phase disposition pulse width modulation

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(PDPWM). This technique uses four level-shifted carriers and switching state table. However, this trend shows a major drawback because it requires a large capacitor in order to stabilize the voltage across the capacitor. The reason is that the charge and discharge cycles of the PUC5 capacitor in [16] depend on the fundamental frequency. To overcome this problem, another control strategy was proposed in [18]. This strategy uses only two level-shifted triangular carriers and six logic gates. The charging and discharging cycles of the capacitor depend on the switching frequency, which helped to reduce the size of the capacitor. However, this technique is characterized with high complexity and rise of computational burden. To the best of authors' knowledge, the idea to control both capacitor voltage and output current using state feedback through the average model of the PUC5 inverter has not been discussed yet in the literature.

Thus, this paper proposes a solution with new average model based control strategies for the PUC5 inverter operating in standalone and grid-connected modes. First, a simple feedforward control (FFC) technique using only two phase-shifted PWM carriers is applied to achieve the balancing of the capacitor voltage [19]–[21]. The proposed control strategy is characterized by its simplicity, significant effect on the decrease of the capacitor size, and contribution in improving the output power quality (lower THD). In addition, the proposed controller shows a noticeable improvement in the output current spectrum resulting in a decrease of the filter size compared to the control strategy proposed in [16], [18]. The presented results are characterized by a high-quality steady-state tracking and slow transient dynamics. Thus, a nonlinear feedback controller (FC) is proposed to improve the transient performance (fast capacitor voltage charging/discharging) and the tracking of the desired values.

This paper in organized as follows. In Section II, the PUC5 topology is introduced and the modeling steps are detailed. In Section III, an FFC strategy is developed based on the average model of the PUC5 inverter. In Section IV, a FC design is presented. The simulation and experimental results are reported in Section V. Finally, the conclusions and the main contributions of this work are outlined in Section VI.

II. PUC5 TOPOLOGY AND MODELING

A. TOPOLOGY OVERVIEW

The single-phase PUC5 converter topology is depicted in Fig. 1. This converter is composed of three cells: DC source cell ($E, S_1, \bar{S_1}$), the capacitor cell ($C, S_2, \bar{S_2}$), and a third cell consisting of two packing switches S_p, $\bar{S_p}$ having the role of alternating between the positive and negative signals of the output voltage. The switching function is defined by:

$$S_i = \begin{cases} 1 & if\ S_i\ is\ open \\ 0 & if\ S_i\ is\ closed \end{cases} \quad (1)$$

where $i \in (p, 1, 2)$. Eight switching state patterns could be identified from this topology. The corresponding output voltages for each state are listed in Table 1. At first glance,

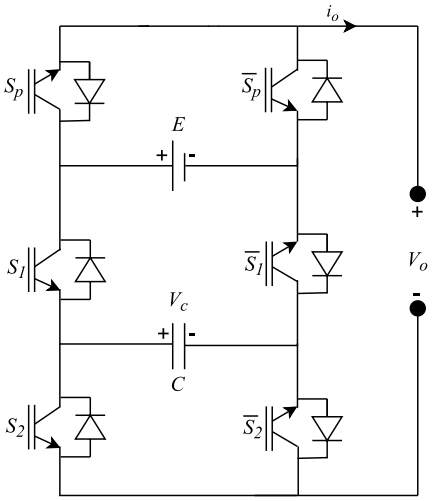


FIGURE 1. The PUC inverter topology.

TABLE 1. Output voltage levels and capacitor voltage dynamics for the 8 switching states.

State	S_p	S_1	S_2	V_o	ΔV_c	
					$i_o > 0$	$i_o < 0$
1	1	0	0	E	0	0
2	1	0	1	$E - V_c = \frac{E}{2}$	+	−
3	1	1	0	$V_c = \frac{E}{2}$	−	+
4	1	1	1	0	0	0
5	0	0	0	0	0	0
6	0	0	1	$-V_c = -\frac{E}{2}$	−	+
7	0	1	0	$V_c - E = -\frac{E}{2}$	+	−
8	0	1	1	$-E$	0	0

it can be noticed that the PUC topology shown is capable of generating a seven-level output voltage. This can be achieved by regulating the capacitor voltage at $E/3$. This configuration will maximize the output voltage levels (7-levels, namely $\pm E, \pm 2E/3, \pm E/3, and 0$), where 0 is a redundant state. However, the 7-level configuration suffers from uncontrollability issues (the controllability can be lost in some configurations where the capacitors are bypassed). On the other hand, if the capacitor voltage is regulated at $E/2$, the PUC inverter will generate 5-levels ($\pm E, \pm E/2, and\ 0$), where both 0 and $\pm E/2$ are redundant switching states. These redundant states have an important effect on the full controllability of the inverter as it can be seen by the dynamics of the capacitor voltage ΔV_c given in Table 1, where +, −, and 0 represent the charging, discharging and bypass of the capacitor C, respectively.

B. MATHEMATICAL MODELING

The PUC5 converter is classified as a Variable Structure System (VSS) where the control input signals are binary. The average model of the PUC5 inverter is used in this paper by

considering the averaged control signals. Therefore, if the actual control signal is $s(t)$, its T-average is given by:

$$u(t) = \frac{1}{T}\int_{t-T}^{T} s(\tau)d\tau \tag{2}$$

where T is the averaging period. The switching signal $s(t)$ can be generated from $u(t)$ by Pulse Width Modulation (PWM). Applying the Kirchhoff's laws, the average dynamical model of the PUC5 inverter is expressed by:

$$\begin{aligned} C\frac{dV_c(t)}{dt} &= i_o(t)(u_2 - u_1) \\ V_o &= E(u_p - u_1) + V_c(t)(u_1 - u_2) \\ L\frac{di_o(t)}{dt} &= V_o - V_x \end{aligned} \tag{3}$$

where

E: DC voltage
V_c: capacitor voltage
V_o: output voltage
i_o: output current
L: grid/load inductor
C: cell capacitor

where u_1, u_2 and u_p are the T-average inputs, which stand for the duty cycles of the switches s_1, s_2 and s_p. V_x represents the $R * i_o$ voltage in the standalone case and the grid voltage V_g in the grid-connected case.

III. FEEDFORWARD CONTROL DESIGN

In this section, an FFC technique is proposed for the PUC5 inverter. The aim is to generate adequate switching patterns in order to track a given output voltage reference while ensuring the balancing of the capacitor voltage. The proposed design is depicted in Fig. 2. It's worth noting that the proposed FFC does not require any feedback. Based on the average model of the PUC5 inverter, the control strategy is designed by the application of only two phase-shifted triangular carriers. From Table 3, it can be noticed that the switch S_p toggles between 1 and 0 according to the sign of the output voltage reference V_o^*. Therefore, u_p is equivalent to S_p and expressed by:

$$u_p = \begin{cases} 1 & V_o^* \geq 0 \\ 0 & V_o^* < 0 \end{cases} \tag{4}$$

At steady-state, $\frac{dV_c}{dt} = 0$, and $V_o = V_o^*$. Thus:

$$\begin{aligned} i_o(t)(u_2 - u_1) &= 0 \\ E(u_p - u_1) + V_c(t)(u_1 - u_2) &= V_o^* \end{aligned} \tag{5}$$

This yields to:

$$u_1 = u_2 = u_p - \frac{V_o^*}{E} \tag{6}$$

where $\frac{V_o^*}{E} = MIsin(\omega t)$ and MI is the modulation index.

It is worth noting that the above equation will only conserve the initial capacitor voltage and is not sufficient to control V_c and V_o to their references. However, by using two triangular carriers phase-shifted by π between u_1 and u_2, V_c can be regulated to its reference $E/2$ from any initial condition. The natural balancing mechanism of the PUC5 inverter can be proved by the first-harmonic model of the inverter, which is similar to the multi-cell neutral balance analytic presented in [22].

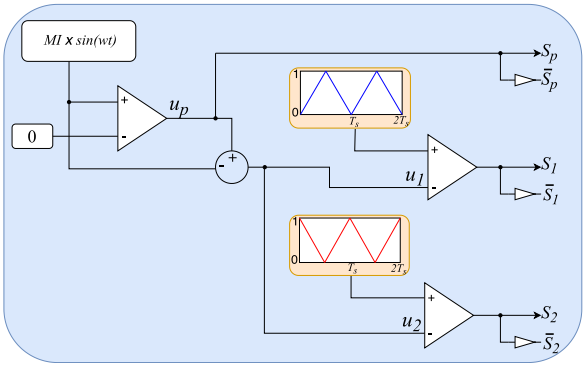


FIGURE 2. Synoptic of the proposed feedforward control.

IV. FEEDBACK CONTROL DESIGN

The motivation of the FC is to design a stabilizing control law that combines the PWM control technique (optimal steady-state) and a linearizing PI control strategy (fast transient, robustness). To achieve this goal, a feedback function that controls both V_c and i_o to their references is designed through a dual-loop concept. The first loop generates the output voltage reference V_o^* through the measurement of the output current i_o and its reference i_o^*. The role of the second loop is used to calculate the control inputs u_1 and u_2 in terms of the actual value of the capacitor voltage V_c, the reference V_c^*, and the output voltage reference V_o^* generated by the first loop.

A. FIRST LOOP

From 3-(c), and using the actual and reference values of the output current, the reference of the output voltage V_o^* is determined by:

$$\frac{di_o}{dt} = \frac{V_o^*}{L} - \frac{V_x}{L} = \omega_1 \tag{7}$$

which yields

$$V_o^* = V_x + L\omega_1 \tag{8}$$

where ω_1 is a Proportional-Integral (PI) action of the form

$$\omega_1 = \frac{di_o^*}{dt} + K_p(i_o^* - i_o) + K_i\int(i_o^* - i_o)dt \tag{9}$$

Hence, the inclusion of the derivative of the current reference $\frac{di_o^*}{dt}$ in the PI controller will help to increase the convergence speed to any current amplitude reference.

B. SECOND LOOP

Here, the control input signals u_1 and u_2 are defined by controlling the variable V_c and V_o. As the system is square

(number of controls equals to the number of states). The system can be linearized through the state feedback as follows:

$$\begin{aligned} \frac{dV_c}{dt} &= \frac{i_o}{C}(u_2 - u_1) = \omega_2 \\ (u_p - u_1)E + v_c(u_1 - u_2) &= V_o^* \end{aligned} \tag{10}$$

where ω_2 is a PI controller of the form

$$\omega_2 = K_p(V_c^* - V_c) + K_i \int (V_c^* - V_c)dt \tag{11}$$

u_1 and u_2 are deduced from (10) and calculated in terms of V_o^* and ω_2 as follows:

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} -\frac{i_o}{C} & \frac{i_o}{C} \\ v_c - E & -v_c \end{bmatrix}^{-1} \begin{bmatrix} \omega_2 \\ V_o^* + Eu_p \end{bmatrix} \tag{12}$$

The synoptic of the proposed FC strategy is depicted in Fig. 3.

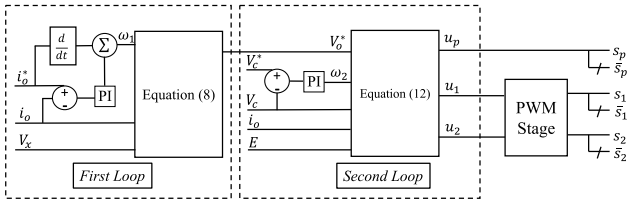


FIGURE 3. The proposed feedback control.

C. CONTROL PARAMETERS DESIGN

Substituting ω_1 and ω_2 in (7) and (10) by their respective expressions given by (9) and (11) yields to:

$$\dot{e} + K_p e + K_i \int e\, dt = 0 \tag{13}$$

where e represents the vector composed of the output current and the capacitor voltage errors. The Laplace transformation of (13) leads to a second-order system characterized by K_p and K_i, where the designed parameters are as follows:

$$\begin{aligned} K_p &= 2\xi\omega_n \\ K_i &= w_n^2 \end{aligned} \tag{14}$$

where ξ is the damping ratio equal to 0.707 and ω_n is the natural frequency which satisfies the $2\omega_n < \omega_s$ constraint, ω_n is chosen equal to $\omega_n = \frac{\omega_s}{5}$, where ω_s is the PWM angular frequency in rad/s.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed FFC and FC schemes are presented in Fig. 2 and Fig. 3 respectively. In order to prove the performance of the proposed techniques, simulation and experimental validations have been performed through MATLAB/SIMULINK environment and using a dSPACE 1103 platform as depicted in Fig. 4. The system parameters are listed in Table 2.

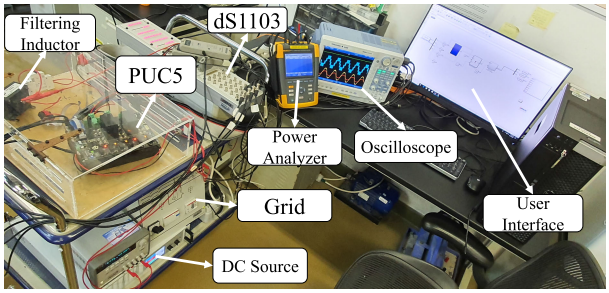


FIGURE 4. Experimental setup of the PUC5 inverter.

TABLE 2. System parameters.

Parameters	Values
Stand-Alone	
DC-link voltage E	$200V$
Fundamental frequency f	$50Hz$
PUC5 capacitor C	$100\mu F$
RL Load	$R = 40\Omega, L = 10mH$
Carrier frequency f_{cr}	$2KHz$
Grid-Connect	
Grid voltage (rms) V_g	$115V$
Grid inductance L_g	$L_g = 2mH$

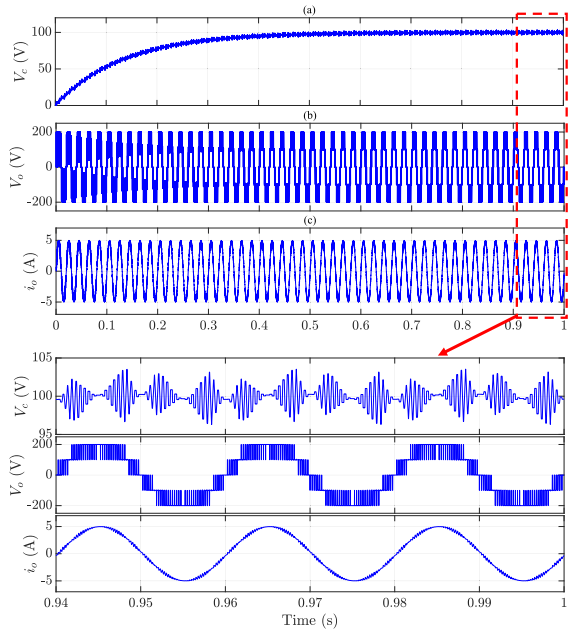


FIGURE 5. Simulation results showing the transient and steady-state performance of the FFC in standalone mode: (a). Capacitor voltage, (b). Output voltage, (c). Load current.

A. STANDALONE MODE VALIDATION

1) FEEDFORWARD CONTROL

The proposed FFC scheme presented in Fig. 2, is validated through simulation and experimental investigations on the studied PUC5 inverter.

TABLE 3. Comparative study between the ffc scheme and existing techniques.

	Computational Burden			Power Quality		
	Number of PWM timers (Carriers)	Number of If- Else loops	Number of logic gates	Capacitor voltage ripple	Output voltage THD	Load current THD
Controller [16]	4	6	6	±54%	29.76%	9.79%
Controller [23]	4	12	0	±54%	30.21%	9.75%
Controller [18]	2	0	6	±3%	25.71%	3.4%
Proposed Controller	2	0	0	±3%	25.61%	3.39%

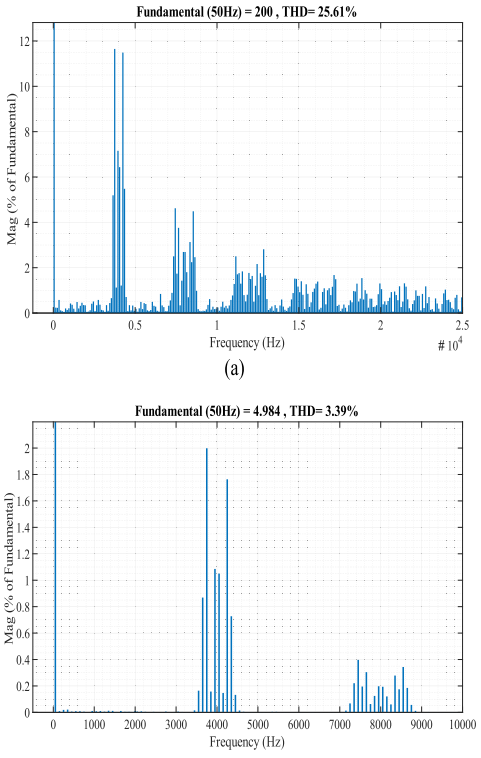


FIGURE 6. Simulated FFT analysis: (a). Output voltage, (b). Load current.

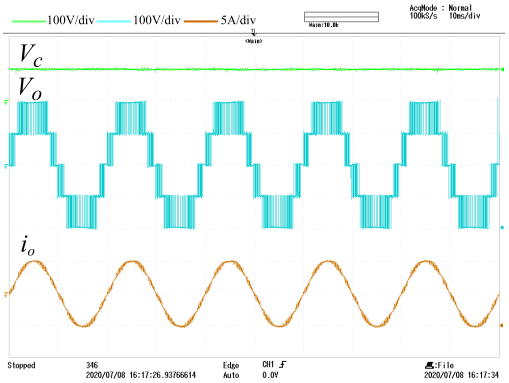


FIGURE 7. Experimental results showing the steady-state performance of the FFC in standalone mode.

a: SIMULATION RESULTS

Fig. 5 shows the transient and steady state waveform of the capacitor voltage, output voltage, and load current. It is clear that the self-balancing of the capacitor voltage is achieved

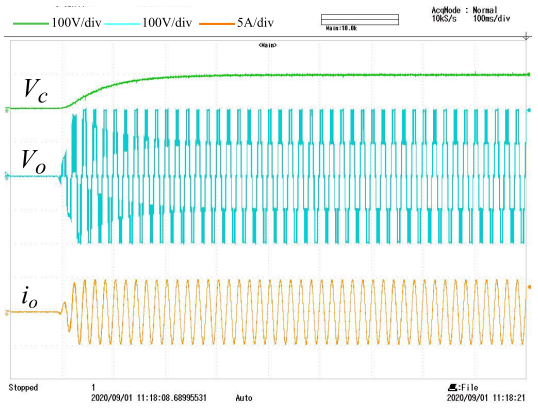


FIGURE 8. Experimental results showing the transient and steady-state performance of the FFC in standalone mode.

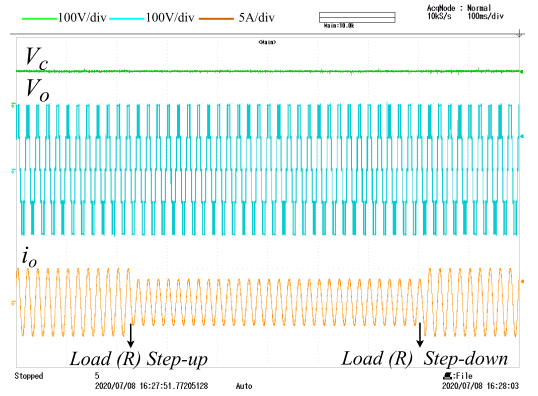


FIGURE 9. Experimental results showing the dynamic performance of the FFC in standalone mode under load resistor change.

with small ripples ($\pm 3V$). This is due to the dependence between the charging and discharging cycles of the capacitor voltage and the switching frequency. The FFT analysis of the output voltage V_o and output current i_o are presented in Fig. 6. The load current THD is 3.39% while the output voltage THD is 25.61%.

A comparative study between the proposed FFC scheme and three existing control techniques, which were used to achieve the self-balanced operation of the PUC5 inverter, is reported in Table 3 (the same parameters listed in Table 2 have been used for all modulation techniques). The controller 1 reported in [16] uses four level-shifted carriers and a switching state table. Controller 2 uses four phase-shifted carriers in [23]. The third controller was proposed in [18] and uses two

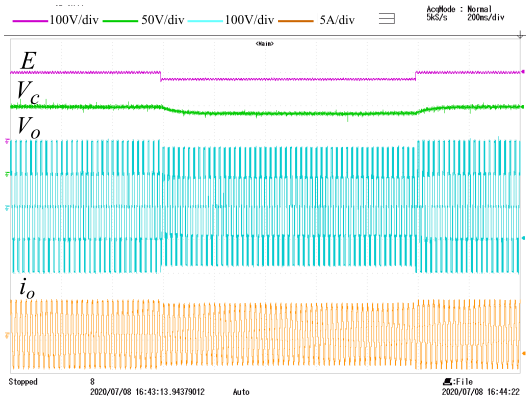


FIGURE 10. Experimental results showing the dynamic performance of the FFC in standalone mode under DC source voltage change.

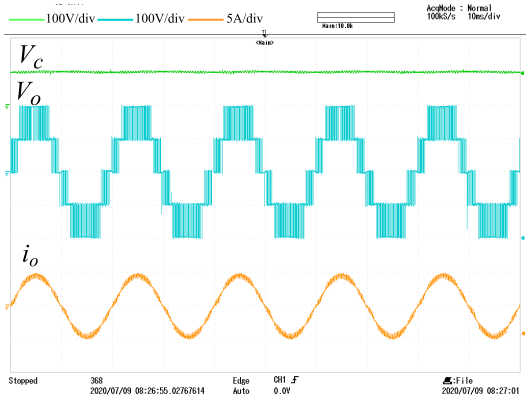


FIGURE 11. Experimental results showing the dynamic performance of the FFC in standalone mode for $MI = 0.9$.

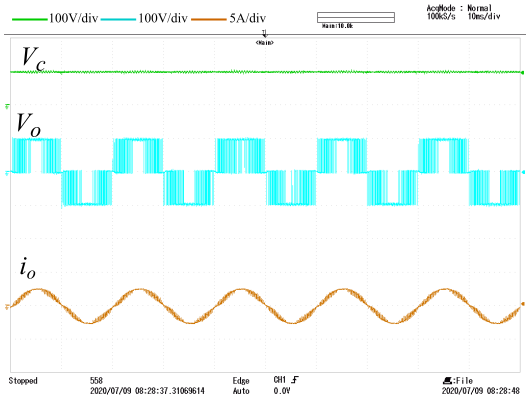


FIGURE 12. Experimental results showing the dynamic performance of the FFC in standalone mode for $MI = 0.5$.

level-shifted carriers and logic gates. According to Table 3, the proposed strategy shows higher performance in terms of capacitor voltage ripples, load current THD, and controller complexity compared to [16] and [23]. Moreover, though the method presented in [18] shows a similar performance, it suffers from higher computational burden and system complexity.

b: EXPERIMENTAL RESULTS

Fig. 7 shows the experimental steady-state results of the proposed FFC. Similar to the simulation results, the capacitor

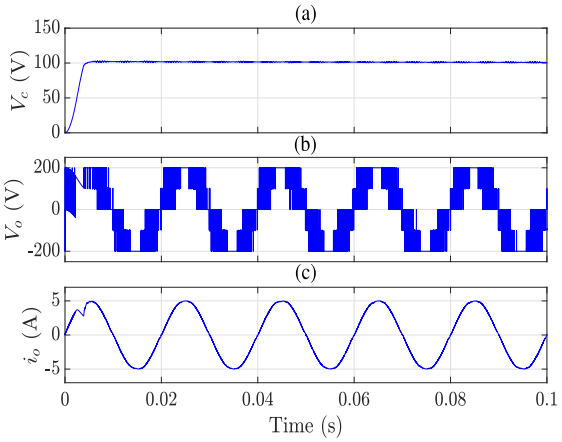


FIGURE 13. Simulation results showing the transient and steady-state performance of the FC in standalone mode.

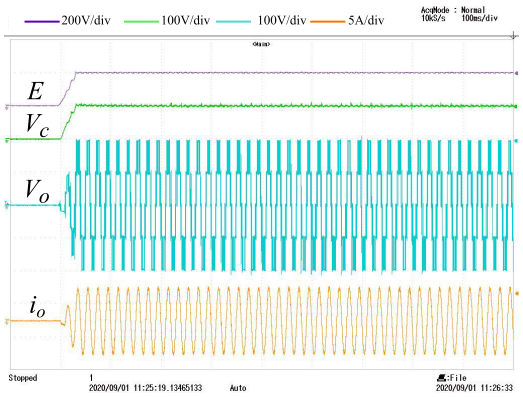


FIGURE 14. Experimental results showing the transient and steady-state performance of the FC in standalone mode.

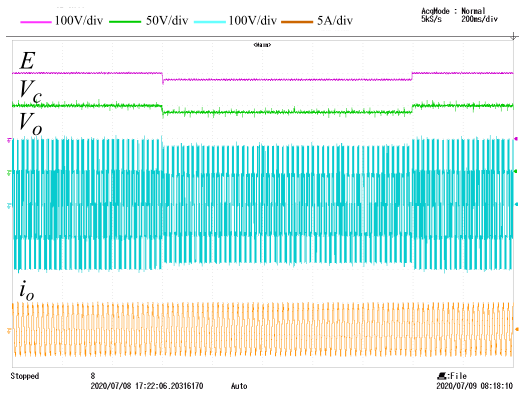
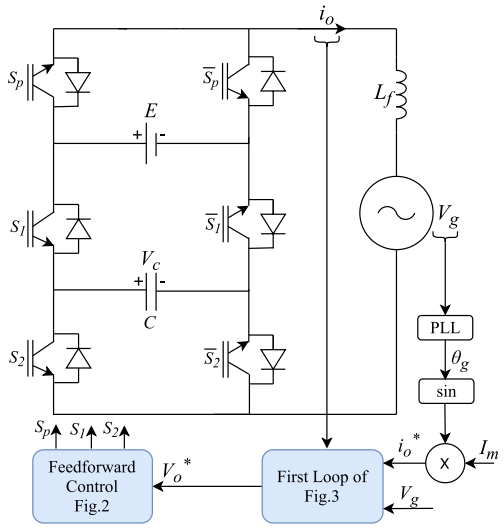
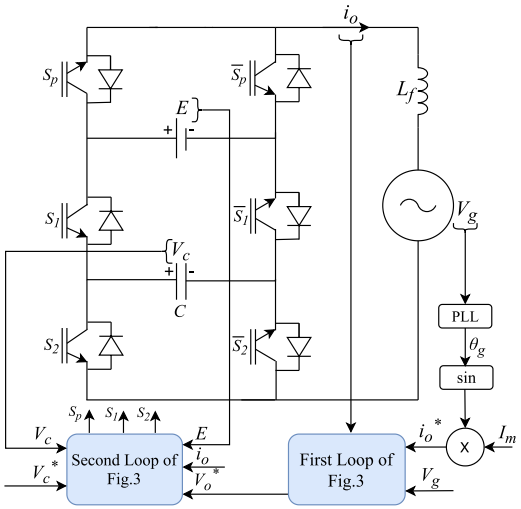


FIGURE 15. Experimental results showing the dynamic performance of the FC under DC source voltage change.

voltage self-balancing is achieved with very small ripples. The load current tracks its reference with low harmonic content. The FFT analysis using the power analyzer shows high quality harmonic spectrum with a current THD of 1.1%. Fig. 8 shows the transient of the PUC5 inverter. In order to further assess the dynamic performance of the proposed FFC, two dynamic tests have been performed.



(a) Reduced sensor control



(b) Feedback control

FIGURE 16. Grid-connected PUC5 converter controllers.

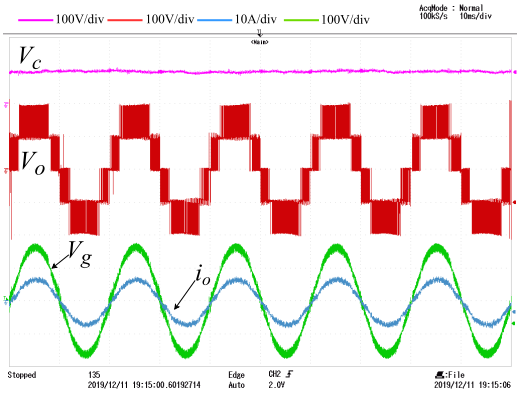


FIGURE 17. Experimental results showing the steady-state performance of the reduced-sensor control in grid-connected mode.

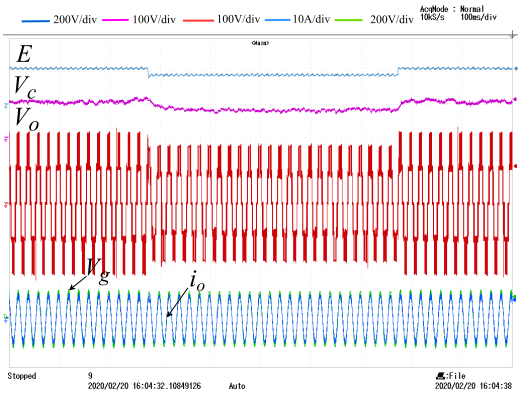


FIGURE 18. Experimental results showing the dynamic performance of the reduced-sensor control in grid-connected mode and under DC source voltage change.

The first test is performed with varying the load resistor (load current variation) as depicted in Fig. 9. The second one is performed with applying a step up/down change on the DC source voltage (E) as shown in Fig. 10. It is clear that the capacitor voltage keeps tracking its reference $E/2$ in both cases in a stable manner (although with no feedback). Moreover, a performance evaluation of the proposed FFC technique was performed under different operating conditions. Fig. 11 and Fig. 12 present the performance results under modulation index $MI = 0.9$ and $MI = 0.5$, respectively. One can notice that the self-balancing of the capacitor voltage can be obtained at a wide range of modulation indexes, by simply performing an appropriate phase-shift of the two carrier signals.

2) FEEDBACK CONTROL

a: SIMULATION RESULTS

Fig. 13 depicts the transient and steady-state performances of the capacitor voltage, output voltage, and load current. It is worth noting that the capacitor voltage is reaching its reference value of $E/2$, from the zero initial condition, in a very short time compared to the results shown in Fig. 5 for the FFC.

b: EXPERIMENTAL RESULTS

Fig. 14 illustrates the experimental results showing the transient and steady-state performance of the FC in controlling the PUC5 inverter in standalone mode. From the presented results it is clear that the capacitor voltage converges from the zero initial condition to its reference in a short time without any overshot and with low steady-state error. Another test was made by applying a step-down/up change on the DC source voltage (Fig. 15). This figure shows that the capacitor voltage re-tracks rapidly its reference $E/2$. These results prove the high dynamic performance of the proposed FC in standalone mode.

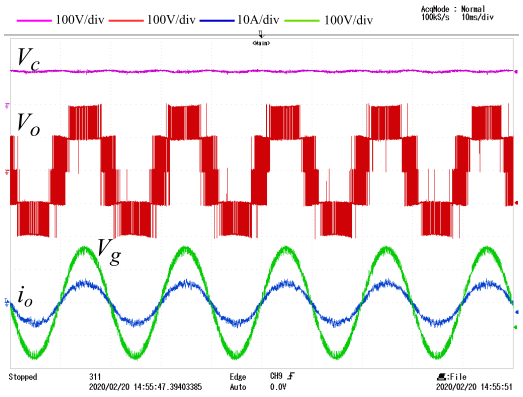


FIGURE 19. Experimental results showing the steady-state performance of the FC in grid-connected mode.

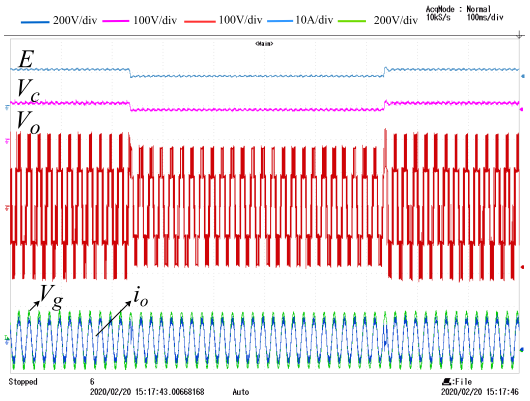


FIGURE 20. Experimental results showing the dynamic performance of the FC in grid-connected mode and under DC source voltage variation.

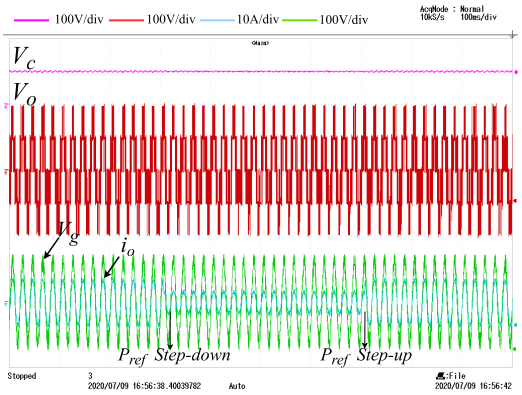


FIGURE 21. Experimental results showing the dynamic performance of FC in grid-connected mode during active power change.

B. GRID-CONNECTED MODE

1) REDUCED-SENSOR CONTROL

The reduced-sensor control strategy is illustrated in Fig. 16-(a). The controller combines the first loop of the FC with FFC controller using only the measurement of the grid current and a phase-locked loop (PLL) in order ensure the grid synchronization. Fig. 17 presents the experimental results showing the performance of the proposed reduced-sensor strategy in controlling the PUC5 inverter in grid-connected mode. The upper part of the figure shows the capacitor voltage tracking around the reference value. The middle part shows the 5 voltage levels generated at the output terminal, whereas the lower part of the figure shows the synchronization of the grid current with the grid voltage ($\theta_g = 0$). Moreover, an additional test was performed by applying a DC voltage change. As it can be seen in Fig. 18, the capacitor voltage keeps tracking the new reference values using the reduced-sensor technique. However, even though the reduced-sensor approach seems to be more attractive in terms of cost due to the fact that it uses less sensors, Fig. 18 presents an erratic oscillation on the capacitor voltage. This is due to the active nature of the grid (exchange of energy with the grid). Therefore, the performance of the FC will be investigated in the following subsection for comparison purposes.

2) FEEDBACK CONTROL

The synoptic of the proposed FC scheme is shown in Fig. 16-(b). Fig. 19 illustrates the capacitor voltage, output voltage and the injected grid current. As it can be seen, the injected current waveform is kept in phase with grid voltage (unity power factor) while maintaining the capacitor voltage around its reference value. The FFT analysis of the injected current shows a low THD of 2.9%. Moreover, a DC source voltage change was applied to verify the performance of the proposed FC controller in tracking the voltage reference of the capacitor. As illustrated in Fig. 20, the capacitor voltage tracks its reference of $E/2$ with high accuracy and fast response. From Fig. 20, it can be clearly seen that the capacitor voltage ripples are lower compared to the reduced-sensor control while the erratic behavior shown in Fig. 18 has vanished using the proposed FC. An additional test was performed by varying the injected active power as illustrated in Fig. 21. The presented results prove the effectiveness of the proposed FC in balancing the capacitor voltage and injecting a sine-wave current to the grid with low THD.

VI. CONCLUSION

This work presented novel control strategies for the PUC5 inverter operating in both standalone and grid-connected modes. At a first stage, feed-forward control (FFC) was used to provide self-balancing operation of the PUC5 inverter by an appropriate selection of phase-shift between two carrier signals. The obtained current and voltage waveforms are characterized by a high-quality steady-state and slow dynamic tracking. Therefore, a nonlinear feedback control (FC) was designed to improve the transient and steady-state performances. Simulations and experimental results were provided to validate the proposed techniques. The presented results clearly show the effectiveness of both methods in maintaining a balanced capacitor voltage with high performance in tracking the reference current.

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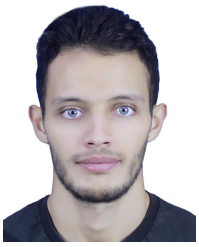

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