IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received August 26, 2020, accepted September 13, 2020, date of publication September 21, 2020,
date of current version September 30, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3024769

Charged Controlled Mem-Element Emulator and Its Application in a Chaotic System

PANKAJ KUMAR SHARMA[1], (Graduate Student Member, IEEE), RAJEEV KUMAR RANJAN[1], (Member, IEEE), FABIAN KHATEB[2,3], AND MONTREE KUMNGERN[4]

[1]Department of Electronics Engineering, IIT (ISM) Dhanbad, Dhanbad 826004, India
[2]Department of Microelectronics, Brno University of Technology, 60190 Brno, Czech Republic
[3]Faculty of Biomedical Engineering, Czech Technical University in Prague, 3105 Kladno, Czech Republic
[4]Department of Telecommunications Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand

Corresponding author: Fabian Khateb (khateb@feec.vutbr.cz)

This work was supported by the King Mongkut's Institute of Technology Ladkrabang under Grant KREF026201.

ABSTRACT This article proposes a charged controlled emulator model for memristor and memcapacitor using second-generation Current Conveyor (CCIIs) and Analog Multiplier (AM). The grounded and floating mem-element circuits have been designed using two CCIIs and one multiplier in addition to some passive components. The grounded type of design requires three resistors and three capacitors while floating design necessitates only two resistors and two capacitors. With the help of a switch, the proposed design can be easily switched into a memristor or memcapacitor. The proposed emulator model has been theoretically analyzed and simulated in PSpice to substantiate the effectiveness and accuracy. The practicability of the circuit has been established using commercially available ICs AD844AN and AD633JN. Non-linear characteristics of the proposed memristor emulator have been used to design a chaotic system.

INDEX TERMS Memristor, memcapacitor, pinched hysteresis loop, Chua's circuit.

I. INTRODUCTION

With the advancement in VLSI technology, demand for high speed and low power technology has increased manifold. One of the major challenges in designing nanoscale transistors is the design of gates. As the gate size decreases, it becomes difficult to control the current flow through a thin channel. In 2008, Strukov and his team at HP Lab [1] developed a working memristor using Titanium Dioxide (TiO_2), a fourth fundamental passive element of the circuit after the resistor, capacitor and inductor which were earlier predicted by Leon Chua in 1971 [2] in his paper 'The Missing Memristor Found.' He found the missing relationship between charge and magnetic flux. After the discovery of memristor, the notion of passive memory device is not limited to memristor and has further extended to the memcapacitor and meminductor by Di Ventra *et al.* in 2009 [3]. The memcapacitor can possibly be the most valuable and novel segment on account of its efficacy and dynamic semblance to the memristor. Memcapacitor gives a pinched hysteresis loop in charge and voltage plain as current and voltage in the case of a memristor. Similarly, meminductor depicts pinched hysteresis behaviour in the current-flux plan, where it acts as a memory device. Since these elements store the past value of their input signals, pinched hysteresis loops are generated when bipolar inputs are applied to these elements.

The attributes of the pinched hysteresis loop are unique in these mem-elements, which enable them to be used as non-volatile memories. Although these mem-elements have the potential for memory applications, they are not expected to appear soon due to difficulties of fabrication with current technologies. Therefore, the utilization of emulators would be an alternative solution to develop application circuits. In fact, some research groups have proposed many emulator circuits for memristor and memcapacitor. Kim *et al.* proposed a memristor emulator using off-the-shelf solid-state devices in 2012 [4], who, later in 2015, extended its experimental results for the replacement of real memristor [5]. Some researchers have recommended a memristor emulator based on operational amplifiers [4], [6]. However, an operational amplifier based emulator has many shortcomings like low linearity, large supply voltage, small voltage fluctuation, and

The associate editor coordinating the review of this manuscript and approving it for publication was Di He.

limited operating frequency. These drawbacks can be overcome using current mode circuits. These circuits have a better performance than voltage-mode circuits in terms of speed, dynamic range, bandwidth, slew rate, high linearity, and better accuracy. They require less operating voltage than voltage-mode circuits, thus enabling them to produce higher current swing at less supply voltage, and resulting in reduced distortion. Due to better performance than voltage-mode circuits in terms of operating speed, CMOS current-mode circuits have grabbed the attention of the industry [7]. The results illustrate considerable progress in current-mode analog signal processing, multiprocessors, telecommunication systems, instrumentation, computer interfaces with high speed. In complex electronic systems, various current mode building blocks have been reported.

The second-generation Current Conveyor (CCII), which is the basic current mode building block, is used to design emulator model for the memcapacitor. In 2014, Lopez *et al.*, have proposed CCII based floating memristor emulator [8]. However, the proposed memristor emulator is a flux-controlled model that is different from real charged controlled HP-memristor. In [9], [10], Ranjan *et al.*, have advocated a memristor emulator that uses only one kind of an element. In 2010, Krems *et al.*, had built a memcapacitor using solid-state materials i.e. nano-pores [11]. Under this, when ions are allowed to enter nano-pores and an electric field is subjected across the material, memcapacitive behaviour is observed. In 2010, Biolek *et al.*, proposed SPICE modeling of memcapacitor [12] followed by behavioral modeling in [13]. In this modeling, width of the dielectric is controlled by the charge flowing through it. However, this model cannot be used for practical circuits. Mutators were developed for transforming memristor to memcapacitor or meminductor in [14]–[19]. However, the properties of these memcapacitor depend upon the used memristor which uses excessive components. Memristor-less Memcapacitor circuits were introduced in [20]. Vista and Ranjan had proposed a simple charge controlled floating memcapacitor emulator using Dual X current conveyor differential input transconductance amplifier (DXCCDITA) [21]. In 2018, Babacan *et al.*, proposed OTA based memcapacitor and meminductor [22]. [23], [24] includes applications based on memcapacitor. Yu *et al.*, recommended a memcapacitor based relaxation oscillator in 2016 [23]. In 2018, Feali *et al.*, implemented adaptive neuron based on memristor and memcapacitor [24]. Vista and Ranjan proposed MOSFET based floating memristor [25]. Rajagopal *et al.*, proposed a hyper-chaotic memcapacitor oscillator with infinite equilibrium and co-existing attractors [26]. In 2020, Raj *et al.*, proposed memristor based hyper chaotic system [27]. Voltage-tunable fully balanced voltage differencing buffered amplifier (FB-VDBA) based memristor emulator was presented by Yadav *et al.*. in 2019 [28]. Yesil *et al.*, had proposed an electronically tunable memristor using only one voltage differencing current conveyor (VDCC) [29]. In 2019, a universal emulator was proposed by Zhao *et al.*, for memristor, memcapacitor, and meminductor and its chaotic circuit [30].

In this article, a charged controlled switch-based mem-element emulator has been proposed. With the help of switches, a mode for memristor and memcapacitor can be selected. Proposed circuit, as shown in Fig. 1, first acts as a grounded mem-element emulator. It requires two CCIIs, one Multiplier, three resistors, three capacitors, and three switches. The second proposed circuit is depicted in Fig. 2 acting as floating mem-element emulator. It requires two CCIIs, one Multiplier, two resistors, two capacitors, and two switches. Proposed emulators are charged controlled and can be easily shifted to incremental and decremental modes using a simple switch. Effectiveness and precision of the proposed emulator model are theoretically analyzed and simulated in PSpice. The practicability of the circuit is experimentally verified. Chaotic system has been designed using floating type memristor emulator as part of an application of proposed emulator. Chua's diode is replaced with floating memristor for realization of chaotic circuit. Chua's diode and memristor both exhibit non-linear properties. The negative resistance in Chua's circuit is realized using IC3080.

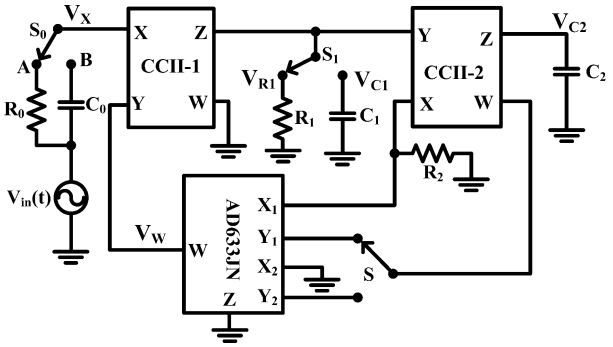

FIGURE 1. Grounded Charged Controlled Mem-Element Emulator.

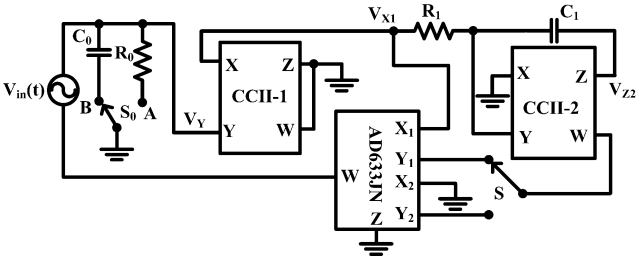

FIGURE 2. Floating Charged Controlled Mem-Element Emulator.

II. MATHEMATICAL MODEL OF CHARGED CONTROLLED EMULATOR

The mathematical relations of mem-element are realized by analyzing the relationships among current (i), charge (q), voltage (v), and flux (φ). Charge (q) and flux (φ) are the time integral of the current I ($q = \int_{t_0}^{t} i(\tau)d\tau$) and the voltage v ($\phi = \int_{t_0}^{t} v(\tau)d\tau$), respectively.

The memristance $M\,(q)$, can be defined as:

$$v\,(t) = M\,(q)\,i\,(t) = a.i\,(t) - b.q\,(t)\,.i(t) \tag{A}$$

Recently, the concept of memristor was extended to the memcapacitor (C_M) and is defined as:

$$v_C\,(t) = C_M^{-1}\,(\sigma)\,q\,(t) = a.q\,(t) - b.\sigma\,(t)\,.q(t) \tag{B}$$

where $\sigma = \int_{t_0}^{t} q(\tau)d\tau$.

Likewise, memcapacitor also shows the pinched hysteresis loop in charge-voltage plane. It acts as a memory device. Two simple dedicated mem-element emulator circuits are presented using two AD844AN blocks [31] and one AD633JN block [32]. IC AD844AN represents port relationship $V_X = V_Y$, $I_Z = I_X$, $V_W = V_Z$, $I_Y = 0$ of the second-generation Current Conveyor (CCII) whereas IC AD633JN acts as an analog multiplier. The proposed grounded mem-element is described in Section 2.A while Section 2.B takes care of a floating mem-element.

A. GROUNDED CHARGED CONTROLLED MEM-ELEMENT EMULATOR

The proposed grounded charged controlled mem-element emulator circuits are shown in Fig. 1, which consist of two CCIIs (AD844AN), one analog multiplier (AD633JN), three resistors and three capacitors. The switches S_0 and S_1 are used for memristor and memcapacitor switching. If S_0 and S_1 switches are connected to point A and V_{R1} respectively, the circuit will work as a memristor and if they are connected to point B & V_{C1} respectively, it will work like a memcapacitor. Switch S is used for incremental and decremental behaviours. When switch S is connected to Y_2 terminal and Y_1 is grounded of AD633JN, it emulates incremental behaviour, and if switch S is connected to the Y_1 terminal and Y_2 is grounded, it follows decremental behaviour.

1) GROUNDED MEMRISTOR EMULATOR AND ITS FREQUENCY ANALYSIS

For memristor operation, S_0 switch is connected to point A and S_1 switch is connected to V_{R1}. Fig. 1 displays a proposed grounded type memristor.

Input voltage can be written as:

$$V_{in}(t) = I_{in}(t)R_0 + V_x \tag{1}$$

The voltage at x terminal of CCII-2 is given as:

$$V_{R1} = -I_{in}(t)R_1 \tag{2}$$

The voltage at the Z terminal of CCII-2 is shown as:

$$V_{C2} = -\frac{R_1}{R_2C_2}q(t) \tag{3}$$

With the properties of AD633JN V_w can be written as:

$$V_w = \pm\frac{R_1^2}{10R_2C_2}I_{in}(t)q(t) \tag{4}$$

As $V_w = V_X$, substitute the value of V_X in Eqn. 1 we get,

$$V_{in}(t) = I_{in}(t)R_0 \pm \frac{R_1^2}{10R_2C_2}I_{in}(t)q(t) \tag{5}$$

From Eqn. 5, the memristance value can be written as:

$$R_M(q(t)) = R_0 \pm \frac{R_1^2}{10R_2C_2}q(t) \tag{6}$$

It is essential to note that the input signal $V_{in}\,(t)$, and the values of passive components manage the memristance value. The frequency characteristic of the presented grounded memristor circuit can be analyzed by assuming an input voltage $V_{in}\,(t) = V_m\sin\omega t$, where V_m is the amplitude, and ω is the frequency of the signal. The average input current can be calculated by substituting the time-varying part to zero in Eqn. 6. So, it is stated as:

$$I_{in}\,(t) = \frac{V_{in}\,(t)}{R_0} = \frac{V_m\sin\omega t}{R_0} \tag{7}$$

As a result, $q(t)$ can be expressed as:

$$q\,(t) = -\frac{V_m}{\omega R_0}\cos\omega t = \frac{V_m}{\omega R_0}\cos(\omega t - \pi) \tag{8}$$

By substituting equation (8) in equation (6), memristance of the circuit can be established as:

$$R_M(q(t)) = R_0 \pm \frac{R_1^2V_m}{10\omega R_0R_2C_2}\cos(\omega t - \pi) \tag{9}$$

Eqn. 9 illustrates that $R_M(q(t))$ has a linear time-invariant part and linear time-variant part. Here, the linearity is described in terms of voltage and current. The linear time-variant part is dominated by the linear time-invariant part as the frequency increases. Also, the linear curve is attained between current and voltage for higher frequencies.

2) GROUNDED MEMCAPACITOR EMULATOR AND ITS FREQUENCY ANALYSIS

S_0 switch is now changed into point B and S_1 switch is connected to V_{C1} in Fig.1 for grounded memcapacitor emulator operation.

Input voltage can be written as:

$$V_{in}(t) = \frac{q(t)}{C_0} + V_X \tag{10}$$

The voltage at x terminal of CCII-2 is given as:

$$V_{C1} = -\frac{q(t)}{C_1} \tag{11}$$

The voltage at the Z terminal of CCII-2 is written as:

$$V_{C2} = \frac{\sigma(t)}{R_2C_1C_2} \tag{12}$$

With the properties of AD633JN (used as an analog multiplier) V_w expression can be presented as:

$$V_w = \pm\frac{\sigma(t)}{10R_2C_1^2C_2}q(t) \tag{13}$$

As $V_w = V_X$, substitute the value of V_X in Eqn. 10 we get,

$$V_{in}(t) = \frac{q(t)}{C_0} \pm \frac{\sigma(t)}{10R_2C_1^2C_2}q(t) \tag{14}$$

From Eqn. 14, the mem-capacitance value can be put up as:

$$C_M^{-1}(q(t)) = \frac{1}{C_0} \pm \frac{\sigma(t)}{10R_2C_1^2C_2} \tag{15}$$

It is important to note that the memcapacitance value can be directed by an input signal $V_{in}(t)$, and the values of passive components. Frequency response can be analyzed by providing a sinusoidal input $V_{in}(t) = V_m \sin\omega t$, where V_m is the amplitude, and ω is frequency of the signal. The average stored charge can be calculated by replacing the time-varying part to zero in Eqn. 15. Therefore, it is expressed as:

$$q(t) = V_m C_0 \sin\omega t \tag{16}$$

As a result, $\sigma(t)$ can be given as:

$$\sigma(t) = \frac{V_m C_0}{\omega}\cos(\omega t - \pi) \tag{17}$$

Substituting Eqn. 17 in Eqn. 6, memcapacitance of the circuit can be written as:

$$C_M^{-1}(q(t)) = \frac{1}{C_0} \pm \frac{V_m C_0}{10\omega R_2 C_1^2 C_2}\cos(\omega t - \pi) \tag{18}$$

Eqn. 18 depicts that $C_M^{-1}(q(t))$ is having linear time-variant and linear time-invariant parts. When the frequency increases, the linear time-invariant part dominates the linear time-variant part. During this, a linear curve is achieved between the charge and the voltage for higher frequency values.

B. FLOATING CHARGED CONTROLLED MEM-ELEMENT EMULATOR

The proposed floating charged controlled mem-element emulator circuit is shown in Fig. 2, containing two CCIIs (AD844AN), one analog multiplier (AD633JN), two resistors, and two capacitors. S_0 switch is used for memristor and memcapacitor switching. If switch S_0 is connected to point A, the circuit will work as a memristor and if it is connected to point B, it will work as a memcapacitor. Switch S is used for switching incremental and decremental behaviours. When switch S is connected to the Y_2 terminal and Y_1 is grounded of AD633JN, it emulates incremental behaviour and if switch S is connected to the Y_1 terminal and Y_2 is grounded, it illustrates decremental behaviour.

1) FLOATING MEMRISTOR EMULATOR AND ITS FREQUENCY ANALYSIS

For the memristor operation, S_0 switch is connected to point A in proposed floating mem-element as shown in Fig. 2.

Input voltage can be written as:

$$V_{in}(t) = V_Y - V_W \tag{19}$$

In the case of memristor, V_Y can be put up as:

$$V_Y = R_0 i_{in}(t) = V_{X1} \tag{20}$$

The voltage at the Z terminal of CCII-2 is given as:

$$V_{Z2} = -\frac{R_0}{R_1C_1}q(t) \tag{21}$$

With the properties of AD633JN, V_w expression can be explained as:

$$V_W = \mp\frac{R_0}{10R_1C_1}i(t)\,q(t) \tag{22}$$

Substituting the value of V_Y and V_W in Eqn. 19 we get,

$$V_{in}(t) = R_0 i_{in}(t) \pm \frac{R_0}{10R_1C_1}i(t)\,q(t) \tag{23}$$

From Eqn. 23, the memristance value can be written as:

$$R_M(q(t)) = R_0 \pm \frac{R_0}{10R_1C_1}q(t) \tag{24}$$

Memristance value can be controlled by the input signal $V_{in}(t)$, and the values of passive components. For frequency analysis, let $V_{in}(t) = V_m \sin\omega t$, where V_m is the amplitude, and ω is frequency of the input signal. The average input current can be estimated by substituting the time-varying part to zero in Eqn. 24. Therefore, it is expressed as:

$$I_{in}(t) = \frac{V_{in}(t)}{R_0} = \frac{V_m \sin\omega t}{R_0} \tag{25}$$

As an effect, $q(t)$ can be expressed as:

$$q(t) = -\frac{V_m}{\omega R_0}\cos\omega t = \frac{V_m}{\omega R_0}\cos(\omega t - \pi) \tag{26}$$

By substituting Eqn. 26 in Eqn. 24, the circuit's memristance can be determined as:

$$R_M(q(t)) = R_0 \pm \frac{V_m}{10\omega R_1 C_1}\cos(\omega t - \pi) \tag{27}$$

Eqn. 27 shows that $R_M(q(t))$ contains a linear time-invariant part and a linear time-variant part. With the increase in frequency, the linear time-invariant part starts dominating the linear time-variant part. In contrast, the linear curve is obtained between current and voltage for higher frequency.

2) FLOATING MEMCAPACITOR EMULATOR AND ITS FREQUENCY ANALYSIS

For floating memcapacitor emulator operation, S_0 switch is now connected to point B as shown in Fig. 2. Input voltage can be put up as:

$$V_{in}(t) = V_Y - V_W \tag{28}$$

In the case of memcapacitor, V_Y can be written as:

$$V_Y = \frac{q(t)}{C_0} = V_{X1} \tag{29}$$

The voltage at the Z terminal of CCII-2 is given as:

$$V_{z2} = \frac{-\sigma(t)}{R_1C_0C_1} \tag{30}$$

With the properties of AD633JN, V_w expression can be shown as:

$$V_w = \mp \frac{q\,(t)\,\sigma\,(t)}{10R_0C_0^2C_1} \tag{31}$$

After substituting the value of V_Y and V_W in Eqn. 19, we get:

$$V_{in}(t) = \frac{q\,(t)}{C_0} \pm \frac{q\,(t)\,\sigma\,(t)}{10R_0C_0^2C_1} \tag{32}$$

From Eqn. 32, the memcapacitance value can be written as:

$$C_M^{-1}(q(t)) = \frac{1}{C_0} \pm \frac{\sigma\,(t)}{10R_0C_0^2C_1} \tag{33}$$

The memcapacitance value can be managed by an input signal $V_{in}\,(t)$, and the values of passive components. Frequency analysis of proposed floating memcapacitor can be studied by providing an input signal $V_{in}\,(t) = V_m \sin\omega t$, where V_m is the amplitude, and ω is frequency of the input signal. The average stored charge can be assessed by substituting the time-varying part to zero in Eqn. 33. Therefore, it is expressed as:

$$q(t) = V_m C_0 \sin\omega t \tag{34}$$

As a result, $\sigma\,(t)$ can be expressed as:

$$\sigma(t) = \frac{V_m C_0}{\omega}\cos(\omega t - \pi) \tag{35}$$

By substituting Eqn. 35 in Eqn. 33, memcapacitance of the circuit can be written as:

$$C_M^{-1}(q(t)) = \frac{1}{C_0} \pm \frac{V_m}{10\omega R_0 C_0 C_1}\cos(\omega t - \pi) \tag{36}$$

Eqn. 36 conveys that C_M^{-1}(q(t)) is having linear time-invariant and linear time-variant parts. When the frequency increases, linear time-invariant part governs the linear time-variant part. This leads to a linear curve between charge and voltage for higher values of frequencies.

III. RESULTS AND DISCUSSION

A. SIMULATION RESULTS OF GROUNDED TYPE MEMRISTOR

Pspice simulation has been performed to verify the functioning of the grounded type memristor circuit as illustrated in Fig. 1. For the grounded type memristor emulator, switch S_0 is connected to point A, and S_1 is connected to V_{R1}.

Grounded memristor behaviour is tested by providing a sinusoidal input signal with $V_m = 1.5$ V. The parameter taken for implementing grounded type memristor is as follows: $R_0 = 10$ kΩ, $R_1 = 10$ kΩ, and $R_2 = 75$ kΩ. The capacitor value C_2 is a variable that varies with the input frequency. Fig. 3 shows the pinched hysteresis loop obtained from proposed grounded memristor. The supply voltage given to CCII and analog multiplier is ± 10 V.

From Fig.3, we can deduce the following:

1) With increase and decrease in capacitor value C_2, the area of the pinched hysteresis curve decreases and increases respectively as shown in Fig. 3(a). This happens because the linear time-invariant part of the memristor is dominated by the linear time-variant part, as mentioned in Eqn. 9.
2) With an increase in frequency, the pinched hysteresis curve area decreases, and the memristor behaves like an ordinary resistor, i.e., a linear curve is observed in a current-voltage plane at higher frequencies.

Thus, simulated results are well agreed upon with a theoretical analysis as discussed in Section 2.A.1.

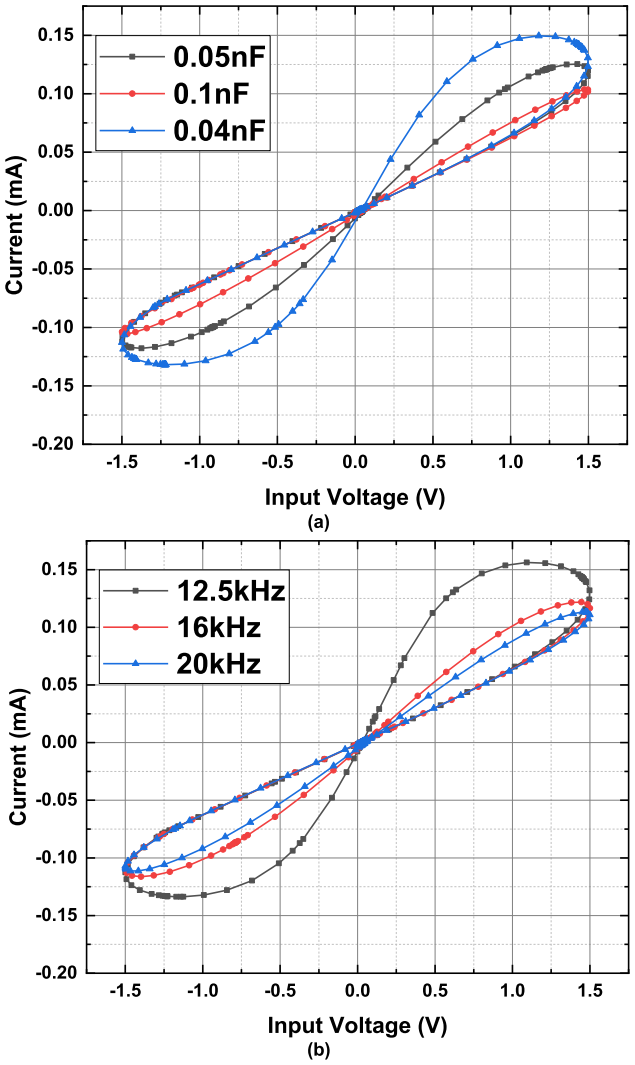

FIGURE 3. Pinched hysteresis loop of the proposed grounded memristor emulator (a) at 10 kHz with different capacitor value (b) at different frequency when capacitor value is 0.03 nF.

B. SIMULATION RESULTS OF GROUNDED TYPE MEMCAPACITOR EMULATOR

To implement a grounded type capacitor, S_0 switch is connected to point B, and S_1 switch is connected to V_{C1} as shown in Fig. 1. Pspice simulation has been performed to verify practicality of the proposed grounded capacitor. The values taken for simulation are $C_0 = 500$ nF, $C_1 = 1$ nF, and $R_1 = 75$ kΩ. The capacitor value C_2 is a variable that varies with the input frequency.

Hysteresis loop for memcapacitor is obtained by providing a sinusoidal input signal with $V_m = 1.5$ V. The supply voltage given to CCII, and an analog multiplier is ± 10 V. Fig. 4 displays the pinched hysteresis loop obtained at different frequencies. The capacitor voltage is taken at C_1.

From Fig.4, we receive two observations:

1) With increase and decrease in capacitor value C_2, the pinched hysteresis curve area decreases and increases respectively. This happens because the linear time-invariant part of the memcapacitor is dominated by the linear time-variant part, as mentioned in Eqn.18.
2) With an increase in frequency, the pinched hysteresis curve area decreases, and the memcapacitor behaves like an ordinary capacitor, i.e., a linear charge-voltage curve is observed at higher frequencies.

Thus, simulated results are well agreed upon with a theoretical analysis, as discussed in Section 2.A.2.

C. SIMULATION RESULTS OF FLOATING TYPE MEMRISTOR EMULATOR

Floating type memristor emulator is acquired by attaching S_0 switch to point A as shown in Fig. 2. Pspice simulation has been executed to verify functioning of the proposed floating type memristor circuit. The parameter values taken for simulation are $R_0 = 10$ kΩ, and $R_2 = 50$ kΩ. The capacitor value C_1 is a variable that varies with the input frequency.

Floating memristor emulator hysteresis behaviour is tested by providing a sinusoidal input signal with $V_m = 1.5$ V. The supply voltage given to CCII and an analog multiplier is ± 10 V. Fig. 5 demonstrates the pinched hysteresis loop obtained at different frequencies and capacitor values.

From Fig. 5, we can easily ascertain that with an increase in frequency, the hysteresis loop becomes narrower. Besides, we can study that with reduction of the capacitor C_1, the hysteresis loop becomes wider. The above two observations are well agreed upon with Eqn. 27, as discussed in Section 2.B.1. It can be observed that some offset are present in the simulation results. However, these offsets are because of the nonlinearity and tracking error of the building blocks CCII and Analog Multiplier. However, these can be reduced by using the offset reduction method.

D. SIMULATION RESULTS OF FLOATING TYPE MEMCAPACITOR

Pspice simulation has been conducted to validate the proposed floating memcapacitor emulator circuit obtained by connecting S_0 switch to point B as given in Fig. 2. $C_0 = 15$ nF, and $R_1 = 50$ kΩ are taken for simulation. Capacitor value C_1 is a variable that varies with the input frequency. The input sinusoidal with $V_m = 1.5$ V has been provided to obtain hysteresis behaviours. Supply voltage is given to CCII and analog multiplier is ± 10 V. Fig. 6 shows the pinched hysteresis loop obtained at different frequencies. The capacitor voltage is taken at C_0. Fig.6 displays that when capacitor value C_1 increase or decreases, the pinched hysteresis curve area decreases and increases respectively, and as the frequency increases, the pinched hysteresis curve area decreases, i.e., a linear charge-voltage curve is observed at a higher frequency. The above two observations are well agreed upon with Eqn. 36 as discussed in Section 2.B.2.

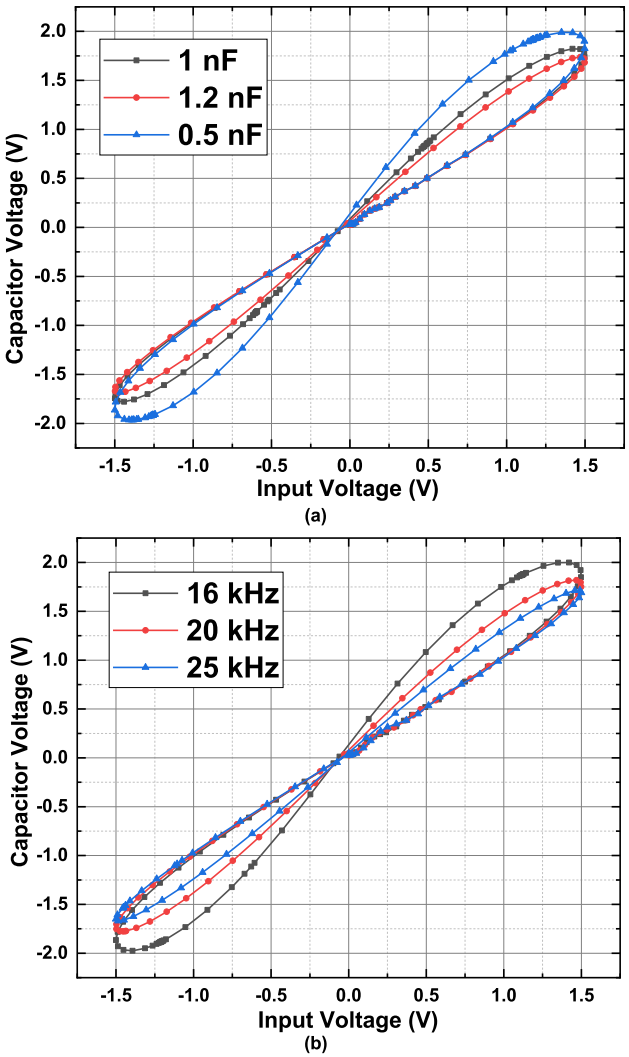

FIGURE 4. Pinched hysteresis loop of proposed grounded memcapacitor emulator at (a) at 10 kHz with different capacitor value (b) at different frequency when capacitor value is 0.4 nF.

IV. NON-VOLATILITY TEST

A critical feature of the mem-element emulator circuit is its non-volatility, i.e., the emulator circuit should retain its value when no input signal is applied. To test the non-volatility of the proposed memristor shown in Fig. 2, an input pulse train has been applied. The input pulse has 1.5 V amplitude with 25 μ sec duration and 175 μ sec pulse period. During the simulation, other parameters of the memristor emulator were considered with $R_0 = 10$ kΩ, $R_1 = 50$ kΩ, and $C_1 = 5$ nF.

Fig. 7 shows the memristance value and applied input pulse voltage with respect to time. One can observe that there is no alteration in memristance during the off period of an applied

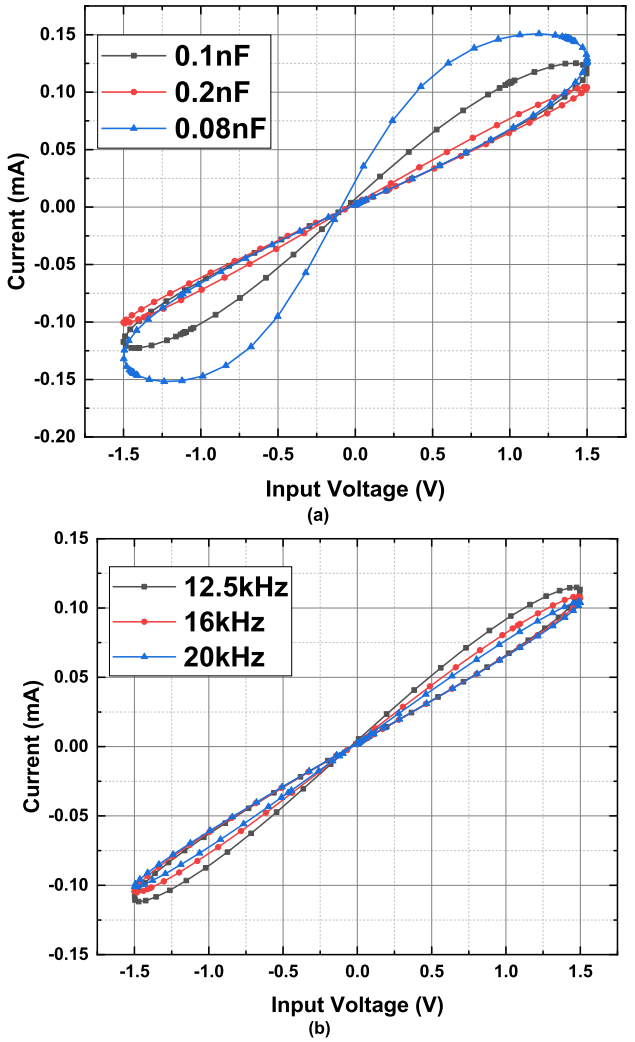

FIGURE 5. Pinched hysteresis loop of the proposed floating memristor emulator (a) at 10 kHz with different capacitor value (b) at different frequency when capacitor value is 0.1 nF.

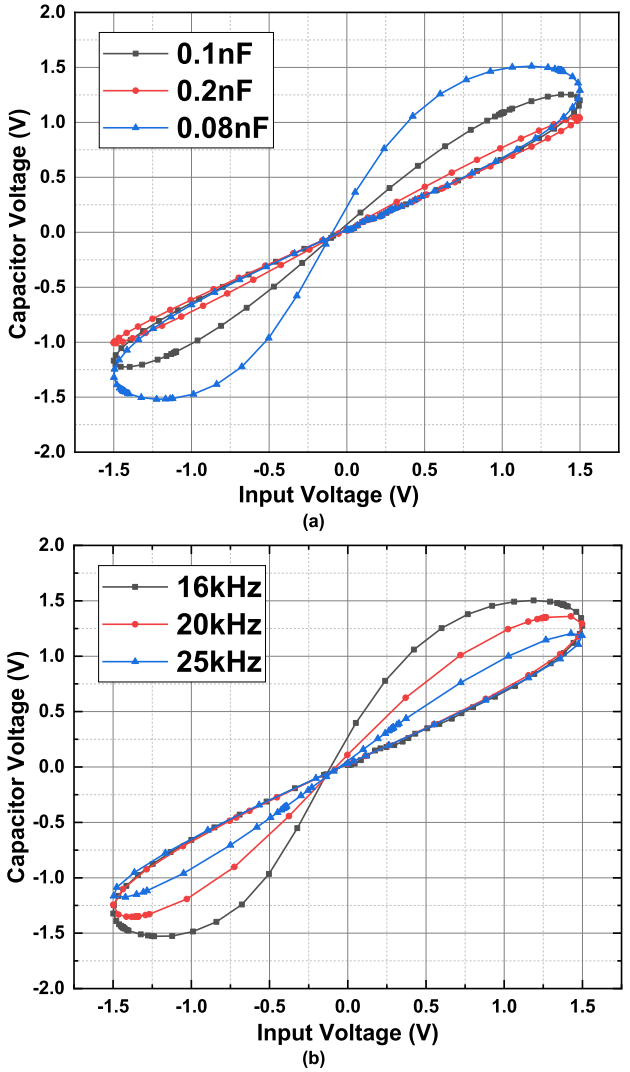

FIGURE 6. Pinched hysteresis curve of proposed floating memcapacitor emulator (a) at 10 kHz with different frequency, and (b) at different frequency when capacitor value is 0.05nF.

input pulse. During the pulse period, there is an abrupt change in voltage, so the proposed emulator shows a non-volatile nature.

V. COMPARISON TABLE

A comparative study of the proposed mem-element emulator with an existing mem-element emulator has been undertaken in Table 1.

From the table, it can be observed that,

- Unlike circuits proposed in [14], [16] and [18] whose memcapacitor properties depend upon the memristor, the proposed grounded and the floating circuit is designed without using a memristor.
- Memristor, Memcapacitor, and Meminductor proposed in [19] was independent. But it uses more active and passive component along with op-amp and varactor diode (V_D).
- Universal emulator for memristor, memcapacitor, and meminductor proposed in [30] required 5 CCIIs, one analog multiplier, one voltage buffer along with 7 passive components for floating configuration.

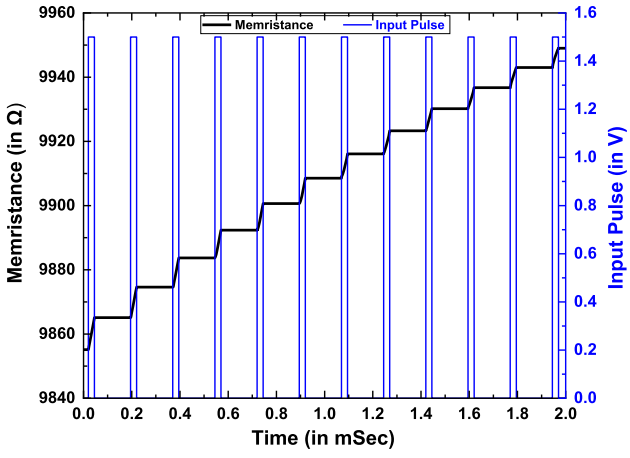

FIGURE 7. Variation of Memristance with Time for a given Pulse.

TABLE 1. Comparison of proposed circuits with previously existing work.

Ref. No.	Type of Mem-Element	No. of active components	No. of passive components	Floating/ Grounded
[6]	Memristor Only	4 CCIIs, 1 Multiplier, 1 Op-amp	8R, 1C	Floating
[14]	Memcapacitor	2 CCIIs, 1MR	1R, 1C	Floating
	Meminductor	2 CCIIs, 1MR	1R, 1L	Floating
[16]	Memristor (MR)	4 CCIIs, 1 Multiplier, 1 Op-amp	7R, 1C	Floating
	Memcapacitor	3 CCIIs, 3 TOAs, 1MR	3R, 1C	Floating
	Meminductor	3 CCIIs, 3 TOAs, 1MR	3R, 1C	Floating
[18]	Memristor (MR)	1 CBTA, 1 Multiplier	2R, 1C	Grounded
	Memcapacitor	1 CBTA, 1 MR	1C	Grounded
	Meminductor	1 CBTA, 1 MR	1C	Grounded
[19]	Memristor (MR)	4 CCIIs, 1 Op-amp	5R, 3C, 1V_D*	Floating
	Memcapacitor	4 CCIIs, 1 Op-amp	6R, 2C, 1V_D*	Floating
	Meminductor	4 CCIIs, 1 Op-amp	6R, 2C, 1V_D*	Floating
[21]	Memcapacitor Only	1DXCCDITA	1R, 2C	Floating
[22]	Memcapacitor	1 OTA	2C	Floating
	Meminductor	1 OTA	1R, 1C, 1L	Floating
[29]	Memristor Only	1 VDCC, 2 PMOS	1C	Grounded
[30]	Memristor, Memcapacitor Meminductor	2 CCIIs, 1 Multiplier	Five Discrete Components (R/C)	Grounded
[30]	Memristor, Memcapacitor Meminductor	5 CCIIs, 1 Multiplier, 1 Op-amp	Seven Discrete Components (R/C)	Floating
Fig. 1	Memristor,	2 CCIIs, 1 Multiplier	3R, 1C	Grounded
	Memcapacitor	2 CCIIs, 1 Multiplier	1R, 3C	Grounded
Fig. 2	Memristor,	2 CCIIs, 1 Multiplier	2R, 1C	Floating
	Memcapacitor	2 CCIIs, 1 Multiplier	1R, 2C	Floating

* V_D = Varactor diode

This proposed design involved only 2CCIIs, one analog multiplier, and 4 passive components. Also, in [30] the hysteresis loop is limited up to 5 kHz, but in the proposed emulator, it is obtained up to 20 kHz.

VI. EXPERIMENTAL VERIFICATION FOR MEMRISTOR AND MEMCAPACITOR EMULATOR

It is important to verify the performance and simulation results of the proposed memristor and memcapacitor emulator experimentally. Therefore, a prototype circuit of mem-element is assembled using commercially available ICs i.e. AD844AN and AD633JN. An input voltage $V_{in} = 0.8\sin(20000\pi t)$ is used to verify the mem-element emulator. The other parameters for experimental testing of emulator are configured same as kept during simulation. The supply voltage of ICs is ± 10 V.

Fig. 8 and Fig. 9 depict a pinched hysteresis loop obtained at 10 kHz for grounded memristor and grounded memcapacitor, respectively. In Fig. 8, the input voltage vs. resistive voltage (V_{R1}) is plotted as V_{R1} reflecting input current. In Fig. 9, the input voltage is plotted against the capacitor voltage (V_{C1}), which is reflecting the charge.

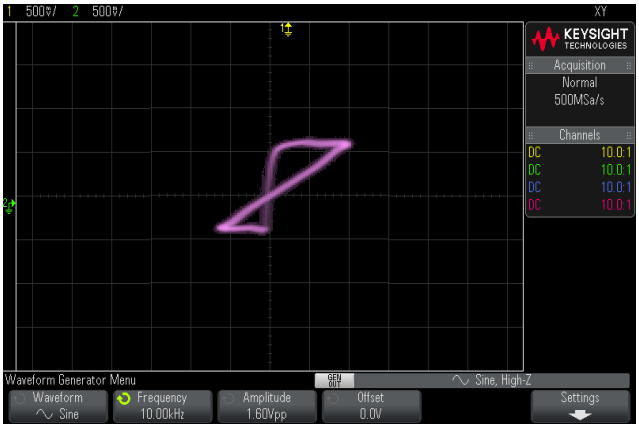

FIGURE 8. Breadboard Implemented a Pinched Hysteresis Loop obtained at 10 kHz for Grounded Memristor.

FIGURE 9. Breadboard Implemented a Pinched Hysteresis Loop obtained at 10 kHz for Grounded Memcapacitor.

In Fig. 10, the experimental and simulation results for floating memcapacitor have been compared at 10 kHz operating frequency. The experiment has been carried out by supplying input voltage $V_{in} = 1.5\sin(20000\pi t)$. The other passive parameters value are kept the same as in simulation. The experimental and simulation.csv data are obtained from digital storage oscilloscope and Pspice simulation, respectively. The.csv data are transferred and plotted in Origin 2019b.

VII. APPLICATION

In this section, we have realized a non-linear Chua's oscillator system using a charged controlled memristor as presented

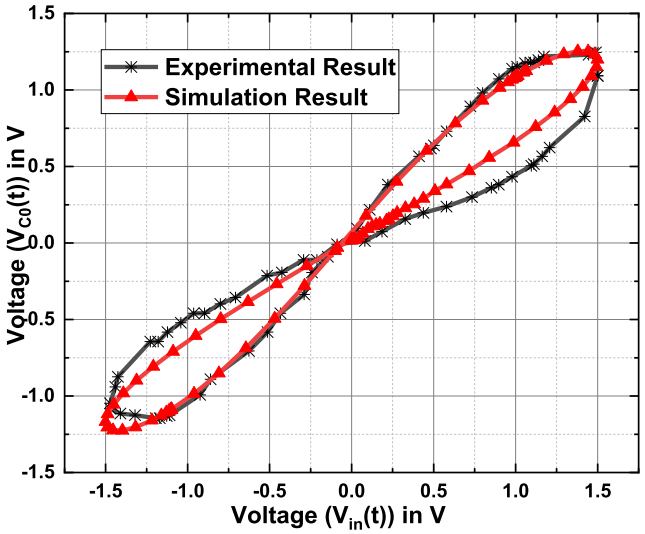

FIGURE 10. Comparison between Experimental and Simulation at 10 kHz for Floating Memcapacitor.

in Fig. 11. The non-linear characteristics of a memristor make it suitable for chaotic circuits. Chua's oscillator is achieved by replacing Chua's diode with a charged controlled memristor. The negative resistance is designed using commercially existing IC CA3080. Chua's circuit consists of one negative resistor, one capacitor, two inductors and one charged controlled memristor.

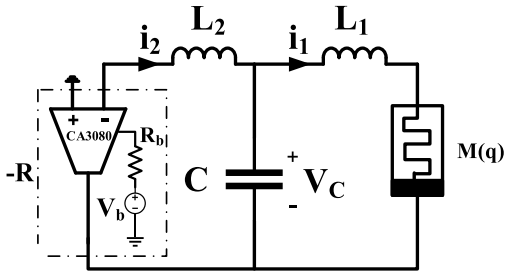

FIGURE 11. Canonical Chua's Oscillator Realization with Proposed Floating Memristor Emulator.

The Chua's circuit displays an ample variety of chaos outputs for different values of circuit components. The dynamic state equation of canonical Chua's oscillator for charged controlled memristor emulator is expressed as:

$$\begin{aligned} L_2 \frac{di_2}{dt} &= Ri_2 - V_C \\ L_1 \frac{di_1}{dt} &= V_C - M\,(q)\, i_1 \\ C \frac{dV_C}{dt} &= i_2 - i_1 \end{aligned} \tag{37}$$

The value of passive components L_1, L_2, and C is taken as 5.5 mH, 55 mH, and 3.5nF, respectively. The negative resistance is created by using IC CA3080. The biasing values selected for IC CA3080 to make it negative resistance are $V_b = 2.5$ V and $R_b = 52\ \Omega$.

Fig. 12 displays the chaotic output plotted for capacitor voltage vs. current through L_1 inductor. As chaotic outputs are very sensitive to components value, even a small change in the value will create a significant change in the output. Fig. 13 shows the output of chaotic circuit with a small change in capacitor voltage. All other component values are the same, and the capacitor value is now changed to 5.5 nF. Chua's circuit can be used in many applications such as: secure communication, analog noise generator, or to improve performance of ultrasonic device in the presence of crosstalk and noise.

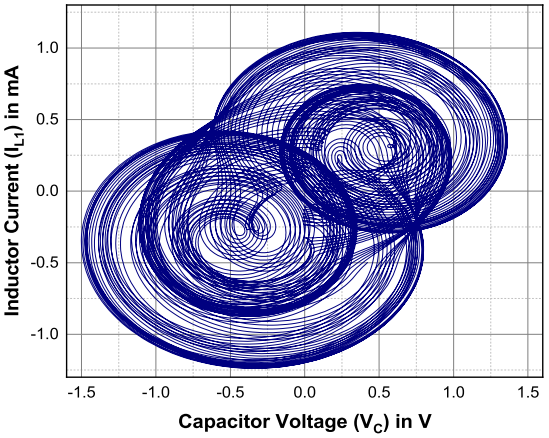

FIGURE 12. Chaotic Circuit Output for C = 3.5 nF.

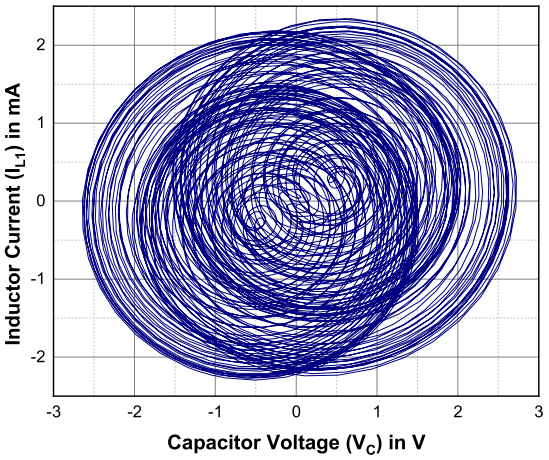

FIGURE 13. Chaotic Circuit Output for C = 5.5 nF.

VIII. CONCLUSION

This article presents two types of mem-element emulators, memristor and memcapacitor, using CCIIs, multiplier, and some passive components. Both grounded and floating mem-elements are presented. The memristor and memcapacitor emulators can be easily changed by simple switching. Also, the incremental and decremental configurations of the mem-element emulator can be simply changed by merely switching the connection. The different values of a parameter

are required for the circuit to work in both the configurations. The theoretical analysis and frequency analysis have been carried out. Simulation and experiment of the proposed mem-element emulator have been undertaken. Simulation results are matched with the experimental results, thus validating the theoretical proposition. A chaotic system has been designed using floating type memristor emulator as part of an application of the proposed emulator.

ACKNOWLEDGMENT

The authors would like to express their heartfelt gratitude to Ms. Nidhee Bhuwal for providing valuable suggestions. The authors would also like to thanks Research and Development Laboratory for Nano Electronics and VLSI Design at IIT (ISM) Dhanbad for the resource.

REFERENCES

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
[2] L. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
[3] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, Oct. 2009.
[4] H. Kim, M. P. Sah, C. Yang, S. Cho, and L. O. Chua, "Memristor emulator for memristor circuit applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2422–2431, Oct. 2012.
[5] C. Yang, H. Choi, S. Park, M. P. Sah, H. Kim, and L. O. Chua, "A memristor emulator as a replacement of a real memristor," *Semicond. Sci. Technol.*, vol. 30, no. 1, pp. 1–9, 2015.
[6] D. Yu, H. Ho-Ching Iu, A. L. Fitch, and Y. Liang, "A floating memristor emulator based relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2888–2896, Oct. 2014.
[7] F. Yuan, *Current Mode Circuits for Data Communication*. New York, NY, USA: Springer, 2007.
[8] C. Sánchez-López, J. Mendoza-López, M. A. Carrasco-Aguilar, and C. Muñiz-Montero, "A floating analog memristor emulator circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 309–313, May 2014.
[9] R. K. Ranjan, N. Bhuwal, N. Raj, and F. Khateb, "Single DVCCTA based high frequency incremental/ decremental memristor emulator and its application," *AEU-Int. J. Electron. Commun.*, vol. 82, pp. 177–190, Dec. 2017.
[10] R. K. Ranjan, N. Rani, R. Pal, S. K. Paul, and G. Kanyal, "Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator and its application," *Microelectron. J.*, vol. 60, pp. 119–128, Feb. 2017.
[11] M. Krems, Y. V. Pershin, and M. Di Ventra, "Ionic memcapacitive effects in nanopores," *Nano Lett.*, vol. 10, no. 7, pp. 2674–2678, Jul. 2010.
[12] D. Biolek, Z. Biolek, and V. Biolkova, "SPICE modeling of memcapacitor," *Electron. Lett.*, vol. 46, no. 7, pp. 520–522, 2010.
[13] D. Biolek, Z. Biolek, and V. Biolková, "Behavioral modeling of memcapacitor," *Radio Eng.*, vol. 20, no. 1, pp. 228–233, 2011.
[14] Y. V. Pershin and M. Di Ventra, "Emulation of floating memcapacitors and meminductors using current conveyors," *Electron. Lett.*, vol. 47, no. 4, pp. 243–244, Feb. 2011.
[15] D. Biolek and V. Biolkova, "Mutator for transforming memristor into memcapacitor," *Electron. Lett.*, vol. 46, no. 21, pp. 1428–1429, 2010.
[16] D. S. Yu, Y. Liang, H. H. C. Lu, and L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 394–399, Aug. 2012.
[17] X. Y. Wang, A. L. Fitch, H. H. C. Iu, and W. G. Qi, "Design of a memcapacitor emulator based on a memristor," *Phys. Lett. A*, vol. 376, no. 4, pp. 394–399, Jan. 2012.
[18] Z. G. Ç. Taşkıran, M. Sağbaş, U. E. Ayten, and H. Sedef, "A new universal mutator circuit for memcapacitor and meminductor elements," *AEU-Int. J. Electron. Commun.*, vol. 119, May 2020, Art. no. 153180.
[19] D. Yu, X. Zhao, T. Sun, H. H. C. Iu, and T. Fernando, "A simple floating mutator for emulating memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 7, pp. 1334–1338, Jul. 2020.
[20] M. E. Fouda and A. Radwan, "Charge controlled memristor-less memcapacitor emulator," *Electron. Lett.*, vol. 48, no. 23, pp. 1454–1455, 2012.
[21] J. Vista and A. Ranjan, "Simple charge controlled floating memcapacitor emulator using DXCCDITA," *Anal. Integr. Circuits Signal Process.*, vol. 104, no. 1, pp. 37–46, Jul. 2020.
[22] Y. Babacan, "An operational transconductance amplifier-based memcapacitor and meminductor," *Istanbul Univ.-J. Electr. Electron. Eng.*, vol. 18, no. 1, pp. 36–38, 2018.
[23] D. Yu, Z. Zhou, H. H.-C. Iu, T. Fernando, and Y. Hu, "A coupled memcapacitor emulator-based relaxation oscillator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 12, pp. 1101–1105, Dec. 2016.
[24] M. S. Feali, A. Ahmadi, and M. Hayati, "Implementation of adaptive neuron based on memristor and memcapacitor emulators," *Neurocomputing*, vol. 309, pp. 157–167, Oct. 2018.
[25] J. Vista and A. Ranjan, "A simple floating MOS-memristor for high-frequency applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 5, pp. 1186–1195, May 2019.
[26] K. Rajagopal, A. Akgul, S. Jafari, and B. Aricioglu, "A chaotic memcapacitor oscillator with two unstable equilibriums and its fractional form with engineering applications," *Nonlinear Dyn.*, vol. 91, no. 2, pp. 957–974, Jan. 2018.
[27] N. Raj, R. K. Ranjan, and F. Khateb, "Flux-controlled memristor emulator and its experimental results," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 28, no. 4, pp. 1050–1061, Apr. 2020.
[28] N. Yadav, S. K. Rai, and R. Pandey, "Novel memristor emulators using fully balanced VDBA and grounded capacitor," *Iranian J. Sci. Technol., Trans. Electr. Eng.*, vol. 20, Jun. 2020.
[29] A. Yesil, Y. Babacan, and F. Kacar, "Electronically tunable memristor based on VDCC," *AEU-Int. J. Electron. Commun.*, vol. 107, pp. 282–290, Jul. 2019.
[30] Q. Zhao, C. Wang, and X. Zhang, "A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit," *Chaos, Interdiscipl. J. Nonlinear Sci.*, vol. 29, no. 1, Jan. 2019, Art. no. 013141.
[31] AD844 Datasheet. *Analog Devices, 60 MHz, 2000 V/μs, Monolithic Op Amp with Quad Low Noise*. Accessed: Jul. 22, 2019. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD844.pdf
[32] AD633 Datasheet. *Analog Devices, Low-Cost Analog Multiplier*. Accessed: Jul. 22, 2019. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD633.pdf

PANKAJ KUMAR SHARMA (Graduate Student Member, IEEE) was born in India, in 1989. He received the B.Tech. degree in electronics and communication engineering from Nilamber-Pitamber University, India, in 2013, and the M.Tech. degree from NIT Hamirpur, India, in 2016. He is currently pursuing the Ph.D. degree with IIT (ISM) Dhanbad, Dhanbad, India. His research interests include analog circuit design, memristor emulator design, and MEMS design.

RAJEEV KUMAR RANJAN (Member, IEEE) was born in India, in 1979. He received the Ph.D. degree from IIT (ISM) Dhanbad, Dhanbad, India, in 2016. He is currently an Assistant Professor with the Department of Electronics Engineering, IIT (ISM) Dhanbad. His main research interests include communications and VLSI signal processing circuits and systems. He has published more than 30 articles in esteemed journals and conferences.

FABIAN KHATEB received the dual M.Sc. and Ph.D. degrees in electrical engineering and communication and business and management from the Brno University of Technology, Czech Republic, in 2002, 2003, 2005, and 2007, respectively. He is currently a Professor with the Department of Microelectronics, Faculty of Electrical Engineering and Communication, Brno University of Technology. He is also with the Department of Information and Communication Technology in Medicine, Faculty of Biomedical Engineering, Czech Technical University in Prague. He holds five patents. He has authored or coauthored over 100 publications in journals and proceedings of international conferences. He has expertise in new principles of designing low-voltage low-power analog circuits, particularly biomedical applications. He is a member of the Editorial Board of *Microelectronics Journal*. He was a Guest Editor of the Special Issue on Current-Mode Circuits and Systems, Recent Advances, Design and Applications on the *International Journal of Electronics and Communications*, in 2017. He was also a Lead Guest Editor of the Special Issues on Low Voltage Integrated Circuits and Systems on *Circuits, Systems, and Signal Processing*, in 2017, *IET Circuits, Devices and Systems*, in 2018, and *Microelectronics Journal*, in 2019. He serves as an Associate Editor for *Circuits, Systems, and Signal Processing*, *IET Circuits, Devices and Systems*, and the *International Journal of Electronics*.

MONTREE KUMNGERN received the B.S.Ind.Ed. degree in electrical engineering from the King Mongkut's University of Technology Thonburi, Thailand, in 1998, and the M.Eng. and D.Eng. degrees in electrical engineering from the King Mongkut's Institute of Technology Ladkrabang, Thailand, in 2002 and 2006, respectively. Since 2007, he has been a Lecturer with the Department of Telecommunications Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang. From 2010 to 2017, he was an Assistant Professor and he is currently an Associate Professor. He has authored or coauthored over 200 publications in journals and proceedings of international conferences. His research interests include analog and digital integrated circuits, discrete time analog filters, non-linear circuits, data converters, and ultralow-voltage building blocks for biomedical applications.