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Online Fault Diagnosis Method for High-Performance Converters Using Inductor Voltage Polar Signatures

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ABSTRACT Recently, the high-performance converter with wide range and high gain has been widely used in these cases such as PV power generation. On the other hand, there are more highly variable stresses on switch and diode in high-performance converter than the traditional DC-DC converters due to the wide range and high gain. Therefore, it is necessary to diagnose switch and diode faults in high-performance converter. In this paper, the switch and diode fault are analyzed and compared with traditional DC-DC converters. Then, an online diagnosis technique based on the inductor voltage polarity of the DC-DC converter is proposed. This technique only uses the inductor voltage polarity and the switch gate drive signal as signatures to diagnose short-circuit or open-circuit fault of the switch and diode. The technique is cost-effective and simple because it uses simple auxiliary windings to sense the inductor voltage polar and uses some logic circuit to generate indicators. The details of the technique are discussed through an example of the quadratic Boost converter. Experiments illustrate the correctness of the proposed technique and show its capability for switch and diode fault diagnosis.

INDEX TERMS Quadratic DC-DC converter, fault diagnosis, inductor voltage, and switch.

I. INTRODUCTION

In recent years, new energy resources such as photovoltaic (PV) cells, wind power, and fuel cell, have been widely used to reduce air pollution from oil resources and others. In these cases, the high-performance converter, such as the quadratic Boost converter, gradually replaces the traditional Boost converter for the advantages of the wide input/output range, high gain, and low cost.

On the other hand, it is vital to assure the safety and reliability of the power generation system in the new energy resource applications. Faults occur in the DC-DC converter, which will cause the power generation system malfunction or reduce the efficiency, and in some cases will cause the second faults. According to statistical research, electrolytic capacitors and power semiconductor devices are the most vulnerable components in the DC-DC converters. More than 30% of converter failures are due to semiconductor devices [1]. Therefore, switch and diode fault diagnosis is essential to achieve desirable reliability for DC-DC converter [2].

Fault detection and diagnosis techniques aiming to the different kinds of converters have attracted many researchers. The traditional non-isolated DC–DC converters faults, such as OCF (open-circuit fault) and SCF (short-circuit fault) of switch and diode, have been widely studied. For example, fast diagnosis methods for switch faults in traditional Buck circuits were investigated in Ref [3], [4]. Fault diagnoses of matrix converters were studied in Ref [5]–[7] and fault diagnoses of multi-level DC-DC converters were studied in Ref [8]–[13]. The fault diagnoses method of zero voltage switch (ZVS) DC-DC converters were studied in Ref [14]. In these diagnoses, it is critical to select and extract fault signatures in implementation of fault diagnosis. In the previous works, output voltage/current [15], inductor voltage/current [16], [17], diode voltage [18],

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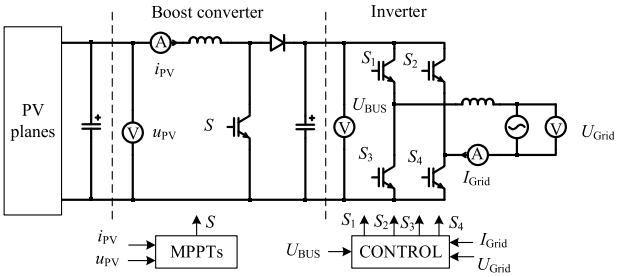

FIGURE 1. **The most common configuration for grid-connected photovoltaic systems.**

magnetic near field waveform [19], and on-state resistance [20] have been used as signatures for switch and diode fault diagnosis in traditional non-isolated DC-DC converters. The inductor voltages captured by an auxiliary winding combined with logic circuits have been utilized to detect switch faults in traditional non-isolated dc–dc converters [18], [21]. This technique is simple and cost-effective.

In fact, there are more highly variable stresses on switch and diode in high-performance converter than the traditional DC-DC converters due to the wide range and high gain, which make switch and diode more fault-prone. But fewer signatures mentioned can be directly applied to diagnose switch faults in the high-performance converters, such as the quadratic single-switch DC-DC converters. In some cases, output voltage/current used as signatures for fault detection is cost-effective. However, these signatures are not suitable for quadratic non-isolated DC-DC converter in the PV power system. For example, Figure 1 illustrates the output/input voltage/current of the Boost converter in the PV power generation grid-connected system, which has been measured for system operation. However, input voltage/current is subject to the PV cells for tracking maximum power points (MPPTs) and output voltage/current is subject to the DC-AC converter for power balancing [22], which results in considerable error detection rate. Secondly, a large LC filter leads to detection delay [2], [23], [24].

Aim to the fault diagnosis of the switch and diode in high performance converters, such as quadratic converters, this paper proposes a new diagnosis method, in which the voltage of the magnetic component that is easier to extract and the switch gate drive signal are selected as the fault detection signals. According to the voltage of the magnetic component before and after the failure of the switch tube and diode, fault diagnosis circuit is designed based on the characteristics of the change. This technology has the advantages of low cost, easy operation, wide fault coverage, good online performance, and fast speed. The proposed method is suitable for quadratic single-switch DC-DC converters, including but not limited to quadratic Boost converters, quadratic Buck converters, and quadratic Buck-Boost converters, and has good scalability.

The rest of this article is organized as follows. In Section 2, the existing faults diagnosis technology for the switch and diode of the Buck converter is described in brief. The basic

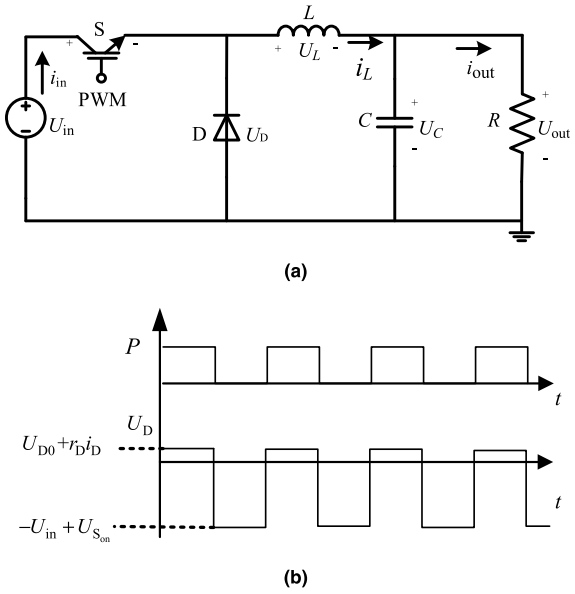

FIGURE 2. **Buck converter: (a) circuit diagram; (b) gate signal and diode voltage for normal condition.**

configuration and operation process of the high-performance converter are given in Section 3. In Section 4, the fault conditions of switch tubes and diodes of high-performance converters are analyzed, and fault diagnosis techniques that can judge the fault types are proposed. In Section 5, a simple logic fault diagnosis circuit is designed to perform fault diagnosis on high-performance converters. Section 6 includes some experimental results, and the final section gives conclusions.

II. PREVIOUS POWER DEVICE FAULT DIAGNOSIS METHODS

Reliable operation of DC-DC converters is vital for many applications. An appropriate converter monitoring scheme is required for fault detection and the adoption of effective remedial strategies. Ref [18] presents a simple diagnosis technique for open-circuits and short-circuits faults of the switch and diode in single inductance traditional Non-isolated DC-DC converter, such as Buck converter shown in Figure 2. The technique only employs diode voltage as the detection signature. In this paper, not only the diode voltage is used as signature, but also the gate driver signal is used to be processed in a simple logic circuit to generate some indicators for switch and diode fault diagnosis. Now contents of the technique using these signatures are discussed in detail.

The fault diagnosis technique in Ref [18] aims to detect four types of fault in Buck converters including switch OCF, switch SCF, diode OCF, and diode SCF.

Figure 2(a) illustrates a Buck converter in which different parameters of the converter are denoted for analysis. In Figure 2(a) parameters P, U_{in}, U_{D}, U_L, and U_{out} represent gate signal as well as voltages of input supply, diode, inductor, and output, respectively.

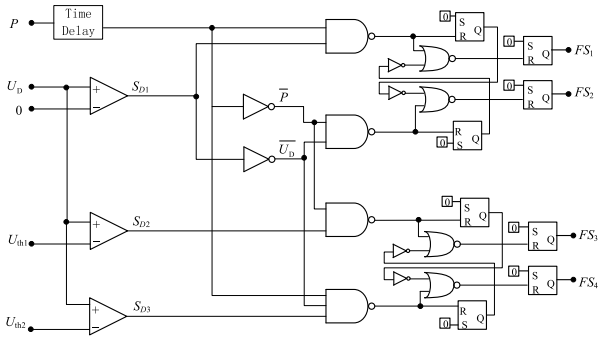

FIGURE 3. Logic circuit of the proposed fault diagnosis technique.

The converter switch, diode, inductor, capacitor, and load are denoted by S, D, L, C, and R, respectively. Currents of input supply, diode, and inductor are denoted by i_{in}, i_{D}, and i_L, respectively. Waveforms of the gate drive signal P and diode voltage for the converter normal operation are depicted in Figure 2(b). In this figure, K, T, U_{D0}, U_{Son}, and r_{D} denote the duty cycle of the gate signal, period of the gate signal, diode built-in potential, on state voltage drop of the switch, and diode internal resistance, respectively. Using Kirchhoff's voltage law (KVL) in Figure 2(a), the diode voltage could be expressed as $P = 0 \Rightarrow$ Switch: OFF $\Rightarrow U_{\text{D}} = U_{\text{D0}} + r_{\text{D}} i_{\text{D}}$, $P = 1 \Rightarrow$ Switch: ON $\Rightarrow U_{\text{D}} = -U_{\text{in}} + U_{\text{Son}}$. Due to U_{D0} and $r_{\text{D}} i_{\text{D}}$ are positive so when $P = 0$, $U_{\text{D}} > 0$. Due to $U_{\text{Son}} \ll U_{\text{in}}$ so when $P = 1$, $U_{\text{D}} < 0$. It should be noted that for the sake of simplicity, diode conduction current and on-state voltage drop of the switch are assumed to be constant in Figure 2(b).

Through the analysis of open circuit and short circuit faults of the switch tube and diode of the Boost converter, the following Equ (1) can be obtained to judge the fault condition of the Buck converter, where U_{th1} and U_{th2} can be seen in Ref [15], [18]:

$$\begin{cases} \text{if } P = 1 \text{ and } U_{\text{D}} > 0 \Rightarrow \text{switch OCF} \\ \text{if } P = 0 \text{ and } U_{\text{D}} < 0 \Rightarrow \text{switch SCF} \\ \text{if } P = 0 \text{ and } U_{\text{D}} > U_{\text{th1}} \Rightarrow \text{diode OCF} \\ \text{if } P = 1 \text{ and } U_{\text{th2}} < U_{\text{D}} < 0 \Rightarrow \text{diode SCF} \end{cases} \tag{1}$$

Figure 3 Show the Buck converter logic circuit for diagnosis, four signals denoted by FS_1, FS_2, FS_3, and FS_4 are generated as indicators of switch OCF, switch SCF, diode OCF, and diode SCF, respectively. In fact, Equ (1) is realized through the logic circuit. Initial setting for inputs of all Reset-Set (SR) flip-flops is S = 1, R = 0. As a result, Q outputs of all flip-flops are initially at a high level. In the next step, S inputs of the flip-flops are set to zero as observed in Figure 3. The research results of previous papers show that the fault diagnosis circuit can accurately and quickly diagnose the switching tube and diode faults of the Buck converter.

However, the diode voltage as the detection signature needs to add one independently auxiliary transformer and is not suitable for high-performance converters, such as the quadratic Boost converter, shown in Figure 4.

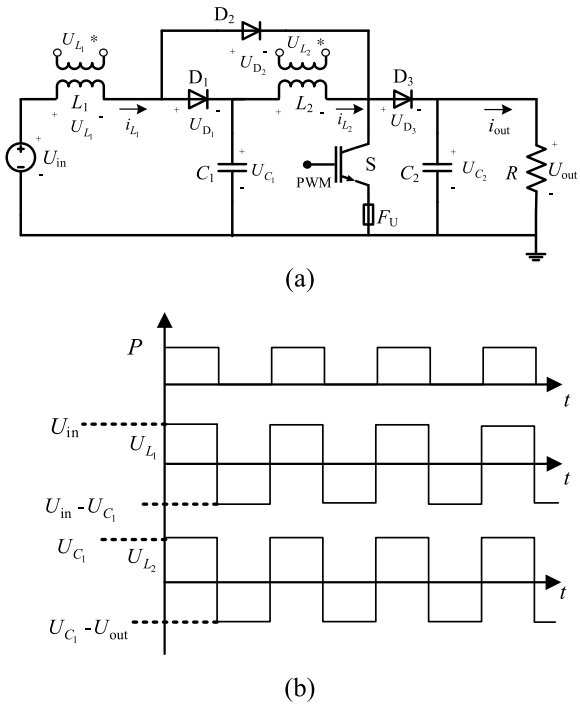

FIGURE 4. Quadratic Boost converter: (a) Quadratic Boost converter circuit diagram; (b) gate signal and inductor voltage for normal case.

III. BASIC CONFIGURATION AND OPERATIONAL PROCESS OF HIGH-PERFORMANCE CONVERTER

In this paper, the quadratic Boost converter is discussed as an example for fault diagnosis. Figure 4 shows the quadratic Boost converter and the waveforms of inductor voltages and gate driving signals. The structure is composed of pre-stage circuit, including inductor L_1, diode D_1 and D_2, capacitor C_1 and switch S, and post-stage circuit including inductor L_2, capacitor C_2, diode D_3 and switch S. In order to avoid the occurrence of secondary fault, the switch S is in series with fuse F_U.

In Figure 4, parameters P, U_{in}, U_L, and U_{out} represent gate driving signal as well as voltages of input supply, inductor, and output, respectively. Currents of input supply, output, and inductor are denoted by i_{in}, i_{out}, and i_L, respectively.

The faults considered in this paper are switch and diode faults, including switch SCF, switch OCF, diode D_1 SCF, diode D_1 OCF, diode D_2 SCF, diode D_2 OCF, diode D_3 SCF, and diode D_3 OCF.

Traditionally, the electrical quantities used to diagnose the fault of the DC-DC converter include the voltage across the switch, the diode voltage, the inductor voltage and current, and the output voltage. If the output voltage is selected as the fault diagnosis feature, the output voltage is easily affected by the load. Due to the existence of output filtering, the output control variable changes slowly and the diagnosis time is long. For the quadratic Boost converter, the number of diodes is large. If the diode voltage is selected, it is difficult to effectively determine the diode fault through analysis. Moreover, after the diode D_2 of the quadratic Boost converter

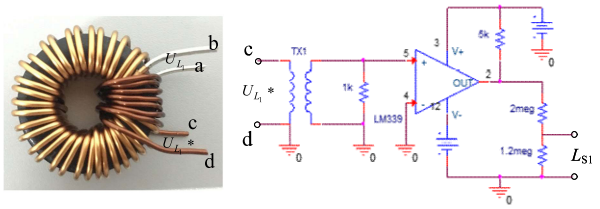

FIGURE 5. The auxiliary winding for L1 and sign of the post-processing circuit.

has an open-circuit fault, the circuit is equivalent to a traditional Boost converter. Therefore, it is difficult to distinguish whether the circuit is faulty using the traditional output voltage or output current as the characteristic electrical quantity for fault diagnosis. If both the inductor voltages U_{L_1}, U_{L_2} are selected as fault diagnosis characteristics at the same time, the electrical quantity can correctly reflect the fault while improving the fault diagnosis efficiency and reducing the cost. The inductor voltage can be obtained by adding auxiliary windings to the corresponding magnetic core. The auxiliary windings and signs of the post-processing circuits are shown in Fig 4(a).

In summary, U_{L_1} and U_{L_2} are selected as the electrical quantities for the fault diagnosis of the quadratic Boost converter. The follow-up diagnosis method only needs to use the polarity of U_{L_1} and U_{L_2} in combination with the drive signal P to make a logical combination to judge the open circuit and short circuit fault of the switch tube or diode. The auxiliary winding processing circuit and the circuit for obtaining the polarity of the inductor voltage is shown in Fig 5. Sign of U_{L_1} and its polarity indication signal L_{S1} is given. In fact, a sign of U_{L_2}, $U_{L_2} - U_{L_1}$ of their directors L_{S2}, L_{S3} can be obtained similarly. The principle of fault diagnosis is described in the following.

According to the operation of the quadratic Boost converter, let the duty ratio $K = T_{on}/T$, where T is the switching period, T_{on} is switch turn-on time in one switching period, then the voltage of capacitor U_{C1} and output voltage U_{out} is calculated using Equ (2) as follows:

$$\begin{cases} U_{C_1} = \left(\dfrac{1}{1-K}\right) U_{in} \\ U_{out} = \left(\dfrac{1}{1-K}\right)^2 U_{in} \end{cases} \tag{2}$$

According to Equ (2), the following equations can be obviously deduced:

$$\begin{cases} U_{C_1} > U_{in} \\ U_{out} = U_{C_2} > U_{C_1} \end{cases} \tag{3}$$

And

$$U_{out} - U_{C_1} > U_{C_1} - U_{in} \tag{4}$$

Using Kirchhoff's voltage law (KVL) in Fig 4(a), the voltage of the inductors L_1 and L_2 under normal cases are expressed as:

$$P = 1 \Rightarrow \begin{cases} U_{L_1} = L_1 \dfrac{di_{L_1}}{dt} = U_{in} > 0 \\ U_{L_2} = L_2 \dfrac{di_{L_2}}{dt} = U_{C_1} > 0 \end{cases} \tag{5}$$

and

$$P = 0 \Rightarrow \begin{cases} U_{L_1} = L_1 \dfrac{di_{L_1}}{dt} = U_{in} - U_{C_1} < 0 \\ U_{L_2} = L_2 \dfrac{di_{L_2}}{dt} = U_{C_1} - U_{out} < 0 \end{cases} \tag{6}$$

The signs of U_{L_1}, U_{L_2} and $U_{L_2} - U_{L_1}$ are related to the driving signal P and fault states of switch and diodes. According to Figure 4, the inductor voltages, U_{L_1}, U_{L_2} are given in Table 1. It should be noted in Table 1 that the considered quadratic Boost converter operates in continuous-conduction mode [25].

IV. PROPOSED FAULT DIAGNOSIS TECHNIQUE OF HIGH-PERFORMANCE CONVERTER

A. SWITCH SCF AND OCF

1) SWITCH SCF

In the case of switch SCF, when $P = 1$, the states of the converter are consistent with the normal states. Switch SCF is not diagnosable while $P = 1$. When $P = 0$, switch SCF occurs, which causes that currents of inductors L_1 and L_2 flow through the switch. According to KVL, in this case the inductor voltage values $U_{L_1} = U_{in}$ and $U_{L_2} = U_{C1}$ are obtained, which are different from the values $U_{L_1} = U_{in} - U_{C_1}$ and $U_{L_2} = U_{C_1} - U_{out}$ in normal case, respectively. Therefore, Switch SCF is detected when $P = 0$. These results in the case of switch SCF are shown in Table 1.

As described in Equ (3)-(6), we easily know that $U_{in} > 0$ and $U_{C_1} > 0$, and $U_{in} - U_{C_1} < 0$ and $U_{C_1} - U_{out} < 0$.

Therefore, fault diagnosis logic relation of the switch SCF is:

$$\text{if} \begin{cases} P = 0 \\ U_{L_1} > 0 \text{ or } U_{L_2} > 0 \end{cases} \Rightarrow \text{switch SCF has occurred} \tag{7}$$

If switch SCF occurs during $P = 0$, it would be detected immediately; if it occurs during $P = 1$, it would not be detected until the instant at which P changes to 0. Therefore, the maximum delay for switch SCF detection is KT, which is less than one switching cycle.

2) SWITCH OCF

In the case of switch OCF, when $P = 0$, the states of the converter are consistent with the normal states. Switch OCF is not diagnosable while $P = 0$. When $P = 1$, switch OCF occurs, which causes that currents of inductors L_1 and L_2 not flow through the switch. According to KVL, in this case the inductor voltage values $U_{L_1} = U_{in} - U_{C_1}$ and $U_{L_2} = U_{C_1} - U_{out}$ are obtained, which are different from the values $U_{L_1} = U_{in}$ and $U_{L_2} = U_{C_1}$ in normal case, respectively. Therefore, Switch OCF is detected when $P = 1$. These results in case of switch OCF are shown in Table 1.

TABLE 1. The relationship between detection variables and operating status of quadratic Boost converter.

Detection volume / Fault status	P	U_{L_1}	U_{L_2}
Normal	1	U_{in}	U_{C_1}
	0	$U_{in}-U_{C_1}$	$U_{C_1}-U_{out}$
Switch SCF	1	U_{in}	U_{C_1}
	0	U_{in}	U_{C_1}
Switch OCF	1	$U_{in}-U_{C_1}$	$U_{C_1}-U_{out}$
	0	$U_{in}-U_{C_1}$	$U_{C_1}-U_{out}$
D_1 SCF	1	*resonates*	0
	0	*resonates*	0
D_1 OCF	1	U_{in}	U_{C_1}
	0	$U_{in}-U_{out}$	$U_{C_1}-U_{out}$
D_2 SCF	1	U_{in}	U_{C_1}
	0	$U_{in}-U_{C_1}$	0
D_2 OCF	1	$U_{in}-U_{C_1}$	U_{C_1}
	0	$U_{in}-U_{C_1}$	$U_{C_1}-U_{out}$
D_3 SCF	1	0	*resonates*
	0	0	*resonates*
D_3 OCF	1	U_{in}	U_{C_1}
	0	$U_{in}-U_{C_1}$	$U_{C_1}-U_{out}-R_{\infty}i_{L_2}$

As described previously, we know that $U_{in}-U_{C_1}<0$ and $U_{C_1}-U_{out}<0$. Therefore, fault diagnosis logic relation of the switch OCF is:

$$\text{if}\begin{cases}P=1\\ U_{L_1}<0 \text{ or } U_{L_2}<0\end{cases}\Rightarrow\text{switch OCF has occurred} \quad (8)$$

If switch OCF occurs during $P=1$, it would be detected immediately; if it occurs during $P=0$, it would not be detected until the instant at which P changes to 1. Therefore, the maximum delay for switch OCF detection is (1-K)T, which is less than one switching cycle.

B. D_1 SCF AND OCF

1) D1 SCF

In the case of D_1 SCF, when $P=0$, the states of converter are consistent with the normal states. When $P=1$, D_2 turns on, D_3 turns off. In this case, there exist two short branches, the L_2-D_1-D_2 branch and the C_1-D_1-D_2-S branch. The energy stored in L_2 and C_1 are discharged through D_2 and S rapidly, which will easily lead to the secondary failure of S and D_2. Therefore, the F_U shown in Fig 4 blows out at the instant of D_1 SCF occurrence. After that instant, whether $P=0$ or $P=1$, switch S branch is always open, and the branch L_1-D_1-C_1-U_{in} resonates and U_{L_1} gradually attenuates in a period of time. At the same instant, the current i_{L_2} flows through the branch L_2-D_1-D_2. Considering $r_{D_1,SCF}$ and r_{D_2} as the D_1 resistance after D_1 SCF and the diode D_2 on-resistance, respectively, the inductance voltage U_{L_2} in the D_1 SCF case is expressed as follows:

$$U_{L_2}=i_{L_2}(r_{D_1,SCF}+r_{D_2}) \quad (9)$$

In fact, U_{L_2} is almost equal to the on-state voltage $U_{D_2,on}$ at the instant and then quickly attenuates to zero. Therefore, U_{L_2} and $P=1$ are used for detecting D_1 SCF. These results in case of D_1 SCF are shown in Table 1.

As described in Equ (9) and to reduce noise interference, we choose two threshold voltages $U_{th1}=U_{D_2,\,on}$ and $U_{th2}=-U_{D_2,\,on}$ to obtain the signature of U_{L_2} with a comparator. Therefore, fault diagnosis logic relation of the D_1 SCF is:

$$\text{if}\begin{cases}P=1\\ U_{L_2}<U_{th1}\\ U_{L_2}>U_{th2}\end{cases}\Rightarrow D_1\text{ SCF has occured} \quad (10)$$

Whether D_1 SCF occurs during $P=0$ or $P=1$, the fault detection will be delayed after two switching cycles.

2) D1 OCF

In the case of D_1 OCF, when $P=1$, D_2 turns on and D_3 turns off, the states of the converter are consistent with the normal states. When $P=0$, the current of L_1 flows through D_2 and D_3. According to KVL, in this case the inductor voltage values $U_{L_1}=U_{in}-U_{out}$ and $U_{L_2}=U_{C_1}-U_{out}$ are obtained. The value $U_{L_1}=U_{in}-U_{out}$ is different from the value $U_{L_1}=U_{in}-U_{C_1}$ in normal case. Therefore, D_1 OCF is detected when $P=0$. These results in the case of D_1 OCF are shown in Table 1.

As described in Equ (6), U_{L_1} and U_{L_2} are both less than 0 when $P=0$, and the polarity of the inductor voltage is consistent with the normal state. So, the polarity of inductor voltages cannot be used as D_1 OCF signature. Under normal case and $P=0$, according to Equ (2)-(6) we obtain $U_{L_1}-U_{L_2}$ as follows:

$$U_{L_1}-U_{L_2}=U_{in}-2U_{C_1}+U_{out}=\left(\frac{K}{1-K}\right)^2U_{in}>0 \quad (11)$$

And when $P=0$ and in case of D_1 OCF, $U_{L_1}-U_{L_2}$ is as follows:

$$U_{L_1}-U_{L_2}=U_{in}-U_{C_1}=\left(-\frac{K}{I-K}\right)U_{in}<0 \quad (12)$$

Therefore, the polarity of $U_{L_1}-U_{L_2}$ is used as D_1 OCF signature and the diagnosis logic relation of the D_1 OCF is as follows:

$$\text{if}\begin{cases}P=0\\ U_{L_1}-U_{L_2}<0\\ U_{L_2}<0\end{cases}\Rightarrow D_1\text{ OCF has occured} \quad (13)$$

If D_1 OCF occurs during $P=0$, it would be detected immediately; if it occurs during $P=1$, it would not be

detected until the instant at which P changes to 0. Therefore, maximum delay for D_1 OCF detection is KT, which is less than one switching cycle.

C. D_2 SCF AND OCF

1) D_2 SCF

In the case of D_2 SCF, when $P = 1$, the states of the converter are consistent with normal states. D_2 SCF is not diagnosable when $P = 1$. When $P = 0$ and D_2 SCF occurs, D_1 turns on, D_3 turns off. Since D_1 and D_2 simultaneously turn on, the inductor L_2 is short-circuited. Considering $r_{D_2,SCF}$ and r_{D_1} as the D_2 resistance after D_1 SCF and the diode D_1 on-resistance, respectively, and according to KVL, the inductor voltage values are $U_{L_1} = U_{in} - U_{C_1}$ and. $U_{L_2} = i_{L_2}\left(r_{D_2,SCF} + r_{D_1}\right) \approx U_{D_1,on}\sqrt{2}$.The value $U_{L_2} \approx U_{D_1,on} > 0$ is different from the value $U_{L_2} = U_{C_1} - U_{out}$ in normal case. Therefore, D_2 SCF is detected when $P = 0$. These results in case of D_2 SCF are shown in Table 1.

Therefore, the fault diagnosis logic relation of the D_2 SCF is as follows:

$$\text{if} \begin{cases} P = 0 \\ U_{L_1} < 0 \\ U_{L_2} > 0 \end{cases} \Rightarrow D_2 \text{ SCF has occured} \tag{14}$$

If D_2 SCF occurs during $P = 0$, it would be detected immediately; if it occurs during $P = 1$, it would not be detected until the instant at which P changes to 0. Therefore, the maximum delay for D_2 SCF detection is KT, which is less than one switching cycle.

2) D_2 OCF

In the case of D_2 OCF, when $P = 0$, the states of the converter are consistent with normal states. D_2 OCF is not diagnosable when $P = 0$. When $P = 1$, D_2 OCF occurs, D_1 turns on and D_3 turns off. According to KVL, in this case the inductor voltage values are obtained as $U_{L_1} = U_{in} - U_{C_1}$ and $U_{L_2} = U_{C_1}$. The value $U_{L_1} = U_{in} - U_{C_1}$ is different from the value $U_{L_1} = U_{in}$ in normal case. Therefore, D_2 OCF is detected when $P = 0$. These results in case of D_2 SCF are shown in Table 1.

Because $U_{L_1} = U_{in} - U_{C_1} < 0$ and $U_{L_2} > 0$ when $P = 1$ in case of D_2 OCF. Therefore, fault diagnosis logic relation of the D_2 OCF is as follows:

$$\text{if} \begin{cases} P = 1 \\ U_{L_1} < 0 \\ U_{L_2} > 0 \end{cases} \Rightarrow D_2 \text{ OCF has occured} \tag{15}$$

If D_2 OCF occurs during $P = 1$, it would be detected immediately; if it occurs during $P = 0$, it would not be detected until the instant at which P changes to 1. Therefore, the maximum delay for D_2 OCF detection is $(1\text{-}K)T$, which is less than one switching cycle.

D. D_3 SCF AND OCF

1) D_3 SCF

In the case of D_3 SCF, when $P = 0$, the states of the converter are consistent with normal states and D_3 SCF is not diagnosable. D_3 SCF occurs when $P = 1$, D_1 turns off, D_2 turns on. In this case, branch C_2-D_3-S is short. The energy stored in C_2 is discharged through D_3 and S rapidly, and the F_U shown in Fig 4 blows out at the instant of D_3 SCF occurrence. After that instant, whether $P = 0$ or $P = 1$, S branch is always open and D_1 turns on and D_2 turns off. And branch L_2-C_1-C_2 resonates for a period of time and U_{L_2} gradually attenuates in a period of time to zero. At the same instant, i_{L_2} reduces to zero and U_{L_1} reduces to 0, quickly. These results in case of D_3 SCF are shown in Table 1.

In order to reduce noise interference, we choose two threshold voltages $U_{th3} = U_{D_1,on}$ and $U_{th4} = -U_{D_1,on}$ to obtain the signature of U_{L_1} with a window comparator. Therefore, fault diagnosis logic relation of the D_3 SCF is as follows:

$$\text{if} \begin{cases} P = 1 \\ U_{L_1} < U_{th3} \\ U_{L_1} > U_{th4} \end{cases} \Rightarrow D_3 \text{ SCF has occured} \tag{16}$$

Whether D_3 SCF occurs during $P = 0$ or $P = 1$, fault detection will be delayed after some switching cycles.

2) D_3 OCF

In the case of D_3 OCF, when $P = 1$, the states of the converter are consistent with the normal states and D_3 OCF is not diagnosable. D_3 OCF occurs when $P = 0$, D_1 and D_2 turn on. In this case, there is no freewheeling branch for L_2 to discharge energy due to D_3 OCF, and switch S and diode D_2 experience a large electric shock. Considering the off-resistance of D_3 to be $r_{D_3,off}$ and according to KVL, the inductor voltage values U_{L_1} and U_{L_2} are obtained as:

$$\begin{cases} U_{L_1} = U_{in} - U_{C_1} \\ U_{L_2} = U_{C_1} - U_{out} - r_{D_3,off} i_{L_2} \end{cases} \tag{17}$$

are obtained. The value $U_{L_2} = U_{C_1} - U_{out} - r_{D_3,off} i_{L_2}$ is different from the value $U_{L_2} = U_{C_1} - U_{out}$ in normal case. Therefore, D_3 OCF is detected when $P = 0$. These results in case of D_3 OCF are shown in Table 1.

Since $r_{D_3,off}$ is large, the inductor voltage U_{L_2} has an extremely large negative voltage after D_3 OCF occurrence. Selecting a larger threshold voltage U_{th5} ($U_{th5} = -V_{DC}/2$). it is easily known that $U_{L_1} < 0$ and $U_{L_2} < U_{th5}$. Therefore, fault diagnosis logic relation of the D_3 OCF is as follows:

$$\text{if} \begin{cases} P = 0 \\ U_{L_1} < 0 \\ U_{L_2} < U_{th5} \end{cases} \Rightarrow D_3 \text{ OCF has occured} \tag{18}$$

If D_3 OCF occurs during $P = 0$, it would be detected immediately; if it occurs during $P = 1$, it would not be detected until the instant at which P changes to 0. Therefore,

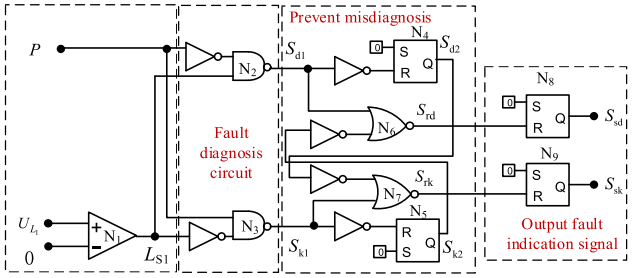

FIGURE 6. Logic circuit for diagnosis of switch faults.

maximum delay for D_3 OCF detection is KT, which is less than one switching cycle.

There are three common quadratic DC-DC converters, that is, quadratic Boost converter, quadratic Buck converter and quadratic Buck-Boost converter. The proposed diagnosis technique can be revised for quadratic Buck converter and quadratic Buck-Boost converter.

V. THE FAULT DIAGNOSIS METHOD

A. SWITCH FAULT DIAGNOSIS CIRCUIT

According to Section 3.1 analysis, the polar signature of voltage U_{L_2} and PWM signal is used for the switch faults and the fault diagnosis logic circuit, shown in Fig 6. The diagnosis circuit mainly consists of comparators, logic gates and R-S latches. The polar signature of voltage U_{L_1} is extracted by using the voltage comparator N_1 as the logic signal L_S, that is, $U_{L_1} > 0$, $L_{S1} = 1$; $U_{L_1} < 0$, $L_{S1} = 0$. Available from Equ (7) and (8), the logic circuit is described as follows:

$$\begin{cases} P = 0, & L_{S1} = 1 \Rightarrow \text{switch SCF} \\ P = 1, & L_{S1} = 0 \Rightarrow \text{switch OCF} \end{cases} \tag{19}$$

It can be seen from Equ (19) that under fault states of switch S the signal P and the signal L_{S1} is an exclusive-or logic relation. Signals S_{sd} and S_{sk} in Fig 6 are used to indicate the short-circuit fault and the open circuit fault respectively, that is, the following logic expression is obtained:

$$\begin{cases} S_{sd} = \overline{\overline{P} L_{S1}} \\ S_{sk} = \overline{P \overline{L_{S1}}} \end{cases} \tag{20}$$

It should be pointed out that after the S OCF occurs, the parasitic capacitance of the inductor L_2, the switch S and the diode D_2 forms a series-resonant circuit, which leads to the signals S_{sd} and S_{sk} output error diagnosis results, shown in Fig 6 with red waveform. In order to avoid misdiagnosis, the error preprocessing circuit is added in Fig 7, and the preprocess logic relation is as follows:

$$\begin{cases} S_{rd} = S_{d1} \cup \overline{S_{k2}} \\ S_{rk} = S_{k1} \cup \overline{S_{d2}} \end{cases} \tag{21}$$

Finally, signals S_{rd}, S_{rk} are latched in the R-S registers, and the fault indication signals S_{sd}, S_{sk} is output.

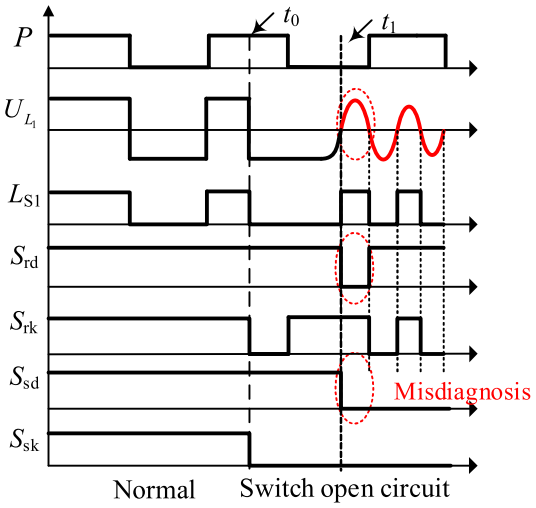

FIGURE 7. Confusion diagram of open circuit and short-circuit faults.

B. DIODES FAULT DIAGNOSIS CIRCUIT

Fig 8 presents the implementation of the proposed diagnosis technique for diode fault diagnosis. According to the results analyzed in Sections 4.2, 4.3, and 4.4, the logical signal P and the inductor voltages U_{L_1}, and U_{L_2} are used to diagnose diode faults. Six signals S_1, S_2, S_3, S_4, S_5 and S_6 are generated as indicators to represent D_1 SCF, D_1 OCF, D_2 SCF, D_2 OCF, D_3 SCF, and D_3 OCF, respectively. The conditions for P, U_{L_1} and U_{L_2} are checked, simultaneously, to generate the logical signatures. Same as section 5.1, the polarity of the inductor voltage, and can be extracted by using a voltage comparator, $U_{L_2} > 0$, $L_{S2} = 1$; $U_{L_3} < 0$, $L_{S3} = 0$.

According to the Equ (10), (13), (14), (15), (16) and (18), the flowchart for diode fault diagnosis is presented in Fig 8(a), which are divided into six parallel procedures.

The proposed algorithm, shown in Fig 8(a), is implemented with a diagnosis logical circuit, shown in Fig 8(b), in which the initial setting for inputs of all Reset-set (SR) flip-flops are S = 1, R = 0, and Q outputs of all flip-flops are initially at the high level. According to the algorithm flow chart, each of diode faults is identified with three signatures and the corresponding signal $S_i (i = 1 \ldots 6)$ changes from high level to low level. Logic values for all indicators including for S faults are given in Table 2.

According to Table 2, signals S_{sd}, S_{sk}, S_1, S_2, S_3, S_4, S_5 and S_6 are all at a high level during normal operation of the quadratic DC-DC converter. If S SCF of the quadratic converter occurs, S_{sd} changes from 1 to 0 while other indicators remain at a high level. Similarly, in case of D_1 SCF occurrence, S_1 becomes 0. It is obvious that when one of fault occurs there is only the corresponding indicator changing to 0 while others remaining high. Therefore, all switch or diode faults in quadratic DC-DC converter can be diagnosed by monitoring S_{sd}, S_{sk}, S_1, S_2, S_3, S_4, S_5 and S_6.

It is worth noting that when diodes D_1 SCF or D_3 SCF occur, the fuse blows out. Depending on the instant that the

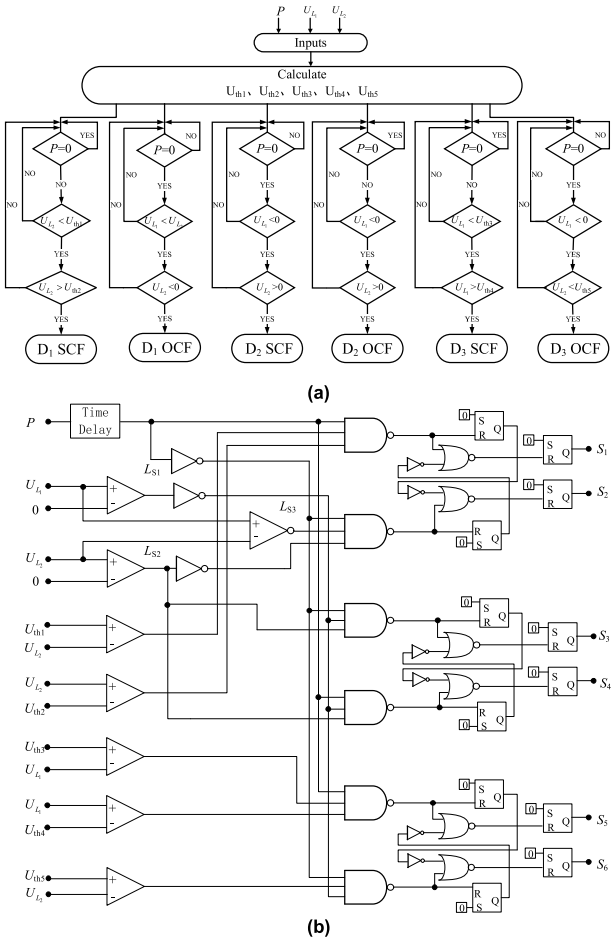

FIGURE 8. Implementation of the proposed fault diagnosis technique (a) diode fault diagnosis flowchart, (b) logic circuit for diode fault diagnosis.

TABLE 2. Values of the logic signals for all fault diagnosis circuits.

Signal / Condition	S_{sd}	S_{sk}	S_1	S_2	S_3	S_4	S_5	S_6
Normal	1	1	1	1	1	1	1	1
S SCF	**0**	1	1	1	1	1	1	1
S OCF	1	**0**	1	1	1	1	1	1
D_1 SCF	1	1	**0**	1	1	1	1	1
D_1 OCF	1	1	1	**0**	1	1	1	1
D_2 SCF	1	1	1	1	**0**	1	1	1
D_2 OCF	1	1	1	1	1	**0**	1	1
D_3 SCF	1	1	1	1	1	1	**0**	1
D_3 OCF	1	1	1	1	1	1	1	**0**

fault occurs, the algorithm can immediately detect or detect the fault by delay. However, the detection time will be more than one switching cycle, as described in Section 3. In Figure 8(b), a time delay unit is applied to the gate drive signal to avoid false diagnostics due to switch turn-on and turn-off delays. The delay unit has been digitally implemented and its value has been set according to the converter switch data.

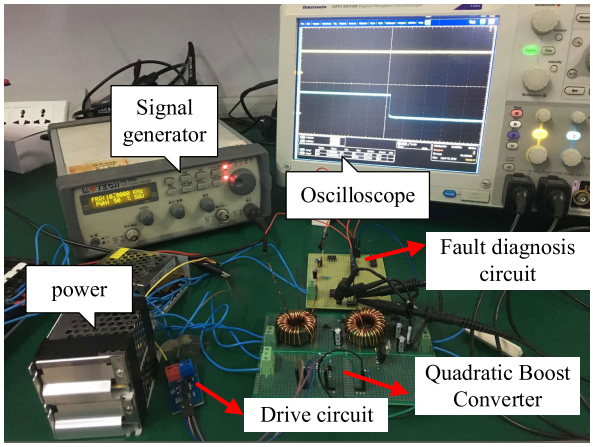

FIGURE 9. Utilized test bench.

TABLE 3. Experimental parameter statistics.

Parameter	value
Uin/V	10
L_1/μH	150
L_2/μH	400
C_1/μF	110
C_2/μF	47
R/Ω	50
f/ KHZ	50
duty cycle	0.5
Switch	IRF540
Diode	MUR460

VI. EXPERIMENTAL RESULTS

In order to verify the effectiveness and the performance of the proposed fault diagnosis method, several experiments have been carried out on quadratic DC-DC converters. The test bench is shown in Figure 9 and the specifications are presented in Table 3. The rated current value of IRF540 is 50A, and then the rated value of F_U is set as 10A, which can assure to avoid the second failure of switch S after D_1 SCF or D_3 SCF occurrence.

In experiments, to implement the short or open fault of the converter semiconductor switches, auxiliary mechanical switches are introduced to emulate switch and diode faults. To emulate OCF, the auxiliary switch is connected in series with the device under test, while for SCF; the auxiliary switch is connected in parallel. In normal cases, the auxiliary switch in series is ON and is turned-off for OCF. Similarly, the auxiliary switch in parallel is OFF and is turned-on for SCF. The on-resistance of auxiliary mechanical switch is negligible.

The data and waveform acquisition are captured by a digital oscilloscope with attenuation probes. In this paper, experimental verifications of quadratic Boost converter, quadratic Buck converter and quadratic Buck-Boost converters are carried out. However, only some experimental results are given as follows due to page limitation.

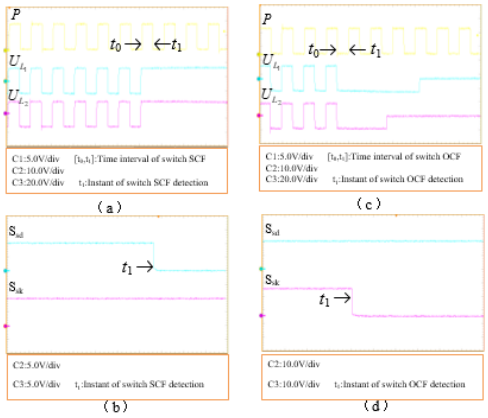

FIGURE 10. Switch fault experimental waveforms of quadratic Boost converter. (a) The voltage of L_1, L_2 after switch SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after switch OCF occurrence; (d) logic signals.

A. SWITCH FAULT EXPERIMENTAL RESULTS

Fig. 10 shows switch fault waveforms diagrams of quadratic Boost converter, in which switch faults have occurred at an instant in $[t_0, t_1]$ interval. It can be seen that all switch faults have been detected. Switch SCF is detected during $P = 0$ because logic signal S_{sd} becomes low, and switch OCF is detected during $P = 1$ because logic signal S_{sk} becomes low.

As the results analyzed in Section 4.1, switch SCF cannot be detected at state $P = 1$ and switch OCF cannot be detected at state $P = 0$. It is obvious that the maximum detection delay is related to the time point of fault occurrence. The maximum delay may be KT and $(1\text{-}K)T$, respectively, which is less than one switching cycle.

Figure 11 shows switch fault experimental waveforms of quadratic Buck converter in which switch faults have occurred at an instant in $[t_0, t_1]$ interval. It can be seen that all switch faults have been detected. Switch SCF is detected during $P = 0$ because logic signal S_{sd} becomes low, and switch OCF is detected during $P = 1$ because logic signal S_{sk} becomes low. It is different from the quadratic Boost converter, the inductor voltage U_{L_1} is greater than the inductor voltage U_{L_2}, and $U_{L_1} = 2U_{L_2}$ when $K = 0.5$.

Same as quadratic Boost converter, switch SCF cannot be detected at state $P = 1$ and switch OCF cannot be detected at state $P = 0$. It is obvious that the maximum detection delay is related to the time point of fault occurrence. The maximum delay may be KT and $(1\text{-}K)T$, respectively, which is less than one switching cycle.

Figure 12 shows the switch fault waveform diagram of the quadratic Buck-Boost converter in which switch faults has occurred at an instant in $[t_0, t_1]$ interval. It can be seen that all switch faults have been detected. Switch SCF is detected during $P = 0$ because logic signal S_{sd} becomes low, and switch OCF is detected during $P = 1$ because logic signal S_{sk} becomes low. It is different from the quadratic Boost converter, when $K < 0.5$, the quadratic Buck-Boost converter operates as a quadratic Buck converter, when $K > 0.5$,

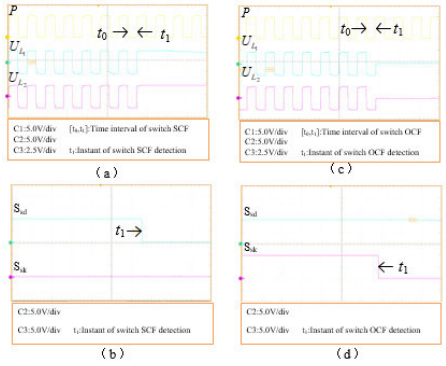

FIGURE 11. Switch fault test waveforms of quadratic Buck converter. (a) The voltage of L_1, L_2 after switch SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after switch OCF occurrence; (d) logic signals corresponding to (c).

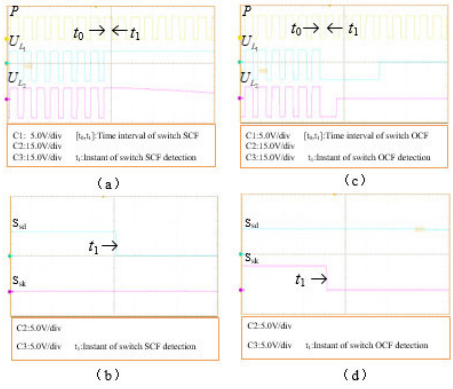

FIGURE 12. Switch fault test waveforms of quadratic Buck-Boost converter. (a) The voltage of L_1, L_2 after switch SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after switch OCF occurrence; (d) logic signals corresponding to (c).

the quadratic Buck-Boost converter operates as a quadratic Boost converter. This paper chooses $P = 0.6$.

Same as quadratic Boost converter, switch SCF cannot be detected at state $P = 1$ and switch OCF cannot be detected at state $P = 0$. It is obvious that the maximum detection delay is related to the time point of fault occurrence. The maximum delay may be KT and $(1\text{-}K)T$, respectively, which is less than one switching cycle.

B. DIODES FAULT EXPERIMENTAL RESULTS

Due to page limitation, the diode experimental results only are given in the quadratic Boost converter. Figure 13 shows the D_1 fault waveforms of the quadratic Boost converter in which D_1 faults have occurred at an instant in $[t_0, t_1]$ interval. The D_1 SCF cannot be detected until t_2 because U_{L_2} becomes zero after two switching cycles and the logic signal S_1 becomes low in which the fuse is disconnected since the current of the switch exceeds 10A. After the D_1 SCF occurrence, fault detection is realized when $P = 1$. According to the converter diode in table 3, $U_{\mathrm{th1}} = 0.7$ and $U_{\mathrm{th2}} = -0.7$ are used in the paper and $U_{\mathrm{th1}} < U_{L_2} < U_{\mathrm{th2}}$ is satisfied at t_2. The D_1 OCF cannot be detected until t_1 because $U_{L_1} < U_{L_2}$ at $P = 0$ and the logic signal S_2 becomes low.

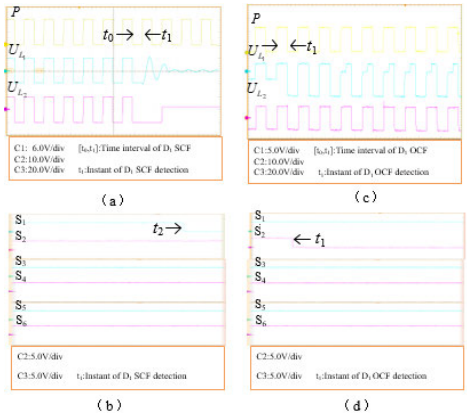

FIGURE 13. D_1 fault test waveforms diagram of quadratic Boost converter (a) The voltage of L_1, L_2 after D_1 SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after D_1 OCF occurrence; (d) logic signals corresponding to (c).

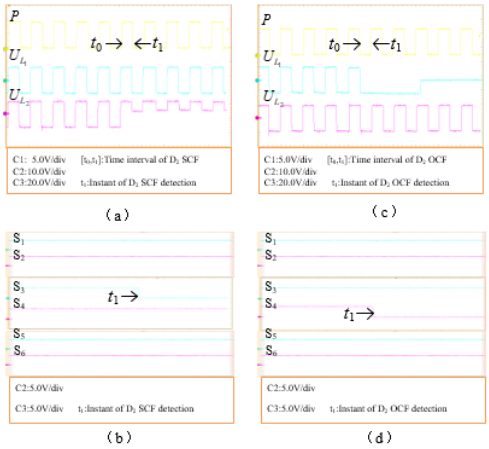

FIGURE 14. D_2 fault test waveforms of quadratic Boost converter. (a) The voltage of L_1, L_2 after D_2 SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after D_2 OCF occurrence; (d) logic signals corresponding to (c).

As the results analyzed in Section 4.2, D_1 SCF cannot be detected at state $P = 0$(according to Equ (10)) and D_1 OCF cannot be detected at state $P = 1$(according to Equ (13)). It is obvious that the maximum detection delay is related to the time point of fault occurrence. The D_1 OCF's maximum delay may be KT, which is less than one switching cycle. But the D_1 SCF will be delayed after two switching cycles.

Fig 14 shows the D_2 fault waveforms of a quadratic Boost converter in which D_2 faults have occurred at an instant in $[t_0, t_1]$ interval. The D_2 SCF cannot be detected until t_1 because U_{L_2} remains positive at $P = 0$ and the logic signal S_3 becomes low. The D_2 OCF cannot be detected until t_1 because U_{L_1} becomes negative and the logic signal S_4 becomes low only at $P = 1$.

As the results analyzed in Section 4.3, D_2 SCF cannot be detected at state $P = 1$ and D_2 OCF cannot be detected at state $P = 0$. It is obvious that the maximum detection delay is related to the time point of fault occurrence. The maximum delay may be KT and $(1\text{-}K)T$, respectively, which is less than one switching cycle.

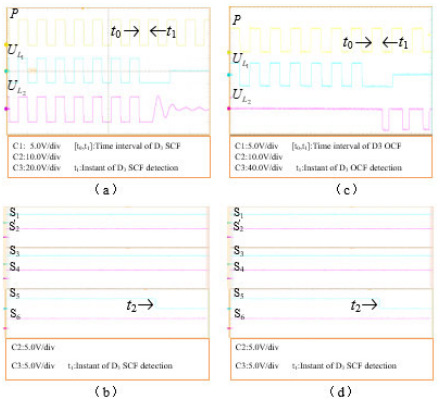

FIGURE 15. D_3 fault test waveforms of quadratic Boost converter. (a) The voltage of L_1, L_2 after D_3 SCF occurrence; (b) logic signals corresponding to (a); (c) The voltage of L_1, L_2 after D_3 OCF occurrence; (d) logic signals corresponding to (c).

Fig 15 shows the D_3 fault waveforms of a quadratic Boost converter in which D_3 faults have occurred at an instant in $[t_0, t_1]$ interval. The D_3 SCF could not detected until t_2, because the U_{L_1} becomes zero after two switching cycles and the logic signal S_5 becomes low in which the fuse is disconnected since the current of the switch exceeds 10A and after D_3 SCF. And fault detection is realized when $P = 1$ For the converter diode in table 3, choose $U_{\text{th3}} = 0.7$ and $U_{\text{th4}} = -0.7$ We can see $U_{\text{th3}} < U_{L_1} < U_{\text{th4}}$ at t_2. The D_3 OCF cannot be detected until t_1, because $U_{L_2} > U_{\text{th5}}$ at $P = 0$ and the logic signal S_6 becomes low. According to Equ (17), the D_3 experiences a large voltage in this case, we choose $U_{\text{th5}} = 5\text{V}$.

As the results analyzed in Section 4.4, D_3 SCF cannot be detected at state $P = 0$ and D_3 OCF cannot be detected at state $P = 1$. It is obvious that the maximum detection delay is related to the time point of fault occurrence. The D_3 OCF's maximum delay may be KT, which is less than one switching cycle. But the D_3 SCF will be delayed after some switching cycles.

VII. CONCLUSION

This paper firstly studies the previous fault diagnosis technology of power devices aiming at traditional DC-DC converters. The selection of fault detection signals is diverse and cannot be universally applied to high-performance converters. This paper put forward a simple logic fault diagnosis method to detect switch and diode faults of high-performance converters. This method uses inductor voltage signal and PWM signal to identify all switches and diodes SCF and OCF in the quadratic DC-DC converter. This paper fully explains the theoretical basis and design of the diagnostic circuit. This diagnostic method has interesting advantages, including implementation in one switching cycle, with full coverage of faults, low cost, high efficiency, and strong real-time performance. The experimental results verified the accuracy and effectiveness of this method. The fault diagnosis method proposed in this paper has good scalability and

establishes a foundation for fault diagnosis of non-isolated DC-DC converters.

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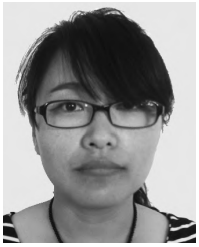

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