IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received August 12, 2020, accepted August 20, 2020, date of publication September 18, 2020, date of current version October 12, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3021710

Adaptive on Time Controlled Double-Line-Frequency Ripple Suppressor With Fast Dynamic Response and High Efficiency

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The research work was supported by the National Natural Science Foundation of China under Grant 61601378 and by the Sichuan Science and Technology Program under Grant 2019YJ0237, 20QYCX0095, and 2019JDTD0003.

ABSTRACT Due to the input power and output power do not match in real time, single-stage power factor correction converters have large double-line-frequency ripple at the output voltage. The double-line-frequency ripple voltage will cause some electronic devices to work abnormally, and limit the control loop bandwidth of power factor correction converter. In order to reduce the output double-line-frequency ripple voltage, a single-stage Flyback power factor correction converter with Buck ripple suppressor is used in this paper, the Buck ripple suppressor can generate same magnitude but 180° phase shifted voltage as Flyback power factor correction converter output voltage ripple. Adaptive on-time control is adopted in the Buck ripple suppressor benefiting with its wider bandwidth and fast dynamic response. The switching frequency range and stability of Buck ripple suppressor under constant on-time control and adaptive on-time control are discussed. By establishing the input-output audio susceptibility model, the output double-line-frequency ripple suppression performance is analyzed. Buck ripple suppressor using adaptive on-time control can suppress double-line-frequency ripple voltage effectively with the fast dynamic response and high efficiency. Simulation and experimental results are given to verify the theoretical analysis.

INDEX TERMS Adaptive on-time control, audio susceptibility model, double-line-frequency ripple, dynamic response, power factor correction, stability analysis.

I. INTRODUCTION

Single stage power factor correction (PFC) converter suffers from serious double-line-frequency (DLF) ripple voltage due to the difference between the instantaneous variable AC input power and the constant DC output power [1], [2]. DLF ripple will cause some electronic devices to work abnormally, and will limit the control loop bandwidth of PFC converter. The control loop bandwidth of the PFC converter is generally set at about 10-20 Hz [3], which seriously affects the load dynamic response.

The most direct way to reduce the DLF ripple of the PFC converter output voltage is to use a large capacity electrolytic capacitor. However, using this method will reduce the power density and dynamic response [4]. In order to improve the dynamic response and reduce the output voltage ripple, a DC-DC converter is usually cascaded after the PFC converter [5], [6]. The two-stage cascaded PFC converter has low efficiency and high cost because the energy is converted twice, so it is not suitable for low power applications.

To achieve DC output, a bidirectional converter is connected in parallel to the output of the PFC converter [7]–[13]. When the output current exceeds the average value, the excess flows to the bidirectional converter storage. When the output current is less than the average value, the energy stored in the bidirectional converter flows to the load. This method allows the current to the load to contain only a DC component. However, the passive and active components of the shunt compensation device suffer from high voltage stresses.

In addition to the parallel method, some scholars have combined the output of the DC-DC converter and the PFC converter in series to suppress the DLF ripple [14]–[18], so that the DC-DC converter generates same magnitude but 180° phase shifted voltage as PFC converter output voltage

The associate editor coordinating the review of this manuscript and approving it for publication was Shihong Ding.

ripple. After the two output voltages are superimposed in series, the DLF ripple voltage at the output can be effectively reduced. In [19], a virtual output impedance method was adopted to reduce the DLF ripple voltage, and the amplitude at 100 Hz was also predicted. Reference [20] has designed a quasi-proportional resonance (QPR) compensator, which can suppress the output voltage ripple at a specific frequency. However, in the above-mentioned series compensation method, the dynamic response is not fast enough, and the compensation circuit design is difficult. Some control methods with excellent dynamic response are proposed in [21] and [22], which are greatly improve the system performance. Pervious research [23] uses constant on-time (COT) to control the Buck ripple suppressor (RS), which improves the dynamic response and simplifies the design of the control loop. However, the switching frequency changes greatly, so the design of the electro-magnetic interference (EMI) filter is difficult. Adaptive on-time (AOT) control is developed by COT control, but it has the characteristic of variable on-time, it has been widely used to improve transient response [24]–[27]. In view of this, the paper proposes AOT control method for quasi-single-stage (QSS) Flyback PFC converter to obtain fast dynamic response and low output voltage ripple. As will be disclosed latter, the frequency of Buck RS with AOT control is analyzed, comparing to the COT control, the proposed AOT control has a narrower range of frequencies. Similar to the COT control, the stability analysis is concerned widely, especially in fault diagnosis [28], [29], hence, the stability condition of AOT control is provided. In order to investigate the relationship between control method and DLF ripple suppression, audio susceptibility model of Buck RS is established, it is found that the closed-loop audio susceptibility of Buck RS with AOT control is lower at DLF, so the Buck RS can achieve better DLF ripple suppression. Comparing to exiting control methods, the proposed AOT-controlled QSS has the following advantages: 1) achieves very fast load dynamic response and high efficiency; 2) simple control without compensation network; 3) lower output voltage ripple and friendly to EMI design.

This paper is organized as follows. In Section II, a QSS Flyback PFC converter is introduced. The difference between COT control and AOT control is analyzed. In Section III, the switching frequency range of Buck RS under COT control and AOT control are investigated. In Section IV, the stability of Buck RS is discussed. In Section V, the output voltage ripple is analyzed by the audio susceptibility model and validated by time domain simulation. In Section VI, an experimental prototype is established and the experimental results are given to verify the theoretical analysis. Finally, the conclusion is given in Section VII.

II. THE CIRCUIT CONFIGURATION OF QUASI-SINGLE-STAGE FLYBACK PFC CONVERTER

Assuming that the power loss of a single-stage PFC converter can be ignored, and the PF=1, then its input power can be expressed as $2P_o\sin^2\omega_L t$, where P_o is the output power and ω_L is the line angular frequency. The difference of instantaneous power between output power and input power is $P_o\cos 2\omega_L t$, Therefore, the output voltage contains a large DLF ripple, and the waveforms are shown in Fig. 1 [1].

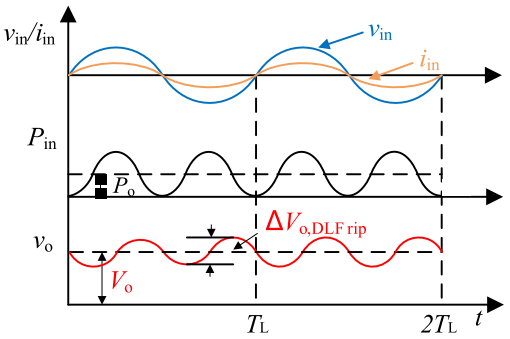


FIGURE 1. Input and output waveforms of single-stage PFC converter.

The Flyback PFC converter has a simple structure and low cost, and can be used in a wide range of applications with multiple isolated outputs. In this paper, QSS Flyback PFC converter is composed of a Flyback PFC converter and a Buck converter in series, as shown in Fig. 2. It can be seen from Fig. 2 that the QSS Flyback PFC converter consists of two parts: 1) Flyback PFC converter with two output winding, and 2) Buck RS. The two output voltages of the Flyback PFC converter are respectively the main output voltage v_{o1} and the auxiliary output voltage v_{o2}, where v_{o2} is used as the input voltage of the Buck RS, and the output voltage v_b of the Buck RS is connected in series with v_{o1} to form the total output voltage v_o.

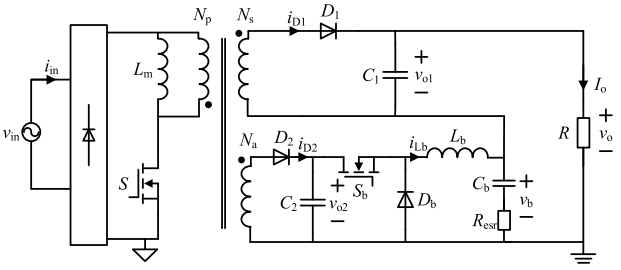


FIGURE 2. Quasi-single-stage Flyback PFC converter.

As can be seen from Fig. 3, the output voltage v_{o1} and v_{o2} of the Flyback PFC converter both contain DLF and have the same phase. By controlling the Buck RS to output a voltage v_b that is same magnitude but 180° phase shifted as the DLF ripple of v_{o1}, add v_b and v_{o1} in series can obtain a voltage v_o with little DLF ripple.

Referring to references [14], [19], and [20] that the suppression capability of DLF ripple depends on the bandwidth of the control loop of the Buck RS, its bandwidth is designed as wide as possible to achieve small ripple. However, the compensation network with wide bandwidth is hard to design. COT control is simple to implement and easy to design

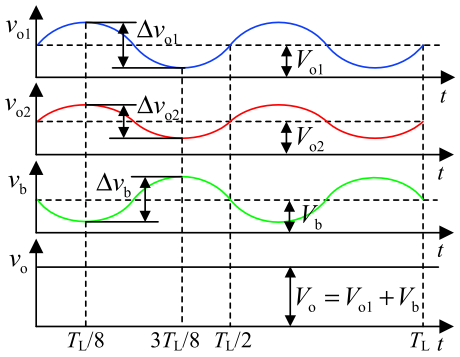


FIGURE 3. Key waveforms of QSS Flyback PFC converter.

without compensation network [30]. Moreover, COT control features wide bandwidth and benefits with fast input and load dynamic response. The COT-controlled Buck RS is proved to be effective in the output voltage DLF ripple suppression and improvement of dynamic response [23]. However, COT control suffers from significant variation of switching frequency because both input voltage and output voltage of Buck RS fluctuate at DLF. Given that, AOT control is applied to control Buck RS, it not only has the similar wide bandwidth as well as COT control but also can further suppress output voltage DLF ripple effectively, and narrower variation of switching frequency can be achieved.

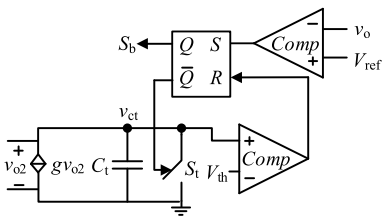


FIGURE 4. Schematic diagram of AOT control controller.

III. ANALYSIS OF BUCK RS SWITCHING FREQUENCY

Fig. 4 shows schematic diagram of the AOT control controller. From Fig. 4, it can be known that when feedback voltage v_o decreases to V_{ref}, switch S_b is on and S_t is off, which makes both v_o and v_{ct} increase. During off-time of switch S_t, capacitor C_t is charged by voltage-controlled current source gv_{o2}, so v_{ct} is increasing. The time for v_{ct} increases from zero to voltage V_{th} is linearly proportional to V_{th}/v_{o2}. When v_{ct} increases to V_{th}, switch S_b is off and switch S_t is on. The on-time t_{on} of switch S_b in a switching period is thus adaptively controlled by the charging of capacitor C_t through voltage-controlled current source v_{o2} as:

$$t_{on} = \frac{v_{th} C_t}{g v_{o2}} \tag{1}$$

After on time interval t_{on}, both v_o and v_{ct} decrease. When v_o decreases to V_{ref}, switch S_b is on and switch S_t is off again.

Assume that Buck converter works in continuous conduction mode (CCM). The DLF ripples voltage across capacitors C_1 and C_2 are [31].

$$\Delta v_{o1} \approx \frac{(1-\lambda) P_o}{2\pi f_L V_{o1} C_1} \tag{2}$$

$$\Delta v_{o2} \approx \frac{\lambda V_{o1} (C_1 + C_b)}{V_{o2} (1-\lambda) C_2} \tag{3}$$

where P_o is output power and $\lambda = V_b/V_o$.

From Fig. 3, it can be known that in one AC line cycle T_L, the maximum duty cycle D_{b_max} of switch S_b exists at $t = 3T_L/8$, when input voltage v_{o2} is minimum and output voltage v_{o2} is maximum. Similarly, the minimum duty cycle D_{b_min} exists at $t = T_L/8$, when Δv_b is equal to Δv_{o1}.

$$D_{b\_max} = \frac{v_{b\_max}}{v_{o2\_min}} = \frac{V_b + \Delta v_{o1}/2}{V_{o2} - \Delta v_{o2}/2} \tag{4}$$

$$D_{b\_min} = \frac{v_{b\_min}}{v_{o2_{max}}} = \frac{V_b - \Delta v_{ol}/2}{V_{o2} + \Delta v_{o2}/2} \tag{5}$$

Since the AOT control is based on the COT control, the input voltage of the Buck converter is introduced into the controller. In order to analyze the performance of the AOT, the switching frequency under the COT control also be analyzed. The variation of switching frequency Δf_{b_COT} of COT control is:

$$\begin{aligned} \Delta f_{b\_COT} &= f_{b\_max} - f_{b\_min} = D_{b\_max}/T_{on} - D_{b\_min}/T_{on} \\ &= \frac{(kV_b + V_{o2})\,\Delta v_{ol}}{T_{on}\left[V_{o2} - 0.25k^2\,(\Delta v_{o1})^2\right]} \end{aligned} \tag{6}$$

where $k = \Delta v_{o2}/\Delta v_{o1}$.

For AOT control, as its on-time is adaptive, there is:

$$f_{b\_max} = \frac{D_{b\_max}}{t_{on\_max}} = \frac{g D_{b\_max}\,(V_{o2} - \Delta v_{o2}/2)}{V_{th} C_t} \tag{7}$$

$$f_{b\_min} = \frac{D_{b\_min}}{t_{on}\,min} = \frac{g D_{b\_min}\,(V_{o2} + \Delta v_{o2}/2)}{V_{th} C_t} \tag{8}$$

Plugging equation (4) and (5) into (7) and (8), the variation of switching frequency Δf_{b_AOT} of AOT control is:

$$\Delta f_{b\_AOT} = f_{b\_max} - f_{b\_min} = \frac{g \Delta v_{o1}}{C_t V_{th}} \tag{9}$$

From (6) and (9), Δf_{b_AOT} and Δf_{b_COT} as function of Δv_{o1} are shown in Fig. 5. Obviously, with the Δv_{o1} increases, Δf_{b_AOT} and Δf_{b_COT} will increase, but Δf_{b_AOT} is always smaller than Δf_{b_COT}. Moreover, Δf_{b_COT} is affected by multiple variables, once the conditions of converter change, the unexpected frequencies will appear. For instance, with the increase of k, e.g., the increase of Δv_{o2}, Δf_{b_COT} increases but Δf_{b_AOT} is unaffected.

From the above analysis, AOT control not only inherits the characteristics of COT control, but also has the advantage of reducing the frequency variation range, which is favourable for the EMI design.

IV. STABILITY ANALYSIS

Fig. 6 shows the key waveforms of a COT-controlled Buck converter with different equivalent series resistance (ESR) of output capacitors.

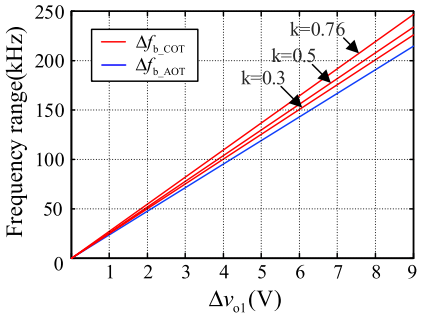


FIGURE 5. Variation of switching frequency as the function of Δv_{o1}.

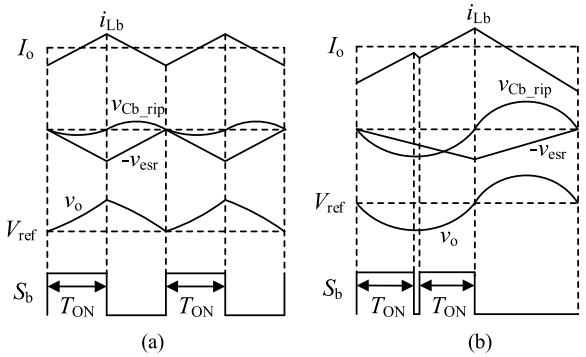


FIGURE 6. Waveforms with different ESR cases. (a) Large ESR. (b) Small ESR.

It can be seen from Fig.6 (b) that when the ESR is small, pulse cluster discovery phenomenon will occur [30]. We can also know that when the ESR is small, both the inductor current ripple and the output voltage ripple will increase, which will not only reduce the power quality, but also increase the switching loss. A similar phenomenon will also occur when using AOT control. In order to make the Buck RS work normally, analyzing the stable working conditions of the AOT-controlled Buck RS is necessary in this paper.

It can be seen from Fig. 2, $v_o = v_{o1} + v_b$. When using AOT control, the ESR of capacitor C_b cannot be ignored. When considering ESR, $v_b = v_{cb} + v_{esr}$. To ensure stable operation of Buck RS, the slope of v_o should be higher than zero during the on time of S_b.

$$\frac{dv_o}{dt} = \frac{d\left(v_{o1} + v_{cb} + v_{esr}\right)}{dt} > 0 \tag{10}$$

The slope of v_{o1} is:

$$\frac{dv_{o1}}{dt} = \frac{i_{D1} - I_o}{C_1} = \frac{i_{D1} - V_{ref}/R}{C_1} \tag{11}$$

The slope of $v_{cb}$and slope of v_{esr} are:

$$\begin{cases} \dfrac{dv_{cb}}{dt} = \dfrac{i_{Lb} - I_o}{C_b} \\ \dfrac{dv_{esr}}{dt} = R_{esr}\dfrac{d\left(i_{Lb} - I_o\right)}{dt} = R_{esr}\dfrac{v_{o2} - v_b}{L_b} \end{cases} \tag{12}$$

Plugging equation (11) and (12) into (10):

$$\frac{i_{D1} - V_{ref}/R}{C_1} + \frac{i_{Lb} - I_o}{C_b} + R_{esr}\frac{v_{o2} - v_b}{L_b} > 0 \tag{13}$$

TABLE 1. Parameters of QSS Flyback PFC converter.

	Symbol	Description	Value
Specification	V_{in}	Input voltage	110 V
	f_{2L}	Double line frequency	100 Hz
	V_o	Output voltage	48 V
	P_o	Output power	50 W
Flyback PFC converter	V_{o1}	Main output voltage	42 V
	C_1	Output capacitor	480 μF
	C_2	Buck RS input capacitor	220 μF
	N_p:N_s:N_a	Transformer turns ratio	30:11:9
	L_m	Magnetizing inductor	220 μH
	f_f	PFC converter switching frequency	50 kHz
Buck converter	V_b	Buck RS output voltage	6 V
	C_b	Buck RS output capacitor	47 μF
	L_b	Buck RS output inductor	50 μH
On-time controller	g	Controlled coefficient	1/35
	V_{th}	Threshold voltage	1 V
	C_t	Charging capacitor	1.2 μF

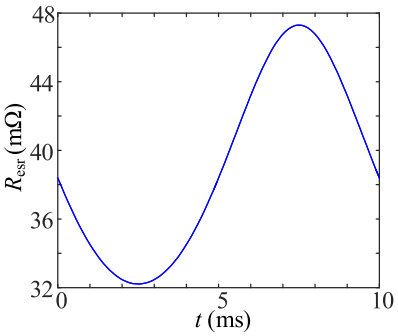


FIGURE 7. R_{esr} change curve in DLF.

Then, the stable condition of R_{esr} can be obtained:

$$R_{esr} > \left(\frac{V_{ref}/R - i_{D1}}{C_1} - \frac{i_{Lb} - I_o}{C_b}\right)\frac{L_b}{v_{o2} - v_b} \tag{14}$$

Both v_{o2} and v_b contain DLF ripple. In order to obtain the maximum value of R_{esr}, i_{Lb} and i_{D1} are set equivalent to 0. The parameters in Table 1 is used to analyze equation (14).

Fig. 7 is the simulation analysis of equation (14) with Matlab. It can be seen that the maximum value of R_{esr_max} is 47.5 mΩ in a DLF cycle. That means R_{esr} needs to be greater than 47.5 mΩ to make Buck RS work in a stable state while parameters are used in Table 1.

PSIM software is used to simulate the above analysis. It can be seen from Fig. 8 (a) that when R_{esr} is small, a pulse cluster finding phenomenon occurs, and at this time, the ripple of the v_o and i_{Lb} are both large. It can be seen from Fig. 8 (b) that when R_{esr} takes the maximum value of 48 mΩ calculated by equation (14), the system works in a normal state, and the ripple of the v_o and i_{Lb} are smaller than that of Fig. 8 (a). Simulation results show that the stable operating conditions provided by equation (14) can be used as a reference for circuit design.

V. OUTPUT VOLTAGE RIPPLE ANALYSIS

A. OPEN-LOOP AUDIO SUSCEPTIBILITY ANALYSIS

According to the description in [20], a H-parameter two-port network as shown in Fig. 9 is used to describe a switching

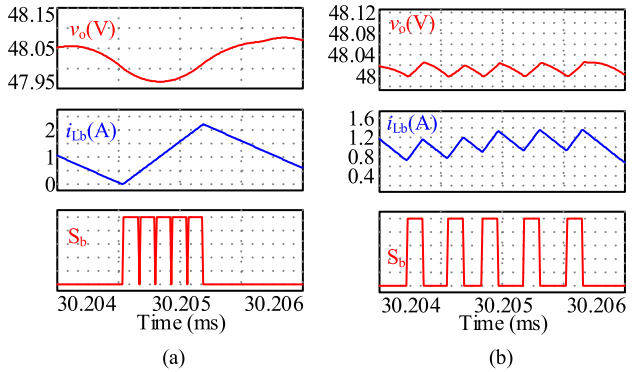


FIGURE 8. Simulation results under different cases. (a) $R_{esr} = 38$ mΩ. (b) $R_{esr} = 48$ mΩ.

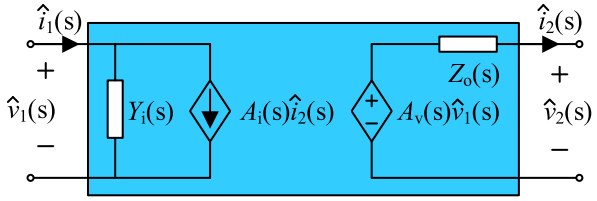


FIGURE 9. H-parameter two-port network.

converter, where$\hat{v}_1$, $\hat{i}_1$, $\hat{v}_2$, $\hat{i}_2$ are input voltage/current and output voltage/current small signal, respectively.

The definition of audio susceptibility is as follows:

$$A_v(s) = \frac{\hat{v}_2(s)}{\hat{v}_1(s)} \tag{15}$$

The audio susceptibility expressed by equation (15) is used to measure the input-output noise transmission rejection ratio. It can be seen from the equation that the smaller the audio susceptibility, the better the ability to suppress noise in the input.

In order to analyze the suppression performance of output voltage DLF ripple, the following assumptions are made:

(1) Switching frequency f_b of the Buck RS and the switching frequency f_f of the Flyback PFC converter are much larger than f_{2L}.

(2) The amplitude of the switching ripple is much smaller than the amplitude of the DLF ripple.

So v_{o1} and v_{o2} can be regarded as DC quantities within one switching cycle of the Buck RS. The equivalent circuit is shown in Fig. 10, since AOT control strategy is adopted for Buck RS, the value of R_{esr} cannot be ignored.

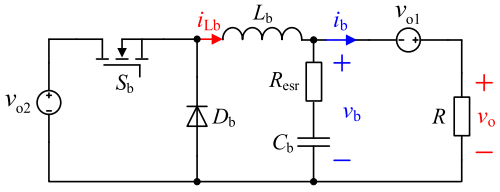


FIGURE 10. Equivalent circuit of QSS Flyback PFC converter.

The suppression of the output voltage DLF ripple can be regarded as the suppression of the DLF disturbance signal in the two input power supplies of the Buck RS. Therefore, the DLF ripple suppression of the Flyback PFC converter can be equivalent to the suppression of the DLF disturbance signal in the input voltage v_{o1} and v_{o2}.

In order to obtain the open-loop audio susceptibility model, the time-averaged equivalent of Fig. 10 is used, and the AC small signal model is shown in Fig. 11.

It can be seen from Fig. 11 that the circuit has two disturbance signals, $\hat{v}_{o1}(s)$ and $\hat{v}_{o2}(s)$, and the influence of the two disturbance signals on the output voltage can be analyzed by the superposition theorem.

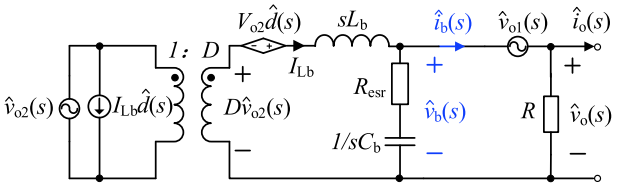


FIGURE 11. AC Small signal equivalent circuit.

When only the disturbance signal $\hat{v}_{o1}(s)$ is presented. Fig. 11 can be further equivalent to Fig. 12 (a). When only the disturbance signal $\hat{v}_{o2}(s)$ is presented, Fig. 11 can be further equivalent to Fig. 12 (b).

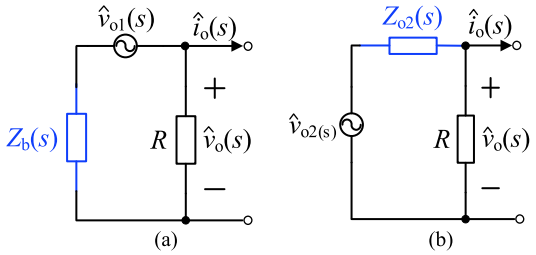


FIGURE 12. Thevenin equivalent of open-loop control. (a) Only the $\hat{v}_{o1}(s)$ is presented. (b) Only the $\hat{v}_{o2}(s)$ is presented.

From Fig. 12, the audio susceptibility $A_{v1}(s)$ and $A_{v1}(s)$of the two disturbance signals on the output voltage can be respectively obtained as follows:

$$A_{v1}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{o1}(s)} = \frac{R}{Z_b(s) + R} \tag{16}$$

$$A_{v2}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{o2}(s)} = \frac{R}{Z_{o2}(s) + R} \tag{17}$$

According to equation (16) and (17), the audio susceptibility model and the output impedance model are unified.

From Fig. 11, detailed models of $A_{v1}(s)$ and $A_{v2}(s)$ can be obtained:

$$A_{v1}(s) = \frac{s^2 L_b C_b R + s C_b R R_{esr} + R}{s^2 L_b C_b (R + R_{esr}) + s (L_b + C_b R R_{esr}) + R} \tag{18}$$

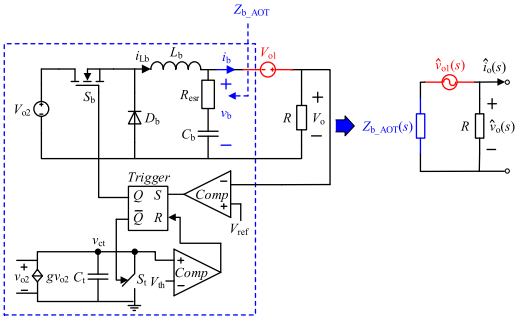
$$A_{v2}(s) = \frac{(s C_b R R_{esr} + R) D}{s^2 L_b C_b (R + R_{esr}) + s (L_b + C_b R R_{esr}) + R} \tag{19}$$

The transfer function of output to control can also be obtained from Fig. 11:

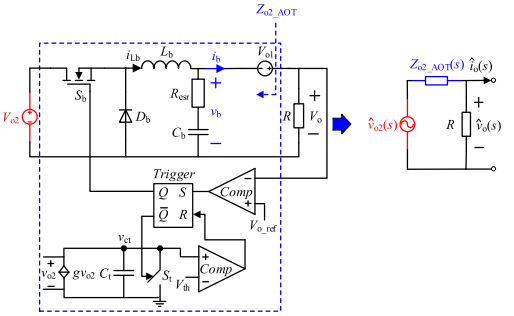
$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{(sC_bRR_{esr} + R)\,V_{o2}}{s^2L_bC_b\,(R + R_{esr}) + s\,(L_b + C_bRR_{esr}) + R} \quad (20)$$

B. CLOSED-LOOP AUDIO SUSCEPTIBILITY ANALYSIS

Closed-loop audio susceptibility also be applied to measure the output voltage DLF ripple suppression performance. To get the audio susceptibility model, the Thevenin equivalent of main circuit and controller are performed, as shown in Fig. 13.



(a)



(b)

FIGURE 13. Thevenin equivalent of closed-loop control. (a) Only the $\hat{v}_{o1}(s)$ is presented. (b) Only the $\hat{v}_{o2}(s)$ is presented.

Fig. 13 (a) is the AC equivalent circuit when there is a disturbance signal in v_{o1}, and Fig. 13 (b) is the AC equivalent circuit when there is a disturbance signal in v_{o2}.From Fig. 13, the closed loop audio susceptibility can be obtained:

$$A_{v1\_AOT}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{o1}(s)} \quad (21)$$

$$A_{v2\_AOT}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{o2}(s)} \quad (22)$$

Under the combined effect of output voltage ripples $\hat{v}_{o1}(s)$ and $\hat{v}_{o2}(s)$, the total output voltage ripple $\hat{v}_o(s)$ is:

$$\hat{v}_{o\_AOT}(s) = \hat{v}_{o1}(s)A_{v1\_AOT}(s) + \hat{v}_{o2}(s)A_{v2\_AOT}(s) \quad (23)$$

The output waveform of the CCM mode of the Buck RS controlled by the AOT control with valley voltage detection is shown in Fig. 14. Where $v_s(n)$ is the sampled signal amount of the output voltage and $\Delta v_o(n)$ is the added output disturbance variable. The dotted line represents the output waveform after the disturbance is added, and the solid line is the output waveform during normal operation.

From Fig. 13 and Fig. 14, the slope m_1, m_2 can get respectively:

$$m_1 = \frac{v_{o2} - v_b}{L_b}R_{esr},\ m_2 = \frac{v_b}{L_b}R_{esr} \quad (24)$$

After the disturbance is added, the output voltage needs to keep stable. According to the modulation rule of the valley control algorithm [32], it can be known that the following relationship must be satisfied:

$$m_2t_{off} + v_{ref} = v_s(n) + m_1t_{on} \quad (25)$$

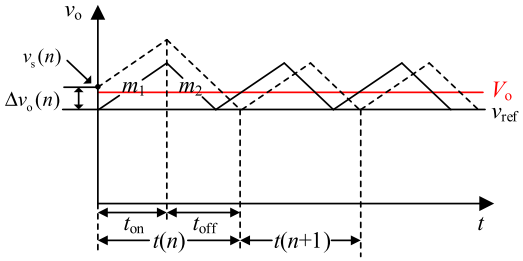


FIGURE 14. Key operating waveforms in continuous conduction mode.

According to the above analysis, it can be obtained that the t_{off} of the switch after the disturbance is:

$$t_{off} = \frac{v_s(n) + m_1t_{on} - v_{ref}}{m_2} \quad (26)$$

The relationship between the duty cycle and the sampled signal can be derived from the AOT control in steady state operation:

$$v_s(n) = v_o - \frac{1}{2}m_1t_{on} \quad (27)$$

$$d = \frac{t_{on}}{t_{on} + t_{off}} = \frac{m_2t_{on}}{(m_1 + m_2)\,t_{on} + v_s(n) - v_{ref}} \quad (28)$$

Plugging equations (1), (24) into (28), it can be obtained:

$$d = \frac{2v_bR_{esr}\gamma}{(v_{o2} + v_b)\,R_{esr}\gamma + 2L_bv_ov_{o2} - 2L_bv_{ref}v_{o2}} \quad (29)$$

where $\gamma = C_tV_{th}/g$.

In order to perform the analysis of the AC small signal model, the disturbances of the duty cycle, input voltage, output voltage, and reference voltage are set as $\hat{d}$, $\hat{v}_{o2}$, $\hat{v}_b$ and $\hat{v}_{ref}$, then making the following assumptions:

$$\begin{cases} d = \hat{d} + D & v_{o2} = \hat{v}_{o2} + V_{o2} \\ v_b = \hat{v}_b + V_b & v_{ref} = \hat{v}_{ref} + V_{ref} \end{cases} \quad (30)$$

From Fig.14, the following relationship for DC components can also be obtained:

$$V_o - V_{ref} = \frac{(V_{o2} - V_b)\,R_{ess}t_{on}}{2L_b} \quad (31)$$

Plugging equations (30) and (31) into (29), ignoring the higher-order terms and DC components of the quadratic term and above, it can be simplified as:

$$\hat{d} = K_{\text{ref}}\hat{v}_{\text{ref}} - K_{\text{v1}}\hat{v}_{\text{o1}} - K_{\text{v2}}\hat{v}_{\text{o2}} - K_{\text{v0}}\hat{v}_{\text{o}} \tag{32}$$

where

$$K_{ref} = \frac{DL_b}{R_{esr}\gamma}, K_{v1} = \frac{2-D}{2V_{o2}}, K_{v2} = \frac{DV_b}{2V_{o2}^2}, K_{v0} = \frac{DL_b}{R_{esr}\gamma} - \frac{2-D}{2V_{o2}}.$$

According to equation (32) and the open-loop transfer function obtained foregoing, the AC small signal block diagram of AOT control is shown in Fig. 15.

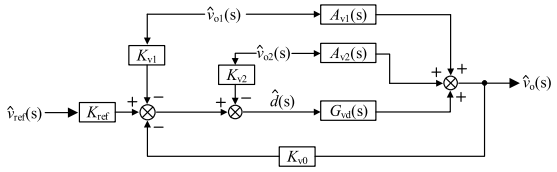


FIGURE 15. AC small signal block diagram of closed loop control.

According to Fig. 15, the closed-loop audio susceptibility $A_{\text{v1\_AOT}}$ and $A_{\text{v2_AOT}}$can be obtained:

$$A_{\text{v1\_AOT}}(s) = \frac{\hat{v}_{\text{o}}(s)}{\hat{v}_{\text{o1}}(s)} = \frac{A_{\text{v1}}(s) - K_{\text{v1}}(s)G_{\text{vd}}(s)}{1 + K_{\text{v0}}(s)G_{\text{vd}}(s)} \tag{33}$$

$$A_{\text{v2\_AOT}}(s) = \frac{\hat{v}_{\text{o}}(s)}{\hat{v}_{\text{o2}}(s)} = \frac{A_{\text{v2}}(s) - K_{\text{v2}}(s)G_{\text{vd}}(s)}{1 + K_{\text{v0}}(s)G_{\text{vd}}(s)} \tag{34}$$

According to Fig.15 and equations (23), (33) and (34), when the disturbance on reference voltage can be neglected, the disturbance component of the output voltage can be presented as:

$$\hat{v}_{\text{o\_AOT}}(s) = \hat{v}_{\text{o1}}(s)\frac{A_{\text{v1}}(s) - K_{\text{v1}}(s)G_{\text{vd}}(s)}{1 + K_{\text{v0}}(s)G_{\text{vd}}(s)} + \hat{v}_{\text{o2}}(s)\frac{A_{\text{v2}}(s) - K_{\text{v2}}(s)G_{\text{vd}}(s)}{1 + K_{\text{v0}}(s)G_{\text{vd}}(s)} \tag{35}$$

According to the same method, the disturbance component of the output voltage $v_{\text{o\_COT}}(s)$ during COT control can also be derived as:

$$\hat{v}_{\text{o\_COT}}(s) = \hat{v}_{\text{o1}}(s)A_{\text{v1\_COT}}(s) + \hat{v}_{\text{o2}}(s)A_{\text{v2\_COT}}(s) \tag{36}$$

where

$$A_{\text{v1\_COT}}(s) = \frac{\hat{v}_{\text{o}}(s)}{\hat{v}_{\text{o1}}(s)} = \frac{A_{\text{v1}}(s) - F_{\text{v1}}(s)G_{\text{vd}}(s)}{1 + F_{\text{v0}}(s)G_{\text{vd}}(s)} \tag{37}$$

$$A_{\text{v2\_COT}}(s) = \frac{\hat{v}_{\text{o}}(s)}{\hat{v}_{\text{o2}}(s)} = \frac{A_{\text{v2}}(s) - F_{\text{v2}}(s)G_{\text{vd}}(s)}{1 + F_{\text{v0}}(s)G_{\text{vd}}(s)} \tag{38}$$

where

$$F_{v1} = \frac{2-D}{2V_{o2}}, F_{v2} = \frac{D}{2V_{o2}}, F_{v0} = \frac{DL_b}{V_{o2}R_{esr}t_{on}} - \frac{2-D}{2V_{o2}}.$$

In order to analyze the DLF ripple suppression performance of Buck RS with AOT control, the parameters are set as: V_{o2} =35 V, V_{o1} =42 V, V_{ref} =48 V, V_{b} =6 V, C_{b} =47 μF, L_{b} =50 μH, t_{on} =1.2 μs, R = 46 Ω, R_{esr} =60 mΩ, D = 6/35, T_{s} = t_{on}/D = 7 μs, V_{th} =1 V, C_{t} =1.2 μF, g=1/35. According to audio susceptibility model, bode plots are drawn in Fig. 16. It can be seen from Fig.16 (a) that under AOT control, the audio susceptibility of v_{o1} to v_{o} is the same as that of COT control, because AOT control is essentially a feed-forward voltage loop that introduces the input voltage v_{o2} of the Buck RS and independent of input voltage v_{o1}. So, when there is a disturbance in v_{o1}, the disturbance of the total output voltage v_{o} is consistent with the COT control, and its audio susceptibility is -53 dB at 100 Hz. As can be seen from Fig. 16 (b), if Buck RS adopts AOT control, the audio susceptibility of v_{o} to v_{o2} is smaller than that of COT control, that is its audio susceptibility is -70.5 dB at 100 Hz, less than -59.5 dB of COT control. It can be known from equation (35) and (36), compared with COT control, the ripple of the output voltage can be better suppressed when using AOT control.

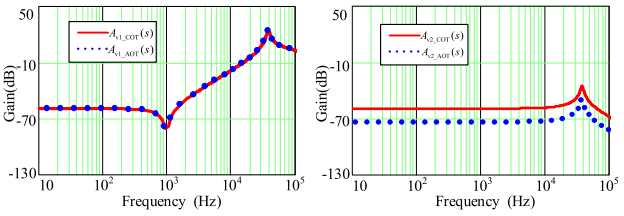


FIGURE 16. Bode plots of audio susceptibility. (a) $A_{\text{v1\_AOT}}$ (s) and $A_{\text{v1\_COT}}$ (s). (b) $A_{\text{v2\_AOT}}$ (s) and $A_{\text{v2\_COT}}$ (s).

C. TIME DOMAIN SIMULATION VERIFICATION

In order to verify the correctness of the above theoretical analysis, a simulation circuit was established based on PSIM software, and simulation was performed according to the parameters listed in Table 1.

Fig. 17 is the simulated waveforms of the output voltage ripple. From Fig. 17 (a), it can be seen that under COT control, the average value of v_{o1} of QSS Flyback PFC converter is 42 V and Δv_{o1} is 6 V, after supperssion of Buck RS, the average value of the total output voltage is 48 V, and Δv_{o} is 90 mV. It can be seen from Fig. 17 (b) that after using AOT control, the ripple Δv_{o} is 70 mV, which is less than the COT control. It can be obtained that the AOT-controlled Buck RS can effectively suppress the DLF ripple of QSS Flyback PFC converter, and the result is better than that of COT control, which conforms to the above conclusion.

According to equations (35), (36), the data in Table 1 and Fig. 17 can be calculated as follows:

$$\left|\hat{v}_{\text{o\_COT}}(s)\right|_{s=j2\pi f_{2L}} = 3 \times 10^{\frac{-53}{20}} + 2.3 \times 10^{\frac{-59.5}{20}} \approx 9.15\text{m}V$$

$$\left|\hat{v}_{\text{o\_AOT}}(s)\right|_{s=j2\pi f_{2L}} = 3 \times 10^{\frac{-53}{20}} + 2.3 \times 10^{\frac{-70.5}{20}} \approx 7.4\text{m}V$$

The results show that when COT control is adopted, the amplitude of v_{o} at $f_{2\text{L}}$ is 9.15 mV, and that of v_{o} at $f_{2\text{L}}$ in AOT control is 7.4 mV, indicating that Buck RS can effectively suppress DLF of v_{o} under the two control modes.

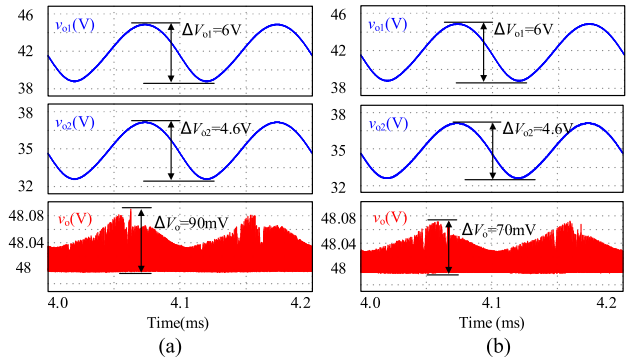


FIGURE 17. Output voltage waveforms with different control. (a) COT control. (b) AOT control.

The waveforms in Fig. 18 are Fast Fourier Transform (FFT) of v_o in COT and AOT control.

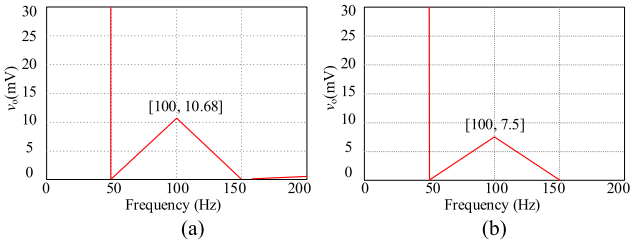


FIGURE 18. Output voltage ripple of FFT. (a) The result of COT control at f_{2L}. (b) The result of AOT control at f_{2L}.

From the FFT results, it can be seen that the component of v_o at f_{2L} is 10.68 mV in COT control, and the component of v_o at f_{2L} is 7.5 mV in AOT control.

The calculation results are close to the simulation results, and the deviation is caused by the approximate equivalent of the modeling. From the results of simulation and calculation, the theoretical analysis is proved correct.

Table 2 summarizes simulation results from Fig. 17.

TABLE 2. Simulation results of Buck RS under different control.

Control strategy	On-time	f_b	Δf_b	Δv_o
COT	1.2 μs	66 kHz~233 kHz	167 kHz	90 mV
AOT	1.1 μs~1.3 μs	72 kHz~214 kHz	142 kHz	70 mV

According to Table 2, it can be known that: 1) both AOT and COT controlled Buck RS can effectively reduce DLF voltage ripple Δv_o; 2) variation of switching frequency of AOT controlled Buck RS is about 85% of that of COT controlled.

VI. EXPERIMENTAL VERIFICATIONE

In order to prove the above theoretical analysis, the prototype of QSS Flyback PFC converter is designed. The circuit parameters are the same as Table 1. The R_{esr} of C_b is measured to be 106 mΩ. Based on previous analysis, this capacitor can ensure Buck RS work in stable state.

Fig. 19 illustrates the measured waveforms of QSS Flyback PFC converter when Buck RS adopts AOT control. From Fig. 19, the DLF ripple voltage Δv_{o1} of Flyback PFC converter is 6 V. The Buck RS produces a 180° phase shifted ripple voltage to suppress the DLF ripple voltage Δv_{o1}. The DLF ripple voltage of total output voltage is Δv_o =78 mV, which is larger than Δv_o =70 mV by simulation result. The difference between the simulation and experiment results comes from non-ideal characteristics of devices. The measured power factor at full load is 0.996.

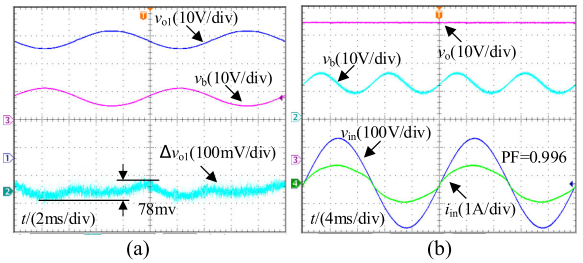


FIGURE 19. Experiment result. (a) v_{o1}, v_b and Δ v_o. (b) v_o, v_b, v_{in} and i_{in}.

Fig. 20 illustrates the measured results of variation of switching frequency with AOT control.

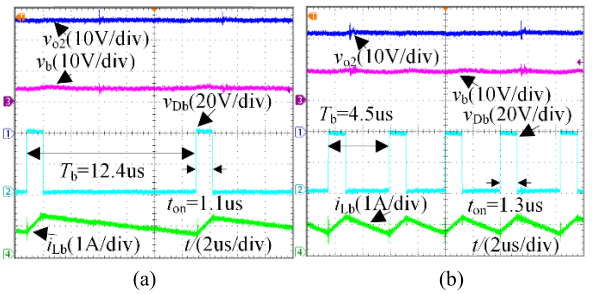


FIGURE 20. Experimental results of v_{o2}, v_b, v_{Db} and i_{Lb}. (a) f_{min}. (b)f_{max}.

Fig. 20 (a) shows that minimum switching frequency of Buck RS is 80.6 kHz, when the input voltage v_{o2} is the maximum and the on-time t_{on} is 1.1 μs. Fig. 20 (b) shows that maximum switching frequency of Buck RS is 222.2 kHz, when the input voltage v_{o2} is the minimum and the on-time t_{on} is 1.3 μs. The variation of switching frequency Δf_{b_AOT} of AOT control is 141.6 kHz, which is close to the simulation results.

Fig. 21 is an experimental waveform when the ESR of the Buck RS output capacitor C_b is small. According to the above stability analysis, a pulse cluster discovery phenomenon may occur.

In order to verify the effect of ESR on system stability, a small-capacity CBB capacitor is connected in parallel across C_b to reduce the value of ESR. The measured ESR after parallel connection is 10 mΩ that smaller than the calculated stable condition. According to the experimental results, when the ESR is reduced, the pulse cluster will occur in the circuit, and when the ESR is increased, the circuit can be restored to

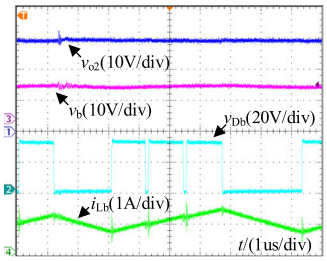


FIGURE 21. Output waveforms when ESR is small.

TABLE 3. Comparison of the other ripple suppressors.

	Control strategy	Po /W	Vo /V	Efficiency /%	$\frac{\Delta v_o}{v_o}$	LDRT	
Parallel	VMC	20	28	84	8	/	[13]
	FF	33	48	87	8	/	[10]
Series	VMC	30	50	85.5	3.32	/	[17]
	FF	50	48	88	4.16	/	[19]
	FF +QPR	50	48	88	1.2	20 ms	[20]
	COT	50	48	88.5	0.2	5 ms	[23]
	AOT	50	48	89.5	0.16	2 ms	Prop osed

the normal working state. The experimental results verify the effect of ESR value on stability.

Fig. 22 shows the dynamic performance. It can be seen from the waveform of v_{o1}that whenever the load decreases or the load increases, the output voltage v_o does not present a significant change. Although v_{o1} generates over/drop voltage, v_b can respond in time to suppress the over/drop voltage caused by the load variation. And can also be derived from Fig. 22, the QSS Flyback PFC converter has a fast load dynamic response, so that the output voltage v_o can achieve almost constant output voltage.

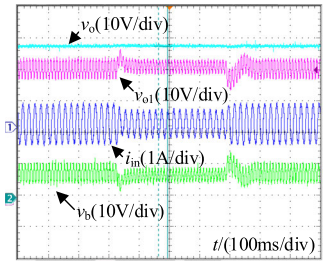


FIGURE 22. Dynamic waveforms: 100%-60% load and 60%-100% load.

Table 3 compares the efficiency, ripple suppression ratio and the dynamic response of the PFC with other parallel/series ripple suppressors.

It can be seen when Buck RS adopts AOT control, the QSS Flyback PFC converter has effective improvement in performance of ripple suppression ratio and efficiency. At the same time, the load dynamic response time (LDRT) has also been greatly decreased when the load changes.

VII. CONCLUSION

In this paper, the AOT control without compensation network is used to control Buck RS in QSS Flyback PFC converter with wide bandwidth and narrow switching frequency range, which suppresses output voltage DLF ripple effectively. The results show that the AOT control has a narrower switching frequency variation range than that of COT control. The stability of the Buck RS with AOT control is related to the value of equivalent series resistance in output capacitor, the pulse cluster finding phenomenon should be avoided. According to the analysis of the audio susceptibility model, it can be known that both AOT and COT control can well suppress the interference of v_{o1} and v_{o2} DLF ripple voltage on v_o, and the AOT control has better ripple suppression performance. The experimental results also show AOT-controlled QSS Flyback PFC converter has higher efficiency and faster dynamic response. Future works will focus on further reducing the switches frequency range by introducing new variables in AOT controller.

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