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Reverse Recovery of 50 V Silicon Charge Plasma PIN Diode

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ABSTRACT In this article, a novel approach is used for the first time to design a high-voltage PIN diode without any chemical doping process of cathode and anode region. This approach favors ''p'' and ''n'' plasma region formation through various metal contacts with appropriate work-functions for anode and cathode respectively. In this study, the forward and reverse characteristics, as well as the switching performance (reverse recovery) of this novel device, charge plasma (CP) PIN diode, were compared with the Schottky diode and the conventional PIN diode using TCAD simulation.

INDEX TERMS Charge plasma, PIN diode, reverse recovery.

I. INTRODUCTION

P-I-N, diodes are integrated into power electronics as power rectifiers for the high-voltage application [1]. Although the drift region of a PIN diode is near intrinsic, due to the high-level injection of minority carriers, the on-state resistance in the drift region is reduced. However, the same minority carriers are stored within the drift region of the power rectifiers, while the device is in on-state. While switching from forward to reverse bias, these stored charges in the drift region need to be removed before the rectifier can support any high-voltages. This carrier extraction process leads to huge reverse recovery current during switching from on-state to off-states, which is detrimental for application of PIN diodes as a switch. Moreover, PIN diodes are fabricated using high thermal budget processes to create deep P+ and N+ regions by either ion-implantation or diffusion, including multiple steps. This complex and expensive fabrication process could be avoided using, charge plasma doping-less approach.

There have been several studies on different semiconductor devices utilizing the CP concept. Nano scale p-n diodes have been designed and fabricated using charge plasma concept [2]–[4]. Lateral and vertical bipolar junction transistors (BJTs) [5]–[8], LSMOS, SJ VSDMOS, transistirs, Bi-directional Junction-less Transistor, PIN diode, IMOS, TFETs [9]–[20]. The CP approach not only reduces the fabrication complexity but also results in an improved performance.

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In this article, for the first time, a high-voltage PIN diode is proposed without the need for high-temperature diffusion or annealing procedures utilizing the charge plasma approach. In this charge plasma PIN (CP-PIN) diode, the same approach as charge plasma p-n diode was considered, the ''p'' and the ''n'' regions are formed in an intrinsic silicon layer by using an anode metal electrode with the work-function $\Phi_{m,A} > (\chi_{Si} + E_g/2)$, and a cathode metal electrode with work-function $\Phi_{m,C} < (\chi_{Si} + E_g/2)$, respectively [2].

The forward characteristics, reverse characteristics as well as reverse recovery of the proposed PIN diode, is compared with the Schottky diode and the conventional PIN diode utilizing TCAD 2D-simulations [21].

II. DEVICE STRUCTURE AND PARAMETERS

The cross-sectional view of the conventional PIN diode, Schottky diode and the proposed CP-PIN diode are shown in Fig. 1. In Fig. 1(a) P^+ and N^+ indicate the doped anode and cathode regions in conventional chemically doped PIN diode, respectively. In Fig. 1(b) which represents the Schottky diode, ${P^+}_{CP}$ depicts induced positive charges due to the Schottky contact at the anode side and N^+ indicates the doped cathode region. Fig. 1(c) depicts the charge plasma PIN diode and ${P^+}_{CP}$ represents induced positive charges and ${N^+}_{CP}$ indicates induced negative charges in silicon.

Since band gap of silicon $E_g = 1.14\ eV$, and the electron affinity of bulk silicon $\chi_{Si} = 4.17\ eV$, therefore $\Phi_{m,A} > 4.74\ eV$ and $\Phi_{mC} < 4.74\ eV$. For optimal rectifying behavior, the difference between two work-functions should be

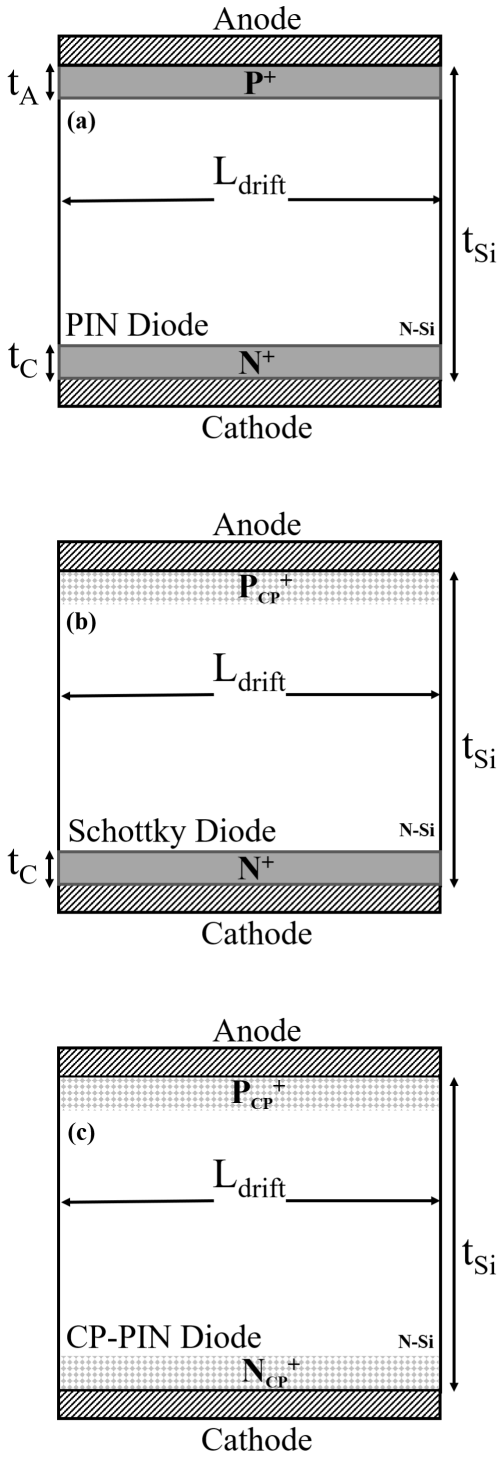

FIGURE 1. Cross-sectional view of the (a) Conventional PIN diode, (b) Schottky diode and (c) Proposed CP-PIN diode.

at least 0.5 eV [2]. Considering a 50 V breakdown voltage for high voltage application, analytical solutions for the doping concentration and the corresponding maximum depletion layer width can be derived for silicon [1]:

$$N_{Si} = 5.34 * 10^{13} / V_{Beakdown}^{4/3} \approx 1e16. \quad (1)$$

$$W = 2.67 * 10^{10} * N_{Si}^{-7/8} \approx 2.51\ \mu m. \quad (2)$$

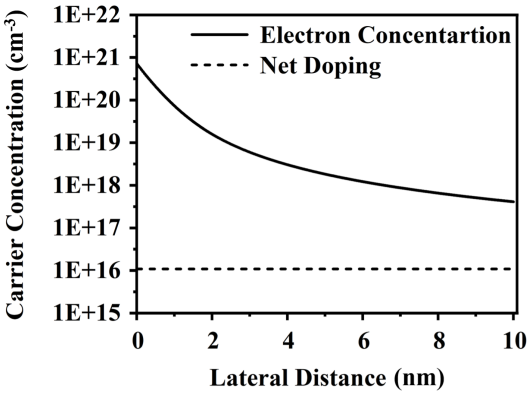

FIGURE 2. Electron concentration and net doping profile underneath an n-type metal contact $\Phi_{mC} = 3.9\ eV$ within 10 nm distance from the metal cathode contact into the silicon.

Hafnium with the work-function of 3.9 eV [6] is used as the cathode electrode, and the work-functions of 4.9 eV [1], [4], is used as the anode electrode to induce electron and hole plasma to create cathode and anode regions, respectively.

The electrons and holes generated due to the work-function difference, are concentrated in silicon at the silicon/metal interface. The concentration of the charge plasma carriers degrades as the distance from the interface increases. The Debye length $L_D = [(\epsilon_{si} \cdot \upsilon_t) / (q \cdot N)]^{1/2}$ (ϵ_{si} is the dielectric constant of silicon, υ_t is the thermal voltage, and N is the carrier concentration in the body), is the distance which ensures the distribution of these carries within the silicon to be higher than the background doping. The typical value of L_D is 15 nm for silicon [2].

Fig. 2 illustrates the distribution of the induced electrons at the cathode side. We observe that the induced electron plasma concentration is at least one order of magnitude higher concentration than the net doping concentration within a distance of 10 nm from the interface. Therefore, 10 nm thick doping regions were considered in the conventional PIN diode as well as Schottky, to have a fair comparison between the three structures.

Detailed design parameters [1] are mentioned in Table 1. Simulations were performed using field and concentration-dependent mobility, Shockley-Read-Hall recombination, Fermi-Dirac statistics, impact ionization, thermionic emission, surface recombination, and barrier lowering models with default silicon parameters. Ohmic contact conditions are assumed for the metal-silicon contacts with negligible contact resistances [21].

III. SIMULATION RESULTS AND DISCUSSION

A. FORWARD AND REVERSE CHARACTERISTICS

Fig. 3 compares the carrier concentration of CP-PIN diode with conventional PIN diode under thermal equilibrium condition, along the vertical cut-line through 2.51 μm thick silicon, from anode (at 0.0 μm) all the way to the cathode side (2.51 μm). As indicated in Fig. 3, the work-function

TABLE 1. Key structure and design parameters.

-	PIN	Schottky	CP-PIN
$t_A\ nm$	10	-	-
$t_C\ nm$	10	10	-
$t_{Si}\ \mu m$	2.51	2.51	2.51
$L_{drift}\ \mu m$	1	1	1
$P^+\ cm^{-3}$	5e19	-	-
$N^+\ cm^{-3}$	5e19	5e19	-
$N_{Si}\ cm^{-3}$	1e16	1e16	1e16

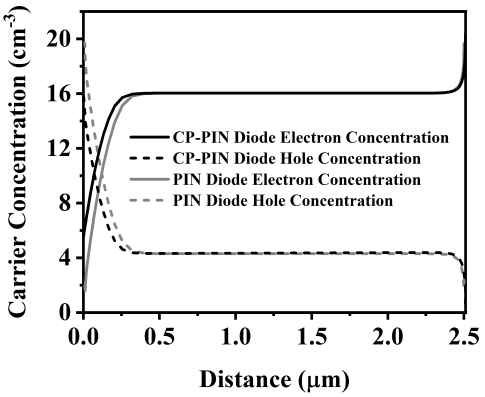

FIGURE 3. Vertical thermal equilibrium carrier concentrations in the CP-PIN diode with metal contacts $\Phi_{mC} = 3.9\ eV$ and $\Phi_{mA} = 4.9\ eV$ and PIN diode with doping concentration of $N^+ = 5e19\ cm^{-3}$ and $P^+ = 5e19\ cm^{-3}$.

difference in the silicon film leads to the formation of a CP-PIN diode without chemical doping process.

In Fig. 4 the forward characteristics of the CP-PIN diode is compared with the forward characteristics of the Schottky diode and the conventional PIN diode. The current transport in the CP-PIN diode and the Schottky diode which have the metal-semiconductor junction is mainly due to the majority carriers as opposed to the minority carriers in a p-n junctions. The current transport in a rectifying contact with an n-type semiconductor is due to the thermal emission [22]. Consequently as can be observed in Fig. 4(a) and Fig. 4(b) the forward characteristic of the CP-PIN is almost identical to the Schottky diode forward characteristic.

This is because the current mechanism of the CP-PIN diode is determined by thermionic emission of the majority carriers over a potential barrier like Schottky diode [22] while for PIN diode is based on the diffusion of minority carriers [1]. Therefore, as shown in Fig. 4(c), the Schottky diode and CP-PIN diode has a turn-on voltage of ∼0.4 V at the on-state current density of 100 A/cm^2, which is approximately 0.35 V smaller than the turn-on voltage of the conventional PIN diode.

The reverse-saturation current in a silicon p-n junction is dominated by the generation current. The leakage current for Schottky rectifiers Due to the relatively small barrier height utilized in silicon Schottky rectifiers, is dominant by the thermionic emission component [1]. The reverse-saturation

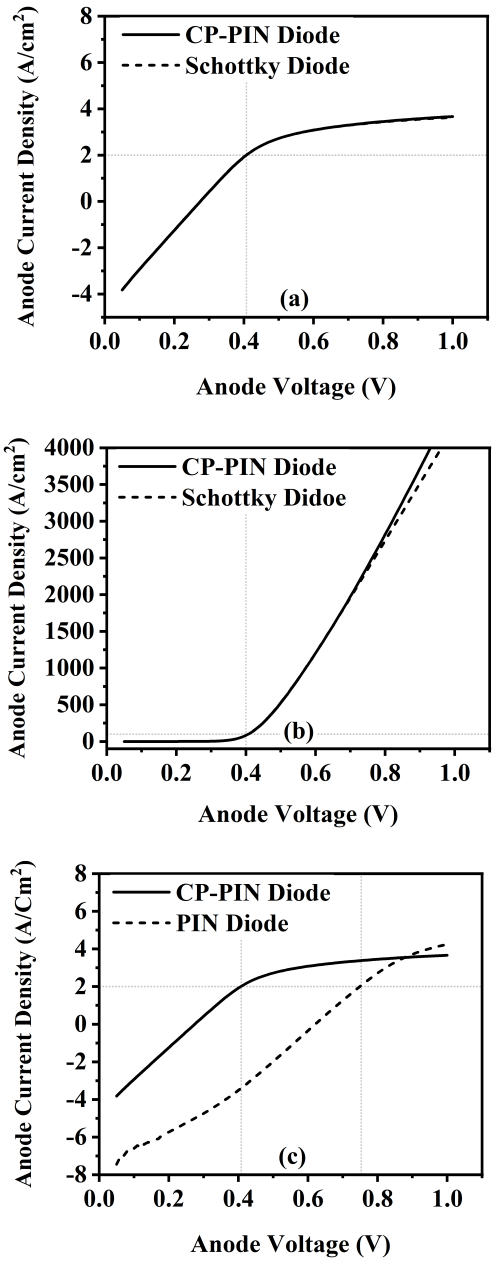

FIGURE 4. (a) Semi log forward characteristics, (b) Linear forward characteristics, (b) Linear forward characteristics.

current density of the Schottky barrier junction due to the thermionic emission process is at least order of magnitude higher than that of the p-n junction diode, which may vary depending upon the work-function of the Schottky contact material in use and temperature [1], [22]. Fig. 5 illustrates the reverse characteristics of the CP-PIN diode, Schottky diode and PIN diode. Fig 5.(a) shows the semi-log reverse characteristics of the CP-PIN diode and the Schottky diode, which have a very similar profile because of the same thermionic emission process. Fig 5(b) clearly demonstrates the difference between reverse characteristics (reverse-saturation currents) between CP-PIN diode and the conventional PIN diode.

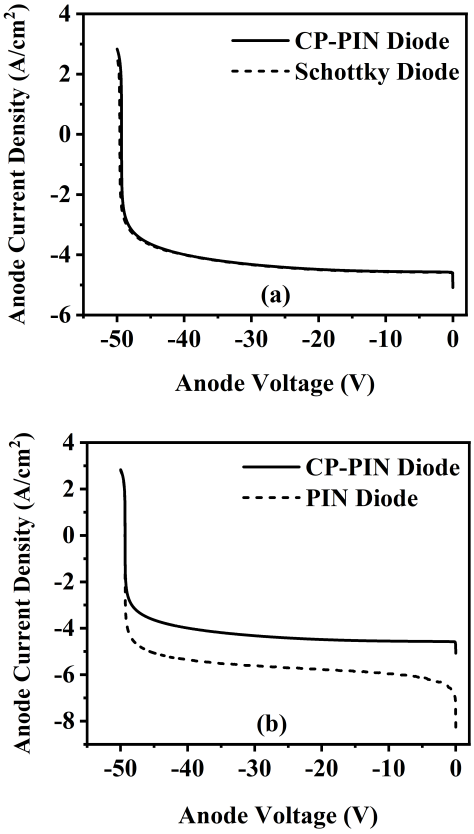

FIGURE 5. (a) Semi log reverse characteristics of CP-PIN diode and PIN diode, (b) Semi log reverse characteristics of CP-PIN diode and Schottky diode.

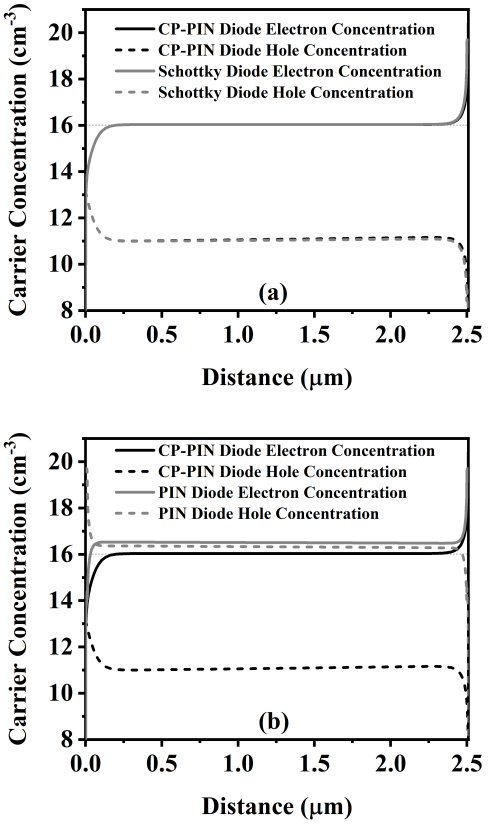

FIGURE 6. Semi log carrier concentration profile of (a) The CP-PIN diode and the Schottky diode, (b) CP-PIN diode and the conventional PIN diode, in the drift region under on-state operation voltages.

B. SWITCHING CHARACTERISTICS

A Schottky diode differs from a p-n junction diode in two properties: a) is magnitudes of the reverse-saturation current densities, and b) is in the switching characteristics [22]. These differences are mainly due to the different current transport mechanism between p-n junction and metal-semiconductor junction. Since CP-PIN diode uses a Schottky contact, its characteristics are similar to the Schottky diode and different as compared to the chemically doped conventional PIN diode.

At high current density of 100 A/cm^2, the injected carrier density in the drift region of the PIN diode exceeds the background doping concentration. During on-state, due to the high concentration of these minority carriers, the on-state voltage drop is low, since the resistivity of the drift region is also low [1]. Fig. 6 indicates the carrier concentration profile of the CP-PIN diode, the Schottky diode and the conventional PIN diode under forward bias at current density of 100 A/cm^2 along the vertical cut-line from anode region to cathode region, where the anode is considered to be a reference point (0.0 μm) and the cathode is considered to be the end point (2.51 μm). As can be seen from Fig. 6, at high forward current density of 100 A/cm^2 the minority carrier concentration of the PIN diode exceeds the background doping of 10^{16} cm^{-3}, while in case of the CP-PIN diode and the Schottky diode, the minority carrier concentration remains lower than the background doping. Therefore, Fig. 6 confirms the negligible impact of minority carries as well as a small concentration of stored charges in the drift region of Schottky diode and the CP-PIN diode.

Fig. 7(a) shows a circuit with an inductive load [23], which used to measure the reverse recovery of diodes. The element D is an ideal diode which is built-in within the Silvaco Atlas [18]. Fig. 7(b) displays the waveforms of the voltage which is being applied to the gates of the MOSFETs. The duration of these waveforms dictates the application of the $V_{Forward}$ and $V_{Reverse}$ voltages, respectively, to the device under test (DUT).

At $t = t_1$ the (DUT) is forward biased, the value of $V_{Forward}$ and resistor are chosen in such a way to determine the bias current, which in our case is on-state operation current density of 100 A/cm^2. At $t = t_2$ the second half of the circuit comes into effect to reverse bias the DUT.

Fig. 8 depicts the reverse recovery of the devices devices, CP-PIN diode, Schottky diode and conventional PIN diode. As it can be seen devices are forward biased till $t = t_1$ with the forward current density of 100 A/cm^2. At $t = t_2$ as soon as the DUTs are reversed biased the current overshoot known as reverse recovery occurs. As represented in Fig. 8(a) and Fig 8(b) the reverse recovery of CP-PIN diode is comparable with the reverse recovery of the Schottky diode as a result of similar current transport mechanism.

During forward bias of PIN diode the presence of a large concentration of the carriers in the drift region is responsible

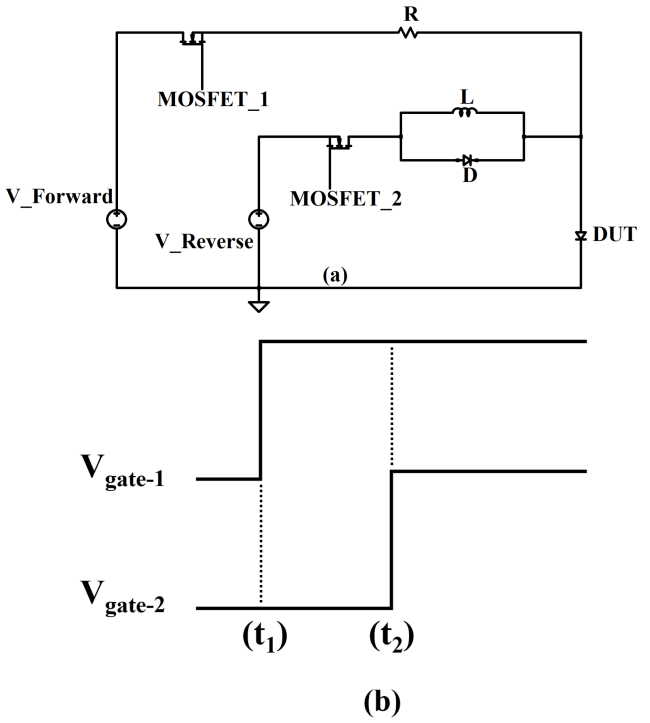

FIGURE 7. (a) Circuit schematic of reverse recovery characterization and (b) The switching waveform of the MOSFETs. t_1 and t_2 indicate time of the forward and reverse bias.

for the lower on-state resistance and consequently, lower voltage drop. As was discussed in Fig. 6, the concentration of these carriers in case of PIN diode is above the background doping. To switch the device from its on-state to the reverse bias depletion region must be formed to support the high reverse electric field in the blocking mode. And this will not be achieved unless these carriers are sufficiently removed from drift region [1]. Therefore the diode is switched from forward to reverse bias, the current does not monotonically reduce to zero. While these excess carriers are being removed by the electric field in the reverse bias mode, there will be an overshoot of current which is known as reverse recovery current [1].

On the other hand, in case of the CP-PIN diode and the Schottky diode, due to the nature of Schottky contact, there are no minority carriers in the drift region during forward bias [22]. As shown in Fig. 6 the negligible effect of minority carriers, makes the CP-PIN diode and the Schottky a majority carrier device thus, as the switching happens from forward to reverse bias, there is hardly any time required for the CP-PIN diode and the Schottky diode to switch into the blocking mode, therefore, the reverse recovery time is nearly zero in these devices. Fig. 8(c) clearly exhibits the differences between the reveres recovery of the CP-PIN diode and the PIN diode.

A lower reverse recovery is desirable to reduce voltages developed across stray inductance in any circuit. These voltages cause an increase in the voltage supported by all the devices in the circuit, making it necessary to enhance

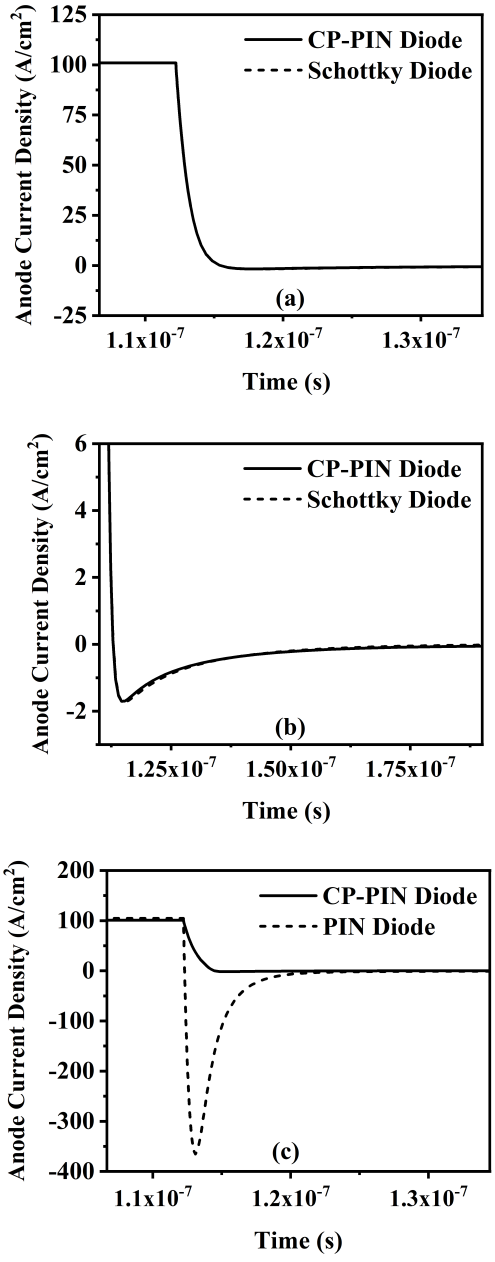

FIGURE 8. (a) Switching characteristics of the CP-PIN and the Schottky diode, (b) Switching characteristics of the CP-PIN diode and the Schottky diode with a zoomed-in view of the reverse recovery peak and (c) comparison of switching characteristics of the CP-PIN diode and the PIN diode. $R = 0.1\ \Omega$ and $L = 2\ nH$.

breakdown voltages. This is detrimental to system performance as it increases the overall power dissipation in the semiconductor components [1].

The rate of the switching has a great impact on the value of reverse recovery current. If the rate is high, the time needed to remove the stored charges is limited, which causes higher reverse recovery current. Therefore smaller value for the ramp rate is desirable.

In the circuit mentioned in Fig. 6. the value of the inductor determines the rate of the switching. Fig. 9 indicates the reverse recovery response of the CP-PIN diode, the Schottky

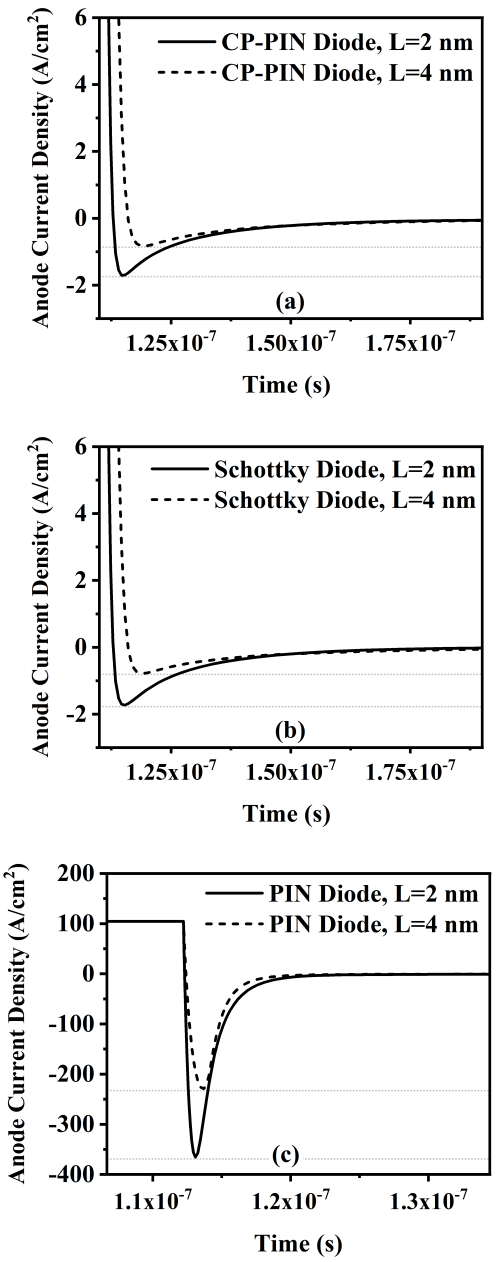

FIGURE 9. Reverse recovery of the (a) CP-PIN diode, (b) Schottky diode and (c) Conventional PIN diode, for two different inductive loads of 2 *nH* and 4 *nH*.

diode and the PIN diode for two different inductor values. Increasing the value of inductor reduces the switching rate and consequently the peak of the reverse recovery current is lower and the recovery is smoother towards the blocking mode.

IV. CONCLUSION

Design of a 50 V silicon PIN diode using charge plasma (CP) technique has been studied in this article. This approach eliminates the high thermal budget and expensive steps in fabrication process. A conventional 50 V PIN diode and a Schottky diode with structure and parameters comparable to the charge plasma PIN (CP-PIN) diode are specifically designed to have a better assessment of CP-PIN diode while analyzing the forward and reverse characteristics as well as the switching properties. All these designs and simulations are done by the Silvaco ATLAS device simulation software. Due to the nature of Schottky contact and p-n junction current mechanism, the CP-PIN diode exhibits almost identical forward characteristics as the Schottky diode and a lower voltage drop at on-state current density of 100 A/cm^2 in compare with the conventional PIN diode. In terms of reverse bias, the CP-PIN diode and the Schottky diode have a similar reverse characteristics. Also due to the differences between a p-n junction and the Schottky contact, the reverse saturation current density of the CP-PIN diode and the Schottky diode are higher than the reverse saturation current density of the conventional PIN diode. Since the switching loss of power semiconductors within the power electronic circuits is of great interest, the CP-PIN diode switching characteristics from on-state to off-state known as reverse recovery, is also compared with the Schottky diode and the PIN diode. The results indicate that the CP-PIN diode has a consistent switching characteristic as the Schottky diode, and unlike the PIN diode, due to the negligible presence of carriers within the drift region during on-state, the reverse recovery of the CP-PIN diode is significantly lower which leads to lower switching loss. Reducing the switching rate results in a lower reverse recovery of CP-PIN diode. The lower on-state voltage drop, being inexpensive with low thermal budget as well as low switching loss makes CP-PIN diode a lucrative contender for power electronics.

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