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4th-Order Switched-Current Multistage-Noise-Shaping Delta-Sigma Modulator With a Simplified Digital Noise-Cancellation Circuit

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ABSTRACT This paper proposes a fourth-order (2-2) switched-current (SI) multistage-noise-shaping (MASH) delta–sigma modulator (DSM) with a simplified digital noise-cancellation circuit (DNCC) by using a Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm 1P6M CMOS process. In view of area-efficiency, we propose a small-area current-mode sample-and-hold circuit (S/H) with a modified feedback memory cell (FMC) and cross-connected bias circuit. As a result of modifications to the feedback impedance, the input impedance of the current-mode differential FMC was decreased by $[2 + (g'_{m3}/g_{m1} - 1) \times A]$ times relative to a traditional FMC. Any input current can be processed faster than usual given low input impedance. The MASH architecture inherited a superior signal-to-noise ratio (SNR) due to a simplified DNCC, consisting of six unit-delay circuits using a master–slave D flip-flop (DFF) and a logic circuit using a Karnaugh map. Post-layout simulations reveal that the simulated SNR was 87.1 dB and the effective number of bits (ENOB) was 14.18 bits. Measurements indicated that the SNR was 64.5 dB and the ENOB was 10.42 bits—at a sampling frequency of 10.24 MHz, an oversampling ratio of 256, a signal bandwidth of 20 kHz, and a supply voltage of 1.8 V. The designed chip was measured to have a power consumption of 18.19 mW, a chip area of 0.13 mm^2, and a measured figure of merit (FoM) of 331.9 (pJ/conv-step). The advantages of our modulator are its small chip area and high processing speed at all input currents.

INDEX TERMS Delta–sigma modulator, switched-current, multistage-noise-shaping, feedback memory cell, digital noise-cancellation circuit, master–slave DFF, Karnaugh map.

I. INTRODUCTION

The key motivation of this study is to develop a new high-order switched-current multistage-noise-shaping (SI MASH) delta–sigma modulator (DSM) with a digital noise-cancellation circuit (DNCC) for applications in motor drive systems, whose bandwidths vary from dc to a few several kilohertz (kHz). For instance, a typical Hall sensor used for motor control operates within a bandwidth that ranges from dc to 25 kHz [1]. A second-order SI DSM was applied in a motor drive with a digital space vector pulse width modulator (SVPWM) [2]. However, quantization noise is a major concern in second-order modulators because quantization noise limits the resolution of analog-to-digital converters (ADCs). One study on a high-order DSM for high-resolution applications reported that high-order quantization error shaping can be achieved easily through either a single-loop or multi-loop architecture [3]. Unfortunately, those second-order or high-order modulators are liable to become unstable, especially for large-input signals [4]. As an alternative, the MASH

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architecture prevents instability by connecting several stable low-order modulators in cascade. The MASH architecture cancels the low-order quantization noise from the previous stage of the DSM by using an effective DNCC [5]. The motivation of this study is to produce a small-area chip of the 2-2 SI MASH DSM with an on-chip DNCC for three-phase induction motor (IM) drive system; its produced chip was fabricated in a Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process.

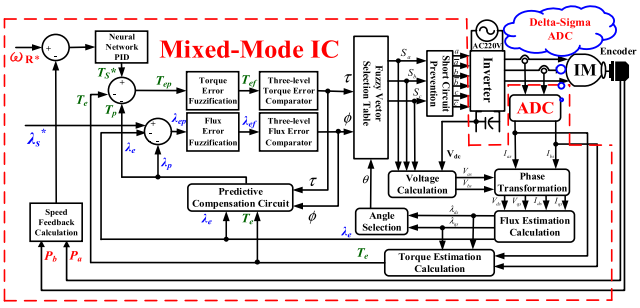

FIGURE 1. Proposed predictive direct torque control mixed-mode IC with fuzzy voltage vector control and neural network PID speed controller, which is composed of an analog IC of the delta-sigma ADC and a digital IC of the motor control ASIC.

Figure 1 shows the proposed predictive direct torque control (DTC) mixed-mode IC with fuzzy voltage vector control and neural network PID speed controller, which is composed of an analog IC of the delta-sigma analog-to-digital converter (ADC) and an application-specific integrated circuit (ASIC) of the three-phase induction motor (IM) drive. The functional block diagram of the proposed ASIC includes the following block diagrams: voltage calculation, phase transformation, flux estimation, torque estimation, angle selection, predictive compensation circuit, speed feedback calculation, neural network PID controller, torque error fuzzification, three-level torque error comparator, flux error fuzzification, three-level flux error comparator, fuzzy vector selection table, and short-circuit prevention. The proposed ASIC is a digital IC, which generally occupies much space in the entire mixed-mode IC. In view of the design of delta-sigma ADC, a 4th-order SI MASH DSM is proposed with a simplified DNCC because of its small chip area. In switched-capacitor (SC), the sampling capacitor is the parasitical capacitor between the spread lines, whereas in SI, the parasitical capacitor is between gate and source of the MOSFET (C_{gs}). Therefore, the chip area in SI is smaller than that in SC [6]. The SI technique is effective for three-phase IM drive system with a small chip area and a suitable resolution (ENOB $\geq$ 10 bits), even though it suffers from non-linearity that is caused by the harmonics in the SI memory cell [7].

The fundamental problem in MASH architecture is the noise leakage, which is due to the mismatch between the analog coefficients and compensating DNCC. An effectively designed MASH architecture can deliver a high signal-to-noise and distortion ratio (SNDR) if its designers correctly considered process variations, thermal noise types, and quantization errors [8]. To counteract this mismatch, the analog circuit must be carefully designed. Relative to a switched-capacitor circuit, a switched-current (SI) circuit performs better owing to its high speed, small chip area, and low supply voltage [9]. Unfortunately, an SI circuit can suffer from transmission errors, clock feedthrough (CFT) errors, nonlinearity, and high power consumption [10]. The CFT errors can be minimized by means of a current minimum function in place of a sampling switch [11]. The transmission speed can be improved by reducing the input impedance by a factor of two. Furthermore, the transmission error can be minimized with the assistance of a current-mode feedback memory cell (FMC) and a common-mode feed-forward (CMFF) circuit. Those adopted circuits not only minimize the offset current but also improve the linearity [12].

Various digital calibration techniques have been published to extract noise and distortion from desired signals [13], [14]; these techniques can deliver high-SNDR ADCs. As reported in [15], a least mean squares (LMS) algorithm-based adaptive line enhancer can assess a desired signal from an input noise signal by informing DNCC coefficients, leading to an enhancement of SNR by >20 dB. The LMS-based arrangement delivers a superior matching coefficient between the analog modulator and DNCC. A study reported a DNCC that occupied a chip area of 0.59 mm^2 with respect to the total active area of 0.68 mm^2; that device consumed a power of 47 mW relative to a total power of 183 mW [16]. Any digital calibration technique, such as DNCC, is complex and occupies the majority of chip area, thus precluding high power consumption.

In this study, a fully differential 2-2 SI MASH DSM with a simplified DNCC was fabricated using TSMC's 0.18 μm 1P6M CMOS process. Simulated and measured results were completed with a bandwidth of 20 kHz, an oversampling ratio of 256, a sampling frequency of 10.24 MHz, and a supply voltage of 1.8 V. The features of this study's device are excellent SNR, a small chip area, and a high figure of merit (FoM)—from the current-mode S/H circuit with modified FMC, cross-connected bias circuit, and simplified DNCC. The rest of this paper is organized as follows. Section II elucidates the system design of the 2-2 SI MASH DSM and its circuit, implemented with a current-mode S/H circuit with two modified FMCs and a differential cross-connected bias circuit. Section III explains the circuit design of the simplified DNCC using a Karnaugh map and its logic circuit, implemented with master–slave DFFs and NAND–NAND circuits. Section IV presents the simulated and measured results. Section V presents the conclusions.

II. SYSTEM DESIGN OF THE PROPOSED 2-2 SI MASH DSM

Figure 2 displays a block diagram of the 2-2 SI MASH DSM with a 1-bit quantizer, which is composed of two cascade second-order modulators: one for the primary stage and the other for the secondary stage. The proposed topology performs with a completed stability in the perspective of

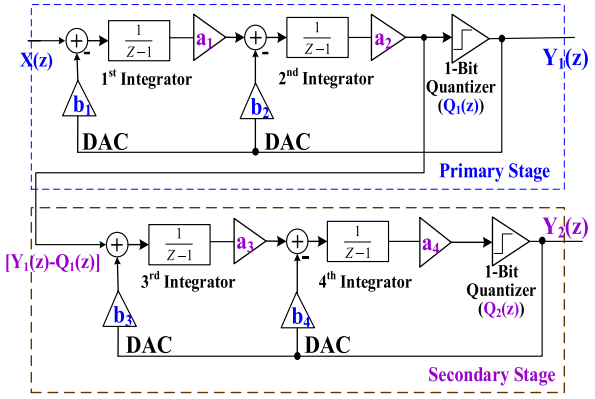

FIGURE 2. Block diagram of the proposed 2-2 SI MASH delta-sigma modulator.

lower-order modulation, whose order is ≤ 2 [4]. As illustrated in Fig. 2, the primary stage is a second-order modulator, which includes two discrete-time integrators, two digital-to-analog converters (DACs), and a 1-bit quantizer. Not only in the first integrator but also in the second integrator, each output swing relies on the input range of the previous integrator and the gain of a DAC. For instance, the first integrator receives the input function, which is equal to $(X(z)-b_1Y_1(z))$ with the input signal $X(z)$; the gain of DAC b_1; and the output signal of the primary stage $Y_1(z)$. The first integrator then drives the second integrator by multiplication with an analog coefficient a_1. Next, the second integrator is fed with a combined function—which contains the output of the first integrator, an analog scaling coefficient a_1, DAC gain b_2, and the output of the primary stage $Y_1(z)$. The output of the second integrator is connected to the following 1-bit quantizer with a quantization error $Q_1(z)$. In a manner similar to that of the secondary stage, the input signal $X(z)$ is replaced with $(Y_1(z)-Q_1(z))$ and those DAC gains and analog coefficients are adjusted. The maximum levels of the in-band input signals, $X(z)$ and $(Y_1(z)-Q_1(z))$, must remain within the maximum levels of the feedback signals, $Y_1(z)$ and $Y_2(z)$, respectively, to maintain the stability of the modulator.

A. 2-2 SI MASH DELTA-SIGMA MODULATOR

The primary stage of the 2-2 MASH DSM comprises two discrete-time integrators, two 1-bit DACs, and a 1-bit quantizer; this stage forms a second-order modulator. To obtain high performance, an integrator must be insensitive to the sampling frequency. This can be accomplished using a SI integrator, which provides an area reduction of approximately 72% compared with a switched-capacitor (SC) integrator [6]. Furthermore, the operating speed of the SI FMC is about 70% greater than that of the traditional FG SI MC [17]. If the quantization errors of the 1-bit quantizer are $Q_1(z)$ and $Q_2(z)$ in the primary stage and secondary stage, respectively, the signal transfer functions, STF_1 and STF_2, and noise transfer functions, NTF_1 and NTF_2, of the primary stage and secondary stage are expressed as follows:

$$Y_1(z) = STF_1 \cdot X(z) + NTF_1 \cdot Q_1(z) \quad (1)$$

$$Y_2(z) = STF_2.\left[Y_1(z) - Q_1(z)\right] + NTF_2.Q_2(z) \quad (2)$$

where

$$STF_1 = \frac{a_1a_2z^{-2}}{1+(a_2b_2-2)\,z^{-1}+(1+a_1a_2b_1-a_2b_2)\,z^{-2}} \quad (3)$$

$$NTF_1 = \frac{\left(1-z^{-1}\right)^2}{1+(a_2b_2-2)\,z^{-1}+(1+a_1a_2b_1-a_2b_2)\,z^{-2}} \quad (4)$$

$$STF_2 = \frac{a_3a_4z^{-2}}{1+(a_4b_4-2)\,z^{-1}+(1+a_3a_4b_3-a_4b_4)\,z^{-2}} \quad (5)$$

$$NTF_2 = \frac{(1-z^{-1})^2}{1+(a_4b_4-2)\,z^{-1}+(1+a_3a_4b_3-a_4b_4)\,z^{-2}} \quad (6)$$

The signal transfer function (STF) and the quantization noise transfer function (NTF) of each modulator depend on the analog scaling coefficients and DAC gains. These coefficients and gains are selected for minimal quantization noise, superior signal levels in the transition, and physically realizable blocks, such as integrators and DACs [11], [17]. The analog scaling coefficients of the modulator and the DAC gains are listed in Table 1.

TABLE 1. Analogue scaling coefficients and DAC gains.

analogue coefficients				DAC gains			
a_1	a_2	a_3	a_4	b_1	b_2	b_3	b_4
0.5	0.5	0.5	2.0	1.0	1.0	1.0	1.0

From Table 1, we have:

$$Y_1(z) = \frac{1}{1-1.5z^{-1}+0.75z^{-2}} \times \left[0.25z^{-2} \times X(z) + \left(1-z^{-1}\right)^2 \times Q_1(z)\right] \quad (7)$$

and

$$Y_2(z) = z^{-2}\left[Y_1(z) - Q_1(z)\right] + \left(1-z^{-1}\right)^2 \times Q_2(z) \quad (8)$$

As illustrated in Fig. 3, the system requires a delay unit (z^{-1}) to complete an integrator. The function of the integrator can be expressed as follows:

$$[X(z) + Y(z)] \times z^{-1} = Y(z) \quad (9)$$

$$\frac{Y(z)}{X(z)} = \frac{z^{-1}}{1-z^{-1}} = \frac{1}{z-1} \quad (10)$$

Two current-mode sample-and-hold circuits, S/H-1 and S/H-2, are used to establish a delay unit (z^{-1}). If one integrates the non-overlapping clocks, ϕ_1 and $\overline{\phi_1}$, with the specifications of a sample-and-hold circuit (S/H), the desired sample-and-hold circuit can be implemented with a pair of FMCs.

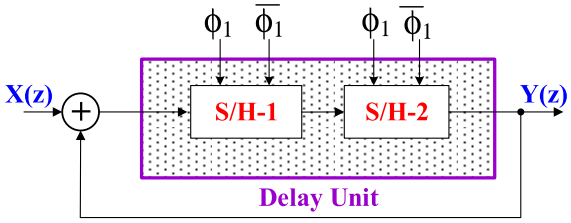

FIGURE 3. Block diagram of the current-mode integrator.

B. PROPOSED SWITCHED-CURRENT FEEDBACK MEMORY CELL

A traditional FMC, which was reported in [11], offered a system with low input impedance and small transmission error. The input impedance R_{in} of the traditional FMC is given by

$$R_{in} = \frac{1}{2g_{m1}}, \tag{11}$$

where g_{m1} is the transistor transconductance of the first input MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor). In general, a diode-connected NMOS transistor introduces an input impedance of $1/g_m$. The input impedance of the traditional FMC is half that of a diode-connected NMOS transistor. The lower the input impedance is, the higher the transmission rate is.

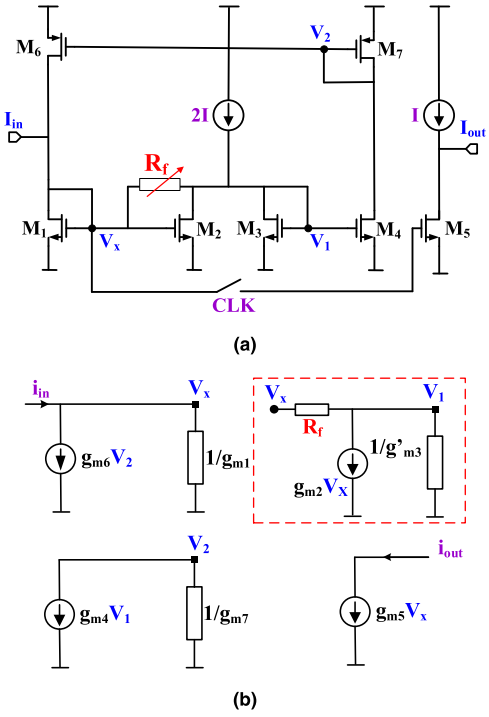

FIGURE 4. Proposed feedback memory cell. (a) Detailed circuit, (b) Small-signal modeling.

Figure 4 depicts the proposed FMC and its small-signal modeling. From the small-signal modeling, the current transfer function is given by

$$\frac{i_{out}}{i_{in}} = \frac{g_{m5}}{(g_{m1}+g_{m2}) + \left(g'_{m3} - \frac{g_{m4}g_{m6}}{g_{m7}}\right) \times A}, \tag{12}$$

where

$$i_{out} = g_{m5}V_x \tag{13}$$
$$i_{in} = g_{m1}V_x + g_{m6}V_2 + g_{m2}V_x + g'_{m3}V_1 \tag{14}$$
$$V_2 = -g_{m4}V_1 \times \left(1/g_{m7}\right) \tag{15}$$
$$V_1 = A \times V_x \tag{16}$$

Specifically, g_{mi} is the transconductance of the i^{th} MOSFET and A is the voltage gain (i.e., $A = V_1/V_X$). As formalized in (12) and (13), the input impedance R_{in} is given by

$$R_{in} = \frac{V_x}{i_{in}} = \frac{1}{(g_{m1}+g_{m2}) + \left(g'_{m3} - \frac{g_{m4}g_{m6}}{g_{m7}}\right) \times A} \tag{17}$$

To have identical transconductances between M1 and M6, and between M4 and M7, respectively (i.e., $g_{m1} = g_{m6}$ and $g_{m4} = g_{m7}$), the width-to-length ratio of each MOSFET must be modified carefully. Subsequently, the input impedance of the proposed FMC can be simplified into the following.

$$R_{in} = \frac{1}{(g_{m1}+g_{m2}) + \left(g'_{m3} - g_{m1}\right) \times A} \tag{18}$$

According to Kirchhoff's Current Law at node V_1 in Fig. 4(b), the relational function between V_x and V_1 can be expressed as follows.

$$\frac{V_1 - V_x}{R_f} + g_{m2}V_x + g'_{m3}V_1 = 0, \tag{19}$$

where R_f is a feedback resistor between the drain and gate of M_2, $g'_{m3} = g_{m3} + (1/r_{o2}) + (1/r_{o3})$, and r_{oi} is the drain-source resistor of the i^{th} MOSFET. The voltage gain A can be obtained as follows.

$$A = \frac{V_1}{V_x} = \frac{1 - g_{m2}R_f}{1 + g'_{m3}R_f} \tag{20}$$

As shown in (18), if $(g'_{m3} - g_{m1}) > 0$ and $A > 0$, then $R_{in} < 1/(g_{m1} + g_{m2})$. If we carefully modify both the transconductances, g_{m1}, g_{m2}, and g_{m3}, and the resistor R_f, we can obtain an input impedance of the proposed FMC that is lower than that of the traditional FMC, as formalized in (11). The advantage of the proposed FMC is that one can modify the input impedance R_{in} by changing R_f, g_{m1}, g_{m2}, and g_{m3}, simultaneously.

C. PROPOSED CURRENT-MODE SAMPLE-AND-HOLD CIRCUIT

Figure 5 depicts the proposed current-mode S/H circuit, which is composed of two switched-current (SI) FMC circuits with cross-connected bias circuits, one coupled differential replicate (CDR) with a CMFF circuit, and two filter capacitors, C_1 and C_2. The proposed SI FMC circuit is utilized

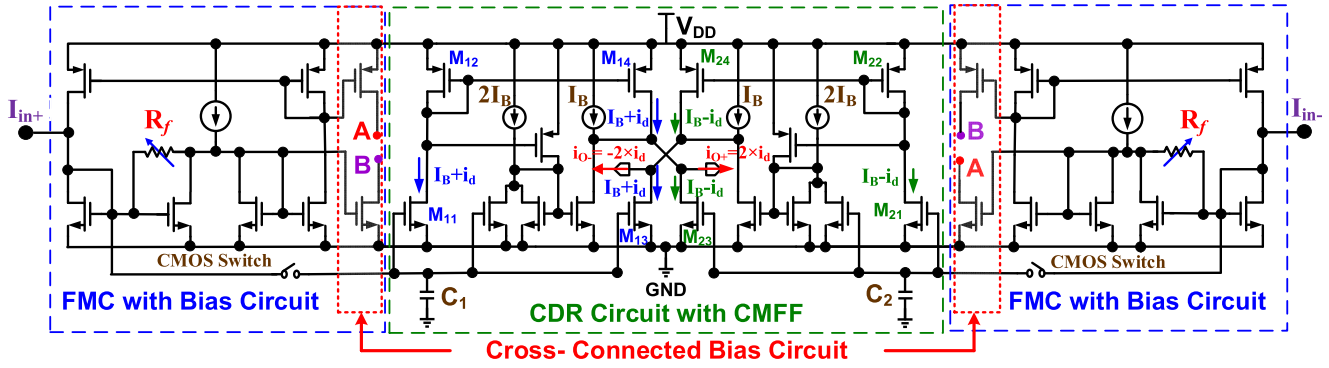

FIGURE 5. Proposed current-mode sample-and-hold (S/H) circuit with two proposed FMC circuits and a CDR circuit with CMFF.

to lower an input impedance and to reduce a small transmission error by modifying the feedback resistor R_f. The cross-connected bias circuit is added to stabilize the bias voltage and to enhance the common-mode voltage gain. Furthermore, the CDR with CMFF circuit is employed in compensating for the error of the current mirror, which is caused by either the difference of the drain voltage or the process variation [18]; the cross-connected CMFF circuit is also used to stabilize the bias voltage at the input terminal.

In the common-mode operation, both CMOS switches are open, and two nodes, A and B, are connected each other in the differential FMC with the bias circuit. This arrangement guarantees the stability of the bias voltage at the input terminal of the proposed current-mode S/H circuit. In the differential-mode operation, a positive small-signal current i_d occurs at M_{13} with an input current of I_{in+} and a negative small-signal current $-i_d$ occurs at M_{23} with another input current of I_{in-}. Subsequently, the collector current of M_{13} is increased to I_B+i_d, and the collector current of M_{23} is reduced to $I_B - i_d$. Meanwhile, the collector current of M_{14} is $I_B + i_d$ and the collector current of M_{24} is changed to $I_B - i_d$ with a constant bias current of I_B. Consequently, the output currents of the positive terminal i_{o+} and the negative terminal i_{o-} are appropriate at $2 \times i_d$ and $-2 \times i_d$, respectively.

Figure 6 presents the simulated transmission errors, in %, of the traditional and proposed FMCs. The proposed FMC performs with an approximately ±0.10% transmission error for the differential input current ranging from -35 μA to $+35$ μA, whereas a traditional FMC operates with not only a large transmission error of ±0.25% with respect to the input current ranging from -20 μA to $+20$ μA but also an oscillation phenomenon. The proposed FMC delivers not only a small transmission error but also has superior stabilization relative to a traditional FMC.

Next, a MOSFET is utilized to complete the feedback resistor R_f by setting it to operate in the triode region. In this study, a PMOS transistor was used as an electronically controllable resistor in the proposed FMC, which plays a crucial role in reducing the input impedance. Unfortunately, the PMOS is highly sensitive to the variation in temperature.

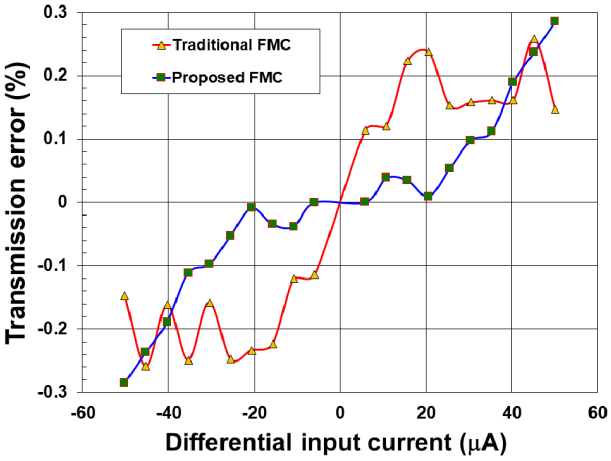

FIGURE 6. Simulated transmission errors in % of the proposed FMC and the traditional FMC.

To remedy this fault, a transmission gate is considered in series with PMOS to have a small temperature variation. Figure 7 presents the percentage transmission error for applied temperatures from -40 °C to 80 °C. In Fig. 7(a), the feedback resistor was only completed with a PMOS, whereas the feedback resistor was implemented with a PMOS in series with a transmission gate in Fig. 7(b). If the temperature range varies from -40 °C to $+80$ °C, the transmission error of Fig. 7(a) changes from 0.0% to 9.8%, and the transmission error of Fig. 7(b) varies from 0.0% to 0.34%. Clearly, the feedback resistor, which is completed with a PMOS in series with a transmission gate, is not highly susceptible to temperature variation.

D. 1-BIT CASCODE CCURRENT-MODE DAC CIRCUIT

Figure 8 presents a 1-bit cascode current-mode DAC with two complementary switches, D_1 and $\overline{D_1}$, which are controlled with thermometer codes [18]. As the switch D_1 is on, the output current I_{out} flows outside the DAC with a bias current I_{DA}, whereas the output current I_{out} flows inside the DAC, so that $I_{out} = -I_{DA}$, as the switch $\overline{D_1}$ is on. Note that the bias current

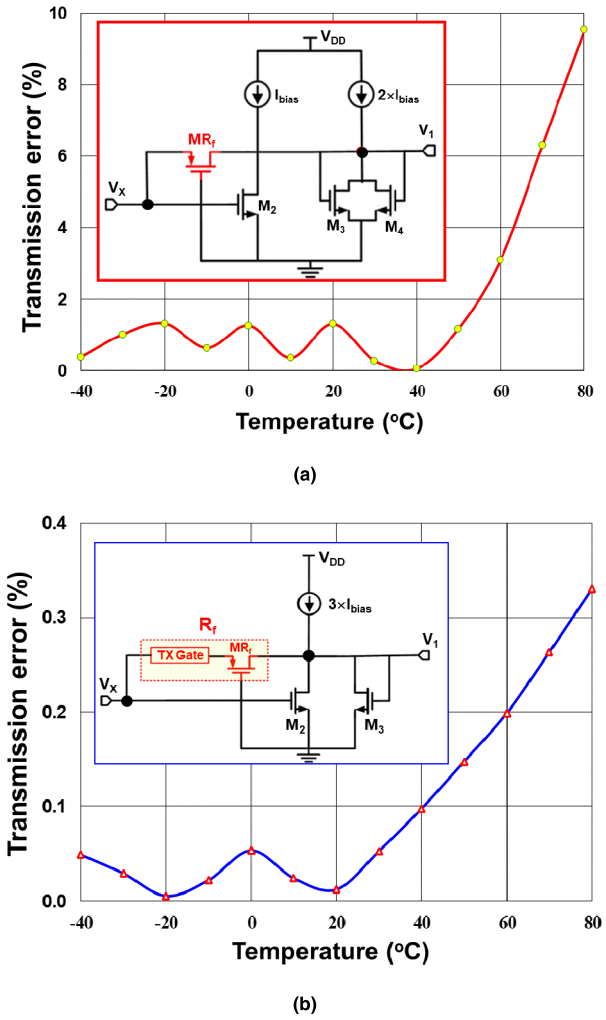

FIGURE 7. Simulated transmission error versus temperature. (a) Using only PMOS, (b) Using PMOS in series with transmission gate.

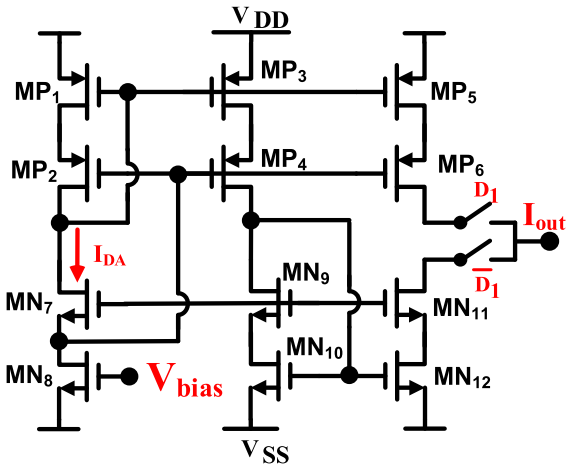

FIGURE 8. 1-bit cascode current-mode DAC with two switches.

I_{DA} is controlled with a bias voltage V_{bias}. The advantages of this DAC circuit are the high current swing and the ability to equalize the output current using thermometer code.

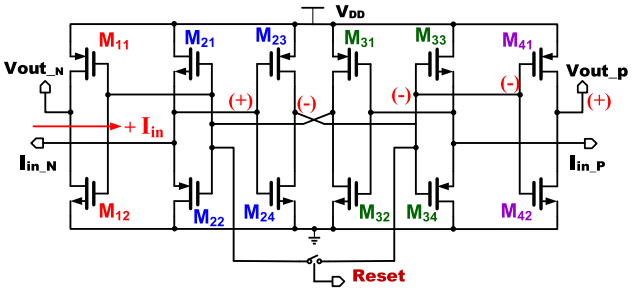

FIGURE 9. 1-bit differential current-mode quantizer.

E. 1-BIT DIFFERENTIAL CURRENT-MODE QUANTIZER

Figure 9 shows a 1-bit differential current-mode quantizer, which is composed of two current comparators, M_{21}-M_{24} and M_{31}-M_{34}, and two inverters, M_{11}-M_{12} and M_{41}-M_{42}. Notify that both input terminals, I_{in_N} and I_{in_P}, are connected to sources of M_{21}, M_{22}, M_{33} and M_{34} to have a low input resistance. If a positive input current $+I_{in}$ flows into the first current comparators M_{21}-M_{24}, then the source voltage of M_{22} will be enhanced (+) and a positive voltage (+) occurs at output node V_{out_P}. In the meantime, a negative voltage (−) is generated at output node V_{out_N}. The function of the inverter, M_{41} and M_{42}, is utilized to have a full-scale output swing from V_{SS} (≈0 V) to V_{DD} (≈1.8 V). If the Reset switch is turned on, both output voltages will be equal. Thus the differential output voltage is roughly zero [18].

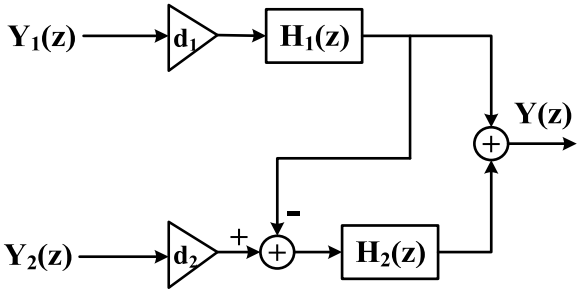

FIGURE 10. Adopted digital noise-cancellation circuit subtracted the second-order NTF of the primary stage from the fourth-order NTF of the secondary stage.

III. CIRCUIT DESIGN OF SIMPLIFIED DNCC

A 2-2 SI MASH DSM provides two second-order NTFs, NTF_1 and NTF_2, in the primary stage [$Y_1(z)$] and second stage [$Y_2(z)$], respectively. By designing a favorable DNCC, we can obtain a fourth-order NTF from the secondary stage and eliminate a second-order NTF from the primary stage of the 2-2 MASH DSM, as illustrated in Fig. 10. The DNCC converts two outputs, $Y_1(z)$ and $Y_2(z)$, of the 2-2 MASH DSM into a single output digital word Y(z), which is a fourth-order output with a fourth-order NTF. The output digital word includes many numbers and characteristics of the digital filter to assist in processing the received signal. The numbers and characteristics of the output digital word depend on the analog

scaling coefficients of the 2-2 MASH DSM as well as the coefficients of the DNCC. The mathematical model of the adopted DNCC is given as follows.

$$Y(z) = d_1 H_1(z)\, Y_1(z)\,[1 - H_2(z)] + d_2 H_2(z)\, Y_2(z), \quad (21)$$

where d_1, d_2, $H_1(z)$, and $H_2(z)$ can be substituted with 1.0, 4.0, z^{-2}, and $(1 - z^{-1})^2$, respectively.

Substituting (7) and (8) in (21) results in the following alternative expression for Y(z).

$$Y(z) = z^{-4}X(z) + 4 \times \left(1 - z^{-1}\right)^4 Q_2(z) \quad (22)$$

The aforementioned equation clearly indicates that the output digital word Y(z) of the DNCC performs with a four unit-delay (z^{-4}) of the input signal X(z) and a fourth-order noise function of the quantization error $Q_2(z)$ in the secondary stage. The adopted DNCC thoroughly eliminates the quantization noise $Q_1(z)$ of the first stage. Subsequently, Eq. (21) can be rewritten as follows.

$$\begin{aligned} Y(z) &= \left(2z^{-3} - z^{-4}\right) Y_1(z) + \left(4 - 8z^{-1} + 4z^{-2}\right) Y_2(z) \\ &= (2A - B) + (4C - 8D + 4E), \end{aligned} \quad (23)$$

where A, B, C, D, and E are $z^{-3}Y_1(z)$, $z^{-4}Y_1(z)$, $Y_2(z)$, $z^{-1}Y_2(z)$, and $z^{-2}Y_2(z)$, respectively. The DNCC is composed of six delays (z^{-1}): four delays for $Y_1(z)$ and two delays for $Y_2(z)$. Figure 11 presents the modified DNCC with six delays.

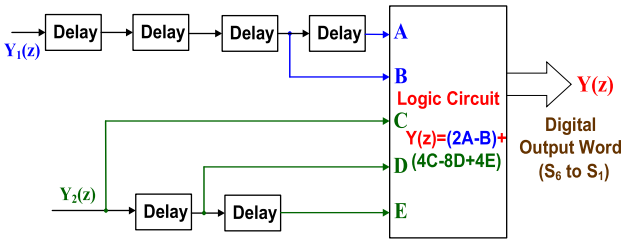

FIGURE 11. Modified digital noise-cancellation circuit with six delays.

Fundamentally, a master–slave flip-flop is utilized to construct the unit delay circuit. With respect to propagation delay and variability, a comparative assessment of the master–slave flip-flop is provided in [19]. Relative to the strong-arm flip-flop (SAFF), data-mapping flip-flop (DMFF), conditional precharge sense-amplifier flip-flop (CPSAFF), conditional capture flip-flop (CCFF), and adaptive-coupling flip-flop (ACFF), the adopted master–slave flip-flop not only improves the propagation delay and timing skew but also minimizes the number of transistors, thereby minimizing the chip area. The advantage of the adopted master–slave flip-flop is that the maximal clock frequency of the entire system is up to a few GHz, and this flip-flop can perform at the system's maximal pace. Figure 12 presents the adopted master–slave flip-flop, which is used to implement the required unit delay circuit. The multiple nonoverlap delayed pulsed clock signals are used to resolve the timing problem between latches.

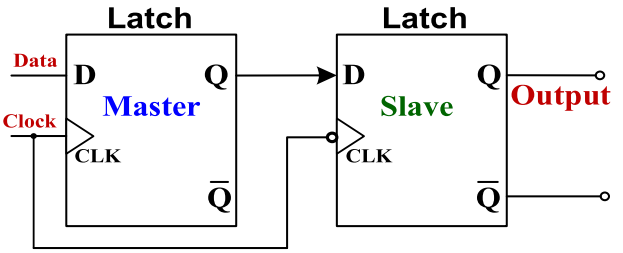

FIGURE 12. An unit delay circuit using master-slave flip-flop.

As illustrated in Fig. 11, the output Y(z) is a digital word, which varies from −19 to +19. If five letters, A, B, C, D, and E, are set to −1, +1, −1, +1, and −1, respectively, the minimum value of Y(z) is calculated as −19. The maximum value of +19 is obtained by flipping the letters' signs to +1, −1, +1, −1, +1, respectively. Therefore, a 6-bit digital word, S_6 to S_1, is utilized to represent those output values from −19 to +19. The term S_6 is the most significant bit (MSB), and S_1 is the least significant bit. Table 2 presents the output digital word of DNCC in six bits, S_6 to S_1, in two's complement form. That is, the negative category values appear as a complementary positive number.

As listed in Table 2, those six bits, S_6 to S_1, are influenced with all inputs, A to E, except for S_1 (=1). The digital output word Y(z) is a function of inputs and can be written as

$$S_6 = \Sigma m(0, 2, 3, 6, 7, 8, 10, 11, 14, 15, 18, 19, 22, 26, 27, 30) \quad (24)$$

$$S_5 = \Sigma m(0, 3, 6, 7, 8, 11, 14, 15, 18, 19, 21, 22, 26, 27, 29, 30) \quad (25)$$

$$S_4 = \Sigma m(0, 2, 5, 7, 8, 10, 13, 15, 17, 19, 20, 22, 25, 27, 28, 30) \quad (26)$$

$$S_3 = \Sigma m(0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15) \quad (27)$$

$$S_2 = \Sigma m(0, 1, 2, 3, 4, 5, 6, 7, 16, 17, 18, 19, 20, 21, 22, 23) \quad (28)$$

$$S_1 = 1 \quad (29)$$

The Boolean expression for each output can be minimized using a 5-variable Karnaugh map. Those simplified Boolean expressions of each output can be implemented with NAND gates for the adopted DNCC. The two advantages of DNCC, which is completed with NAND gates, are (first) that they are insensitive to process variations and (second) that they are area-effective in the proposed combination circuit [20]. Thus, the aforementioned equations, (24)–(28), can be rewritten in the following NAND–NAND forms.

$$S_6 = \overline{(\overline{A \cdot D}) \cdot (\overline{D \cdot E}) \cdot (\overline{C \cdot D}) \cdot (\overline{A \cdot C \cdot E})} \quad (30)$$

$$S_5 = \overline{(\overline{A \cdot D \cdot E}) \cdot (\overline{C \cdot D \cdot E}) \cdot (\overline{A \cdot C \cdot D}) \cdot (\overline{A \cdot C \cdot D \cdot E}) \cdot (\overline{A \cdot C \cdot D \cdot E})} \quad (31)$$

TABLE 2. Output digital word of DNCC in six bits, S_6– S_1, with Two's complement form.

Items	Inputs					Output	2's Complement Form					
	A	B	C	D	E	Y = (2A − B) + (4C − 8D + 4E)	S_6	S_5	S_4	S_3	S_2	S_1
0	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1
1	-1	-1	-1	-1	1	7	0	0	0	1	1	1
2	-1	-1	-1	1	-1	-17	1	0	1	1	1	1
3	-1	-1	-1	1	1	-9	1	1	0	1	1	1
4	**-1**	**-1**	**1**	**-1**	**-1**	**7**	**0**	**0**	**0**	**1**	**1**	**1**
5	-1	-1	1	-1	1	15	0	0	1	1	1	1
6	-1	-1	1	1	-1	-9	1	1	0	1	1	1
7	-1	-1	1	1	1	-1	1	1	1	1	1	1
8	-1	1	-1	-1	-1	-3	1	1	1	1	0	1
9	**-1**	**1**	**-1**	**-1**	**1**	**5**	**0**	**0**	**0**	**1**	**0**	**1**
10	-1	1	-1	1	-1	-19	1	0	1	1	0	1
11	-1	1	-1	1	1	-11	1	1	0	1	0	1
12	-1	1	1	-1	-1	5	0	0	0	1	0	1
13	-1	1	1	-1	1	13	0	0	1	1	0	1
14	-1	1	1	1	-1	-11	1	1	0	1	0	1
15	-1	1	1	1	1	-3	1	1	1	1	0	1
16	1	-1	-1	-1	-1	3	0	0	0	0	1	1
17	1	-1	-1	-1	1	11	0	0	1	0	1	1
18	1	-1	-1	1	-1	-13	1	1	0	0	1	1
19	1	-1	-1	1	1	-5	1	1	1	0	1	1
20	1	-1	1	-1	-1	11	0	0	1	0	1	1
21	1	-1	1	-1	1	19	0	1	0	0	1	1
22	1	-1	1	1	-1	-5	1	1	1	0	1	1
23	1	-1	1	1	1	3	0	0	0	0	1	1
24	1	1	-1	-1	-1	1	0	0	0	0	0	1
25	1	1	-1	-1	1	9	0	0	1	0	0	1
26	1	1	-1	1	-1	-15	1	1	0	0	0	1
27	1	1	-1	1	1	-7	1	1	1	0	0	1
28	1	1	1	-1	-1	9	0	0	1	0	0	1
29	1	1	1	-1	1	17	0	1	0	0	0	1
30	1	1	1	1	-1	-7	1	1	1	0	0	1
31	1	1	1	1	1	1	0	0	0	0	0	1

$$S_4 = \overline{\left(\overline{\left(\overline{A}\cdot C\cdot E\right)}\cdot\overline{\left(\overline{A}\cdot C\cdot E\right)}\cdot\overline{\left(A\cdot\overline{C}\cdot E\right)}\right)\cdot\overline{\left(A\cdot C\cdot\overline{E}\right)}} \quad (32)$$

$$S_3 = \overline{A} \quad (33)$$

$$S_2 = \overline{B} \quad (34)$$

From Eqs. (30) to (34), the NAND–NAND logic circuit of the DNCC can be implemented with a Karnaugh map, as depicted in Fig. 13.

IV. SIMULATION AND MEASUREMENT RESULTS

Figure 14 presents the simulated waveforms of the designed DNCC, which was implemented with a unit delay circuit using a master–slave flip-flop and a NAND–NAND logic circuit using a Karnaugh map. As formalized in Eq. (23), the input of the primary stage $Y_1(z)$ must be delayed 3 clocks (3T) and 4 clocks (4T) to generate A and B, respectively; the input of the secondary stage $Y_2(z)$ must be copied to generate C (0T) and then delayed 1 clock (1T) and 2 clocks (2T) to generate D and E, respectively. In item 9 (A–E) of Table 2, five inputs, A = −1, B = +1, C = −1, D = −1, and E = +1, are entered to generate a digital output word Y(z) of 5, which is calculated with the formula Y = (2A − B) + (4C − 8D + 4E) and is displayed as "000101" in six bits, S_6 to S_1, in two's complement form. A comparison of the simulated results in Fig. 14 with Table 2 proved that the designed DNCC with the unit delay circuit and the NAND–NAND logic circuit works correctly. Next, Laker

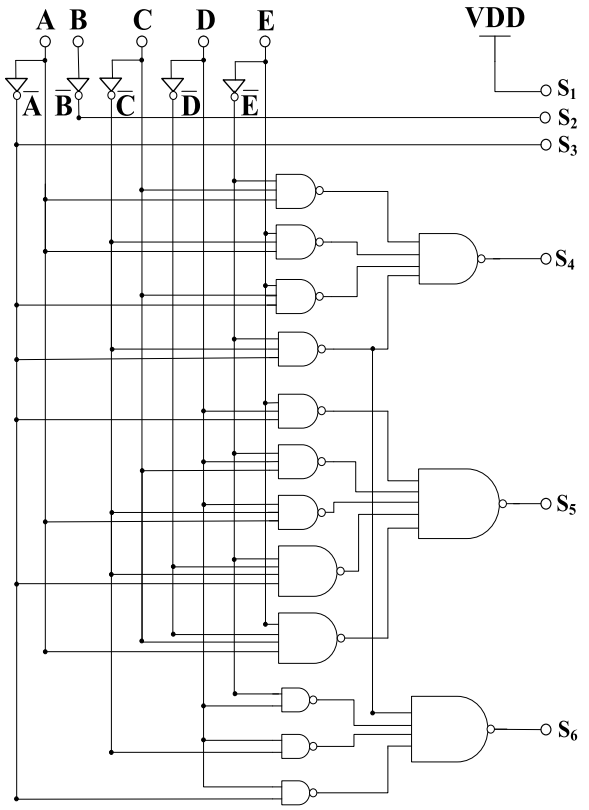

FIGURE 13. NAND–NAND logic circuit of DNCC using a Karnaugh map.

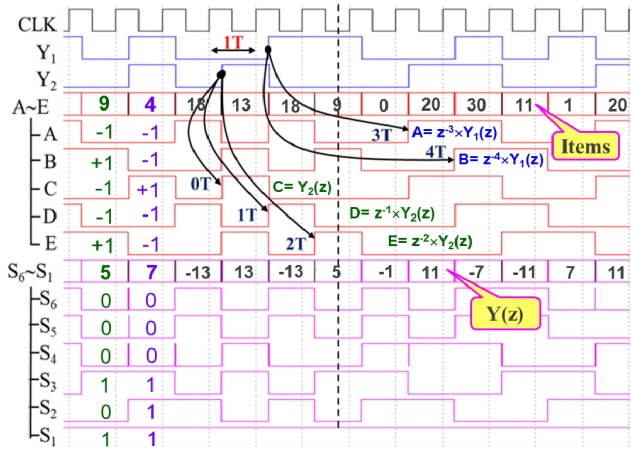

FIGURE 14. Simulated waveforms of the NAND–NAND logic circuit of the designed DNCC using Karnaugh map.

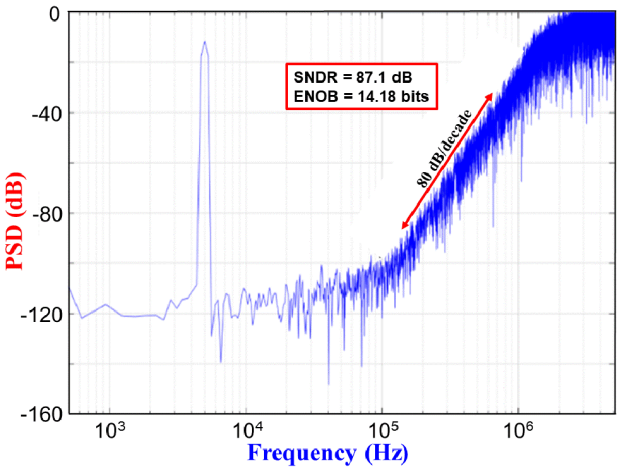

FIGURE 15. Post-layout-simulated PSD (dB) with respect to frequency (Hz) for the designed 2-2 SI MASH DSM with DNCC.

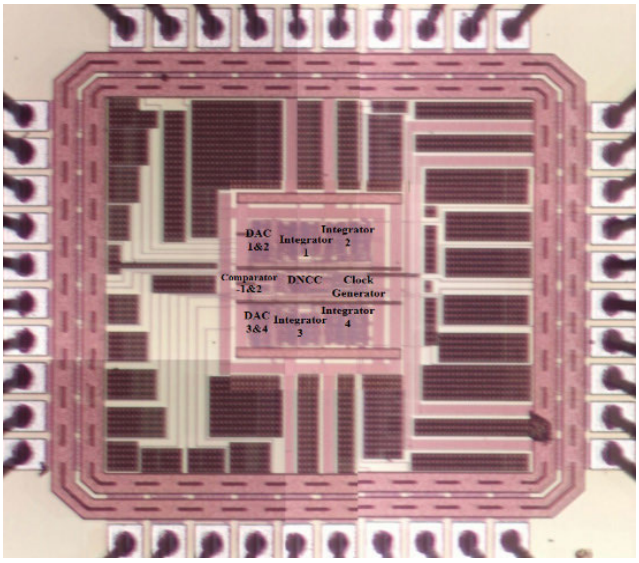

FIGURE 16. Chip microphotograph of the proposed SI MASH DSM with DNCC.

layout software was utilized to complete the circuit layout of the designed 2-2 SI MASH DSM with DNCC. The chip area was approximately 0.359×0.370 mm^2.

According to the post-layout simulation, the SNDR, the effective number of bits (ENOB), and the power dissipation were 87.1 dB, 14.18 bits, and 18.19 mW, respectively—at a clock frequency of 10.24 MHz and an oversampling ratio (OSR) of 256. Figure 15 presents the simulated power spectrum density (PSD) of the designed 2-2 SI MASH DSM with DNCC. After the post-layout simulation had been verified, the designed DSM with DNCC was implemented using TSMC's 0.18μm 1P6M CMOS process. Figure 16 depicts the chip microphotograph of the proposed 2-2 SI MASH DSM with DNCC.

Figure 17 presents the measured platform, including information on the device under test (DUT) printed circuit board (PCB), ultralow distortion function generator (SRS DS360), synthesized signal generator (Anritsu MG3642A), precision measurement dc supply (2280S-60-3), digital signal analyzer–oscilloscope (Keysight DSAV134A), logic analyzer (Agilent 16902B), and MATLAB software. The signal generator provided a sampling frequency of 10.24 MHz, the ultralow distortion function generator generated a differential input sine wave, and the oscilloscope was used not only to display the output waveform in the time domain, but also to

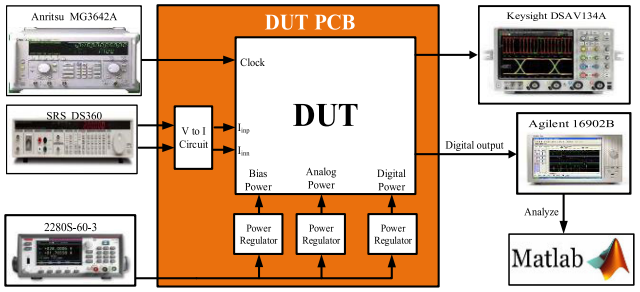

FIGURE 17. Measured platform of the proposed 2-2 SI MASH DSM with DNCC.

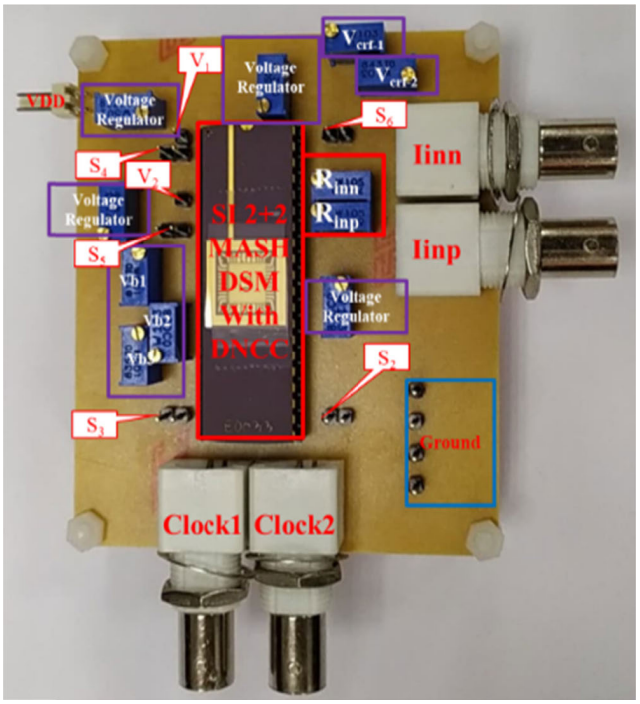

FIGURE 18. Measured PCB of the proposed SI 2-2 MASH DSM with DNCC.

process the fast Fourier transform analysis in the frequency domain. Finally, the digital output code was captured by the logic analyzer and imported into the MATLAB environment for calculation of the SNDR and ENOB. The power regulators of a bias circuit (bias power), a digital circuit (digital power), and an analog circuit (analog power) were separated to prevent power interference in the DUT PCB. The precision measurement dc supply was considered to have a stable power supply.

In view of the negative effect of power noise, guard rings were utilized to separate the analog circuit from the digital circuit. Figure 18 presents the measured PCB of the proposed SI 2-2 MASH DSM with DNCC. The input sine wave was fed to the designed chip to measure the SNDR of the 2-2 MASH DSM and the 6-bit digital output word of DNCC. This study argues that the bias voltage at the input terminal was changed with DAC feedback. Thus, a cross-connected CMFF circuit

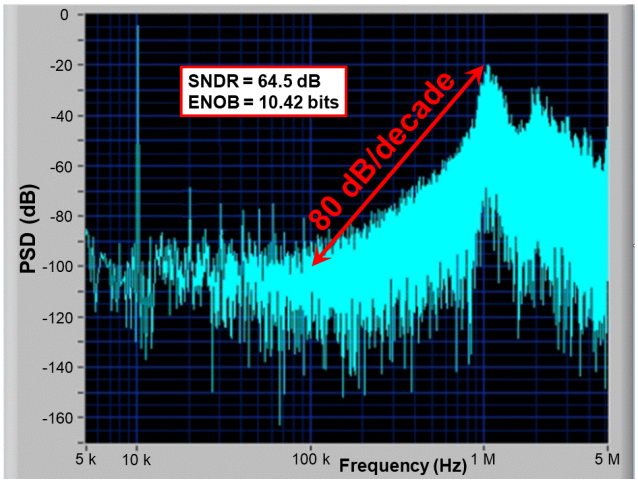

FIGURE 19. Measured PSD (dB) with respect to frequency (Hz) for the proposed 2-2 SI MASH DSM with DNCC.

was utilized to stabilize the common-mode bias voltage at the input terminal, as illustrated in Fig. 5.

Figure 19 presents the measured 65535-point PSD of the proposed 2-2 SI MASH DSM with DNCC at an input current of 20 μA, a sampling frequency of 10.24 MHz, a signal bandwidth of 20 kHz, and an OSR of 256. When a signal frequency of 10.47 kHz was considered with coherent sampling calculation [21], the proposed SI MASH DSM with DNCC yielded an SNDR of 64.5 dB, which was approximately 10.42 bits; this was achieved by setting two control voltages, V_{crf1} and V_{crf2}, to 0.9 V, simultaneously, and three bias voltages, V_{b1}, V_{b2}, and V_{b3}, to 0.25 V, 1.05 V, and 1.4 V, respectively, as shown in Fig. 18. The post-layout-simulated SNDR of 87.1 dB can be compared with the measured SNDR of 64.5 dB; the difference was generated from the analog circuit. Furthermore, process variation, thermal noise, and time delay caused the discrepancy between the measured and simulated SNDRs, especially for the DSM circuit. To remedy those effects, we considered the modified FMC and the cross-connected bias circuit, and sought to enhance the resolution of the ADC. Those impairments still persisted, despite our implementation of numerous improvements.

Table 3 summarizes the performance of the proposed SI MASH DSM developed herein and compares it with other SI DSMs. The performance comparison proved that the input current and measured SNR are better than those in [18]. Furthermore, the simulated SNR, measured SNR, simulated ENOB, measured ENOB, simulated FoM and measured FoM of the proposed 2-2 SI MASH DSM are superior to those of other SI MASH DSMs [11], [22]–[23]. The proposed 2-2 SI MASH DSM was significantly improved by the modified FMC and the cross-connected bias circuit. Besides, the proposed 2-2 SI MASH DSM has many advantages, such as its sampling frequency and chip area. The core area of 0.13 mm^2 is the smallest size of all that had been cited. Unfortunately, the power dissipation of 18.19 mW is inferior

TABLE 3. Performance summary and comparison with other SI MASH DSMs.

Ref. (Year)	[22] (2006)	[23] (2013)	[11] (2017)	[18] (2019)	This work (2020)
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8
Input current (μA)	–	–	5.00	14.00	20.00
DSM Architecture	2-1	–	1-1-1	2-1	2-2
Sampling Category	SI	SI	SI	SI	SI
Signal Bandwidth (kHz)	200	50	20	20	20
Sampling Frequency (MHz)	70.4	12.5	10.24	10.24	10.24
Simulated SNR (dB)	74	39	84.85	90.4	87.1
Measured SNR (dB)	–	–	64.1	59.13	64.5
Simulated ENOB (bits)	12.00	6.19	13.8	14.73	14.18
Measured ENOB (bits)	–	–	10.36	9.53	10.42
Power dissipation (mW)	57	1.72	18.82	12.99	18.19
Core Area (mm^2)	–	–	0.30	0.146	0.13
Simulated FoM (pJ/conv-step)	34.79	235.59	32.9	11.95	24.5
Measured FoM (pJ/conv-step)	–	–	357.6	439.27	331.9

to that of its counterparts in SC DSM [24], [25]. The FoM is defined as follows [26].

$$FoM = \frac{Power}{2^{ENOB} \times 2 \times BW} \left({}^{pJ}/_{conversion-step} \right) \quad (35)$$

V. CONCLUSION

In this paper, we proposed a novel current-mode S/H circuit with very low input impedance using a feedback resistor R_f. By integrating a modified FMC with a cross-connected bias circuit, the post-layout simulation proved that the SNR was 87.1 dB and the ENOB was 14.18 bits at a sampling rate of 10.24 MHz, an OSR of 256, and a signal bandwidth of 20 kHz. Subsequently, a master–slave flip-flop was utilized to construct a unit delay circuit, which performed at a high clock frequency [19]. The main advantage of the proposed SI MASH DSM with DNCC is its small chip area, which is approximately 0.13 mm^2. The performance of the proposed SI DSM was significantly improved by the modified current-mode S/H circuit with its modified FMC and cross-connected bias circuit. Measurements revealed that the SNR and ENOB were 64.5 dB and 10.42 bits, respectively. Both the simulated FoM of 24.5 pJ/conv-step and the measured FoM of 331.9 pJ/conv-step were better than those characteristics of a similar SI architecture. In future projects, we need to improve the resolution of SI MASH DSM by eliminating the impact of charge injection, clock feedthrough, offset of the second integrator, and quantization errors. If a small chip area and a fast sampling frequency (i.e., low input impedance) are required, the SI MASH DSM with DNCC is an excellent selection.

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