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A Dual-Transformer-Based Bidirectional DC–DC Converter of Using Blocking Capacitor for Wide ZVS Range

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ABSTRACT In order to improve the efficiency of battery charging and discharging in a wide conversion gain, a dual-transformer-based full bridge converter using a block capacitor was proposed. By adding the blocking capacitor in the primary side of one transformer, an extended zero voltage switching (ZVS) range is obtained in a wide output voltage range, which is achieved by regulating the secondary voltage of the transformers to match the output voltage according to the voltage-second balance in both boost and buck modes. Besides, a mirror-symmetrical modulation is introduced in reverse power flow to avoid a limited ZVS range of the traditional dual-transformer converter. The power characteristics and ZVS range are analyzed in detailed. The analysis results and transformer current are compared with the published dual-transformer converter and the conventional dual active bridge (DAB) converter to demonstrate the advantages. Finally, a 300W prototype was built and tested to verify the effectiveness of the proposed converter.

INDEX TERMS Dual-transformer, blocking capacitor, ZVS, symmetrical.

I. INTRODUCTION

Isolated bidirectional DC-DC converters are widely used in electric vehicles, new energy generation and other micro grid systems with energy storage devices for galvanic isolation, soft switching and buck/boost functions. Storage elements such as batteries and super capacitors have the characteristics of wide range voltage variation [1], [2]. How to realize the high efficient operation of bidirectional converters in a wide range of voltage has become a major challenge. In isolated bi-directional converter, DAB is potential for inherit zero voltage switching and bidirectional energy flow. If the ratio of input and output voltage is equal to the turn ratio of transformer, DAB can realize the full load range ZVS and low reactive power with a single-phase-shift (SPS) control. Otherwise, there are a large peak current and circulating current, and ZVS cannot be guaranteed under light load. Large peak current leads to high conduction loss and switching-off loss. Circulating current increases copper loss of transformer, and the turn-on switching losses will increase when soft-switching is loss. Above factors result in low efficiency of DAB converter and have been studied in many papers.

Various improved modulation schemes on the DAB has been proposed to expand ZVS and reduce circulating current in [3]–[15]. In [3], a three-level PWM switching control strategy was proposed to achieve full-load ZVS by driving H-bridge with internal phase-shifting at high voltage side. When the voltage conversation gain is not 1, the extended phase-shifting (EPS) will be used to expand the soft switching range and reduce the circulating current [4]. Dual phase shift (DPS) that inner phase-shift on both primary and secondary H-bridge for the regulated duty cycle and outer phase-shift between the primary and secondary voltages was proposed in [5]. The directions of phase shift on both sides of H-bridge are opposite, which can improve the efficiency at the light load [6]. Power loss of DAB with the DPS control is analyzed and the relevant control strategy is

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given in [7]. In [8], a composite scheme combing SPS and DPS was proposed to extend soft-switching. Furthermore, triple phase shift (TPS) including three variables is adopted to improve the performance of DAB converter in [9]. For different optimization objectives, such as the total losses, RMS of inductor current, and inductor current stress were developed to improve the performance in [10]–[15]. But these algorithms are based on complex mathematical calculation and the optimization target is highly dependent on the system parameters. These modulation strategies only can improve efficiency in narrow voltage output range.

Various simple modified topologies were proposed to overcome the low efficiency in wide output voltage range of traditional DAB converters [16], [17]. In [16], a DC blocking capacitor connected in series with the primary winding of transformer is introduced. There are two working modes of the H-bridge on the primary side, i.e. full- and half-bridge, which makes the voltage conversation around 1. For example, when voltage gain $K = nV_2/V_1 = 0.5$, where V_1 is input voltage and V_2 is the output voltage, the primary bridge can work as half-bridge so that the voltage gain is 1. In [17], a hybrid modulation strategy was proposed with blocking capacitors in series with both primary and secondary windings, which comprehensively considered the principle of minimum inductance current. Considering the high voltage in micro-grid, [18]–[20] reported a DC-DC converter with neutral point clamped (NPC) three-level structure. In [18], asymmetric PWM plus phase-shift control is used to realize wide voltage and high efficiency operation where K is greater than 2. Although they can achieve lower inductor current to improve the efficiency in wider gain range, ZVS cannot be ensured under quite a part of working conditions.

To achieve ZVS in a wide operation range, a dual-transformer asymmetrical dual-bridge which can work in buck and boost modes was proposed in [21]. However, the power flow is unidirectional. In [22] a dual-transformer structure was proposed for two variable input voltage. In [23] three-level T-type isolated bidirectional DC–DC converter was reported. The four-level voltage was generated to match the output voltage for a hybrid bridge-based DAB converter in [24]. PWM plus phase-shift control based on dual transformers active bridge (DTAB) converter was proposed in [25]. In both [24] and [25], the primary side can generate a continuous adjustable voltage to match the output voltage which achieves a wide ZVS range for most switches. But there is a limited ZVS range for phase-shift leg on primary side with reverse mode and the efficiency is improved with $K = (0.5\text{-}1)$. However, to apply the DC-DC converter for the battery chargers in the electric vehicles (EVs), a wider output voltage range is required (e.g., 200V-450V). The ranges of voltage gain K in the previous DC-DC converters are not wide enough for the battery charging and discharging.

Therefore, to achieve ZVS in wide conversion gain range and satisfy most battery charging and discharging range, a dual-transformer-based full bridge converter using a block capacitor was proposed. For the proposed converter, four-level voltage on secondary winding is regulated to match output voltage according to voltage second balance on both boost and buck modes. The proposed converter expands the ZVS range with not only $K = (0.5\text{-}1)$ but also $K = (1\text{-}1.5)$. When power flow is reverse, a mirror-symmetrical modulation is used to avoid a seriously limited ZVS range in reverse mode compared with DTAB converter. A 300W prototype is established to verify the theoretical analysis.

This article is organized as follows. In Section II, the dual-transformer-based full bridge converter with a blocking capacitor is illustrated. The power characteristics of converter, operation principle and ZVS range are deduced. A comparison with DTAB converter and DAB converter is demonstrated in Section III. In Section IV, the experimental results are presented based on a 300W prototype. Finally, the conclusion is in Section V.

II. TOPOLOGY AND MODULATION SCHEME

A. TOPOLOGICAL STRUCTURE AND MODULATION METHOD

The topology consists of three bridge legs on the primary side and a H-bridge on the secondary side. The transformers T_1 and T_2 are connected in parallel on primary and series connection on secondary. A blocking capacitor is in series connected in primary winding and a transmission inductor is in series connected in secondary winding as shown in Fig. 1.

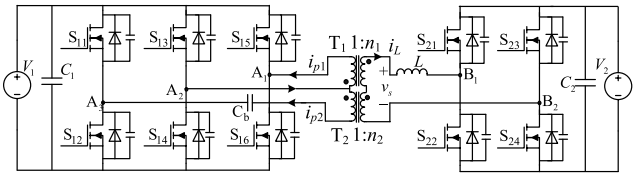

FIGURE 1. Dual transformer based active bridge DC-DC converter.

The typical voltage/current waveforms in the boost mode for this dual-transformer converter are shown in Fig. 2. The case of $0 < \phi < d$ is given as an example to explain the operation principle, where d is the duty cycle of the primary side and ϕ is the phase shift ratio between v_s and v_{B1B2}. The duty cycle d is adjusted to extend ZVS range, by regulating the four-level voltage v_s in the secondary side of the transformers to match a variable voltage v_{B1B2} according to voltage-second balance. The phase shift ratio ϕ is controlled to regulate power flow. Two full bridges on the primary side share the common leg including S_{13} and S_{14}. The full bridge connected with T_2 can operate in either the half bridge or the full bridge mode. When S_{11} keeps off and S_{12} keeps on, the full bridge connected with T_2 works as the half bridge mode. An offset DC voltage can be introduced on the blocking capacitor and v_s equals $n_2V_1/2 + n_1V_1$, which is corresponding to the buck mode of the converter. If the full bridge connected with T_2 work as the full bridge mode, there is no offset DC voltage on the blocking capacitor and v_s equals $n_2V_1 + n_1V_1$, which is corresponding to the boost mode of the converter.

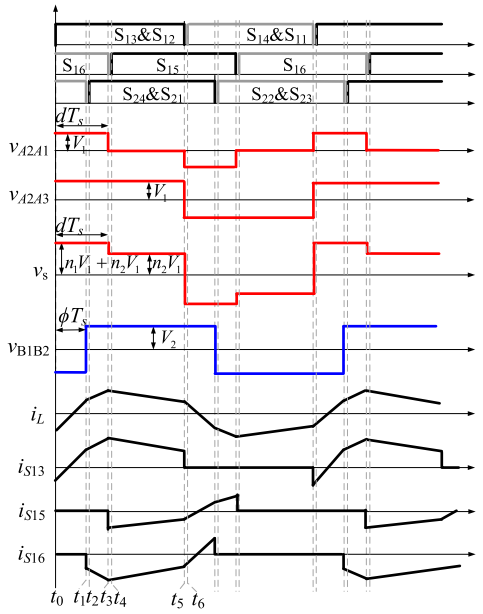

FIGURE 2. Typical waveforms in the boost mode.

B. OPERATION MODES ANALYSIS

Since the steady state waveform is symmetrical in the positive and negative half switching cycles. Only half cycle operation mode needs to be analyzed, which can be divided into six intervals from t_0 to t_6 as presented in Fig. 2. The corresponding equivalent circuits are shown in Fig. 3.

Stage 1 (t_0-t_1): before t_0, S_{16}, S_{22} and S_{23} have been conducting and other switches remain off. At t_0, S_{12} and S_{13} are turned ON. During this interval, v_s is equal to $n_1V_1+n_2V_1$ and v_{B1B2} is equal to $-V_2$. The voltage applied to L is $v_s - v_{B1B2}$. At the beginning of this interval, the inductor current i_L starts to increase with a constant slew rate, which can be expressed as:

$$i_L(t - t_0) = i_L(t_0) + (n_1V_1 + n_2V_1 + V_2)(t - t_0)/L \quad (1)$$

Stage 2 (t_1-t_2): Before the turn-on of S_{21} and S_{24}, the inductor current i_L is positive as shown in Fig.2. At time t_1, S_{22} and S_{23} are turned off. The inductor current i_L begins to discharge the parasitic capacitor of S_{21} and S_{24} from $V_2/2$ to zero and to charge the parasitic capacitor of S_{22} and S_{23} from zero to $V_2/2$. When the charging and discharging process is over, i_L freewheels through body diode of S_{21} and S_{24} as i_L is positive. S_{21} and S_{24} is turned on before i_L changes its polarity. Because the charging and discharging process is very short and can be ignored to simplify ZVS analysis. Hence, the ZVS constraints for S_{21} and S_{24} can be obtained as

$$i_L(t_1) > 0 \quad (2)$$

Stage 3 (t_2-t_3): At t_2, S_{21} and S_{24} is turned ON under ZVS. In this interval, the secondary-side voltage of the two transformers v_s is still equal to $n_1V_1+n_2V_1$ and v_{B1B2} changes to V_2. In this interval, the inductor current i_L is increasing with a lower constant slew rate, and i_L can be expressed as

$$i_L(t - t_2) = i_L(t_2) + (n_1V_1 + n_2V_1 - V_2)(t - t_2)/L \quad (3)$$

Stage 4 (t_3-t_4): At t_3, i_{p1} arrive at peak current. S_{16} is turned OFF. i_{p1} begins to discharge the parasitic capacitor of S_{15} and charge the parasitic capacitor of S_{16}. After this charging and discharging process, i_{p1} freewheels through the body diode of S_{15} as i_{p1} is positive. S_{15} is turned on before i_{p1} changes its polarity. The ZVS constraints for S_{15} is

$$i_{p1}(t_3) = i_L(t_3)n_1 > 0 \quad (4)$$

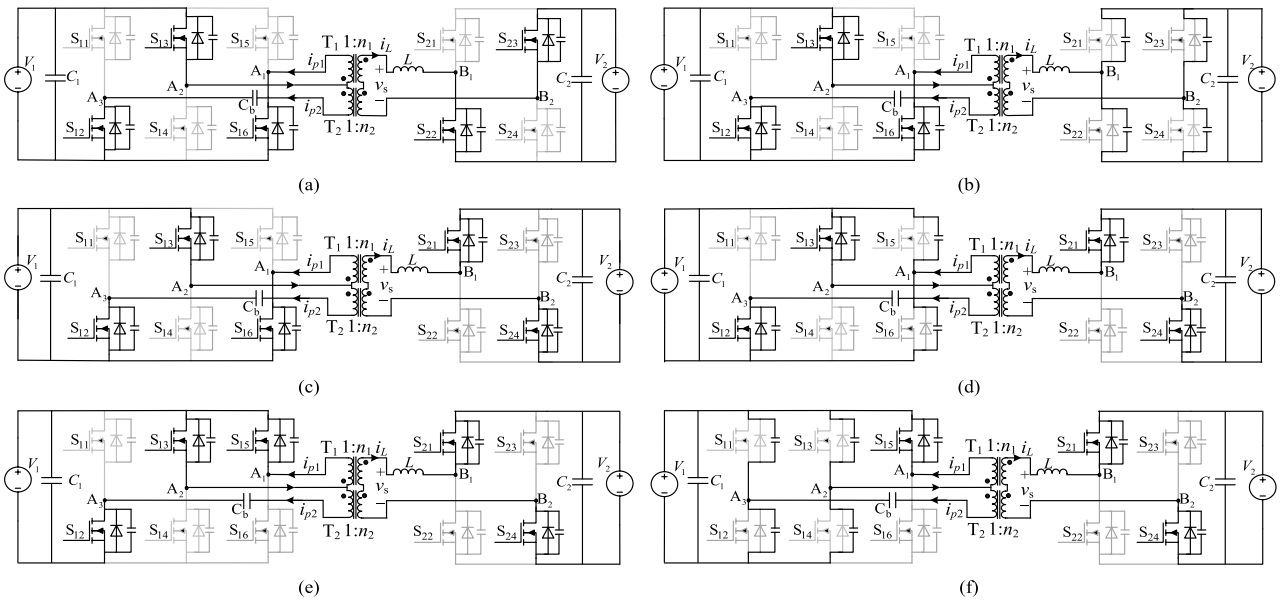

FIGURE 3. Equivalent circuit for each mode. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

Stage 5 (t_4-t_5): At t_4, S_{15} is turned ON under ZVS. During this interval, v_{A1A2} changes to be zero and v_s becomes n_2V_1. The inductor current expressions for i_L can be obtained as

$$i_L(t-t_4) = i_L(t_4) + (n_2V_1 - V_2)(t-t_4)/L \tag{5}$$

Stage 6 (t_5-t_6): S_{13} and S_{12} is turned OFF at t_5. During this interval, the parasitic capacitor of S_{14} and S_{11} is discharged from $V_2/2$ to zero. At the end of this stage, i_{p2} freewheels through the bode diode of S_{11}, and $i_{p1} + i_{p2}$ freewheels through the bode diode of S_{14}. The ZVS constraints for S_{14} and S_{11} can be obtained as

$$\begin{cases} i_{p2}(t_5) = i_L(t_5)n_2 > 0 \quad (S_{11}) \\ i_{p1}(t_5) + i_{p2}(t_5) = i_L(t_5)(n_1+n_2) > 0 \quad (S_{14}) \end{cases} \tag{6}$$

C. POWER CHARACTERISTICS

The full bridge connected with T_2 is as full bridge in the boost mode with $K = (1\sim1.5)$. There are three possible combinations that consist of d and ϕ for pattern A:$0 < \phi < d$, pattern B: $d < \phi < 0.5$ and pattern C: $d - 0.5 < \phi < 0$. The simplified operating waveforms are illustrated in Fig. 4. Ignoring the loss of the circuit, the output power can be calculated as:

$$P = \frac{1}{T_s}\int_{t_0}^{t_6} v_s i_L(t)\,dt \tag{7}$$

According to three possible working patterns and current value, the output average power can be obtained as (8), as shown at the bottom of the next page.

The average power is illustrated in Fig.5 with duty-cycle and phase-shift control. At different duty cycles, three working patterns can be obtained for the power transfer. Similar to the DAB converter, the maximum power transfer can be observed at different duty cycles and phase shift angles.

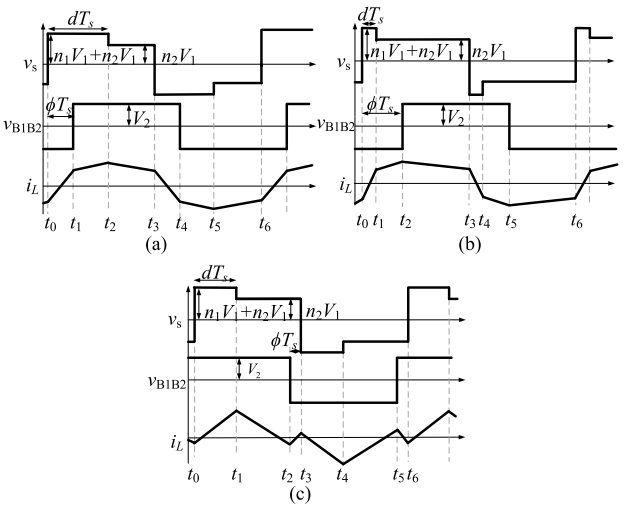

FIGURE 4. Typical simplified operating waveforms in boost and forward mode. (a) A: $0 < \phi < d$. (b) B: $d < \phi < 0.5$. (c) C: $d - 0.5 < \phi < 0$.

When the full bridge connected with T_2 works as a half bridge in the buck mode with $K = (0.5\sim1)$, n_2V_1 in Fig.4 will change to $n_2V_1/2$. There are also three possible combinations that consist of d and ϕ ($0 < \phi < d, d < \phi < 0.5, d - 0.5 < \phi < 0$). The output average power can be obtained as (9), as shown at the bottom of the next page.

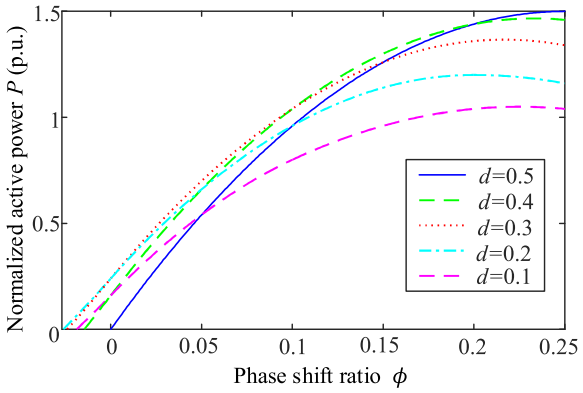

FIGURE 5. Power characteristics with different duty cycle in boost mode.

The normalized power P_{BASE} and corresponding normalized current I_{BASE} are defined as follows:

$$P_{BASE} = KV_1^2T_s/8L \tag{10}$$

$$I_{BASE} = V_1T_s/8L \tag{11}$$

As shown in Fig.6, the mirror-symmetrical modulation is introduced in reverse power flow. The typical voltage and current waveforms are mirror-symmetrical to those in Fig.4 (a). The reverse power characteristics have the same operation modes. The power characteristics in reverse mode are symmetrical to those in forward mode with respect to output voltage.

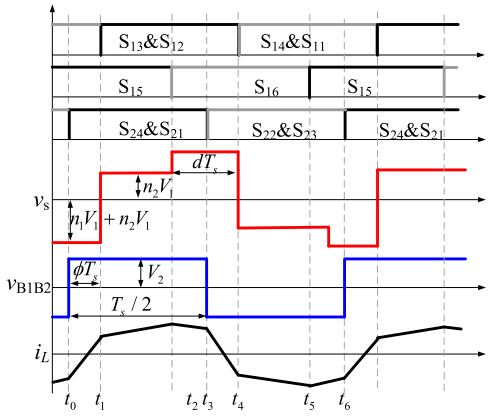

FIGURE 6. Typical voltage and current waveforms in the reverse flow.

D. ZVS CONSTRAINS AND BASIC OPERATION PRINCIPLE

It can be seen from part B that the ZVS implementation of corresponding switch is based on the current polarity of the transformer when switch is turned ON ignoring the charge and discharge time. The constraints for ZVS of all switches are listed in Table 1.

TABLE 1. ZVS current constraints.

Working patterns	$S_{11},S_{12},S_{13},S_{14}$	S_{15},S_{16}	$S_{21},S_{22},S_{23},S_{24}$
$A: 0<\phi<d$	$i_L(t_0)<0$	$i_L(t_2)>0$	$i_L(t_1)>0$
$B: d<\phi<0.5$	$i_L(t_0)<0$	$i_L(t_1)>0$	$i_L(t_2)>0$
$C: d-0.5<\phi<0$	$i_L(t_0)<0$	$i_L(t_1)>0$	$i_L(t_2)<0$

Applying volt-second balance principle, the integration of the inductor current is zero in one cycle as:

$$\frac{1}{T_s}\int_{t_0}^{t_6} i_L(t)\,tdt = 0 \tag{12}$$

Take pattern A for example, in one cycle, the instantaneous secondary current value has the following relationship at the instants of turning on.

$$\begin{cases} i(t_1) = -i(t_4) = i(t_0) + (n_1V_1 + n_2V_1 - V_2)(t_1 - t_0)/L \\ i(t_2) = -i(t_5) = i(t_1) + (n_1V_1 + n_2V_1 - V_2)(t_2 - t_1)/L \\ i(t_3) = -i(t_6) = i(t_2) + (n_1V_1 - V_2)(t_3 - t_2)/L \end{cases} \tag{13}$$

From equations (12) and (13), the current values required in Table 1 can be deduced as:

$$\begin{cases} i(t_0) = -i(t_3) = -(2V_2\phi + n_1V_1d \\ \qquad + 0.5n_2V_1T_s - 0.5V_2T_s)/2L \\ i(t_1) = -i(t_4) = (-n_1V_1d - 0.5n_2V_1T_s \\ \qquad + 0.5V_2T_s + 2n_2V_1\phi + 2n_1V_1\phi)/2L \\ i(t_2) = -i(t_5) = (2n_2V_1d + n_1V_1d - 0.5n_2V_1T_s \\ \qquad + 0.5V_2T_s - 2V_2d + 2V_2\phi)/2L \end{cases} \tag{14}$$

Substituting equation (14) into the current constraints in Table 1, the relationships between duty cycle and phase-shift under different voltage for ZVS are shown in Table 2. It can be seen from Table 2 that ZVS conditions are the inequality expressions about d, ϕ, and the transformer turns ratios n_1 and n_2. There are many ZVS optimization objectives for the switches with four variables. While, all the inequalities in Table 2 contain the same factor: $E = V_2 - mn_2V_1 - 2dn_1V_1$. When E is equal to zero, the ZVS conditions for S_{11}, S_{12}, S_{13}, S_{14} and S_{21}, S_{22}, S_{23}, S_{24} can be ensured under full load range. In fact, when $m = 1$ and $m = 0.5$, $E = 0$ means voltage-second balance [26] in boost mode and buck mode as shown in Fig. 7.

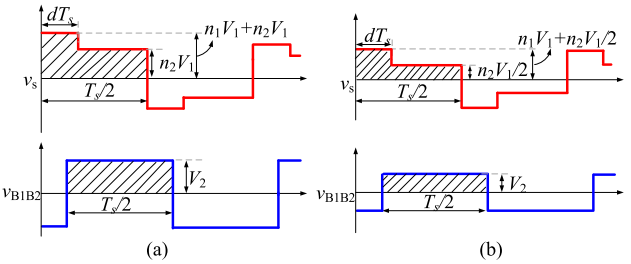

FIGURE 7. Voltage-second balance on the inductor *L*. (a) boost mode. (b) buck mode.

For the input side, the voltage-second product is defined as the time integral of a half-cycle of the secondary winding voltage. For the output side, the product of voltage value in half-cycle is rectangular area. The relationship of voltages (v_s, v_{B1B2}) on both sides of the transmission inductor L can be expressed as

$$n_1V_1dT_s + mn_2V_1T_s/2 = V_2T_s/2 \tag{15}$$

The duty ratio d according to equation (15), which can satisfy inductor voltage-second balance in boost and buck mode is calculated as follow:

$$d = (V_2 - mn_2V_1)/2n_1V_1 \tag{16}$$

E. THE TRANSFORMER TURNS RATIO AND ZVS RANGE

For the proposed converter, the input voltage is V_1 and the output voltage variation is $V_{2\min} \sim V_{2\max}$. The voltage gain K is from 0.5∼1.5. Hence, $K_{\max} = 3\,K_{\min}$ and $V_{2\max} = 3V_{2\min}$. According to voltage-second balance law in the equation (15), the relationship between duty ratio d and the turns

$$\begin{cases} P_A = -\dfrac{n_2V_1V_2\phi T_s - 2n_2V_1V_2\phi^2 - 2n_1V_1V_2\phi^2 + 0.5n_1V_1V_2dT_s - n_1V_1V_2d^2 + 2n_1V_1V_2d\phi}{T_sL} \\ P_B = -\dfrac{n_2V_1V_2\phi T_s - 2n_2V_1V_2\phi^2 - 2n_1V_1V_2d\phi + 0.5n_1V_1V_2dT_s + n_1V_1V_2d^2}{T_sL} \\ P_C = -\dfrac{-n_2V_1V_2\,|\phi|\,T_s + 2n_2V_1V_2\phi^2 + 0.5n_1V_1V_2dT_s - 2n_1V_1V_2d\,|\phi| - n_1V_1V_2d^2}{T_sL} \end{cases} \tag{8}$$

$$\begin{cases} P_A = \dfrac{0.5n_2V_1V_2\phi T_s - n_2V_1V_2\phi^2 - 2n_1V_1V_2\phi^2 + 0.5n_1V_1V_2dT_s - n_1V_1V_2d^2 + 2n_1V_1V_2d\phi}{T_sL} \\ P_B = \dfrac{0.5n_2V_1V_2\phi T_s - n_2V_1V_2\phi^2 - 2n_1V_1V_2d\phi + 0.5n_1V_1V_2dT_s + n_1V_1V_2d^2}{T_sL} \\ P_C = \dfrac{-0.5n_2V_1V_2\,|\phi|\,T_s + n_2V_1V_2\phi^2 + 0.5n_1V_1V_2dT_s - 2n_1V_1V_2d\,|\phi| - n_1V_1V_2d^2}{T_sL} \end{cases} \tag{9}$$

TABLE 2. ZVS conditions.

Working patterns	$S_{11},S_{12},S_{13},S_{14}$	S_{15},S_{16}	$S_{21},S_{22},S_{23},S_{24}$
A: $0<\phi<d$	$E<4V_2\phi$	$4[d(mn_2V_1+n_1V_1-V_2)+V_2\phi]>-E$	$4(n_1+mn_2)V_1\phi>-E$
B: $d<\phi<0.5$	$E<4V_2\phi$	$4[V_1d(n_1+mn_2)+V_2(d-\phi)]>-E$	$4V_1(n_1d+mn_2\phi)>-E$
C: $d-0.5<\phi<0$	$E<4V_2\phi$	$4[V_1d(n_1+mn_2)+V_2(d-\phi)]>-E$	$4V_1(n_1d+mn_2\phi)>-E$

$E=V_2-mn_2V_1-4dn_1V_1$, m=1(boost mode), m=0.5(buck mode)

ratios n_1 and n_2 can be expressed by:

$$2n_1d+mn_2=\frac{V_2}{V_1} \tag{17}$$

where $m=1$ and 0.5 represent boost mode and buck mode respectively.

By using of blocking capacitors, the voltage amplitude of V_{A2A3} can be $V_1/2$ or V_1. When $m=0.5$, V_{A2A3} is $V_1/2$ and duty ratio d can be set to 0∼0.5 to match the output voltage $V_{2\min}\sim V_{2\min}+(V_{2\max}-V_{2\min})/2$. At output voltage $V_2=V_{2\min}$, duty ratio $d=0$. When $m=1$, V_{A2A3} is V_1 and duty ratio d can be set to 0∼0.5 to match the output voltage $V_{2\min}+(V_{2\max}-V_{2\min})/2\sim V_{2\max}$. At output voltage $V_2=V_{2\max}$, duty ratio $d=0.5$. Then the following relationship can be obtained:

$$\begin{cases} n_1+n_2=\dfrac{V_{2\max}}{V_1} \\ n_2/2=\dfrac{V_{2\min}}{V_1} \end{cases} \tag{18}$$

Because of $V_{2\max}/V_{2\min}=3$, the turns ratio for two transformers should satisfy $n_2=2n_1$.

In Table 2, when the time integral of v_s equals to v_{B1B2}, the switches always can be turned ON under ZVS except S_{15} and S_{16}. ZVS conditions of S_{15} and S_{16} are dependent on d and ϕ. Substituting equation (16) into the ZVS conditions with $n_2=2n_1$ in Table 2, ZVS range of S_{15} and S_{16} versus output voltage can be plotted in Fig.8. Region A, B, C represent working patterns as shown in Fig.4. Region A', B', C' represent working patterns in reverse power flow. As presented in Fig.8, hard switching for S_{15} and S_{16} exists only in regions B and B', which is symmetrical versus output voltage.

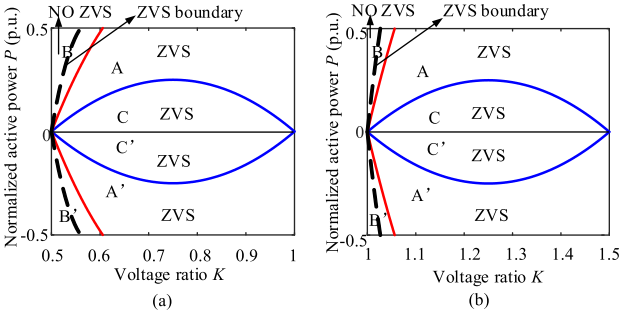

FIGURE 8. ZVS range for S_{15} and S_{16} versus output voltage. (a) buck mode. (b) boost mode.

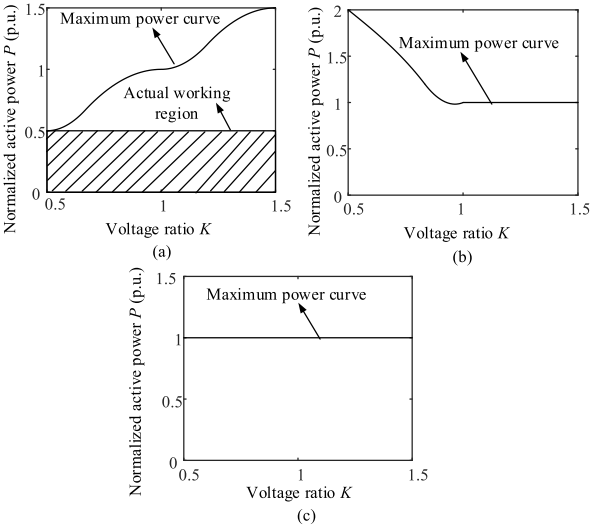

FIGURE 9. Power range versus voltage ratio. (a) proposed converter. (b) DTAB. (c) DAB.

III. COMPARISON

A. POWER RANGE

Power characteristics of the proposed converter can be obtained according to equations (8) and (9). There are two decoupled variables d and ϕ. d is independent of ϕ and varies with output voltage to satisfy voltage-second balance on the inductor. The maximum power of proposed converter is monotonically increasing with K from 0.5 to 1.5 as shown in Fig.9 (a). It is because the constant input voltage V_1 is adjusted by duty cycle to match the varying output voltage V_2. The maximum power with variable gain in DTAB is as shown as Fig.9 (b). It's monotonically decreasing from 0.5 to 1. It is because the varying output voltage V_2 is adjusted by duty cycle to match the constant input voltage V_1. The maximum power of DAB is 1 (p.u.) with variable gain in traditional DAB converter as shown in Fig.9 (c). In practical application, the rated power is designed smaller than 0.5 (p.u.) in order to limit the reactive power [27] [28], which is illustrated as shadow part in the proposed converter. The power range of proposed converter is enough to satisfy the requirements of most wide output voltage situations.

B. ZVS RANGE

As mentioned in the section II, only considering current polarity at turn-on instant for ZVS constrains, the region of hard-switching for S_{15} and S_{16} is very small and the other

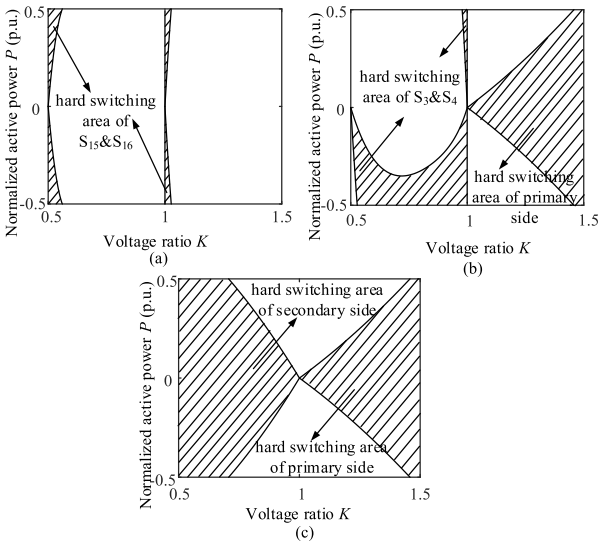

FIGURE 10. ZVS range versus voltage ratio. (a) proposed converter. (b) DTAB. (c) DAB.

switches can turn on under ZVS in whole region as shown in Fig.10 (a). There is a limited ZVS range without a symmetrical modulation in reverse mode for S_3 and S_4 with K from 0.5 to 1 in DTAB as shown in Fig.10 (b). Moreover, it works as a traditional DAB in the range of 1-1.5. In Fig.10 (c), the traditional DAB suffers from secondary-side hard-switching with K from 0.5 to 1 and primary-side hard-switching with K from 1 to 1.5 at light load. Obviously, the proposed converter obtains a wider ZVS range in actual working region.

C. THE TRANSFORMER CURRENT

The loss of dual-transformer-based converter mainly consists of two parts: switching loss and transformer loss. When the switch turns on at ZVS, switching loss is determined by switching off loss and conduction loss which is proportional to RMS current flowing through the switch. Accordingly, transformer losses are divided into coil losses and core losses. The coil loss is proportional to RMS current. Thus, the transformer RMS current is a significant specification for the proposed converter. Fig. 11 shows the plots of the normalized transformer secondary RMS current of the proposed converter, DTAB and traditional DAB converter when the normalized active power P is 0.4 (p.u.) and 0.1 (p.u.), respectively. RMS current in DTAB is lower at relatively low voltage gain. Four-level is generated based a varying output voltage to match a constant input voltage in DTAB, hence a smaller ϕ is obtained for DTAB at the same power. With the gain increasing, the proposed converter has lower RMS current especially at light load. This advantage helps the proposed converter to reduce transformer winding loss and switches conduction loss in most gain range.

The magnitude of peak current is related to the switching loss. The turn-off loss of the switching device is determined by the current magnitude at the instants of switching off.

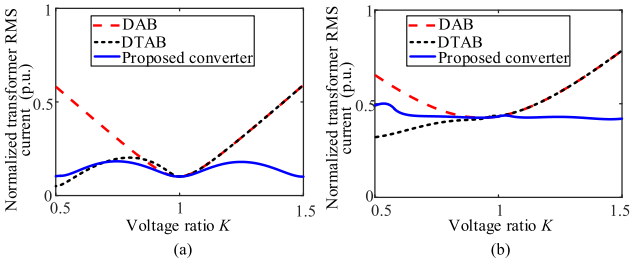

FIGURE 11. the normalized transformer RMS current versus voltage ratio K. (a) $P = 0.1$ (p.u.). (b) $P = 0.4$ (p.u.).

For example, the current of S_{15} reaches its peak value at the instants of switching off as shown in Fig.2. The magnitude of peak current can be derived in (14). Fig. 12 shows the normalized peak current of the transformer secondary winding with different K. Similar to RMS current, peak current in DTAB is lower at relatively low voltage gain. But the proposed converter has lower peak current in most gain range.

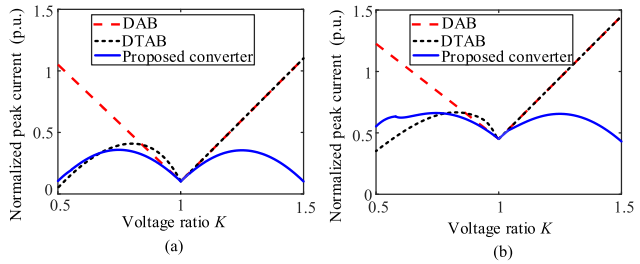

FIGURE 12. Normalized peak current versus voltage ratio K. (a) $P = 0.1$ (p.u.). (b) $P = 0.4$ (p.u.).

D. THE TRANSFORMER CAPACITY

The proposed converter operates at a constant input voltage V_1 and a variable output voltage $n_2V_1/2$ $-3n_2V_1/2$. When the full bridge connected with T_2 works as half bridge, the voltage amplitude applied to transformers T_1 and T_2 is $V_1/2$. The transmission capacity of transformer T_1 is equal to that of T_2 with $d = 0.5$. When the full bridge connected with T_2 works as full bridge, the transmission capacity of transformer T_1 is half of that of T_2 with $d = 0.5$. Finally, transformer T_1 capacity is designed as half of T_2 transmission capacity when $d = 0.5$ in boost mode.

IV. EXPERIMENT

A. VERIFICATION OF THE PROPOSED CONVERTER

The output power is designed as 0.5 (p.u.) with different output voltage as shown in the shadow area of Fig. 9 (a). A 300 W laboratory test setup with $K = 1.5$ was established to validate the proposed converter and the parameters are shown in Table 3. The photo of the experimental setup is shown in Fig. 13. The primary side of the converter is connected with a 50 V constant DC power supply. DC output port of secondary side is connected to the battery simulator. DSP

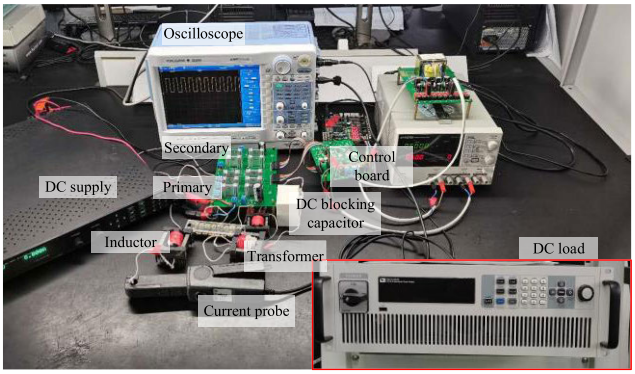

FIGURE 13. Experimental setup.

TABLE 3. Parameters and components.

Parameters	Values
Input voltage	50VDC
Output voltage	25V-75VDC
Output power	300W
Switches	IRFP4568PBF
Transformer core	Ferrite N87
Transformer turns, T_1	2:1
T_2	1:1
Auxiliary inductor L_1	$100\mu H$
Capacitors C_1 and C_2	$330\mu F$
Output Capacitors	$330\mu F$
DC blocking capacitor C_b	$60\mu F$
Switching frequency	20kHz

TMS320F28335 from Texas Instruments is used to control the DC/DC converter.

Fig. 14 shows the experimental waveforms when the normalized active power is 0.4 (p.u.). v_{A2A1} and v_{A2A3} are the voltages of primary full bridges. v_{B1B2} is the voltage of secondary full bridge. v_{Cb} is the voltage of the blocking capacitor. The full bridge connected with T_2 is modulated as half bridge and v_{Cb} exists 25 V DC offset in Figs. 14 (a), (b), and (c). The full bridge connected with T_2 is modulated as full bridge and v_{Cb} exists 0 V DC offset in Figs. 14 (d), (e) and (f). Figs. 14 (a) and (f) is the waveforms when input voltage matches output voltage, which waveforms are similar to the traditional DAB converter with SPS. As Figs. 14 (b) and (c) shown, the converter works under pattern B and pattern A in forward buck mode when V_2 increases to 28 V and 40 V, which are corresponding to the region of pattern B and A in Fig. 8 (a). Corresponding duty cycle is also increasing to keep voltage-second balance. The converter works under pattern A and pattern B in forward boost mode when V_2 increases to 52 V and 60 V, which are corresponding to the regions of pattern B and A in Fig. 8 (b). According to the current polarity at turn-on instant, ZVS is realized in Fig.14.

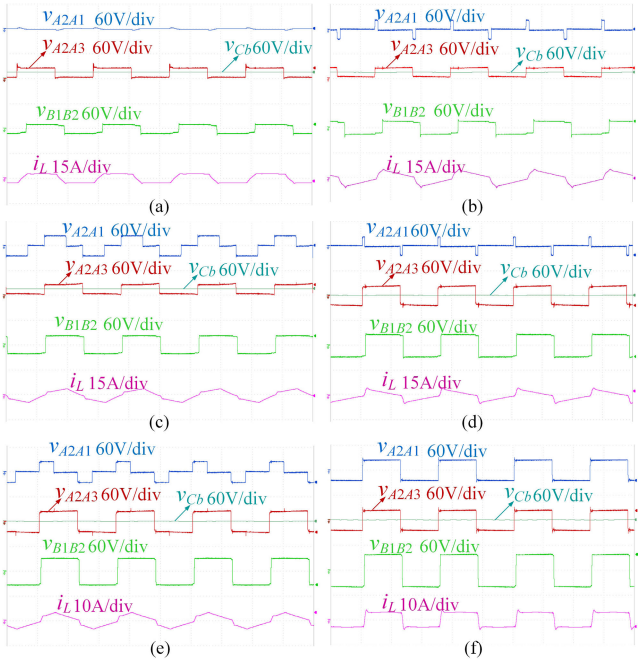

FIGURE 14. Experimental waveforms with the normalized power $P = 0.4$ (p.u.) in forward mode. (a) $V_2 = 25$ V. (b) $V_2 = 28$ V, pattern B. (c) $V_2 = 40$ V, pattern A. (d) $V_2 = 52$ V, pattern B. (e) $V_2 = 60$ V, pattern A. (f) $V_2 = 75$ V.

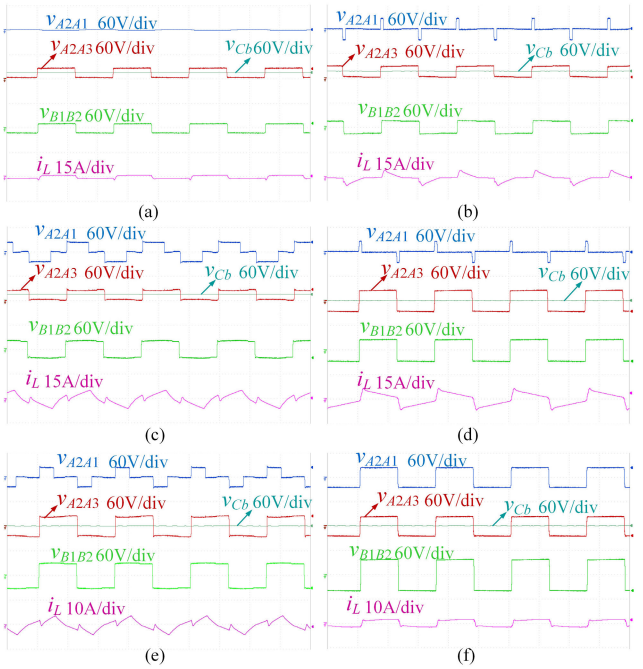

FIGURE 15. Experimental waveforms with the normalized power $P = 0.1$ (p.u.) in forward mode. (a) $V_2 = 25$ V. (b) $V_2 = 28$ V, pattern A. (c) $V_2 = 40$ V, pattern C. (d) $V_2 = 52$ V, pattern A. (e) $V_2 = 60$ V, pattern C. (f) $V_2 = 75$ V.

Fig. 15 presents the operation waveforms with the normalized power $P = 0.1$ (p.u.). Figs. 15 (a), (b), and (c) are the waveforms in forward buck mode which have 25 V DC offset. Also, Figs. 15 (d), (e) and (f) are the waveforms in forward boost mode which have 0 V DC offset.

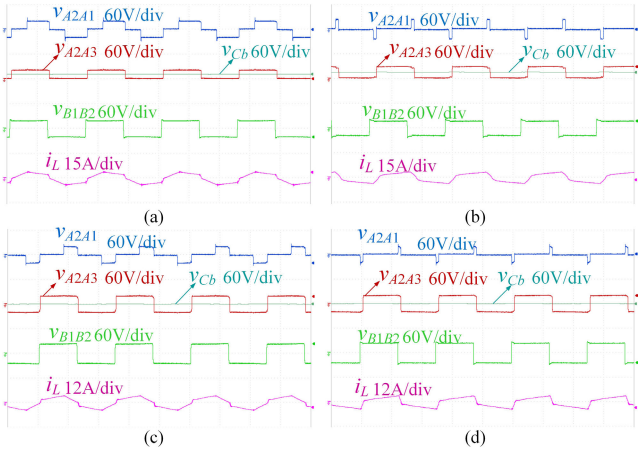

FIGURE 16. Experimental waveforms with the normalized power $P = 0.4$ (p.u.) in reverse mode. (a) $V_2 = 40$ V, pattern A. (b) $V_2 = 28$ V, pattern B. (c) $V_2 = 60$ V, pattern A. (d) $V_2 = 52$ V, pattern B.

Figs. 15 (a) and (f) show the proposed converter works as the conventional DAB. Figs. 15 (b) and (c) show that it works in pattern B and pattern C in forward buck mode when V_2 increases to 28 V and 40 V, which are corresponding to the regions of pattern B and C in Fig. 8 (a). The proposed converter works under pattern B and pattern C when V_2 increases to 52 V and 60 V, which are corresponding to the regions of pattern B and C in Fig. 8 (b). According to the current polarity at turn-on instant, ZVS is realized in Fig. 15.

Fig. 16 shows reverse operation waveforms with the normalized power $P = 0.4$ (p.u.). v_{B1B2} is leading to v_s and duty cycle is set up on opposite direction. Current waveforms i_L are mirror-symmetrical to forward operation mode as shown in Fig. 6.

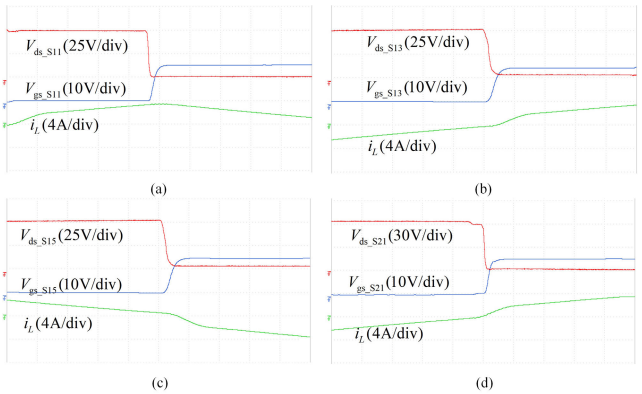

FIGURE 17. ZVS waveforms in forward mode when $V_2 = 60$ V, $P = 0.4$ (p.u.). (a) S_{11}. (b) S_{13}. (c) S_{15}. (d) S_{21}.

Figs. 17 and 18 illustrate gate-source voltage, drain-source voltage and the inductor current at turn-on instants of S_{11}, S_{13}, S_{15} and S_{21}, when the voltage works at 60 V and the normalized active power P is 0.4 (p.u.) in forward and reverse mode. The drain-source voltage of the switches has been reduced to zero before turning ON. All the switches realize ZVS in forward and reverse direction as shown in Fig. 8.

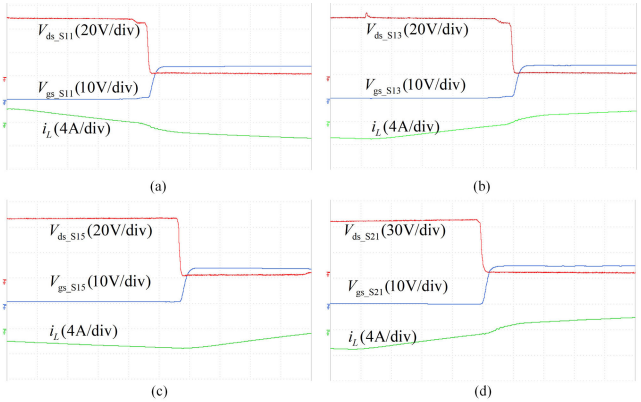

FIGURE 18. ZVS waveforms in reverse mode when $V_2 = 60$ V, the normalized active power $P = 0.4$ (p.u.). (a) S_{11}. (b) S_{13}. (c) S_{15}. (d) S_{21}.

B. EFFICIENCY AND LOSS DISTRIBUTION

In order to verify the performance of the proposed converter, a traditional DAB converter and DTAB are used for comparison at same active power. For the justification of comparison, the half bridge connected to a constant voltage in DTAB is replaced with a full bridge. The efficiency versus output voltage at 80% of load and 20% of load is plotted in Fig. 19. When V_2 is 50 V ($K = 1$), DAB is more efficient than proposed converter and DTAB for one less transformer. When the gain is away from the optimal operating point ($K = 1$), the proposed converter is more efficient. This phenomenon is attributed to lower transformer RMS current and wider soft switching region especially in light load for the proposed converter. Although the DTAB is more efficient in quite low output voltage, it only obtains improved efficiency from 0.5 to 1.

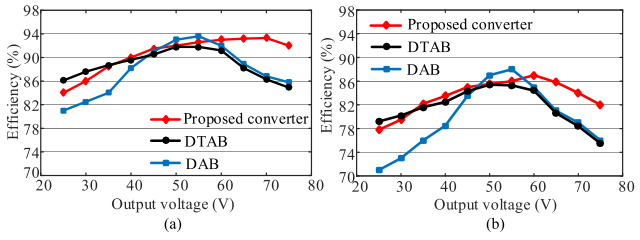

FIGURE 19. Efficiency versus output voltage at different loads in forward mode. (a) $P = 0.4$ (p.u.). (b) $P = 0.1$ (p.u.).

The measured efficiency of proposed converter, DAB and DTAB from 20% load to 100% load is illustrated in Fig. 20. When output voltage is 40 V, the efficiency of proposed converter is very close to that of DTAB, which is more efficient than traditional DAB converter as shown in Fig. 20 (a). That's because DAB converter has a narrow ZVS range at light load. When the load reaches 60% to 100% in reverse mode, DTAB suffers from hard switching as shown in Fig 10 (b),

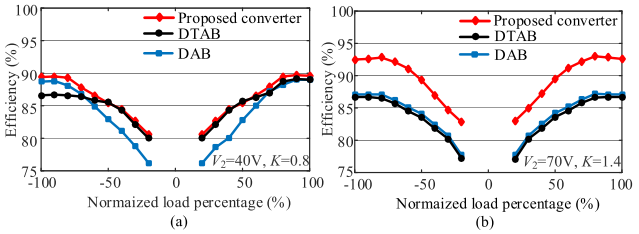

FIGURE 20. Normalized load efficiency at different output voltage. (a) $V_2 = 40$ V. (b) $V_2 = 70$ V.

which leads a low efficiency. In relatively high output voltage range (over 70 V), the proposed converter exhibits distinct advantage over the other two converters.

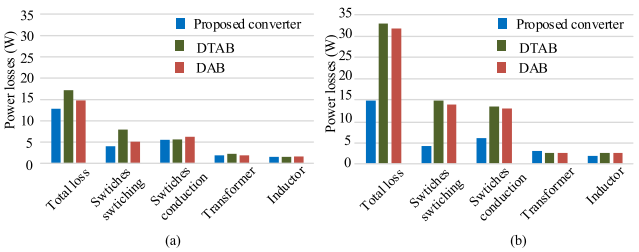

FIGURE 21. Loss evaluation with the normalized active power $P = 0.4$ (p.u.) with 80% load. (a) $V_1 = 40$ V in reverse mode. (b) $V_2 = 70$ V in forward mode.

Fig.21 shows the loss evaluation for the dual transformer based converter with the proposed converter when normalized power P is 0.4 (p.u.), corresponding to 80% of full load. As shown in Fig.21 (a), for reverse mode ($V_1 = 40$ V), switching loss of DTAB is bigger because of hard switching. For forward mode ($V_2 = 70$ V), DAB and DTAB have higher switching loss for hard switching and conduction loss for large RMS current in Fig.21 (b).

V. CONCLUSION

To achieve ZVS in wide conversion gain range to satisfy battery charging and discharging, a dual-transformer-based full bridge converter using a block capacitor was proposed. The duty cycle of primary side is adjusted to extend ZVS range by regulating the four-level voltage in the secondary side of the transformers to match a variable output voltage according to voltage-second balance in both boost and buck modes. It enables efficient operation within $K = (0.5\text{-}1.5)$. The mirror-symmetrical modulation is used to obtain a wide ZVS range in reverse power flow. The performances of the proposed converter were compared to the published dual-transformer converter in terms of power characteristics, ZVS range and RMS current to demonstrate the advantages. A 300 W prototype is implemented to verify the effectiveness of the proposed converter. Theoretical and experimental results demonstrate the proposed converter is suitable for wide output range.

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