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# Injection Locking in Switching Power Amplifiers

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**ABSTRACT** In this work, injection locking in switching power amplifiers (PAs) is studied. Traditionally, injection-locked PAs (ILPAs) have supported phase modulation, with injection locking used primarily to improve the power-added efficiency by reducing the power required to drive the ILPA. Since the output power in conventional ILPA architectures is mainly contributed by the locked oscillator in an ILPA, the amplitude modulation is difficult to achieve unless supply modulation is employed. In the ILPA presented in this work, it is shown that by injection locking a switching PA and a power oscillator, improvement in both power-added efficiency and drain efficiency can be achieved as compared to just a switching PA. Moreover, amplitude modulation at a fixed supply voltage is achieved using an RF-DAC approach to scale both the switching PA and the locked oscillator. This approach employs variable injection-strengths varying from $\leq 1$ (weak injection locking) to $>1$ (strong injection locking) to achieve the required power back-off. Accordingly, new formulations are introduced to extend the existing injection locking theory for injection strengths $>1$ case in ILPAs. Benefits of a larger injection strength on lock-range, maximum allowable symbol rate, AM-PM distortion and phase noise performance for an ILPA is provided. An ILPA is designed to support 64-QAM and implemented in a standard 65-nm bulk CMOS process. A peak drain efficiency of 42.7% and power-added efficiency of 40% is measured at the highest output power of 23 dBm, operating from a 1.45 V PA power supply at 2.5 GHz. Modulation tests with 5/50 MSym/s 64-QAM signals achieve the measured RMS EVM of 1.9%/3.1% with the average output power, drain efficiency and power-added efficiency of 18.1 dBm, 27.9% and 25.8% at 2.5 GHz, respectively.

**INDEX TERMS** AM-PM, CMOS integrated circuits, efficiency, inverse class-D PA (ICDPA), injection locking, injection-locked power amplifier (ILPA), power amplifier (PA), power oscillator, polar modulation, switching circuits.

## I. INTRODUCTION

Modern wireless transmission schemes increase data rate within a limited spectrum by adopting spectral-efficient modulation techniques such as QAM. These varying envelope modulation techniques have high peak-to-average-power ratio (PAPR). Therefore, power amplifiers (PAs) with high drain efficiency ($\eta_D$) and high power-added efficiency (PAE) are required to work efficiently with power back-off.

Injection-locking (IL) in oscillators have been studied extensively and has found several practical applications [1]–[9]. IL has also been used to design injection-locked power amplifiers (ILPAs) [10]–[19]. The focus of several prior-art has been in improving the PAE – including radio frequency (RF) PAs [10]–[15], transmitter (TX) with low power-output for wireless sensor networks [12], [16], or mm-wave PAs with relatively low power-output [17], [18]. Nevertheless, widespread adoption for ILPAs have been limited due to several limitations, the three primary being narrowband operation, inability to support varying-envelope modulation and power back-off, and lack of rigorous analysis for functional reliability.

In traditional ILPAs, the output power depends on locked power oscillator (PO) strength and does not reduce proportionally with the input signal [10], [17], [20]. This poses a problem for implementing amplitude modulation (AM) for

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varying-envelope signals in an ILPA at a fixed supply voltage. In this work, AM is realized by employing a radio frequency digital-to-analog converter (RF-DAC) approach to vary the strengths of both the switching PA and the PO. An inverse Class-D PA (ICDPA) is used as a switching PA. The ICDPA transistors are used to lock the PO and both of them constitute the ILPA. The RF-DAC approach gives rise to varying injection-strength ($K$) to achieve the desired modulation. $K$ is a crucial parameter for ILPA as it controls the lock-range, locking time, phase of currents in IL phasor diagram and phase-noise (PN). This directly influences the PA performance parameters such as modulation bandwidth, AM-PM distortion and error-vector magnitude (EVM). Additionally, this work shows that other parameters such as maximum output power ($P_{out}$), drain efficiency ($\eta_D$) and power-added efficiency (PAE) are also affected and can be improved. Thus, an appropriate selection of $K$ is required to meet the desired PA specifications. Accordingly, this work provides the necessary circuit techniques, theoretical derivations, practical design guidelines and discussion on trade offs. To summarize, this work contributes to the following: (1) drain efficiency improvement is shown in an ILPA along with the PAE improvement, (2) high strength injection locking theory for the PA is derived, (3) excess AM-PM distortion component in an ILPA arising from the injection locking mechanism has been observed and analyzed, (4) analyzing the role of PO in out-of-band phase noise improvement in an ILPA, and (5) design methodology and design equations are provided for the proposed ILPA to achieve the desired symbol rate and higher drain efficiency.

The paper is organized as follows: Section II describes the prior-art in ILPA and PO. Section III introduces IL theory and extends it for high injection strengths. Section IV lays the theoretical framework for ILPA and introduces formulations and circuit techniques that enable both AM and phase modulation (PM) in ILPA, and increase both PAE and $\eta_D$. Trade-offs and design guidelines for the maximal possible symbol rates, AM-PM distortion, and phase noise considerations are described next in Section V. Measurement results for a proof-of-concept prototype are presented in Section VI, and the paper is concluded in Section VII.

## II. PRIOR ART IN ILPAs

ILPAs can be categorized into two types: (1) Dual-tank: Wherein a single switching transistor also provides the necessary negative resistance to create an injection locked oscillator (ILO) with a resonant tank connected to the input, and a separate load network connected to the output (forming another tank), as shown in Fig. 1(a) [12]–[15]. (2) Single-tank: Wherein a differential-pair of transistors are used for switching as well as providing the negative resistance, with a single LC network that serves as an ILO resonant tank as well as load network, as shown in Fig. 1(b) [10], [11], [16]–[18]. A recent work, [21], [22] uses injection locking to achieve 16-QAM modulation using an injection locked power

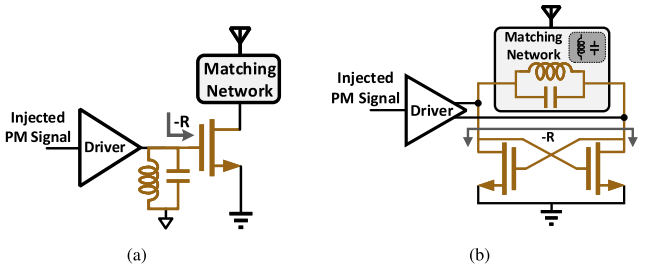



**FIGURE 1.** (a) A dual-tank ILPA. (b) A single-tank ILPA.

up-converter. It works as a linear PA for low power output levels and as a supply modulated PA for achieving high power output levels. The up-converted signal from a mixer stage is injected at the source of the cascode transistor; a different injection scheme than other ILPAs where the drain node is the point of injection. However, an off-chip supply modulator is used for implementing amplitude modulation in these works. The matching network is also off-chip, thereby incurring low loss in matching network leading to higher drain efficiency, at the expense of increased cost.

### A. LIMITATIONS OF DUAL-TANK ILPA

The input transistor of a switching PA is large, and driving a large capacitance leads to a significant power consumption for the driver. Instead, the switching PA can be designed in such a way that its input conductance is negative. Together with an inductor at the input, it acts as an oscillator, injection locked to the driver frequency. Furthermore, as the driver is essentially driving an ideal LC tank, it saves power in the driver [12], [13]. However, this topology faces several drawbacks: (a) A reduction in power consumption of the driver and ILO demands high $Q$ of the input resonant tank, but a higher $Q$ leads to a reduced injection lock-range and modulation bandwidth. (b) The input tank, a single transistor to provide negative resistance as well as switching, and another tuned network at the output for shaping the switching signals and load transformation – are entwined, complicating the design and optimization for efficiency. (c) The driving signal into the switching transistor becomes sinusoidal which increases the transistor's on-off switching time, adversely impacting $\eta_D$. (d) The use of an additional inductor at the input increases area. (e) The negative input conductance of the PA transistor also depends upon the driver output power, further complicating the design [12], [13].

On-off keying is implemented in [14], [15] by driving the cascode transistors in a dual-tank ILPA. However, switching thick-oxide cascode transistors limits the bandwidth, and driving them further incurs large power penalty, and the need for PWM generation circuit, isolator and bandpass filter further nullifies any efficiency improvement due to IL. Moreover, no measurement results are shown for varying envelope modulation.

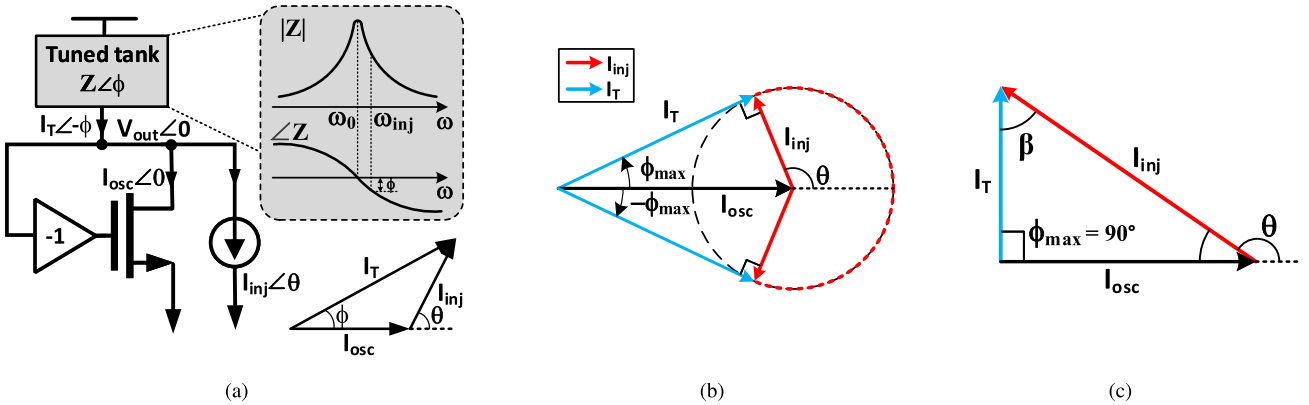



**FIGURE 2.** (a) Injection locking in an LC oscillator, its current vector diagram and magnitude and phase response of a parallel LC tank. (b) Vector diagram at the edge of the lock-range for $K \leq 1$. (c) Vector diagram at the edge of the lock-range for $K > 1$.

### *B. LIMITATIONS OF SINGLE-TANK ILPA*

Based on the severe limitations of dual-tank ILPAs, we choose the single-tank architecture for this work. However, there are still limitations in single-tank ILPA, and ILPAs in general that we must address, as listed below:

(a) A major limitation of any prior-art ILPA, single-tank or dual-tank, is that they inherently lack the capability for AM *at a constant supply voltage* [17], [20]. This is because the output power is generated from the oscillator core which does not vary with the input injected power for weak injection. It can be noted that other ILPAs which implement AM such as [21], [22] use off-chip supply modulator to achieve it. Thus, a conventional ILPA operating at the fixed power supply provides almost constant power for any input signal within its lock-range and is not suitable for QAM.

This work addresses this problem by employing low ($K \leq 1$) to high injection-strengths ($K > 1$) in the proposed ILPA wherein an ICDPA injection locks a PO. To provide further flexibility for AM, the strength of the PO is also tuned. Since prior literature provides the theory for injection locking in PAs only for $K < 1$, a theoretical foundation for $K \geq 1$ has been developed in this work.

(b) Narrow lock-range is another drawback of an ILPA that has limited the modulation bandwidth in prior-art [19].

It is known that large $K$ values are also helpful in improving the lock-range [1]. An increase in lock-range reduces the locking time of the oscillator and consequently increases the injection locking bandwidth. A reduced locking time, therefore, allows ILPA to support a higher data rate. In this work, we explore the maximum symbol rate considerations for an ILPA and derive a 1:1 relationship between the maximum symbol rate and the injection-strength, as well as the associated trade-offs for the maximum PAE.

(c) Although IL has been used for improving the PAE, simultaneously increasing $\eta_D$ is also desirable. In prior-art single-tank ILPAs, the cross-coupled devices providing the negative resistance also does most of the switching, thereby acting as a power oscillator, and the injection devices, sized comparatively smaller, provides the signal for IL and PM.

In this work, it is shown that by sizing the injection devices larger than the cross-coupled devices, the injection devices acts as a main contributor to output power and separate cross-coupled devices further assist the switching through positive feedback, thereby both $\eta_D$ and PAE can be simultaneously improved.

(d) Prior-art in ILPA used weak injection-strength for IL. Signals emanating from different circuits in an SoC environment can parasitically couple to the oscillators and can cause undesired pulling or locking.

*In essence, all of the prior-art ILPA designs [10]–[17], [19] have been designed to predominantly work with weak injection devices and a strong PO. In our work, we design an ILPA with strong injection devices and a weak PO.*

## III. HIGH-STRENGTH INJECTION LOCKING

The theory of IL for oscillators has been described in excellent detail before, but limited to injection strength $K < 1$ [1]–[4]. We extend its theory for even higher injection strengths ($K > 1$) in this Section so as to enable AM for ILPA and permit wideband operation. Next, we briefly describe the basics of IL in order to extend the theory.

An LC oscillator, having a resonance frequency of $\omega_0$ under the impression of an external signal of frequency of $\omega_{inj}$ can start to oscillate at $\omega_{inj}$ if the two frequencies are close to each other. This phenomenon is known as IL and the LC oscillator is said to be injection locked to $\omega_{inj}$. The maximum and minimum values of $\omega_{inj}$ which can lock the oscillator, defines the lock-range of the oscillator.

When the oscillator is locked, the oscillator current, $I_{osc}$, and the injected current, $I_{inj}$, combine together to generate the total current out of the tank, $I_T$, as shown in the vector diagram in Fig. 2(a). The magnitude $|Z|$ and phase $\angle Z$ of the tank impedance as a function of frequency are also shown. As $I_{osc} = -g_m V_{out}$, $V_{out}$ and $I_{osc}$ are in phase with each other in the locked condition for sustained oscillations for any values of $I_{inj}$ and $\omega_{inj}$. If the tank is operating at $\omega_{inj}$ which is different than its natural resonance frequency of $\omega_0$, the tank impedance $Z$ either looks inductive or capacitive and

$I_T$ therefore sees a nonzero phase $\angle Z = -\phi$. This requires that $I_T$ has a phase of $\phi$ to cancel the $-\phi$ phase from the tank so that phase of $V_{out}$ is zero. To provide this necessary phase shift, $I_{inj}$ combines with $I_{osc}$ at an angle $\theta$.

### A. PHASE SHIFT AND LOCK-RANGE AS A FUNCTION OF INJECTION-STRENGTH FOR $K \leq 1$

In this scenario, the relation between $\theta$ and $\phi$ can be found from [2], [4] as

$$\tan\phi = \frac{I_{inj}\sin\theta}{I_{osc} + I_{inj}\cos\theta}, \tag{1}$$

and $K$ is the injection-strength, given by

$$K = \frac{I_{inj}}{I_{osc}}. \tag{2}$$

For the given magnitudes of $I_{inj}$ and $I_{osc}$, the locus of current vector $I_T$ is the dotted circle as shown in Fig. 2(b). For the maximum phase $\phi_{max}$, $I_T$ becomes a tangent to this circle and $I_T$ and $I_{inj}$ form an angle of 90° with each other and therefore $\theta_{max} = 90° + \phi_{max}$. In this condition [2], [3],

$$\sin\phi_{max} = \frac{I_{inj}}{I_{osc}} = K, \tag{3}$$

$$\tan\phi_{max} = \frac{I_{inj}}{I_T} = \frac{I_{inj}}{\sqrt{I_{osc}^2 - I_{inj}^2}} = \frac{K}{\sqrt{1-K^2}}. \tag{4}$$

Thus, $K$ determines $\phi_{max}$ and $\theta_{max}$. From the tank phase response $\angle Z(\omega)$ in Fig. 2(a), the maximum lock frequency, $\omega_{inj,max}$ corresponds to $\phi_{max}$ and the single-sided lock-range is given by $\omega_{inj,max} - \omega_0$. For frequencies in the vicinity of $\omega_0$, the phase shift of the tank at $\omega_{inj}$, $\angle Z(\omega_{inj})$, is given by [1]

$$\tan(\angle Z(\omega_{inj})) = \frac{2Q}{\omega_0}(\omega_0 - \omega_{inj}). \tag{5}$$

From (4) and (5), the lock-range $\omega_L$ can be obtained as [2]

$$\omega_L = |(\omega_0 - \omega_{inj})| = \frac{\omega_0}{2Q}\frac{K}{\sqrt{1-K^2}}. \tag{6}$$

Clearly, $K$ should be increased for extending the lock-range. A large lock-range is desirable for improving the locking time/transient response of an ILO [1], [2], [23]. However, (4) to (6) are valid for small injection-strengths or $K \leq 1$ scenario. For a constant $I_{osc}$, $I_T$ decreases when $K$ is increased for obtaining a higher $\omega_L$. In the limiting case when $\phi_{max}$ approaches 90° for $K = 1$, $I_T$ reduces to zero implying no oscillations. Here, (6) suggests an infinite lock-range for $K = 1$, however, the oscillation amplitude is zero as explained above. Moreover, in a practical scenario, the oscillations are further exacerbated as $\omega_{inj}$ moves further away from $\omega_0$, due to a decrease in the magnitude of tank impedance. Beyond a certain $\omega_{inj}$, the oscillator closed loop-gain becomes less than unity and oscillations cannot be sustained.

### B. PHASE SHIFT AND LOCK-RANGE AS A FUNCTION OF INJECTION-STRENGTH FOR $K > 1$

Next, we explore the edge of the lock-range where $\phi_{max} = 90°$ for $K > 1$ in Fig. 2(c). A recent work [24] provides a phasor-based analysis of IL for all $K$ cases in oscillators. For $K > 1$, the current phasors form a right-angle triangle where $I_{inj}$ is the hypotenuse. This is in contrast with $K \leq 1$ case where $I_{osc}$ is the hypotenuse in the vector diagram. It can be seen that $\phi_{max} = 90°$ can be achieved by all $K > 1$ cases. Also, $I_T$ can be increased with an increase in $K$ for a constant $I_{osc}$ and its magnitude for a particular $K$ is given by

$$I_T = \sqrt{I_{inj}^2 - I_{osc}^2} = I_{osc}\sqrt{K^2 - 1}. \tag{7}$$

$\theta_{max}$, for $K > 1$, is given as

$$\theta_{\max} = 90° + \beta = 90° + \arcsin(\frac{1}{K}). \tag{8}$$

Combining for all $K$ cases, $\theta_{max}$ is given by

$$\theta_{\max} = \begin{cases} 90° + \arcsin(K), & \text{if } K \leq 1 \\ 90° + \arcsin(\frac{1}{K}), & \text{if } K > 1. \end{cases} \tag{9}$$

Thus, $K > 1$ allows higher magnitude of $I_T$ to be sustained at larger $\phi$ values, resulting in AM with high modulation bandwidth and higher lock-range, pivotal to the proposed ILPA. A large $I_T$ also makes up for the degraded tank impedance at higher $\omega_L$ thereby improving the oscillation amplitude.

Having established the operation of IL for all $K$, an ILPA design employing both $K \leq 1$ and $K > 1$ is presented next.

## IV. WIDEBAND QAM ILPA DESIGN

In this section, we first describe the design of an ICDPA, compare its $\eta_D$ to a stand-alone PO, and then combine the two for the proposed ILPA that can support AM and PM, and has improved $\eta_D$ as well as PAE.

### A. ICDPA AND PO DESIGN

The digital-modulated PA architecture [25] has been a popular implementation to achieve AM in non-linear PAs for high-BW, varying-envelope signals with better $\eta_D$ at power back-off than linear PAs. Consider a digitally-modulated ICDPA architecture for implementing AM as shown in Fig. 3(a). $M_1$ and $M_2$ are the power transistors whose width are scaled in a binary fashion over six cells. Digital NAND gates enable/disable a cell to receive the PM signal from the input buffer chain, thereby resulting in an RF-DAC controlled by the 6-bit binary AM word $A_0 - A_5$. A decrease in the AM codeword $A_0 - A_5$ reduces the effective power transistor width which in-turn reduces the current $I_D$ in ICDPA while increasing the effective $R_{on}$ of the power transistors. Thus, power back-off is obtained in an ICDPA at the cost of lower $\eta_D$ as shown in Fig. 4. The buffer-chain is implemented in a tapered topology to reduce power consumption while maintaining the necessary switching speed. Cross-coupled inverters are used to maintain the signal in

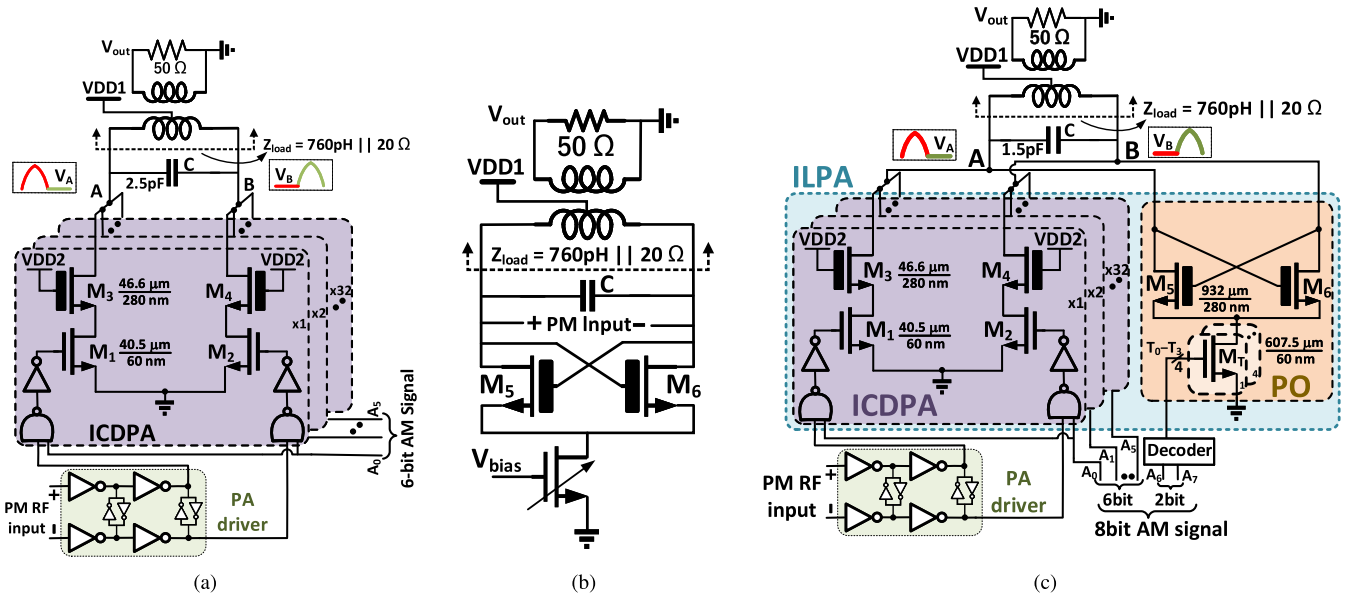



**FIGURE 3.** Schematic of (a) an ICDPA, (b) a PO with tunable tail-width, and (c) an ILPA: An ICDPA assisted by a PO.

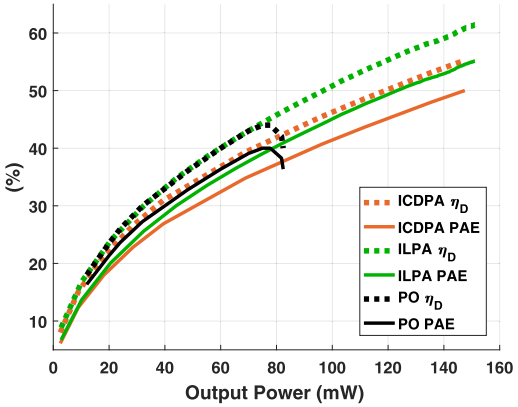



**FIGURE 4.** Simulated $\eta_D$ and PAE vs. $P_{out}$ for an ICDPA, a PO and an ILPA interfaced with same load.

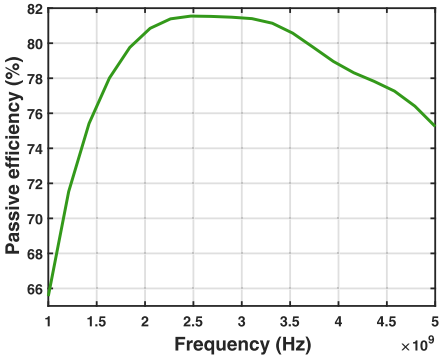



**FIGURE 5.** Passive efficiency of the load transformation network.

differential phase along the buffer chain. The gate of the thick-oxide cascode transistors are DC biased at 2.5 V.

An implementation of a PO with a variable $P_{out}$ capability is shown in Fig. 3(b). Here, the width of the tail transistor controls the tail current which changes the oscillation amplitude given by $(2/\pi)I_{tail}R_{load}$. For implementing PM, the PO can be injection locked to an incoming phase signal and work as an ILPO.

To better understand the capability of a PO (Fig. 3(b)) vs. an ICDPA (Fig. 3(a)), both are interfaced with the same output load consisting of a transformer to convert the off-chip 50 Ω to a smaller effective PA resistance. Fig. 5 shows the passive efficiency of the load transformation network, which is realized by a 1:2 transformer loaded with 50 Ω at its secondary winding. The passive efficiency of the network in post-layout is 81.5% at 2.5 GHz and is higher than 65% in the 1-5 GHz frequency range. The imaginary and real values of Y11 into the transformer primary winding from the post-layout simulations are shown in Fig. 6 and Fig. 7, respectively. At 2.5 GHz, the impedance looking into the primary is a combination of an inductance of 760 pH in parallel with a resistance of 20 Ω. Therefore, the quality factor of the tank is 1.7. A MIM capacitor, used in parallel with the load in both cases, in combination with the large parasitic drain capacitance of the transistors and wiring capacitance tunes out the +j11.9 Ω (0.76 nH inductor) load at an operating frequency $f_0 = 2.5$ GHz.

Both designs are optimized for highest $\eta_D$ and the resulting $P_{out}$ and PAE with power back-off are shown in Fig. 4. The ICDPA shows a maximum $P_{out} = 147.5$ mW, maximum $\eta_D = 55.3\%$ at a power-transistor width $(M_1, M_2)$ of 2.55 mm. A buffer chain driving the ICDPA consumes another 28 mW power, and therefore PAE is calculated as $P_{out}/(P_{DC} + P_{buffer}) = 50\%$. On the other hand, the PO has a $P_{out} = 77$ mW, $\eta_D = 44\%$ at a power-transistor $(M_5, M_6)$ width of 0.69 mm. The efficiency of PO starts to falls off when

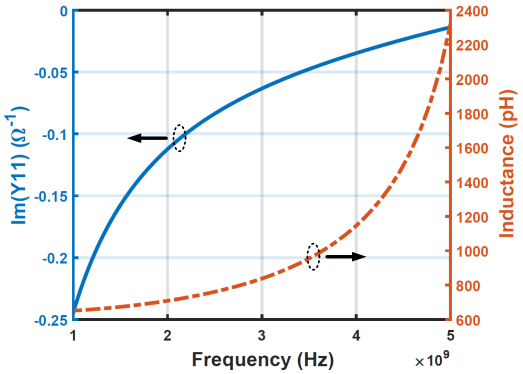



**FIGURE 6.** Im(Y11) and equivalent inductance of the load transformation network.

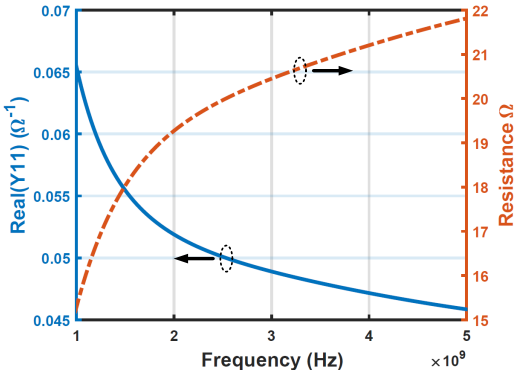



**FIGURE 7.** Re(Y11) and equivalent resistance of the load transformation network.

$P_{out}$ exceeds 77 mW. Thus, when designed for maximum $\eta_D$, at their highest $P_{out}$ values, the ICDPA is about 6% points more efficient, has wider range of $P_{out}$ values and produces 1.9× higher $P_{out}$ than the PO, although also occupying a larger transistor area. However, $\eta_D$ of the PO is better than that of the ICDPA for providing output power from 17 mW to 77 mW, as shown in Fig. 4 which provides the motivation for combining the PO with the ICDPA in this work.

A lower power-transistor width and $P_{out}$ of the PO as compared to the ICDPA can be explained as follows. A PO is self-driven and therefore does not follow the zero-voltage switching condition for obtaining higher efficiency as in a PA. The PO in Fig. 3(b) works as a Class-B oscillator whose theoretical maximum $\eta_D$ is limited to $2/\pi$ [26]. On analyzing the I/V waveforms of the PO, it is observed that power is dissipated throughout the signal time-period, peaking twice per cycle at the drain-gate voltage crossings. A smaller power-transistor width (compared to the ICDPA) provides the highest $\eta_D$ for the PO and allows a comparatively lower current to be commutated into the load which reduces $P_{out}$.

Implementing a large power back-off in a PO can be challenging. A decrease in tail current reduces the $g_m$ of the NMOS cross-coupled transistors and pushes the PO closer to the verge of non-oscillation. Therefore, the tail current

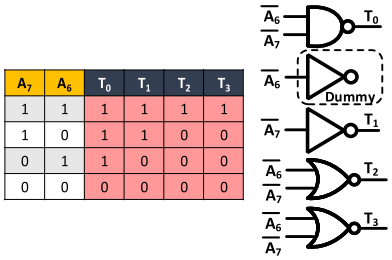



**FIGURE 8.** Decoder design for the PO.

cannot be arbitrarily decreased for AM which limits its power back-off range and hence limits its AM capability. Another drawback is that the PN of the oscillator output degrades for a lower output amplitude. Thus, stand-alone POs are seldom used in transmitters. The output signal of a PO driving a low impedance output load has a degraded PN characteristic. Also, it has a poor frequency stability. In [16], a low PN signal from a clean LO is used to lock the PO (forming an ILPA) for improving its PN performance.

### B. COMBINING ICDPA WITH PO AS AN ILPA

If an ICDPA is used to injection lock a PO, both the ICDPA and PO can be digitally modulated and in combination deliver the desired output power levels for power back-off. Fig. 3(c) shows such a proposed topology which reaps the benefits from both the architectures. The ICDPA is chosen as the PA architecture for this ILPA because of two factors: (1) Its intrinsic implementation as a differential design is suitable for assisting it with a cross-coupled pair implementation (for PO), and (2) both the ICDPA and the PO require a parallel LC tank as the load network. Such an ILPA can also be used in differential class-E design as used in [10], [11]. An optimum digital selection chooses the strengths for PO and PA in a manner which ensures higher $\eta_D$ and PAE of this proposed ILPA for a given output power, as well as higher maximum $P_{out}$ in comparison to a stand-alone ICDPA or PO. Additionally, $\eta_D$ of the ILPA also improves because of the following reasons: (1) reduction of the transistor losses, (2) increased in the fundamental output power, (3) decrease in power in harmonics.

Reduction in transistor loss is caused by a reduction in the effective $R_{on}$ of the PA because the resistance of the triode transistors $M_1$-$M_3$ and $M_5$-$M_T$ are in parallel in an RF half-cycle. When $M_1$ is ON and $M_2$ is OFF, a high drain swing, $V_B$, turns on the transistor $M_5$ to assist transistors $M_3$-$M_1$ in pulling down $V_A$ to zero. $M_6$ is turned off due to low $V_A$ during this half-cycle and facilitates a high voltage swing to build up at node B. Thus, effective $R_{on}$ for discharging node A to ground decreases resulting in an increase in $\eta_D$. Similarly, $R_{on}$ decreases for node B in the other half cycle. From the DC simulations, the effective $R_{on}$ of PA is 480 mΩ from only $M_1$-$M_3$ transistors, which reduces to 370 mΩ when the PO is attached. Further, the high swings of $\pi \cdot$VDD at node A/B, result in a large $V_{gs}$ for the cascode transistors $M_5/M_6$

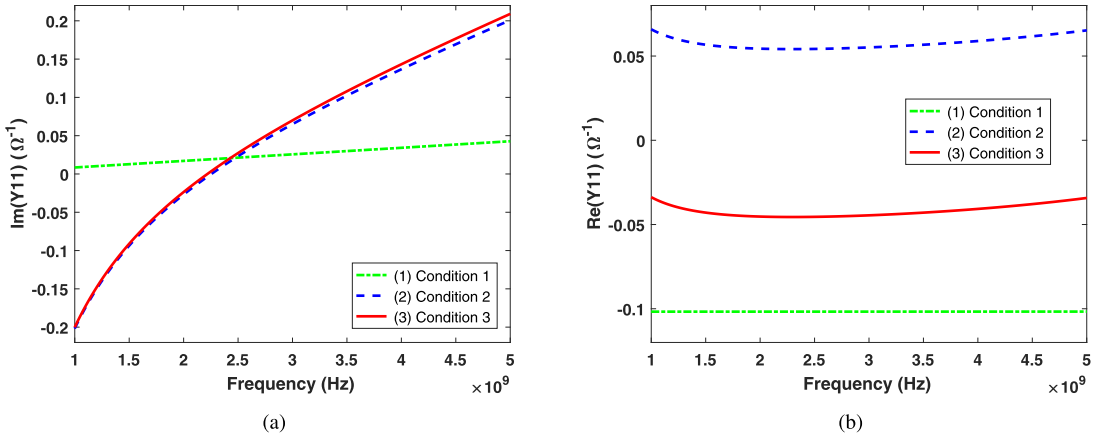



**FIGURE 9.** (a) Im(Y11), and (b) Re(Y11) for the three simulation conditions.

and therefore realize a small triode resistance. Notably, this resistance decreases sharply with the increase in PA VDD because of the $\pi$ multiplier. (2) happens because $-g_m$ from the cross-coupled transistors improves the differential signal swing at the node A-B resulting in a higher output power in the fundamental. The technique helps (3) by reducing the harmonics in the PA output since the cross-coupled pair reduces the even-order harmonics. From the simulations, it was observed that power in harmonics of the ILPA reduces by 1.1% points of the overall DC power as compared to an ICDPA.

The RF-DAC of the ILPA is controlled by the 8-bit word $A_0 - A_7$. Bits $A_0 - A_5$ and bits $A_6 - A_7$ control the effective transistor width and, therefore, the strength of the ICDPA and the PO, respectively. A decoder is used to decode the 2-bit AM signal $A_6 - A_7$ to bits $T_0 - T_3$, which can change the tail current in the PO in a thermometric manner. The decoder design for the PO is shown in Fig. 8. $A_7A_6$ assumes the values: 00, 01, 10 and 11 to enable $0\times$, $0.25\times$, $0.5\times$, and $1\times$ PO tail transistor width, respectively. The size of the transistors in the LSB bit for $M_1/M_2$ is 40.5 $\mu$m/60 nm, and for $M_3/M_4$ is 46.6 $\mu$m/280 nm as shown in Fig. 3(c) and Fig. 3(a). When all bits are ON, the total width of the $M_1/M_2$ transistor is 2.55 mm/60 nm, and for $M_3/M_4$ transistor is 2.93 mm/280 nm. The overall width of transistor $M_T$ when the PO is entirely ON is 607.5 $\mu$m/60 nm.

At the ILPA drain terminals A-B in Fig. 3(c), the loaded impedance of the transformation network is parallel to the cross-coupled pair ($M_5$-$M_6$) and the ICDPA transistors ($M_3$-$M_4$). Fig. 9(a) and Fig. 9(b) shows a plot of simulated real and imaginary values of Y11 for a small input signal at A-B in three conditions: (1) (a) The loaded transformation network and the MIM capacitor are disconnected, (b) the ICDPA section of ILPA is disconnected, and (c) cross-coupled pair is turned ON ($A_6 - A_7 = 11$). This arrangement provides the input impedance of only the cross-coupled pair. (2) (a) The loaded transformation network and the MIM capacitor are connected, (b) the ICDPA part of ILPA is turned OFF, i.e., the AM bits $A_0 - A_5 = 00000$, and (c) cross-coupled pair is turned OFF ($A_6 - A_7 = 00$). This arrangement provides the input impedance of the loaded transformation network and the MIM capacitor with the parasitic drain capacitance of the OFF transistors $M_3$-$M_4$ and $M_5$-$M_6$. (3) (a) The loaded transformation network and the MIM capacitor are connected, (b) the ICDPA part of ILPA is turned OFF, i.e., AM bits $A_0 - A_5 = 00000$, and (c) cross-coupled pair is turned ON ($A_6 - A_7 = 11$). This arrangement gives a combination of the cross-coupled pair, load transformation network and the MIM capacitor with the parasitic drain capacitance of the OFF transistors $M_3$-$M_4$.

From the condition (1), it can be seen that the cross-coupled pair provides a broadband negative resistance of about $-10\ \Omega$ and a constant capacitance of 1.36 pF from 1-5 GHz. A capacitance of 5.4 pF is required to resonate the input inductance of 760 pH of the transformation network at 2.5 GHz. This capacitance is formed by the combination of MIM capacitor with the drain capacitance of the ICDPA and cross-coupled transistors. The value of the MIM capacitor is adjusted for both the ILPA and the ICDPA to achieve the highest $\eta_D$ for each. The value of the MIM capacitor is 1.5 pF for ILPA in Fig. 3(c) and 2.5 pF for ICDPA in Fig. 3(a). The parasitic capacitance from transistor layout and wiring capacitance contribute to 1.1 pF capacitance at node A-B in post-layout. Since 1.36 pF corresponds to small conductance of 0.02 S, the Im(Y11) does not change considerably from condition (2) to (3). However, due to the negative conductance of $-100$ mS from the cross-coupled pair, the Re(Y11) reduces from 54 mS to $-46$ mS. Therefore, from a small signal perspective, the combination of the load transformation network and cross-coupled pair presents a negative Re(Y11) of $-46$ mS. Therefore, the PO can easily oscillate the output load as evident from the measurement results in Fig. 19.

This digital selection of the ICDPA and the PO AM bits allows $K$ to assume a minimum value of 0.0625 and a maximum value of 16. For a specific $P_{out}$, an optimum width of the transistors used in the ICDPA and the PO can be selected

through 8-bit AM word for maximum $\eta_D$. If the minimum $P_{out}$ from the PO exceeds the desired $P_{out}$ from the ILPA, then the PO is fully switched-off and only the ICDPA is backed-off for achieving lower $P_{out}$ levels. In simulations, $\eta_D$ at the highest $P_{out}$ can be increased using this technique by 6.1% points (from 55.3% to 61.4%) using a 1 V supply (VDD1). A comparison of $\eta_D$ of the ILPA with PO and ICDPA is shown in Fig. 4. It can be observed that the ILPA provides equal or higher $\eta_D$ as compared to a PO or ICDPA for all power back-off values. Also, an increase in the highest $P_{out}$ and power back-off range can be noticed. In simulations, for 1 V PA supply, the power gain of ILPA can be calculated as $P_{out}/P_{in} = 150$ mW/12.8 mW $= 11.7$. $P_{in}$ is the power required to switch the PA switches $M_1/M_2$ of size $=$ 2.55 mm at 2.5 GHz, assuming 1 fF/$\mu$m gate capacitance. The power gain increases with an increase in PA supply voltage since $P_{out}$ increases while $P_{in}$ remains the same. The tail transistor $M_T$ does not significantly contribute to the overall power dissipation. The maximum and minimum power loss of the tail transistor is 11.67 mW and 842.2 $\mu$W, for codes $A_7 - A_0 = 01000001$ and 11111111, respectively.

For an ICDPA realized with $n$ binary-weighed bits having its LSB transistor width as $W_{M1}$, the total width ($W_{PA}$) of the ICDPA is given by $W_{PA} = (2^n - 1)W_{M1}$. Based on simulations, a ratio $r = W_{PA}/W_T$ can be found which maximizes the $\eta_D$ of the ILPA, where $W_T$ denotes the maximum width for the PO tail-transistor. In our simulations, the value of $r$ is 4.2. Digital selection bits enable AM while $r$ is roughly maintained for higher $\eta_D$ at the power back-off levels as compared to ICDPA. Next, an analysis of an ILPA design is presented.

The minimum injection-strength, $K_0$, when the LSB of the ICDPA locks the maximum width of the PO, is given by

$$K_0 = \frac{W_{PA}/(2^n - 1)}{W_T/2}. \tag{10}$$

If $C_{Pr}$ is the parasitic drain capacitance per unit width of a transistor, and assuming that the total capacitance, $C_L$, required to tune out the load inductor is provided by the capacitance of transistors (both from the ICDPA and the PO) and the explicit capacitance $C$, then

$$K_0(W_T/2)C_{Pr}(2^n - 1) + (W_T/2)C_{Pr} = 2C_L = \frac{1}{\omega_0^2 L}, \tag{11}$$

which can be simplified as

$$K_0(2^n - 1) = 4C_L/(W_T C_{Pr}) - 1. \tag{12}$$

For an ICDPA, at frequency $\omega_0$, the value of $L$ for the parallel output tank is chosen such that it maximizes the tank $Q$ while providing a reasonable transformer efficiency [27]. This fixes the value of $C_L$. Since $C_L/C_{Pr}$ is fixed by the technology and layout techniques, the product $K_0(2^n - 1)$ is fixed for a value of $W_T$. For an $n$ value, $K_0$ can be determined by the maximum efficiency or symbol rate (as in Section V), and, therefore, $W_T$ and hence $W_{PA}$ can be determined.

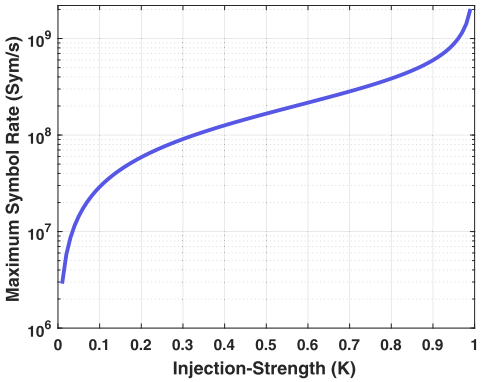



**FIGURE 10.** Maximum symbol rate as a function of $K$ for $\alpha = 0.125$.

## V. DESIGN CONSIDERATIONS FOR AN ILPA

### A. MAXIMUM SYMBOL RATE CONSIDERATION

In Fig. 3(c), the PO, comprised of $M_5$, $M_6$ and $M_T$, is injection locked by the ICDPA transistors $M_1 - M_4$. The capacitance for tuning out the transformer load network is contributed by parasitic drain capacitances of transistors $M_3$-$M_4$-$M_5$-$M_6$ and the MIM capacitor (Fig. 3(c)). The parasitic drain capacitance is dependent on the amplitude codeword and reduces with power back-off. Thus, the PO shifts to a higher self-resonance frequency with a decrease in the amplitude codeword. For the correct operation, the PO should be always locked with the frequency and phase of the incoming PM signal. The maximum locking time of the PO should be smaller than the symbol period (or the data rate) to reduce phase errors in the output EVM. Higher injection strengths reduce the locking time and therefore allow a higher symbol rate. In this scenario, the highest symbol rate which can be supported is now investigated.

The minimum locking time, $T_L$, is inversely proportional to the locking range $\omega_L$ and is given as $T_L = 4/\omega_L$ [23]. To meet the EVM requirements, the frequency and phase of an ILPA should settle within a fraction of the symbol time-period. If $S$ is the symbol rate, then the constraint for settling of the oscillator phase within a fraction, $\alpha$, of the symbol time-period is given as

$$S \leq \left(\frac{\alpha}{4}\right)\left(\frac{\omega_0}{Q}\right)\frac{K}{\sqrt{1 - K^2}}. \tag{13}$$

This implies that a minimum $K$ value is required to support the desired symbol rate for a given EVM. If $\alpha$ is assumed to be 0.125 for the injection-locked PO output to settle within 1/8 of the symbol period, the maximum symbol rate which can be supported by the PO is plotted with the injection-strength in Fig. 10. For a 50 MSym/s data rate and $Q = 1.7$, the required $K$ is 0.17. $K$ is obtained by the ratio of the widths of $M_1$, $M_2$ to half the width of $M_T$. The worst-case scenario occurs for the weakest injection locking when the desired symbol rate is to be maintained for $K_0$, i.e., when the LSB of ICDPA locks the full width of the PO. The maximum symbol

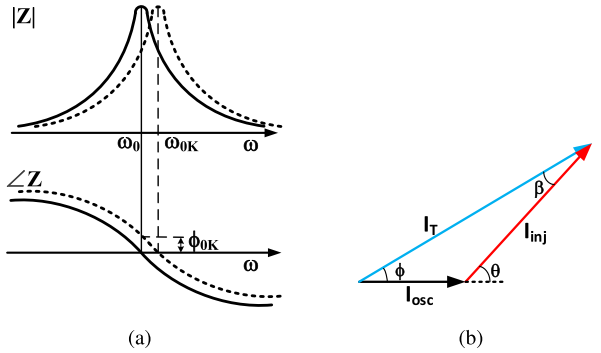



**FIGURE 11.** (a) Change in centre frequency of an ILPA with changing K values. (b) Vector diagram for $K > 1$ case.

rate $S = S_0$ supported by $K_0$, from (10) and (13), is given by

$$S_0 = \left(\frac{1}{32}\right)\left(\frac{\omega_0}{Q}\right)\frac{2(W_{PA}/W_T)}{\sqrt{(2^n-1)^2 - 4(W_{PA}/W_T)^2}}. \quad (14)$$

$K$ values larger than $K_0$ are not a concern for minimum symbol rate requirement as higher $K$s have even shorter locking time and consequently support symbol rate $S > S_0$. From (14), it can be seen that for a given tank bandwidth, the maximum symbol rate for an ILPA having an $n$ bit ICDPA depends only on $K_0$ in (10) or the ratio $W_{PA}/W_T$. Once $W_T$ is chosen, a minimum $W_{PA}$ can be found to support $S_0$. It is to be noted that this $W_{PA}$ or $K_0$ calculation is for supporting a symbol rate, $S_0$, and is different than the $W_{PA}$ or $K_0$ required for maximum $\eta_D$ consideration.

### B. AM-PM DISTORTION

The ILPA tank is tuned at $\omega_0$ for the maximum output power which is achieved at a maximum $K$ value. As $K$ is reduced by switching-off slices of the PA for the power back-off, the capacitance contribution of the PA transistors towards the tank capacitance decreases. This causes the tank to shift to a higher frequency, $\omega_{0K}$, for a $K$ value. This tank looks inductive and provides a phase of $\phi_{0K}$ at the injected frequency, $\omega_0$, as depicted in Fig. 11(a). When this tank is locked at $\omega_0$, a phase difference of $\theta_{0K}$ occurs between the injected current and the oscillator current. This phase difference is contributed by $\phi_{0K}$ and $\beta_{0K}$ as shown in Fig. 11(a) and Fig. 11(b), and is given as

$$\theta_{0K} = \phi_{0K} + \beta_{0K}. \quad (15)$$

From Fig. 11(b), $\beta_{0K}$ and $\phi_{0K}$ are related a

$$\frac{I_{osc}}{\sin(\beta_{0K})} = \frac{KI_{osc}}{\sin(\phi_{0K})}, \quad (16)$$

which can be simplified to

$$\sin(\beta_{0K}) = \frac{\sin(\phi_{0K})}{K}, \quad (17)$$

which implies that $\beta_{0K}$ increases with $\phi_{0K}$ and reduces with $K$. As $K$ reduces for power back-off, the tank shifts to a higher $\omega_{0K}$ which increases both $\phi_{0K}$ and $\beta_{0K}$ leading to a larger $\theta_{0K}$. This change in $\theta_{0K}$ with $K$ leads to AM-PM distortion in the ILPA.

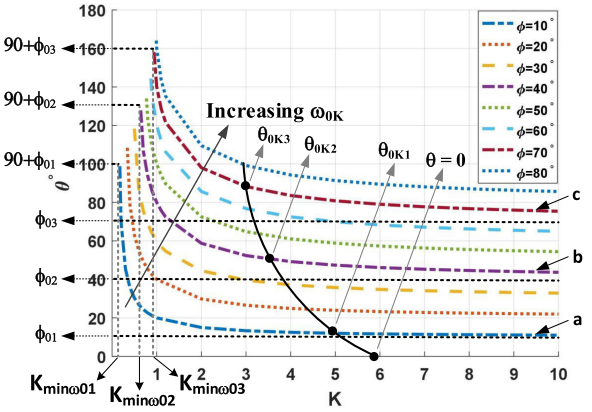



**FIGURE 12.** Calculated $\theta$-$K$ plots for injection-locked LC tanks with different $\phi_{0K}$s.

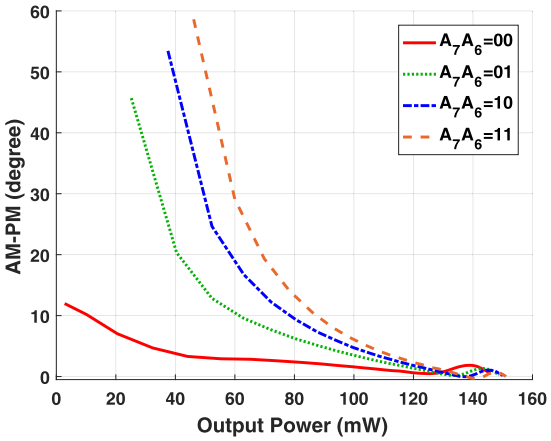



**FIGURE 13.** Simulated AM-PM distortion in the ILPA for different PO AM bits $A_7A_6$.

It should be noted that $\phi_{0K}$ also appears as AM-PM distortion in an ICDPA and, therefore, only $\beta_{0K}$ is the excess contribution to AM-PM distortion from the IL phenomenon in an ILPA. Consequently, an ILPA shows worse AM-PM distortion than an ICDPA. Differentiating (17) and rearranging, it can be seen that

$$\frac{d\beta_{0K}}{dK} = -\frac{\sin\phi_{0K}}{\cos\beta_{0K}K^2} = -\frac{\sin\phi_{0K}}{K^2\sqrt{1-(\frac{\sin\phi_{0K}}{K})^2}} \quad (18)$$

which suggests that the rate of change of $\beta_{0K}$ with $K$ becomes small for higher $K$ values. Therefore, AM employing higher $K$ values alleviates the AM-PM distortion in an ILPA by reducing the change in excess distortion component $\beta_{0K}$.

To elucidate further, Fig. 12 shows the calculated $\theta$-$K$ plots for the LC tanks with center frequencies of $\omega_{0K}$s which are injection locked at $\omega_0$. In a $\theta$-$K$ curve, $\theta$ is the AM-PM distortion for a $K$ value. Three $\theta$-$K$ curves (a), (b) and (c) have been chosen and depicted in the figure for further explanation.

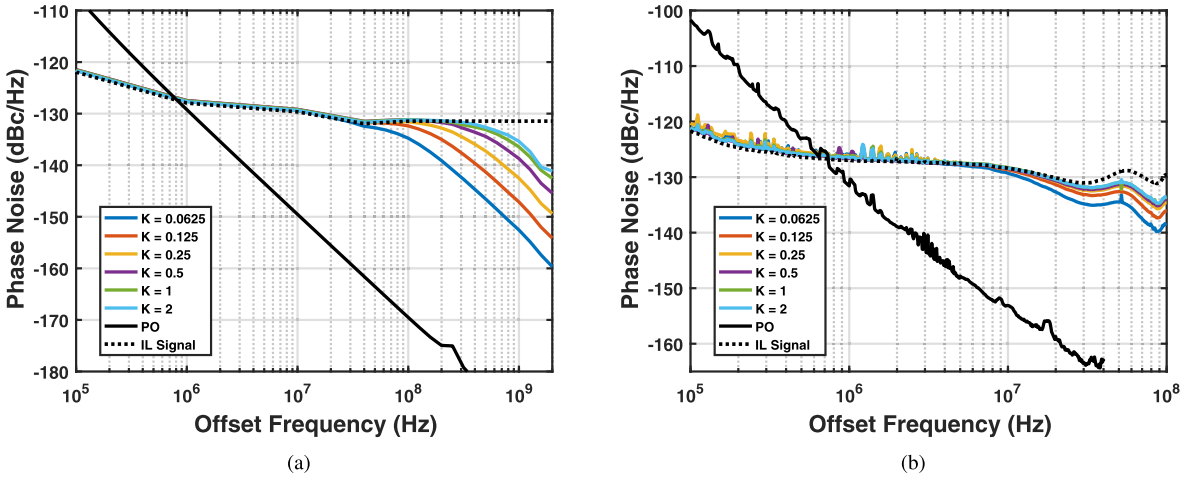



**FIGURE 14.** (a) Simulated and (b) measured PN of the PO and the ILPA for different K values.

Each of the curves in Fig. 12 is a $\theta$-$K$ plot for a certain $\omega_{0K}$ and phase $\phi_{0K}$. For a constant $\phi_{0K}$, a decrease in $K$ results in an increase in $\beta_{0K}$ and, therefore, an increase in $\theta_{0K}$. A minimum $K$ value of $K_{min\omega_{0K}} = \sin\phi_{0K}$ is required to lock the tank, therefore, the $\theta$-$K$ curve starts from $K = K_{min\omega_{0K}}$. Also, the range of $\theta_{0K}$ is confined between $\phi_{0K}$ and $90° + \phi_{0K}$. The value $\theta_{0K} = \phi_{0K}$ is theoretically achieved at an infinite $K$, while $\theta_{0K} = 90° + \phi_{0K}$ is achieved at $K_{min\omega_{0K}}$, i.e., at the edge of the lock-range.

Two observations can be made from these $\theta$-$K$ plots: (1) a larger $K_{min\omega_{0K}}$ value is required to lock a tank having $\omega_{0K}$ further away from $\omega_0$ causing a rightward shift of the start of $\theta$-$K$ curves for a higher $\omega_{0K}$. (2) $\theta$-$K$ curves for a higher $\omega_{0K}$ shift upwards on the $\theta$-axis. In the case where the injected signal frequency is same as the tank center frequency, the $\theta$-$K$ curve lies flat having $\theta = 0$ for all $K$.

The $\theta$-$K$ curve for an ILPA is shown with a black curved line. In the ILPA, $\omega_{0K}$ and $\phi_{0K}$ changes continuously with the reduction in $K$ value. The $\theta$ for an ILPA move upwards and leftwards along the family of $\theta$-$K$ curves with decreasing $K$ to trace the AM-PM distortion trajectory.

The simulated AM-PM distortion of the ILPA is shown in Fig. 13 when the bits $A_0 - A_5$ are varied for power back-off for the $A_7A_6$ bit values of 00, 01, 10 and 11. It can be observed that the AM-PM distortion for the ILPA is minimum when the PO is turned off ($A_7A_6 = 00$), and maximum at the highest PO width ($A_7A_6 = 11$). This agrees with the above AM-PM analysis on degraded AM-PM distortion of ILPA as compared with ICDPA.

### C. PHASE NOISE PERFORMANCE

The EVM of a PA output signal determines the modulated signal quality of a TX. Usually PAs are driven by the signal from a clean LO, and TX PN, therefore, is not an issue. However, when an ILPA is implemented, it incorporates a PO. Prior-art ILPAs [10]–[19] predominantly worked as ILPOs, a topology in which the overall PN behavior of the ILPA is more impacted by the PO, but a PN analysis was never presented.

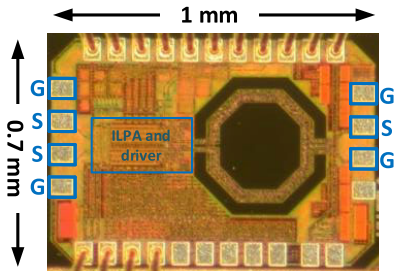



**FIGURE 15.** Chip micrograph of the ILPA.

In an FDD system, with the TX transmitting at maximum power, the noise of the TX at the RX frequency can leak through the diplexer into the RX. Thus it is beneficial to reduce the out-of-band noise of the TX. An ILPA topology further helps to reduce this noise, as is shown next. Without the injection locking, a PO having a low loaded $Q$ suffers from a poor close-in phase noise. With the IL frequency and the center frequency of the PO aligned, the PN of the ILPA follows the PN of the clean injection locking signal up to the lock-range from the center frequency [3], [9].

Fig. 14(a) shows the simulated PO and ILPA phase noise for different $K$ values. The reference injected signal PN and the unlocked PO PN are shown in dotted and solid black lines, respectively. At the minimum $K = 0.0625$, the lock-range is minimum and is 46 MHz from (6). It can be seen that the simulated ILPA PN follows the reference IL signal PN until around 40 MHz, after which it starts to approach the PO PN profile. As lock-range increases for larger $K$ values, the ILPA PN profile follows the reference IL till larger bandwidths before departing towards PO PN. The measured PO and ILPA PN for different $K$ values are shown in Fig. 14(b). At the minimum value of $K = 0.0625$, the measured lock-range is around 10 MHz, which is slightly smaller than the simulated value. This difference is mostly attributed to the practical issue of

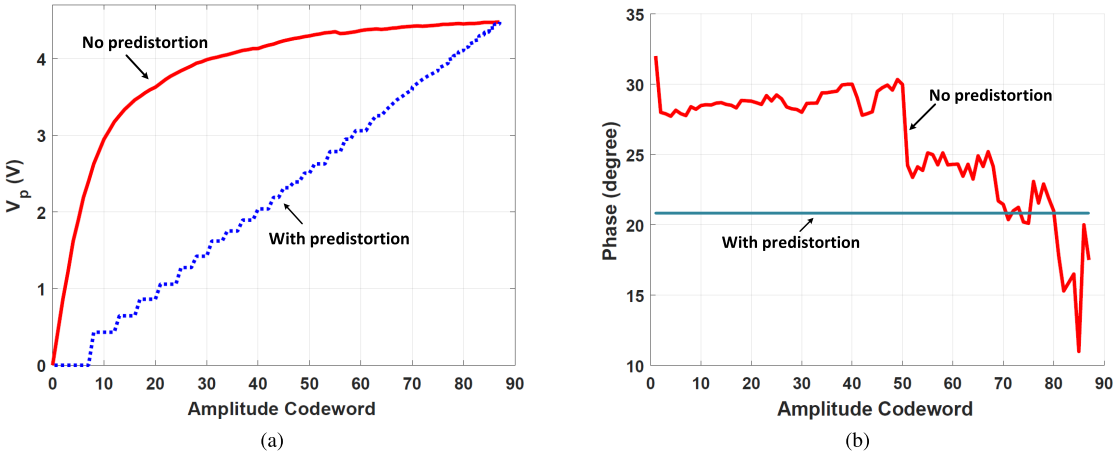



**FIGURE 16.** Measured (a) AM-AM and (b) AM-PM distortion with the amplitude codeword.

drift in the unlocked PO self-resonance frequency in measurements. For higher $K$ values, the measured ILPA PN profile follows the reference IL signal for larger offset frequency, which agrees well with the simulation results in Fig. 14(a) and the theory [3]. PN measurements are performed using BNC 7000 series signal source analyzer (SSA). Measurements are done for the maximum offset frequency supported by the BNC SSA which is 40 MHz for the high drift PN mode (for PO measurements) and 100 MHz for the regular PN mode (for ILPA measurements). Simulations are shown till higher offset frequencies to show the PN improvement more clearly.

An interesting observation is that the lock-range of the ILPA is larger than the PN cross-over frequency of PO and ILPA signals (800 kHz offset frequency, in measured and simulated results) due to low tank $Q$. Therefore, the PN of the ILPA follows the IL signal PN even after the cross-over frequency until the lock-range where it diverges towards the PO PN. The divergence increases for a lower $K$ value. Thus, PN is improved for higher offset frequencies in the ILPA because of the PO.

## VI. MEASUREMENT RESULTS

The proposed ILPA is implemented in 65 nm CMOS process in an area of $1 \times 0.7\ mm^2$, with the chip micrograph shown in Fig. 15. Separate power supplies are used for PA core and input driver buffer. The chip is mounted on FR4 board, and the supply and ground reach the chip through bondwires. Two bond-wires provide the power supply and eight bond-wires are used for ground connections. A single-ended PM signal from an Agilent N5182B vector signal generator (VSG) is converted into a differential input signal through an off-chip balun. Differential inputs are provided through GSSG probe and the single-ended output is taken using a GSG probe. AM bits are provided from an Agilent 81200 data generator.

The measured AM-AM and AM-PM distortion before and after the predistortion are shown in the Fig. 16(a) and 16(b), respectively. It can be seen that AM-PM distortion is code dependent and a maximum phase change of 22° occurs among the codes for realizing 64-QAM. Static digital predistortion is used to correct for the amplitude and phase non-linearities. A digital predistortor is built using two lookup tables (LUTs), one each for the amplitude and the phase [27]-[30]. The inverse of the amplitude curve is used to map AM codeword to a new codeword for the AM-AM LUT to correct for amplitude non-linearity. Similarly, the phase non-linearity corresponding to AM codeword is populated in AM-PM LUT and then subtracted from the PM signal to obtain the predistorted PM signal. The predistorted AM and PM signals are then loaded into digital pattern generator and VSG, respectively, for dynamic measurements. It can be noted that while the RFDAC quantization error limits the accuracy for the pre-distorted AM signal, the PM signal compensated for the AM-PM predistortion was directly loaded into the vector signal generator and, therefore, the phase error is only limited by the instrument's resolution. Thus, the residual AM-PM nonlinearity after the predistortion is negligible [27]. Fig. 17 and 18 shows the measured $\eta_D$ and PAE of the ILPA. The bits $A_5 - A_0$ are used to change ICDPA width, and the bits $A_7A_6$ change the PO tail current in the ILPA as described in Section IV-B. The bits $A_5 - A_0$ are swept for different combinations of bits $A_7A_6$ in the ILPA and then the codes which provide highest $\eta_D$ for a power back-off value are selected for the ILPA operation. Fig. 17 is marked with the PO AM codes, from the AM bit sweeps, which provide the highest drain efficiency across different range of output power. This selection ensures that the highest average drain efficiency is achieved in the modulation measurements. A maximum $\eta_D$ of 42.7% and maximum PAE of 40% is achieved for ILPA at highest $P_{out}$ of 200.5 mW from a 1.45 V PA power supply at 2.5 GHz. The driver operates from 1 V power supply. The PA driver along with supporting digital circuits consumes 38 mW of power. The PA output is attenuated by 6.8 dB due to RF attenuator, cables, connectors, and output probe. For efficiency calculations, the supply and ground have been de-embedded up to the PCB level only and therefore IR drop in the PCB traces and bondwires are

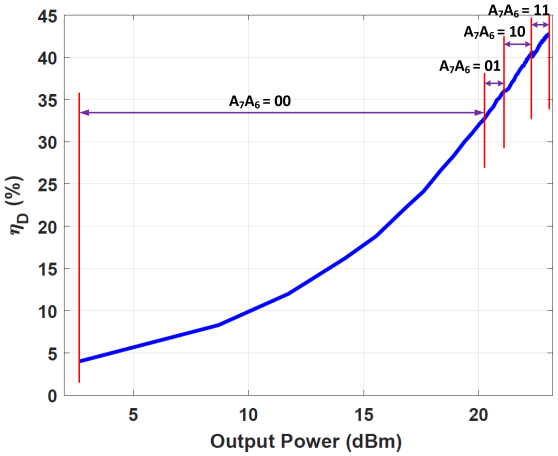



**FIGURE 17.** Measured $\eta_D$ of the ILPA.

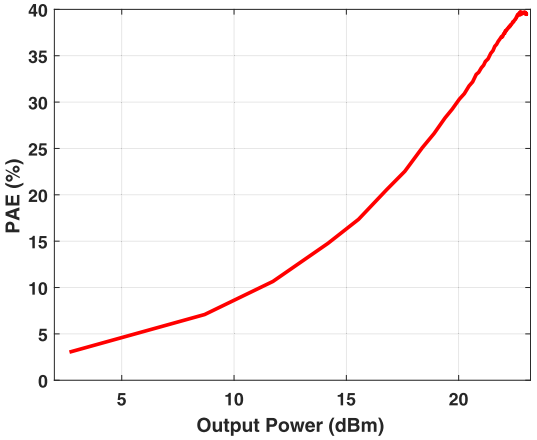



**FIGURE 18.** Measured PAE of the ILPA.

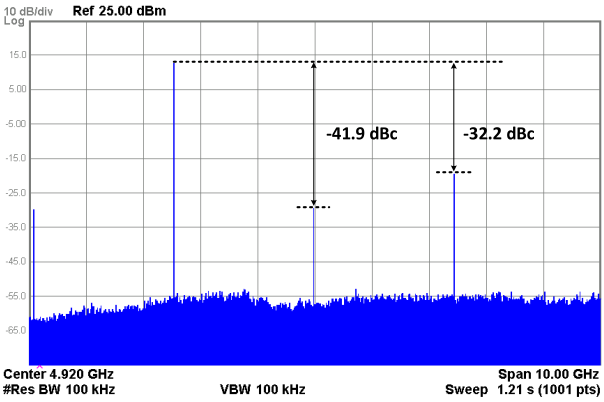



**FIGURE 19.** Measured continuous wave output spectrum when only PO is turned ON.

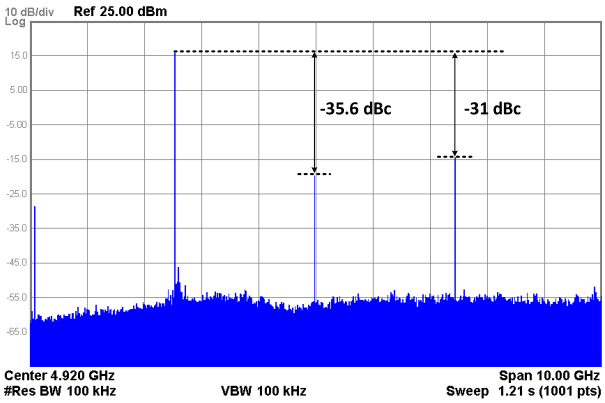
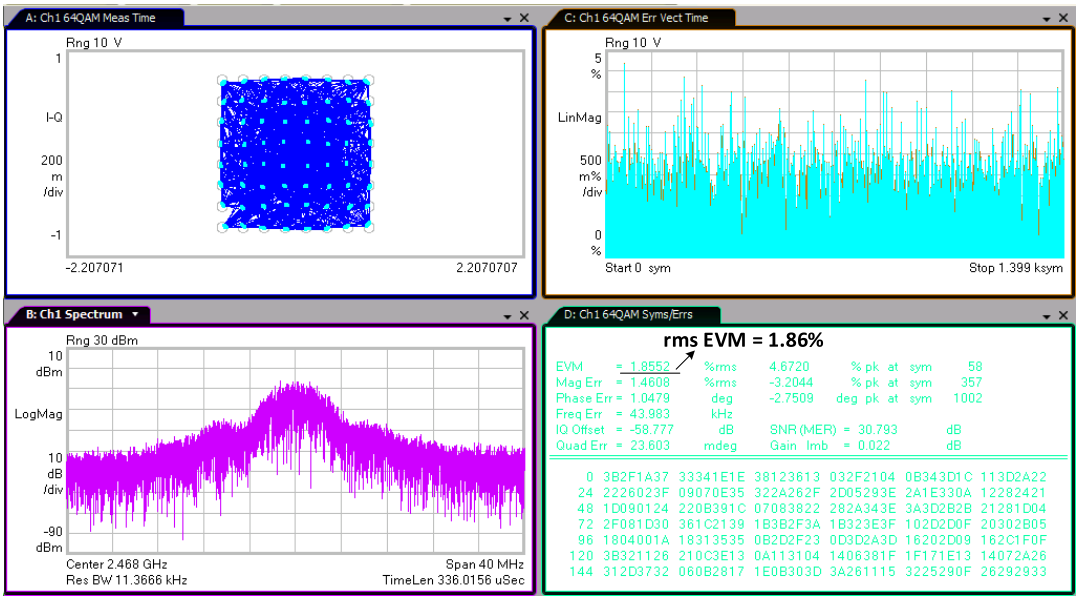



**FIGURE 20.** Measured continuous wave output spectrum when both the PO and the ICDPA are turned ON.

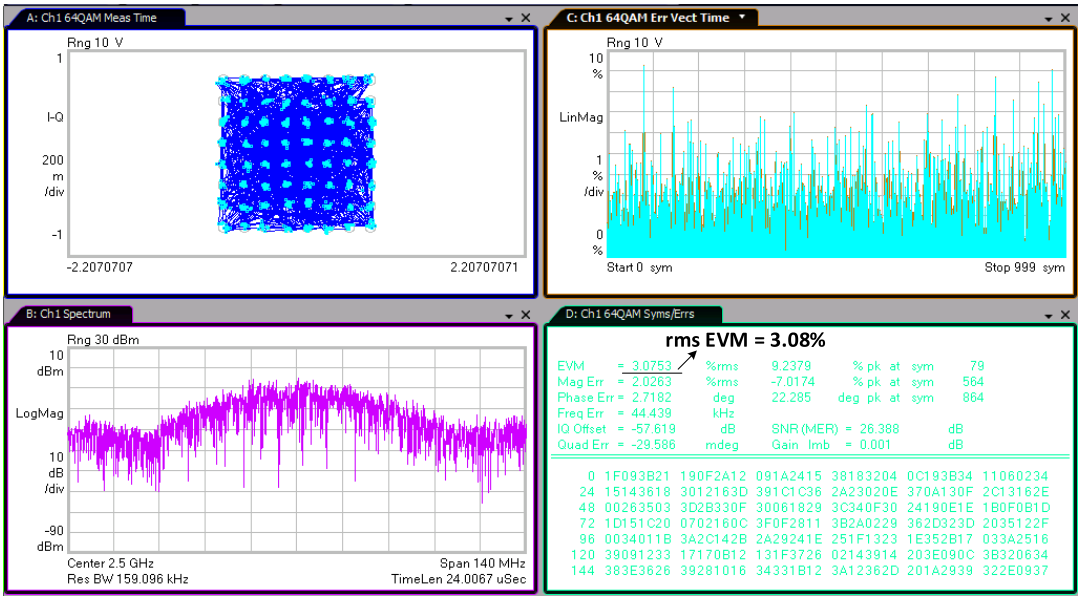
not taken in account. Performance comparison of the ILPA with other digital PAs and ILPAs is shown in Table 1. The ILPAs, [21], [22], use an off-chip matching network and an off-chip supply modulator (SM).

The measured continuous wave output when only PO is turned ON in the ILPA is shown in Fig. 19 and when both the PO and the ICDPA in the ILPA are turned ON, is shown in Fig. 20. The measured self-oscillation frequency of the PO is 2.45 GHz and the $P_{out}$ is 19.6 dBm at 1.45 V. The peak $P_{out}$ increases by 3.4 dB when ICDPA is also turned ON in the ILPA as shown in Fig. 20. This follows the design insights of Fig. 4 for the peak $P_{out}$ of the PO to be less than half of the peak $P_{out}$ of the ILPA for improving $\eta_D$. The measured second and third harmonic rejections at peak $P_{out}$ of the ILPA are $-35.6$ dBc and $-31$ dBc, respectively, without additional filtering.

The dynamic performance of the ILPA is characterized by modulation tests with 64-QAM signals at 1/5/10/20/50 MSym/s. The peak-to-average power ratio of the modulation signals is 4.9 dB. A measurement set-up similar to [30] is used. An upper limit of 50 MSym/s is due to the maximum modulation bandwidth limitation for the VSG (50 MHz). An Agilent EXA N9010A Vector Signal Analyzer (VSA) is used to demodulate the signal. The constellation diagrams at 5 MSym/s and 50 MSym/s for 64-QAM measurements for the ILPA are shown in Fig. 21(a) and Fig. 21(b), respectively. The EVM values at 5/50 MSym/s for ILPA are 1.9%/3.1% RMS. The required delay resolution was estimated to be better than 400 ps for the 50 MSym/s 64-QAM signals used in this work. This is determined as follows: In [32], from simulations, the AM-PM time mismatch $<$ 1 ns was required for achieving better than $-35$ dB EVM for 20 MHz WLAN OFDM signals. The EVM degradation was shown to follow the degradation of the inter-modulation distortion product (IMD) given as IMD $= 2\pi(B_{RF}\Delta\tau)^2$ [33], [34]. $B_{RF}$ is 2-tone frequency spacing, and $\Delta\tau$ is the delay between the AM and PM paths. Therefore, a 2.5$\times$ increase in data rate for this work requires better than 1/2.5 $=$ 0.4 ns time-mismatch. To achieve this, a programmable delay line Model PDL-10A, Colby Instruments Inc., was used in the PM signal path, and the delay was swept in 100 ps step till the minimum EVM was achieved. The measured adjacent channel leakage ratio (ACLR) with 50 MSym/s 64-QAM signals is 16.71 dBc at the lower side,




(a)




(b)

**FIGURE 21.** 64-QAM measurement results for (a) 5 MSym/s and (b) 50 MSym/s.

and 14.03 dBc at the higher side is shown in Fig. 22. No oversampling has been used in the measurements. Oversampled baseband signals can be used to further improve the spectrum leakage and ACLR.

The maximum voltage swing at the source of $M_3$ is 2 V, which is limited by the $V_{th}$ of the cascode transistors. For $V_{g,cascode} = 2.5$ V, the maximum source swing $V_{s,cascode} = V_g - V_{th} = 2.5$ - $0.55 = 1.95$ V. This follows the condition for the transistors $M_1/M_2$ to work reliably as $|V_{ds}|$ (or $|V_{dg}|$) $< 2\cdot$VDD [35]. The maximum drain voltage swing of 2.5 V thick-oxide cascode transistors is $\pi\cdot$VDD from the ICDPA theory [27]. To operate reliably, the $V_{d,cascode}$ swing should remain below $V_{g,cascode} - V_{th} + 2 \cdot \text{VDD} = 7$ V. Therefore, the PA supply should not exceed $7/\pi$ V $= 2.2$ V. The 1.45 V PA supply used for this ILPA meets this condition. As a measure of reliability, the ILPA was left operating with a 2.5 GHz continuous wave input at 1.45 V power supply at its peak output power ($A_7 - A_0 = 11111111$)

**TABLE 1. Performance comparison with digital and injection locking PAs.**

| | This work | [27] | [28] | [29] | [30] | [31] | [12] | [21] | [22] |
|---|---|---|---|---|---|---|---|---|---|
| Freq. (GHz) | 2.5 | 2.25 | 2.4 | 2.6/4.5 | 2.25 | 2 | 2.35 | 1.95 | 0.6-6 |
| VDD (V) | 1.45 | 1 | 2.8/1.55 | 3 | 1.5/3 | 1.2/2.4 | 1 | 3 | 3 |
| Peak $P_{out}$ (dBm) | 23 | 21.8 | 24.6 | 28.1/26 | 25.2 | 20.5 | 9.5 | 28.7 | 27.9 (at 0.75 GHz) |
| Peak PAE (%) | 40 | 41 | – | 35/21.2 | 45 | 20 | 43 | 68 (at 3 dB back-off) | 59.6 (at 1 GHz) |
| $\eta_D$ (%) | 42.7 | 44 | 45.6 | 40.7/27 | – | – | 48.5 | – | – |
| CMOS Tech. (nm) | 65 | 65 | 65 | 65 | 90 | 65 | 180 | 65 | 65 |
| Modulation | 64-QAM (50 MSym) | 64-QAM (20 MHz OFDM WLAN) | 64-QAM (20 MSym) | 256-QAM (8 MSym) | 64-QAM (20 MHz OFDM) | 64-QAM (10 MHz LTE) | CW signal | 16-QAM (20 MHz LTE) | 16-QAM (20 MHz LTE) |
| EVM (dB) | -30.2 | -28 | -25.6 | -36.3/-34.6 | -31.8 | -28.9 | – | -26.6 | -26.1 |
| Av. $P_{out}$ (dBm) | 18.1 | 14 | 17.6 | 20.37/18.53 | 17.7 | 14.5 | – | 20.3 | 18.9 |
| Av. $\eta_D$ (%) | 27.9 | 18 | 27.5 | 16.26/13.42 | – | – | – | – | – |
| Av. PAE (%) | 25.8 | – | – | – | 27 | 12.2 | – | 44.1 (w/o SM) | 27.9 |
| Matching Network | On-chip | On-chip | On-chip | On-chip | On-chip | On-chip | On-chip | Off-chip | Off-chip |
| PA Architecture | Digital | Digital | Digital | Digital | Digital | Digital | class-E | Linear + SM | Linear + SM |
| IL employed | Yes | No | No | No | No | No | Yes | Yes | Yes |

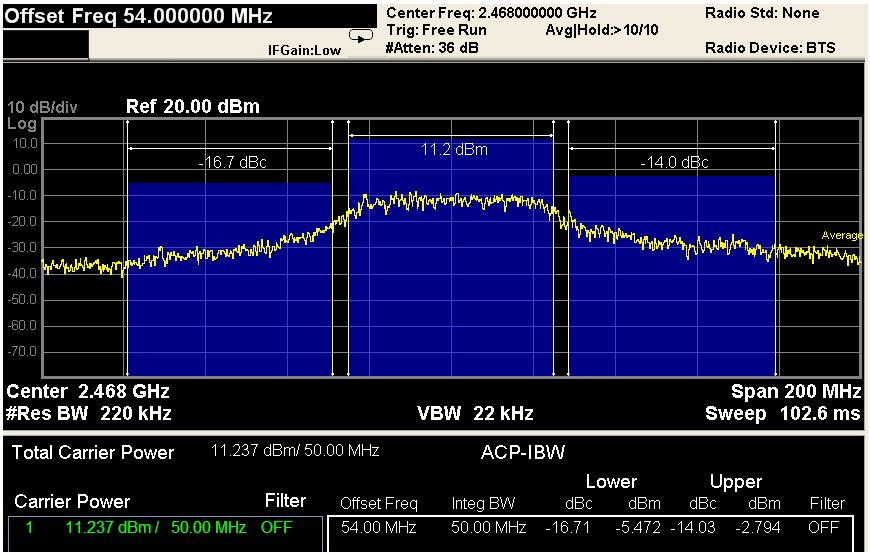



**FIGURE 22. ACLR measurement for 64-QAM, 50 MSym/s modulation.**

for 24 hours and no significant drop in the output power was noticed.

## VII. CONCLUSION

In summary, this work contributes to the following: (1) drain efficiency improvement is shown in an ILPA along with the PAE improvement, (2) high strength injection locking theory for the PA is derived, (3) excess AM-PM distortion component in an ILPA arising from the injection locking mechanism has been observed and analyzed, (4) the role of PO in out-of-band phase noise improvement in an ILPA is analyzed, and (5) design methodology and design equations are provided for the proposed ILPA to achieve the desired symbol rate and higher drain efficiency.

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