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A Three-Phase Constant Common-Mode Voltage Inverter With Triple Voltage Boost for Transformerless Photovoltaic System

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ABSTRACT This paper introduces a new three-phase two-level inverter based on the switched-capacitor voltage multiplier. By adding a voltage multiplier network at the DC side of the traditional three-phase inverter topology, the DC-link voltage of the introduced inverter is stepped up to triple of the input voltage. Compared to the existing solutions, the common-mode voltage of the introduced topology is kept constant. Moreover, the voltage stress across additional semiconductor components is the same as one-third of DC-link voltage. Operating principles, mathematical analysis, circuit analysis, and pulse-width modulation (PWM) method based on the Boolean logic function for introduced inverter are presented. A comparison of the introduced inverter with other inverter topologies is also reported. The simulation results are shown to verify the introduced three-phase triple voltage boost inverter. Besides that, a laboratory-built prototype is developed based on a DSP F280049C microcontroller and the corresponding experimental tests are provided to prove the introduced inverter.

INDEX TERMS Three-phase inverter, transformerless PV system, common-mode voltage, leakage current, switched-capacitor network.

I. INTRODUCTION

In the recent period, transformerless grid-connected photovoltaic (PV) inverters have been receiving more and more attention from many researchers due to their inherent benefits of small size and volume, less complexity, high efficiency, low cost, and easy to install [1], [2]. Nevertheless, the removal of the transformer makes the PV array and the power grid has a direct electrical connection. This raises the leakage current in the PV system if the voltage across on the parasitic capacitance between the ground and PV array varies with high frequency. This leakage current flows between

the ground and PV array through the parasitic capacitor, which causes a variety of unwanted problems such as serious electromagnetic interference (EMI) and insecurity, higher losses, higher current harmonics, and the low reliability of the transformerless grid-connected PV inverter systems [3]–[5]. Because of these, the leakage current flow in the grid-connected PV systems must be less than the VDE standard of 300 mA [6] to avoid the unfavorable effects. The leakage current can be limited by restricting amplitude and frequency of the common-mode voltage (CMV) or floating PV array from the grid on DC side of the inverter during certain time intervals. In order to eliminate leakage current, numerous interesting approaches have been reported in the prior works. In general, these approaches can be labeled into two types,

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namely the modulation-based approaches and the hardware-based approaches. Recently, many CMV modulation-based methods have been discussed in the literature. To limit the amplitude of CMV, the near-state PWM (NSPWM) [7], [8], remote-state PWM (RSPWM) [9], [10] and active zero-state PWM (AZSPWM) methods [11]–[13] presented that only active vectors are considered to generate the desired voltage vector. In NSPWM and AZSPWM methods, the amplitude of CMV is restricted within 33% of the DC-link voltage. With the RSPWM method, CMV can be kept constant. Nevertheless, the RSPWM methods only perform linearly with low modulation index while NSPWM methods only perform linearly with high modulation index. Besides that, NSPWM methods, RSPWM methods, and AZSPWM methods produce bipolar output line to line voltage. Bipolar nature of the output line-to-line voltage rises the losses and voltage stress on filter inductor. In [14], the carrier phase-shift PWM based reverse injection scheme was presented to restrict the amplitude of CMV. In this scheme, low-frequency harmonics in the CMV was significantly reduced. However, the amplitude of CMV was only restricted within 33% of DC-link voltage with a low modulation index. The interleaved carrier technique was discussed in [15] to reduce the RMS value of the CMV by minimizing the appearance of the zero vectors. However, the amplitude of CMV was equal to DC-link voltage. In [16], a virtual space vector modulation method was introduced to limit the third-order harmonics in the CMV. This method only operated linearly with low modulation index. The model predictive control (MPC) based CMV reduction strategies were discussed in [17] and [18] to control the output currents with the fast transient response as well as limit the amplitude of CMV. The amplitude of CMV is restricted within 33% of DC-link voltage.

To overcome the drawbacks associated with the above modulation-based methods, the hardware-based methods have been discussed for the CMV reduction. A hybrid filter which includes an active common-mode filter and a passive filter has been introduced in [19] in order to reduce variations of the CMV. Although this filter technique is effective in restricting variations of the CMV, it has drawbacks of being bulky or complex. Instead of using conventional two-level voltage source inverter (VSI) topology, various inverter topologies and corresponding modulation strategies were introduced in [20]–[25]. A four-leg inverter topology, which adds two-switch paralleled to two-level three-phase voltage source inverter, has been presented in [20] to achieve the constant CMV. However, this topology requires additional weight and volume due to using an additional LC circuit. Besides, the output of this topology is bipolar as well as the modulation index is also limited. Another good solution was introduced in [21]. By combining a voltage-clamping network and two-level three-phase voltage source inverter, CMV of the voltage-clamping inverter topology is bounded in the range from one-third to two-thirds of DC-link voltage. In [22], the embedded-switch inverter (ESI) topology and corresponding modulation scheme were introduced to limit

the high-frequency leakage current by adding six switches and two capacitors into two-level three-phase voltage source inverter. As a result, the CMV is kept as one half of DC-link voltage all the time. An improved circuit topology with eight switches has been introduced in [23]. By controlling two extra switches to disconnect the input DC source from the inverter during zero states, the variation of CMV is restricted within one-third of DC-link voltage. In the improved H8 topology [24], CMV during zero states is clamped to two-fifths of DC-link voltage by controlling two extra switches. As a result, the variation of CMV is also restricted within one-third of DC-link voltage. Xiaoqiang Guo *et al.* [25] presented zero-voltage-state rectifier (ZVR) topology to restrict the high-frequency leakage current. The CMV of the ZVR topology is maintained as half of the DC-link voltage all the time. Due to voltage-boosting capability, the switched-capacitor topologies [26]–[28] have been gaining increasing attention these days. As presented in [26], a switched-capacitor network that consists of seven semiconductors and three capacitors is inserted into between three-phase Neutral-Point-Clamped multilevel inverter and input voltage source. As a result, the DC-link voltage is triple of the input voltage. In [26], the input current of the inverter circulates through four semiconductors on each operating stage, which results in high conduction power loss in the switched-capacitor network. Sze Sing Lee *et al.* [27] presented a single-phase switched-capacitor-based multilevel inverter which combines a T-type inverter and a switched-capacitor network. In [27], the neutral of load (ac output side) and the midpoint of dc-link is connected directly, which results in low leakage current. Unlike [26], to produce a DC link voltage which is triple of input voltage, the switched-capacitor network in [27] requires twelve semiconductors and six capacitors. In [28], SCVD topology, which combines a two-level three-phase voltage source inverter and a voltage-doubler network, has been proposed to reduce CMV. The variation of CMV can be limited within one-sixth of DC-link voltage. However, SCVD topology generates bipolar output line-to-line voltage and the modulation index is also limited.

In light of the above, a new three-phase constant common-mode voltage inverter (CCMVI) with a novel modulation strategy is presented in this paper. The introduced topology is a combination of a voltage multiplier network and a two-level three-phase voltage source inverter. Compared to the topologies and modulations in existing works, CMV of proposed topology can be kept constant. The other remarkable feature of the proposed topology is voltage boost capability. In contrast to [21], the proposed topology uses a voltage multiplier network to restrict the CMV in lieu of a voltage-clamping network. Compared to [28], the DC-link voltage of the proposed CCMVI is 1.5 times more than that of SCVD topology. When compared to the inverter in [26], the switched-capacitor network in the proposed inverter uses one more semiconductor. However, the input current of the proposed inverter only circulates through three semiconductors during even active states. And, this current only circulates

through two semiconductors during zero state. Meanwhile, the input current of the inverter as presented in [26] circulates through four semiconductors on each operating stage. Furthermore, in the introduced topology, the voltage stress across additional semiconductor components is equal to one-third of DC-link voltage instead of half of DC-link voltage as SCVD topology. In contrast to [7]–[13], [20] and [28], the proposed CCMVI produces unipolar output line-to-line voltage. As a result, the stress and losses for filter inductor are significantly reduced. Also, a comparison between the proposed CCMVI and the existing solutions is illustrated. Common-mode leakage current model, operating principle, and the PWM control technique applied to the proposed topology are reported in section II. A comparison of the proposed inverter with the other inverters in terms of the component count, voltage linearity, and voltage gain, etc. is shown in section III. Section IV provides simulation results. Finally, the experimental results are given in section V.

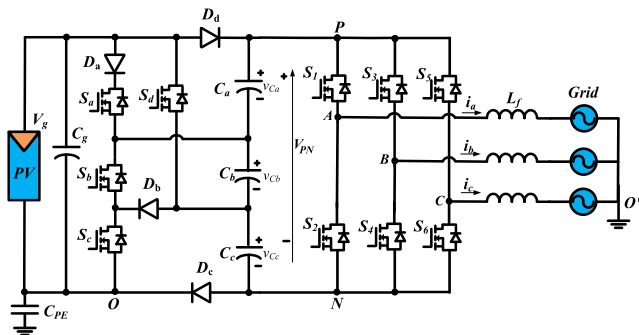


FIGURE 1. Equivalent circuit of proposed CCMVI topology.

II. PROPOSED THREE-PHASE CCMVI TOPOLOGY

The schematic diagram of the proposed CCMVI topology is depicted in Fig. 1. A switched-capacitor voltage multiplier (SCVM) network that consists of four switches, four diodes, and three capacitors is inserted into between two-level three-phase voltage source inverter and input voltage source. The common-mode loop model of the introduced CCMVI topology is depicted in Fig. 2.

A. COMMON-MODE LEAKAGE CURRENT MODEL

Assuming that the grid is ideal, based on Fig. 1, the following mathematical equations are obtained:

$$\begin{cases} V_{AO'} = V_{AO} - V_{O'O} \\ V_{BO'} = V_{BO} - V_{O'O} \\ V_{CO'} = V_{CO} - V_{O'O} \\ V_{AO'} + V_{BO'} + V_{CO'} = 0. \end{cases} \quad (1)$$

where, $V_{AO'}$, $V_{BO'}$, $V_{CO'}$, and $V_{O'O}$ are phase A, B, C voltages, and voltage between grid neutral and the negative terminal of PV, respectively. V_{AO} , V_{BO} , and V_{CO} are the voltages between the outputs of inverter and the negative terminal of PV.

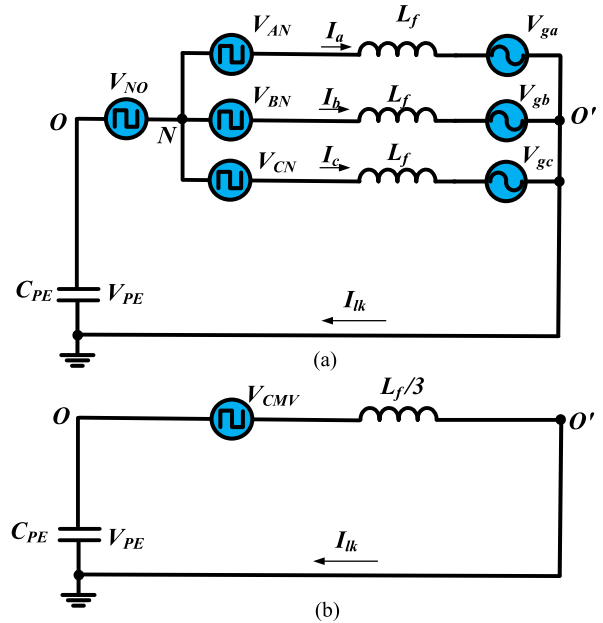


FIGURE 2. Common-mode model of proposed CCMVI. (a) Simplified common-mode model and (b) Final simplified equivalent diagram.

From (1), the CMV of the proposed CCMVI (V_{CMV}) is expressed as

$$V_{CMV} = V_{O'O} = \frac{(V_{AO} + V_{BO} + V_{CO})}{3}. \quad (2)$$

From Fig. 1, the following mathematical equations are obtained:

$$\begin{cases} V_{AO} = V_{AN} + V_{NO} \\ V_{BO} = V_{BN} + V_{NO} \\ V_{CO} = V_{CN} + V_{NO}. \end{cases} \quad (3)$$

Substituting V_{AO} , V_{BO} , and V_{CO} in (3) into (2), the CMV of the proposed CCMVI can be rewritten as follows:

$$V_{CMV} = V_{NO} + \frac{V_{AN} + V_{BN} + V_{CN}}{3} \quad (4)$$

From Fig. 2, the following mathematical equations are obtained:

$$\begin{cases} V_{PE} = V_{AN} + V_{NO} + sI_a L_f + V_{ga} \\ V_{PE} = V_{BN} + V_{NO} + sI_b L_f + V_{gb} \\ V_{PE} = V_{CN} + V_{NO} + sI_c L_f + V_{gc} \\ V_{ga} + V_{gb} + V_{gc} = 0 \\ I_a + I_b + I_c = I_{lk}. \end{cases} \quad (5)$$

The leakage current can be expressed as:

$$i_{lk}(t) = -C_{PE} \frac{dv_{PE}(t)}{dt} \quad (6)$$

where C_{PE} defines parasitic capacitance between the ground and PV array.

From (4)-(6), the voltage across the parasitic capacitor (V_{PE}) is derived by

$$V_{PE}(s) = \frac{1}{1 + s^2 L_f C_{PE}} V_{CMV}(s) \quad (7)$$

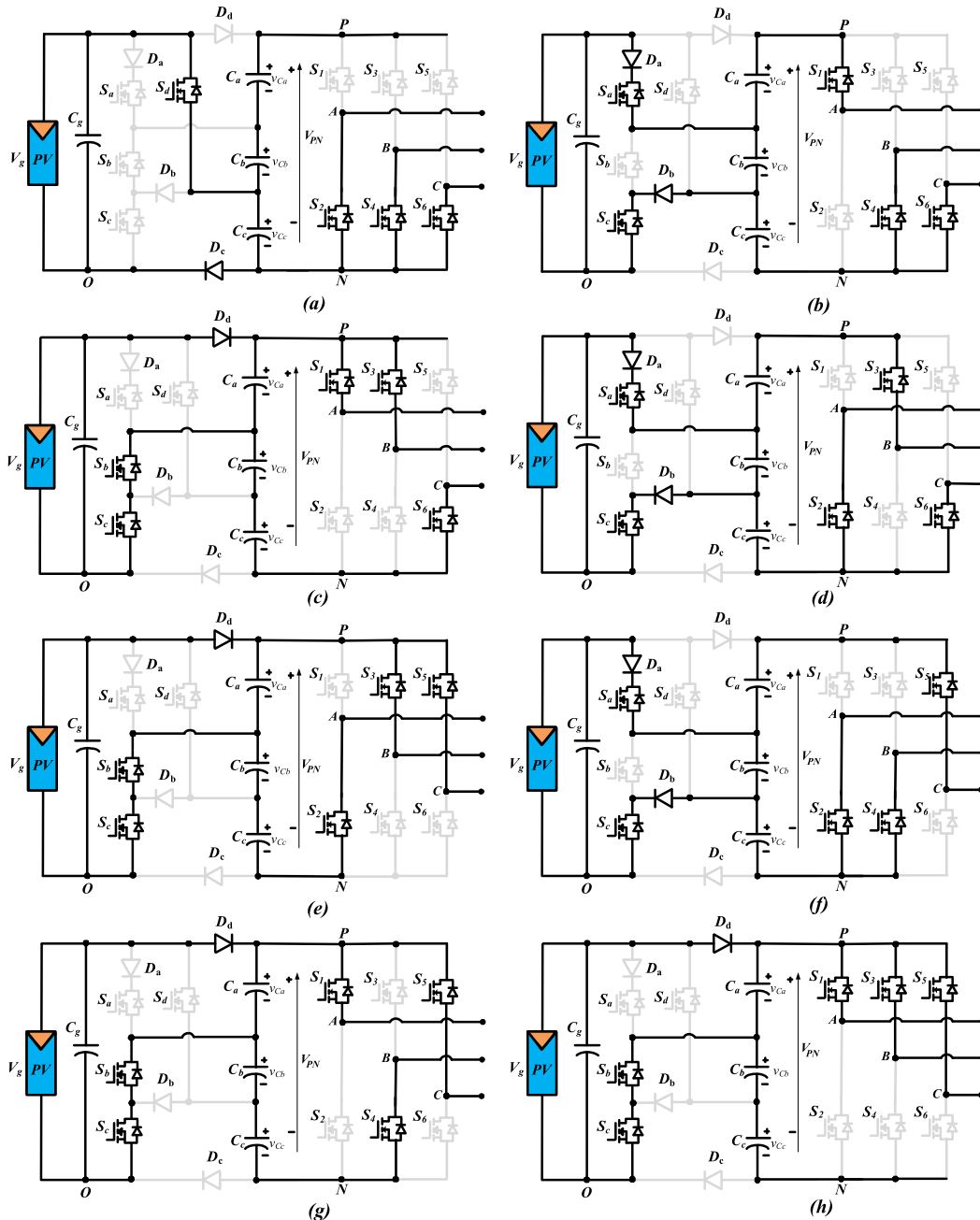


FIGURE 3. Equivalent circuits of the proposed CCMVI. (a) State 0; (b) State 1; (c) State 2; (d) State 3; (e) State 4; (f) State 5; (g) State 6; (h) State 7.

From (6), we can see that the leakage current depends on both the parasitic capacitance C_{PE} and $dV_{PE}(t)/dt$. Therefore, the leakage current can be effectively limited if the voltage across the parasitic capacitor C_{PE} is constant. According to (7), the voltage across the parasitic capacitor C_{PE} is dependent on the CMV.

B. OPERATING PRINCIPLE OF PROPOSED CCMVI

Fig. 3 depicts eight switching states of the proposed CCMVI topology. Table 1 highlights the corresponding CMV and eight switching states of the proposed CCMVI. The operating

principle of the proposed CCMVI topology is explained as follows.

During state 0 [see Fig. 3(a)]: $S_a, S_b,$ and S_c are switched off while S_d is switched on. Therefore, diodes $D_a, D_b,$ and D_d are blocked while diode D_c conducts. Capacitors C_a and C_b are discharged while capacitor C_c is charged. The capacitor C_c voltage is the same as V_g . The CMV of the proposed CCMVI during state 0 is zero.

$$\begin{cases} V_{Cc} = V_g \\ V_{CM} = 0 \\ V_{PN} = V_{Ca} + V_{Cb} + V_{Cc}. \end{cases} \quad (8)$$

TABLE 1. Corresponding CMV and state of semiconductor devices of proposed CCMVI topology under eight switching states.

State	Switch								Diode				V_{CMV}
	S_1	S_3	S_5	S_a	S_b	S_c	S_d	D_a	D_b	D_c	D_d		
State 0	Off	Off	Off	Off	Off	Off	On	Off	Off	On	Off	0	
State 1	On	Off	Off	On	Off	On	Off	On	On	Off	Off	0	
State 2	On	On	Off	Off	On	On	Off	Off	Off	Off	On	0	
State 3	Off	On	Off	On	Off	On	Off	On	On	Off	Off	0	
State 4	Off	On	On	Off	On	On	Off	Off	Off	Off	On	0	
State 5	Off	Off	On	On	Off	On	Off	On	On	Off	Off	0	
State 6	On	Off	On	Off	On	On	Off	Off	Off	Off	On	0	
State 7	On	On	On	Off	On	On	Off	Off	Off	Off	On	$V_{PN}/3$	

During odd active states [see Figs. 3(b), 3(d), and 3(f)]: S_a and S_c are switched on while S_b and S_d are switched off. So, diodes D_a and D_b conduct while diodes D_c and D_d are blocked. Capacitors C_a and C_c are discharged while capacitor C_b is charged. Capacitor C_b voltage is the same as V_g . The corresponding CMV of the proposed CCMVI during this state is zero.

$$\begin{cases} V_{Cb} = V_g \\ V_{CM} = 0 \\ V_{PN} = V_{Ca} + V_{Cb} + V_{Cc}. \end{cases} \quad (9)$$

During even active states [see Figs. 3(c), 3(e), and 3(g)]: S_b and S_c are switched on while S_a and S_d are switched off. So, diodes D_a , D_b and D_c are blocked while diode D_d conducts. Capacitors C_b and C_c are discharged while capacitor C_a is charged. Capacitor C_a voltage is the same as V_g . The corresponding CMV of the proposed CCMVI during this state is zero.

$$\begin{cases} V_{Ca} = V_g \\ V_{CM} = 0 \\ V_{PN} = V_{Ca} + V_{Cb} + V_{Cc}. \end{cases} \quad (10)$$

During state 7 [see Fig. 3 (h)]: like even active states, S_b and S_c are also switched on while S_a and S_d are switched off. So, diodes D_a , D_b , and D_c are blocked while diode D_d conducts. Capacitors C_b and C_c are discharged while the capacitor C_a is charged. Capacitor C_a voltage is the same as V_g . The corresponding CMV of the proposed CCMVI during this state is $V_{PN}/3$.

$$\begin{cases} V_{Ca} = V_g \\ V_{CM} = V_{PN}/3 \\ V_{PN} = V_{Ca} + V_{Cb} + V_{Cc}. \end{cases} \quad (11)$$

From (8)-(11), the voltage gain of the proposed CCMVI topology is defined:

$$B = V_{PN}/V_g = 3. \quad (12)$$

From operating principles of the introduced CCMVI topology, we can see that the CMV is maintained as constant at zero without using state 7. Besides, the DC-link voltage of the introduced CCMVI is triple of that of the VSI for the same input voltage. Based on the above circuit analysis, we can see that the input current of the proposed converter circulates

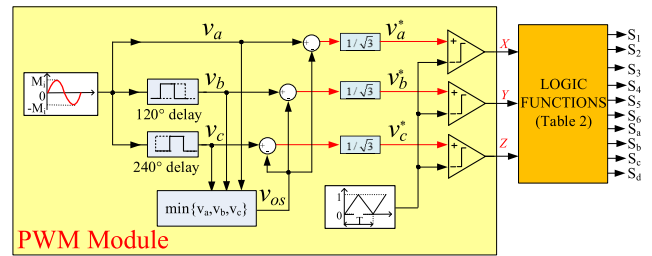


FIGURE 4. Block diagram of proposed control technique for proposed CCMVI.

through three semiconductors during even active states while it circulates through four semiconductors during odd active states. So, conduction loss in the switched-capacitor network is high. As a result, it affects the efficiency of the proposed topology.

C. PWM CONTROL TECHNIQUE FOR PROPOSED CCMVI

In this section, the implementation of the proposed PWM control technique for CCMVI is illustrated. Fig. 4 indicates a block diagram of the PWM generation scheme for all ten switches of the proposed CCMVI topology.

As shown in Fig. 4, we can see that the proposed PWM control technique for CCMVI can be utilized using the scalar approach as follows:

$$\begin{cases} v_a^* = \frac{M_i \sin(\omega t) - v_{os}}{\sqrt{3}} \\ v_b^* = \frac{M_i \sin(\omega t - 2/3\pi) - v_{os}}{\sqrt{3}} \\ v_c^* = \frac{M_i \sin(\omega t + 2/3\pi) - v_{os}}{\sqrt{3}}. \end{cases} \quad (13)$$

where three sinusoidal signals v_a , v_b , and v_c are the original reference signals, M_i is the modulation index, and ω defines the angular frequency of reference signals. v_{os} is the offset signal and is obtained as:

$$v_{os} = \min \{v_a, v_b, v_c\}. \quad (14)$$

Three sinusoidal signals with a phase shift of 120° among them are used to produce three desired three-phase modulation signals (v_a^* , v_b^* , and v_c^*) based on (13). And then, These desired three-phase modulation signals are compared to the high-frequency carrier wave to generate three signals X, Y,

Z. Then, the gating signal can be obtained from three signals X, Y, Z based on the mathematical operations in Table 2.

TABLE 2. Logic functions for the active switches of proposed CCMVI.

$S_1 = X$	$S_2 = \bar{X}$
$S_3 = Y$	$S_4 = \bar{Y}$
$S_5 = Z$	$S_6 = \bar{Z}$
$S_a = \bar{X}(Y \oplus Z) + \bar{Y}(X \oplus Z)$	$S_b = X(Y \oplus Z) + Y(X \oplus Z)$
$S_c = X + Y + Z$	$S_d = \bar{X} + \bar{Y} + \bar{Z}$

Logic functions in the proposed PWM generation scheme are highlighted in Table 2. This guarantees that the CMV of the introduced CCMVI is maintained as constant at zero. Similar to the conventional VSI under discontinuous PWM strategy, the proposed CCMVI topology under the proposed PWM control technique has also the major features such as low switching losses, full modulation range, and low DC-link current ripple. The proposed CCMVI under the proposed PWM control technique has an additional benefit of zero variation in CMV.

III. COMPARISON WITH OTHER THREE-PHASE INVERTER TOPOLOGIES

Table 3 presents the comparison of the component count, CMV, voltage linearity, voltage gain, and voltage stress across filter inductors between the proposed CCMVI topology and the other three-phase topologies. Compared to the conventional VSI, the introduced CCMVI topology uses four more switches, four more diodes, and three more capacitors as depicted in Table 3. According to Table 3, the voltage gain of the introduced CCMVI topology is the highest. The voltage gain of the introduced CCMVI topology is triple of that of the conventional VSI. As a result, the required input of the introduced CCMVI is lowest and one-third of that in the other topologies in [8], [10], [11] and [20]–[25] for the same DC-link voltage. When compared with SCVD topology in [28], the proposed CCMVI topology uses two more switches, two more diodes, and one more capacitor as shown in Table 3. The voltage gain of the proposed CCMVI topology is 1.5 times more than voltage gain of SCVD topology. Therefore, for the same input voltage, the output voltage of the CCMVI topology can be higher than output voltage of the SCVD topology. Compared to four-leg inverter topology in [20], the CCMVI topology uses two more switches, four more diodes, and two more capacitors. However, four-leg inverter topology uses one more inductor in comparison to CCMVI topology. Compared to voltage-clamping topology in [21], the CCMVI topology uses two more switches and two more diodes. Also, the CCMVI topology uses three capacitors like voltage-clamping topology. Compared to the ESI topology in [22], the CCMVI topology uses two less switches and four more diodes as highlighted in Table 3. Compared to H8 topology in [23] and modified H8 topology in [24], the proposed inverter uses three more capacitors, two more switches and four more diodes as shown in Table 3. Compared to the ZVR

topology, the proposed inverter uses eight less diodes, one more capacitor and one more switch as highlighted in Table 3.

As highlighted in Table 3, we can see that the CCMVI topology operates with the full range of modulation index while the conventional VSI using NSPWM in [8] and RSPWM in [10] have limitations on the modulation index. H8 topology in [23], modified H8 topology in [24], and the ZVR topology in [25], also operates with the full range of modulation index as emphasized in Table 3.

The CMV of the introduced CCMVI is zero while that of the conventional VSI under different PWM schemes in [8]–[11] is 33% of DC-link voltage. This variation of the ESI topology in [22] and the ZVR topology in [25] is also zero. Meanwhile, it varies within 33% of DC-link voltage with voltage-clamping topology in [21], H8 topology in [23], and modified H8 topology in [24]. The variation in CMV of SCVD topology in [28] is also 33% of DC-link voltage with DPWM and 16% of DC-link voltage with NSPWM.

In the introduced CCMVI topology, voltage stress across filter inductors is the same as DC-link voltage while that in four-leg inverter topology in [20] is double of DC-link voltage. Like four-leg inverter topology in [20], voltage stress across filter inductor in the conventional VSI under different PWM schemes in [8]–[11] and SCVD topology under NSPWM in [28] is double of DC-link voltage.

IV. SIMULATION RESULTS

To confirm the performance and operating principle of the proposed CCMVI topology, the simulation model is established in PLECS simulation platform, and simulation results are given. The simulation parameters of the proposed CCMVI are depicted in Table 4.

Fig. 5 shows a control system for the proposed CCMVI topology in grid-connected mode. As indicated in Fig. 5, a three-phase inductor of 10 mH/phase is considered between the inverter output and the grid. As indicated in Fig. 5, a combination of a predictive current control as discussed in [29], and the proposed PWM control scheme is used to inject currents into the grid. According to [29], the required output voltage at instant k can be predicted as:

$$\begin{bmatrix} v_d^*(k) \\ v_q^*(k) \end{bmatrix} = A \begin{bmatrix} i_d(k) \\ i_q(k) \end{bmatrix} + B \begin{bmatrix} i_{dref}(k) \\ i_{qref}(k) \end{bmatrix} + \begin{bmatrix} v_{gd}(k) \\ v_{gq}(k) \end{bmatrix}. \quad (15)$$

$$\text{With } A = \begin{bmatrix} \frac{-L_m}{T} & \frac{-\omega L_m}{2} \\ \frac{-\omega L_m}{2} & \frac{-L_m}{T} \end{bmatrix} \text{ and } B = \begin{bmatrix} \frac{L_m}{T} & \frac{-\omega L_m}{2} \\ \frac{\omega L_m}{2} & \frac{L_m}{T} \end{bmatrix}.$$

where $i_d(k)$ and $i_q(k)$ are actual inverter output current in d-axis and q-axis; $v_d^*(k)$ and $v_q^*(k)$ are desired output voltages in d-axis and q-axis; $v_{gd}(k)$ and $v_{gq}(k)$ are grid voltage in d-axis and q-axis; $i_{dref}(k)$ and $i_{qref}(k)$ are reference output current in d-axis and q-axis; ω , L_m , and T are grid angular frequency, the modeled inductance of the output filter and the PWM period, respectively.

Fig. 6 illustrates the simulation waveforms of the proposed topology with an injected current of 6 A. It can be observed from Fig. 6(a) that the DC-link voltage of the introduced topology is triple of the input voltage. The DC-link voltage

TABLE 3. Comparison between the introduced CCMVI topology and other topologies for the same DC-link voltage (V_{PN}).

	Number of Switches + Diodes	Extra Capacitors + Inductors	V_{CMV}	Voltage gain	Voltage linearity	Voltage stress across Filter Inductor
Conventional VSI under NSPWM [8]	6 + 0	-	$V_{PN}/3$	1	0.66 to 1	$2V_{PN}$
Conventional VSI under AZSPWM [11]	6 + 0	-	$V_{PN}/3$	1	0 to 1	$2V_{PN}$
Conventional VSI under RSPWM [10]	6 + 0	-	0	1	0 to 0.57	$2V_{PN}$
Four-leg inverter topology [20]	8 + 0	1 + 1	0	1	0.66 to 1	$2V_{PN}$
Voltage-clamping topology [21]	8 + 2	3 + 0	$V_{PN}/3$	1	0 to 1	V_{PN}
ESI topology [22]	12 + 0	2 + 0	0	1	0 to 1	V_{PN}
H8 topology [23]	8 + 0	-	$V_{PN}/3$	1	0 to 1	V_{PN}
Modified H8 topology [24]	8 + 0	-	$V_{PN}/3$	1	0 to 1	V_{PN}
ZVR topology [25]	9 + 12	2 + 0	0	1	0 to 1	V_{PN}
SCVD topology under NSPWM [28]	8 + 2	2 + 0	$V_{PN}/6$	2	0.66 to 1	$2V_{PN}$
SCVD topology under DPWM [28]	8 + 2	2 + 0	$V_{PN}/3$	2	0 to 1	V_{PN}
Proposed CCMVI Topology	10 + 4	3 + 0	0	3	0 to 1	V_{PN}

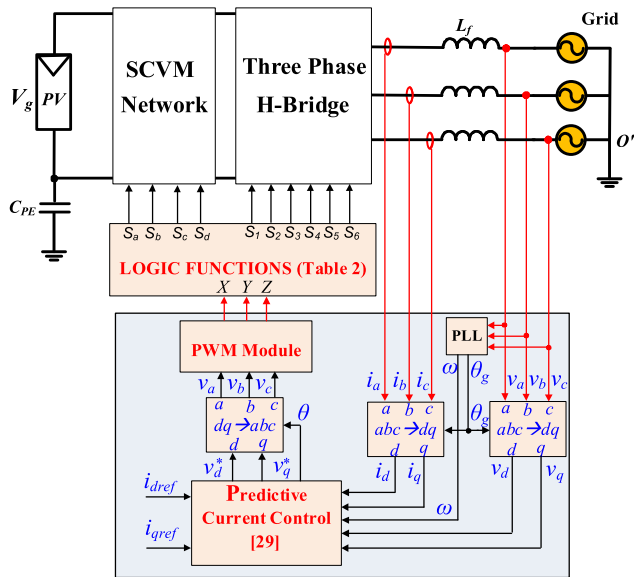


FIGURE 5. Structure of the controller used for the proposed CCMVI in grid-connected mode.

of the introduced topology is obtained as 300 V from the input voltage of 100 V as highlighted in Fig. 6(a). The proposed topology under the proposed PWM control technique generates unipolar output line-to-line voltage as indicated in Fig. 6(a). As a result, voltage stress across the inductor filter is the same as the DC-link voltage. The grid voltages, grid currents, CMV across the parasitic capacitor, and the leakage current are demonstrated in Fig. 6(b). It can be observed

TABLE 4. Simulation parameters.

Parameters	Values
Input voltage (V_g)	100 V
Grid phase voltage (peak)	150 V
PWM carrier frequency	10 kHz
Fundamental frequency	50 Hz
Capacitors (C_a , C_b and C_c)	470 μ F
Parasitic capacitor (C_{PE})	220 nF

from the simulation waveform, the proposed inverter injects sinusoidal currents of 6 A to the grid. The THD value of the grid currents is around 1%. It can be observed from the simulation waveform that CMV across the parasitic capacitor is around 0 V. The RMS value of the leakage current is only 0.5 mA. Figs. 6(c) and 6(d) show waveforms of voltage across additional switches and their expanded view. As shown in Figs. 6(d), the voltage across three switches S_a , S_b , and S_c is 100 V while the voltage across switch S_d is 200 V.

Fig. 7 illustrates dynamic performance waveforms of introduced topology. As indicated in Fig. 7(a), at $t = 0.2$ s, the proposed inverter injects sinusoidal currents of 6 A to the grid. From Fig. 7(a), we can see that the CMV across the parasitic capacitor is around 0 V. The RMS value of the leakage current is around 0.5 mA. The harmonic spectrum analysis of the grid current and leakage current, in this case, is presented in Fig. 8(a). The THD value of the grid current is around 1%. Fig. 7(b) demonstrates dynamic performance waveforms of introduced topology with injected current changed from 6 A to 3 A. From Fig. 7(b), at $t = 0.4$ s, the injected sinusoidal

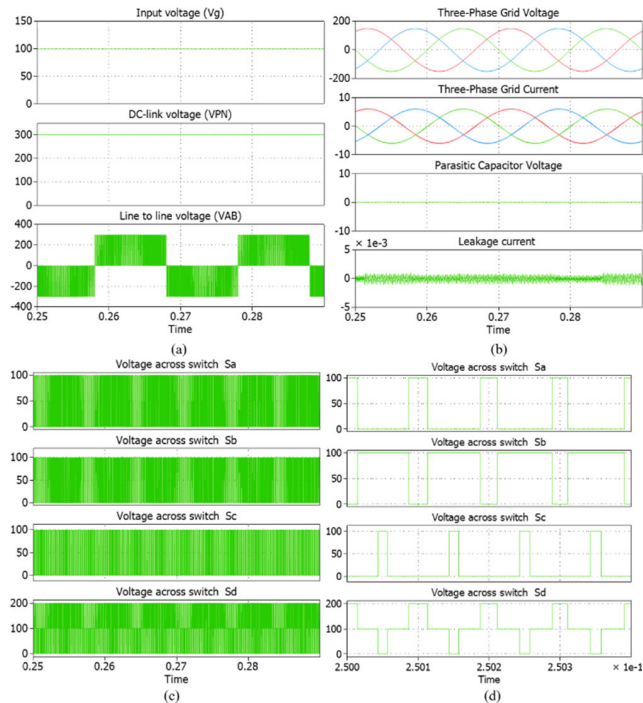


FIGURE 6. Simulation waveforms of introduced topology. From top to bottom: (a) input voltage, DC-link voltage, and line-to-line voltage; (b) grid voltages, grid currents, CMV across parasitic capacitor and the leakage current; (c)-(d) voltage across switch S_a , voltage across switch S_b , voltage across switch S_c and voltage across switch S_d .

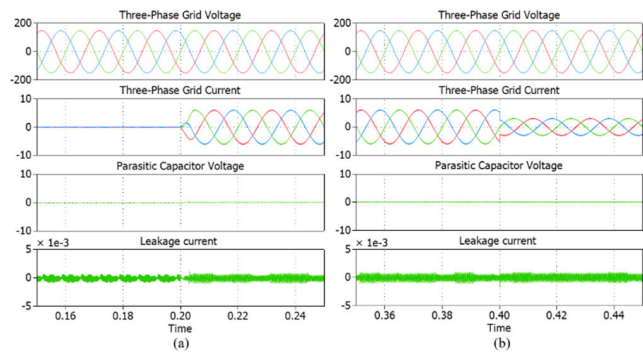


FIGURE 7. Dynamic performance waveforms of introduced topology. From top to bottom: grid voltages, grid currents, CMV across parasitic capacitor and the leakage current. (a) injected current changed from 0 A to 6 A; (b) injected current changed from 6 A to 3 A.

currents are stepped down from 6 A to 3 A. The RMS value of the leakage current is around 0.5 mA. The harmonic spectrum analysis of the grid current and leakage current, in this case, is shown in Fig. 8(b). The THD value of the grid current is around 1.1%.

V. EXPERIMENTAL RESULTS

To prove the efficacy of the introduced CCMVI topology, the laboratory-built prototype based on a DSP F280049C microcontroller is exhibited in Fig. 9, and its components are listed in Table 4. The RHRG3060 diodes and IPW60R040C7 MOSFETs have been used for the experiments. The equivalent series resistance of capacitors is 240 mΩ. Due to the

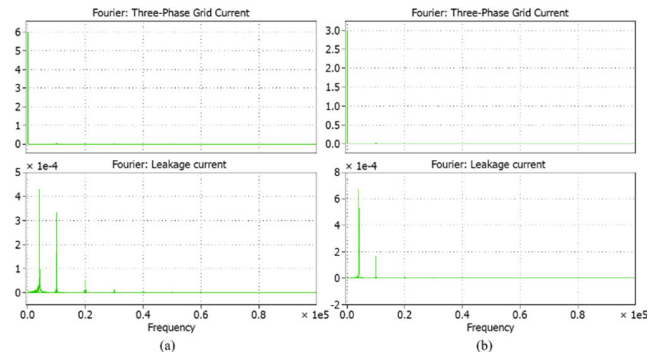


FIGURE 8. The harmonic spectrum of grid currents and the leakage current with (a) injected current of 6 A, and (b) injected current 3 A.

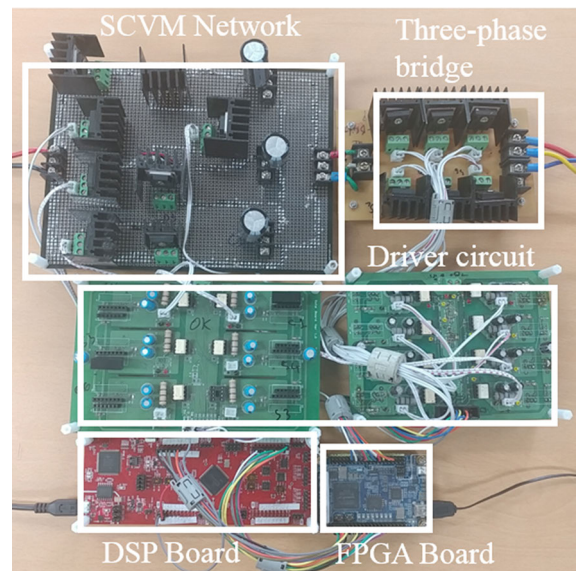


FIGURE 9. Prototype photo of the introduced CCMVI.

limitation of laboratory, the proposed CCMVI topology is only tested in stand-alone mode with an inductive load of 50 Ω - 15 mH / phase. Figs. 10 and 11 indicate the experimental results of proposed CCMVI under the proposed PWM control technique.

As shown in Fig. 10 (a), the DC-link voltage of the proposed CCMVI topology is obtained as 289 V from the input voltage of 100 V. As given in Fig. 10 (a), the output line-to-line voltage of the proposed CCMVI under the proposed PWM control technique is unipolar in nature. As shown in Fig. 10 (b), the amplitude value of output currents is 2.94 A while their THD values are about 0.6 %.

The output phase voltage, line-to-line voltage, and their harmonic spectrum analysis are shown in Figs. 10(c) and 10(d). The fundamental harmonic values of output phase voltage and output line-to-line voltage are 106 V_{rms} and 185 V_{rms} as shown in Figs. 10(c) and 10(d), respectively. Figs. 11(a) and 11(b) indicate waveforms of voltage across additional switches and their expanded view. As shown in Figs. 11(a) and 11(b), the voltage across three switches S_a , S_b , and S_c is 97 V while the voltage across switch S_d is 193V.

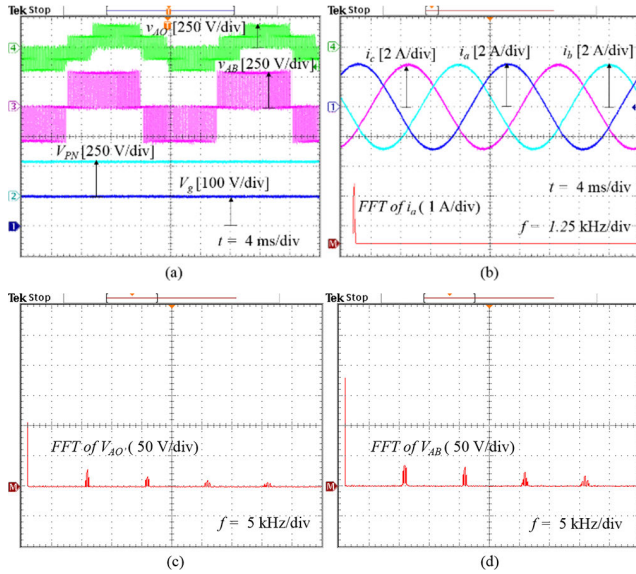


FIGURE 10. Experimental waveforms of introduced CCMVI topology. From top to bottom: (a) Phase-A voltage, line-to-line voltage, DC-link voltage, and input voltage; (b) output currents and FFT of output currents; (c) FFT of Phase-A voltage and (d) FFT of line-to-line voltage.

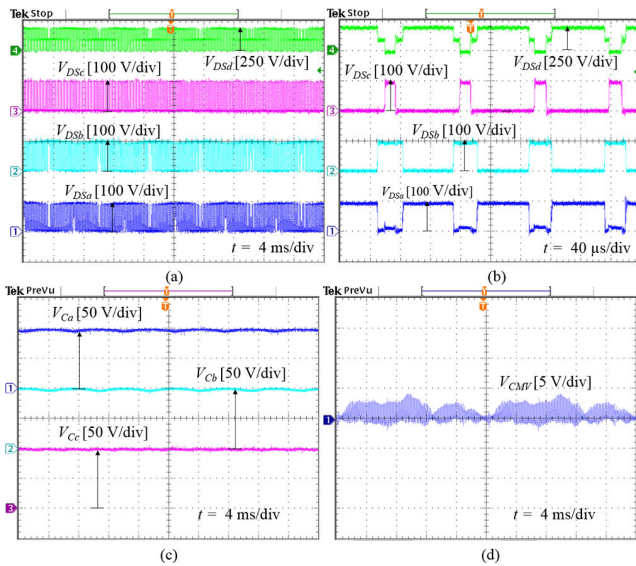


FIGURE 11. Experimental output waveforms of introduced CCMVI. From top to bottom: (a)-(b) voltage across switch S_d , voltage across switch S_c , voltage across switch S_b and voltage across switch S_a ; (c) capacitor C_a voltage, capacitor C_b voltage and capacitor C_c voltage; (d) common-mode voltage.

The voltage across three capacitors (C_a , C_b , and C_c) is also 97 V as highlighted in Fig. 11(c). Fig. 11(d) shows CMV of the proposed CCMVI topology. It can be observed from the waveform that the variation of common-mode voltage is about 3 V due to the effect of voltage ripple on capacitors.

Fig. 12 highlights the losses distribution chart of the proposed topology. The total power loss of proposed topology is 50.5 W at the power of 900 W. From Fig. 12, we can see that the most losses come from conduction loss of the switches. The proposed topology uses four more additional switches, four more additional diodes, and three more capac-

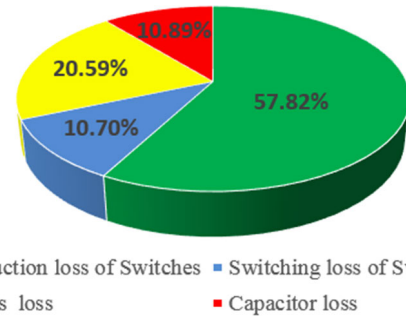


FIGURE 12. Power loss contribution of the introduced CCMVI.

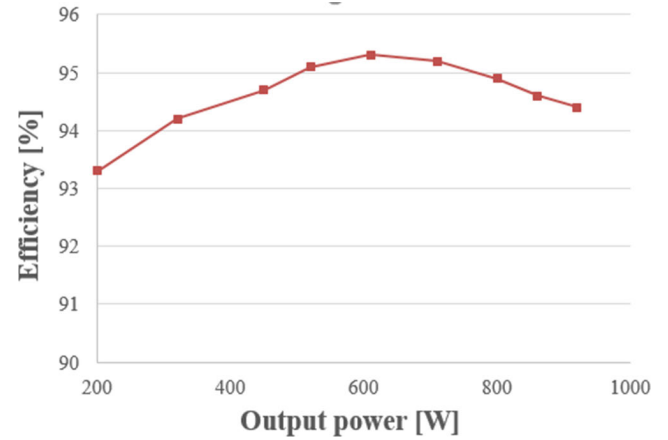


FIGURE 13. Measured efficiency versus output power of the introduced CCMVI.

itors than those of the conventional VSI. So, its efficiency is lower than that of the conventional VSI. However, the voltage across on additional switches (S_a , S_b , and S_c) of the proposed topology is only one-third of DC-link voltage, and the voltage across on additional switch S_d is two-thirds of DC-link voltage. As a result, power loss on extra switches is reduced.

Fig. 13 highlights the measured efficiency of proposed CCMVI with various output power when $V_g = 100$ V and output phase voltage of 150 V. As highlighted in Fig. 13, we can see that the maximum efficiency of the laboratory prototype is around 95.2 % at 610 W. The CEC Efficiency (η_{CEC}) is calculated according to the following [30]:

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (16)$$

where $\eta_{10\%}$, $\eta_{20\%}$, $\eta_{30\%}$, $\eta_{50\%}$, $\eta_{75\%}$, $\eta_{100\%}$ is the efficiency of proposed topology at 10%, 20%, 30%, 50%, 75%, and 100% of the rated power, respectively.

The prototype of the proposed topology reached a California Energy Commission (CEC) weighted power stage efficiency of 94.6%.

VI. CONCLUSION

In this paper, the three-phase constant common-mode voltage inverter with triple voltage boost is proposed. The introduced topology can provide a remarkable DC-link voltage that is

triple of the input voltage. Therefore, the introduced topology can be operated in both buck and boost modes. Besides, the PWM control technique for the introduced topology is also presented, which is easy to follow and implement in practice. In addition, modeling, analysis of the leakage current paths in the PV system have been described. With introduced PWM control technique, the CMV of the introduced inverter is maintained as constant at zero. Thus, by limiting the variation in CMV, the leakage current that flows through the parasitic capacitance existing between the load ground and PV array ground can be effectively reduced. The introduced inverter generates unipolar output. Therefore, voltage stress across filter inductors is the same as the DC-link voltage, resulting in limited size and loss in the filter inductors. It is worth noting that the inrush current of the capacitors and high power conduction loss in the switched-capacitor network are the drawbacks of the introduced inverter. Operating principles, mathematical analysis, circuit analysis, and comparison of the proposed inverter with the other existing inverters are presented. The simulation and experimental results associated with the efficiency measurement of the built inverter prototype have been illustrated to prove the effectiveness and feasibility of the proposed topology.

REFERENCES

- [1] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, and M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2202–2211, Sep. 2009.
- [2] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelon, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Ind. Electron. Mag.*, vol. 9, no. 1, pp. 47–61, Mar. 2015.
- [3] Ó. López, F. D. Freijedo, A. G. Yepes, P. Fernández-Comesaña, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.
- [4] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.
- [5] L. Wang, Y. Shi, Y. Shi, R. Xie, and H. Li, "Ground leakage current analysis and suppression in a 60-kW 5-level T-type transformerless SiC PV inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1271–1283, Feb. 2018.
- [6] *Safety for Power Converters for Use in Photovoltaic Power Systems—Part 2: Particular Requirements for Inverters*, Standard IEC 62109-2, 2011.
- [7] E. Ün and A. M. Hava, "Performance characteristics of the reduced common mode voltage near state PWM method," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
- [8] E. Ün and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, Mar./Apr. 2009.
- [9] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–476, Mar./Apr. 1999.
- [10] M. C. Cavalcanti, K. C. de Oliveira, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010.
- [11] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects—Part I: Basic development," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1605–1612, Nov./Dec. 2004.
- [12] A. M. Hava and E. Ün, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, Jul. 2011.
- [13] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013.
- [14] J. Huang and H. Shi, "Suppressing low-frequency components of common-mode voltage through reverse injection in three-phase inverter," *IET Power Electron.*, vol. 7, no. 6, pp. 1644–1653, Jun. 2014.
- [15] J. W. Kimball and M. Zawodniok, "Reducing common-mode voltage in three-phase sine-triangle PWM with interleaved carriers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2229–2236, Aug. 2011.
- [16] K. Tian, J. Wang, B. Wu, Z. Cheng, and N. R. Zargari, "A virtual space vector modulation technique for the reduction of common-mode voltages in both magnitude and third-order component," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 839–848, Jan. 2016.
- [17] S. Kwak and S.-K. Mun, "Model predictive control methods to reduce common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5019–5035, Sep. 2015.
- [18] L. Guo, N. Jin, C. Gan, and K. Luo, "Hybrid voltage vector preselection-based model predictive control for two-level voltage source inverters to reduce the common-mode voltage," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4648–4691, Jun. 2020.
- [19] J. Huang and H. Shi, "A hybrid filter for the suppression of common-mode voltage and differential-mode harmonics in three-phase inverters with CPPM," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 3991–4000, Jul. 2015.
- [20] X. Guo, R. He, J. Jian, Z. Lu, X. Sun, and J. M. Guerrero, "Leakage current elimination of four-leg inverter for transformerless three-phase PV systems," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1841–1846, Mar. 2016.
- [21] L. Concarì, D. Barater, G. Buticchi, C. Concarì, and M. Liserre, "H8 inverter for common-mode voltage reduction in electric drives," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4010–4019, Sep. 2016.
- [22] X. Guo, Y. Yang, and T. Zhu, "ESI: A novel three-phase inverter with leakage current attenuation for transformerless PV systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2967–2974, Apr. 2018.
- [23] R. Rahimi, S. Farhangi, B. Farhangi, G. R. Moradi, E. Afshari, and F. Blaabjerg, "H8 inverter to reduce leakage current in transformerless three-phase grid-connected photovoltaic systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 2, pp. 910–918, Jun. 2018.
- [24] A. K. Gupta, H. Agrawal, and V. Agarwal, "A novel three-phase transformerless H-8 topology with reduced leakage current for grid-tied solar PV applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1765–1774, Mar. 2019.
- [25] X. Guo, X. Zhang, H. Guan, T. Kerekes, and F. Blaabjerg, "Three-phase ZVR topology and modulation strategy for transformerless PV system," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1017–1021, Feb. 2019.
- [26] A. Taghvaie, M. E. Haque, S. Saha, and M. A. Mahmud, "A new step-up switched-capacitor voltage balancing converter for NPC multilevel inverter-based solar PV system," *IEEE Access*, vol. 8, pp. 83940–83952, 2020.
- [27] S. S. Lee and K.-B. Lee, "Switched-capacitor-based modular T-type inverter (SC-MTI)," *IEEE Trans. Ind. Electron.*, early access, May 12, 2020, doi: [10.1109/TIE.2020.2992963](https://doi.org/10.1109/TIE.2020.2992963).
- [28] T.-T. Tran, M.-K. Nguyen, T.-D. Duong, J.-H. Choi, Y.-C. Lim, and F. Zare, "A switched-capacitor-voltage-doubler based boost inverter for common-mode voltage reduction," *IEEE Access*, vol. 7, pp. 98618–98629, 2019.
- [29] Q. Zeng and L. Chang, "An advanced SVPWM-based predictive current controller for three-phase inverters in distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1235–1246, Mar. 2008.
- [30] B. Gu, J. Dominic, J.-S. Lai, C.-L. Chen, T. LaBella, and B. Chen, "High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2235–2245, May 2013.



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