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Impedance-Based Stability Analysis of Constant-Power-Source-Involved and Cascaded-Type DC Distributed Power Systems

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ABSTRACT This paper proposes impedance specifications for guaranteeing the stability of a cascaded-type DC distributed power system (DPS), which is formed by several cascaded voltage source modules, several load modules, and several constant power source modules. To analyze the stability of a cascaded-type DC DPS, there are conventional approaches like eigenvalue method, root-locus method, bode-diagram method and so on. However, the aforementioned stability analysis approaches will suffer from the incomplete system parameters if the modules of the DPS are designed modularly and independently. This paper defines time-invariant and decentralized impedance specifications for the modules of the cascaded-type DC DPS, where the impedance specifications are independent to each other. Thus, the modules of the cascaded-type DC DPS can be independently and modularly designed, as well the stability of the cascaded-type DC DPS can be guaranteed.

INDEX TERMS Impedance, DC distributed power systems, stability criteria, modular design.

I. INTRODUCTION

Distributed power systems (DPSs) have been attracting increasing attentions for its effectiveness of accessing distributed generations [1]–[4]. According to the topology, a DPS can be classified into a paralleled type [5], [6] or a cascaded type [7]–[14]. In a well-known paralleled-type DPS, all of the modules (voltage sources, constant power sources, and loads) are paralleled and connected to a common bus, of which the respective methodologies are abundant. Nevertheless, in a cascaded-type DPS as shown in Figure 1, the voltage source modules are cascaded to support the voltage of a high-level bus, of which the respective theories and technologies require deep-going research.

Considering the bus frequency, a cascaded-type DPS can be classified into two categories: AC one [7]–[11] and DC one [12]–[14]. For a cascaded-type AC DPS, the key problem is frequency synchronizing and power coordination among the cascaded voltage source modules, so the researchers focus on proposing various cooperation control strategies [7], [8].

However, in a cascaded-type DC DPS as shown in Figure 1, the control strategies of the cascaded voltage source modules are quite simple because there is no frequency problem. In fact, as long as each voltage source module is regulated to have a stable bus-side-port voltage, the voltage of the DC bus will be supported stably, as well the power sharing among the cascaded voltage source modules will be realized. Thus, the key problem in a cascaded-type DC DPS is ensuring the stability of the system.

To solve the stability problem of a cascaded-type DPS, the conventional approaches commonly establish the full dynamic model of the DPS, and conduct eigenvalue analyses, root-locus analyses, or bode-diagram analyses on the established full model [7], [8], [12], [13]. But a full-model-based approach would suffer from the curse of dimensionality when there is a quite large-scale system. Furthermore,

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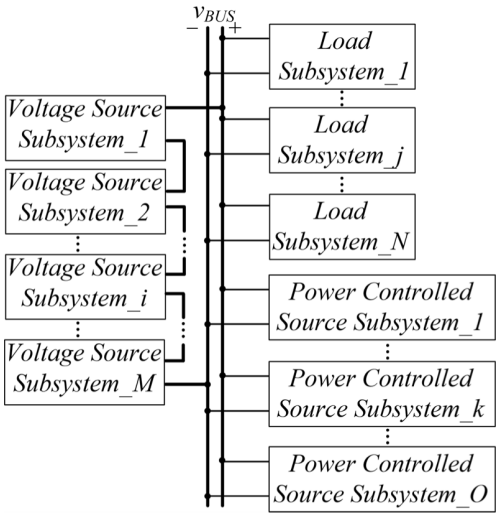

FIGURE 1. Typical structure of a constant-power-source-involved and cascaded-type DPS.

a full-model-based method will suffer from the incomplete system parameters if the modules of the DPS are designed modularly and independently.

The impedance-based stability analysis approach has been considered as an effective method to overcome the aforementioned deficiencies of the full-model-based approaches in a DPS [15], [16]. An impedance-based stability analysis approach just needs the impedance model rather than the full model of the DPS, which has low complexity and is suitable for a large-scale DPS [17]–[20]. An impedance-based approach can be classified into one of the two types: centralized one [17], [18] and decentralized one [19], [20]. The centralized impedance-based approaches need to synthesize all of the impedance models of the modules in a DPS, which still cannot give the system stability conclusions when each module of the DPS is designed independently. By contrast, the main idea of a decentralized impedance-based approach is to define impedance specifications for the modules of a DPS. As long as each module satisfies the given impedance specifications in its modular design stage, the stability of the whole DPS consisted of the well-designed modules can be guaranteed. However, the existing decentralized impedance methods have relatively narrow applicable ranges. The decentralized impedance method in [19] is only suitable for a DC DPS consisted of a voltage source module and several load modules. The method in [20] is only suitable for a DC DPS consisted of a voltage source module, several load modules and several constant power source modules. The method in [21] is only suitable for a DC DPS consisted of several cascaded voltage source modules and several load modules. In a word, the decentralized impedance approach in reference [19]–[21] cannot guarantee the stability of a cascaded-type DC DPS, which is formed by several cascaded voltage source modules, several load modules, and several constant power source modules.

Facing the foregoing problem, the main contribution of this paper is to extend the method in [21] to make it suitable for a

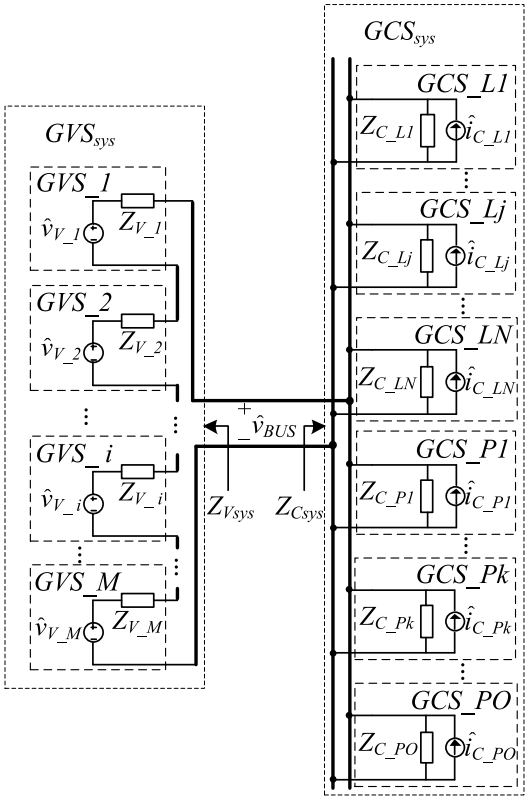

FIGURE 2. A small-signal model of a constant-power-source-involved and cascaded-type DC DPS.

cascaded-type DC DPS which is formed by several cascaded voltage source modules, several load modules, and several constant power source modules. For guaranteeing the stability of a constant-power-source-involved and cascaded-type DC DPS, this paper defines time-invariant and decentralized impedance specifications for the modules, where the impedance specifications are independent to each other. Thus, the modules of the constant-power-source-involved and cascaded-type DC DPS can be independently and modularly designed, as well the stability of the cascaded-type DC DPS can be guaranteed.

This paper will be organized as follows: Section II deduces the methodology of the defined impedance specifications. Section III verifies the proposed approach in a cascaded-type DC DPS by hardware-in-loop tests. Section IV concludes this paper.

II. METHODOLOGY

A. CENTRALIZED IMPEDANCE ANALYSES

Based on the theory in [20], a module of a DC DPS would be sorted as a generalized voltage source (GVS) or a generalized current source (GCS). A voltage source module influences or controls the voltage of the DC bus, which would be sorted as a GVS. A load module or a constant power source module influences or controls the current that injects to the DC bus, which can be sorted as a GCS.

In the stage of the system design, the output voltage of a GVS is designed to be stable when the GVS supplies an

ideal current source. According to this characteristic, one can use a Thevenin equivalent circuit *GVS_i* to establish the small-signal model of a GVS as shown in Figure 2. In circuit *GVS_i*, both of the $\hat{v}_{V\_i}(s)$ and $Z_{V\_i}(s)$ $(i = 1, 2, \ldots, M)$ have no right half plane (RHP) pole, which means that they are stable. In a similar manner, the input current of a GCS is designed to be stable when the GCS is supplied by an ideal voltage source. According to this characteristic, one can use a Norton equivalent circuit *GCS_Lj* (or *GCS_Pk*) to establish the small-signal model of a GCS. In circuit *GCS_Lj* (or *GCS_Pk*), both of the $\hat{i}_{C\_Lj}(s)$ (or $\hat{i}_{C\_Pk}(s)$) and $1/Z_{C\_Lj}(s)$ (or $1/Z_{C\_Pk}(s)$) $(j = 1, 2, \ldots, N; k = 1, 2, \ldots, O)$ have no RHP pole, which means that they are stable.

In a constant-power-source-involved and cascaded-type DC DPS, the GVSs are cascaded and support the voltage of the DC bus. The GCSs are formed by the loads and the constant power sources, where the loads are paralleled and sink power from the DC bus, and the constant power sources are paralleled and inject power into the DC bus. Then, as shown in Figure 2, one can establish the small-signal model of a constant-power-source-involved and cascaded-type DC DPS. Note that GVS_{sys} is a system-level GVS which is formed by the cascaded module-level GVSs. Furthermore, GCS_{sys} is a system-level GCS which is formed by the paralleled module-level GCSs.

According to Millman's Theorem [22], one can calculate the small-signal voltage of the DC bus as (1), as shown at the bottom of the page.

where $\hat{v}_{V\_i}(s)$ and $Z_{V\_i}(s)$ $(i = 1, 2, \ldots, M)$ are the voltage source and impedance in the Thevenin equivalent circuit *GVS_i*, $\hat{i}_{C\_Lj}(s)$ and $1/Z_{C\_Lj}(s)$ $(j = 1, 2, \ldots, N)$ are the current source and admittance in the Norton equivalent circuit *GCS_Lj*, and $\hat{i}_{C\_Pk}(s)$ and $1/Z_{C\_Pk}(s)$ $(k = 1, 2, \ldots, O)$ are the current source and admittance in the Norton equivalent circuit *GCS_Pk*. The cascade of $Z_{V\_i}(s)$ $(i = 1, 2, \ldots, M)$ is

$$Z_{Vsys}(s) = \sum_{i=1}^{M} Z_{V\_i}(s), \tag{2}$$

and the parallel of $Z_{C\_Lj}(s)$ $(j = 1, 2, \ldots, N)$ and $Z_{C\_Pk}(s)$ $(k = 1, 2, \ldots, O)$ is

$$Z_{Csys}(s) = \left(\sum_{j=1}^{N} Z_{C\_Lj}^{-1}(s) + \sum_{k=1}^{O} Z_{C\_Pk}^{-1}(s)\right)^{-1}. \tag{3}$$

Eq. (1) can be recombined as (4), as shown at the bottom of the page.

Defining

$$H(s) = \frac{1}{1 + T_m(s)} = \frac{1}{1 + Z_{Vsys}(s)/Z_{Csys}(s)}, \tag{5}$$

the stability of $H(s)$ will be equivalent to that of the constant-power-source-involved and cascaded-type DC DPS. Further observing $H(s)$, one can treat $H(s)$ as the closed-loop transfer function of the system, and treat $T_m(s)$ as the open-loop gain. Therefore, if $T_m(s)$ obeys the Middlebrook Criterion [23], the constant-power-source-involved and cascaded-type DC DPS will be stable.

It should be noticed that $Z_{V\_i}(s)$ $(i = 1, 2, \ldots, M)$ in circuit *GVS_i* has no RHP pole according to the characteristics of a GVS, thus $Z_{Vsys}(s)$ has no RHP pole according to (2). Besides, $Z_{C\_Lj}^{-1}(s)$ (or $Z_{C\_Pk}^{-1}(s)$) $(j = 1, 2, \ldots, N; k = 1, 2, \ldots, O)$ in circuit *GCS_Lj* (or *GCS_Pk*) has no RHP pole according to the characteristics of a GCS, thus $1/Z_{Csys}(s)$ has no RHP pole according to (3). Hence, the open-loop gain $T_m(s) = Z_{Vsys}(s)/Z_{Csys}(s)$ has no RHP pole.

B. DECENTRALIZED IMPEDANCE SPECIFICATIONS

Observing the form of (5), to analyze the system stability by Middlebrook Criterion, one should use all of the port impedances of the modules in the DC DPS to form the open-loop gain $T_m(s)$, which makes it a centralized stability analysis approach. If the modules of the DC DPS are designed modularly and independently, one module will not able to get the port impedances of the other modules at the system designing stage. In this circumstance, the aforementioned centralized stability analysis approach cannot offer effective instructions to ensure the stability of the system. A practicable method to ensure the stability of a DC DPS at the designing stage is defining feasible decentralized impedance specifications for the modules of the DPS. Once each module satisfies its independent and decentralized impedance specification, the stability of the whole DPS formed by the modules can be ensured.

Reference [20] has defined decentralized impedance specifications to ensure the stability of a DC DPS. However, the method requires that there is only one GVS in the DC DPS. Considering that there are multiple cascaded GVSs in a constant-power-source-involved and cascaded-type DC DPS, thus, one should redefine the respective decentralized impedance specifications.

Considering the constant-power-source-involved and cascaded-type DC DPS as shown in Figure 1, one can

$$\hat{v}_{bus}(s) = \frac{\left(\sum_{i=1}^{M} \hat{v}_{V\_i}(s)\right)/Z_{Vsys}(s) + \sum_{j=1}^{N} \hat{i}_{C\_Lj}(s) + \sum_{k=1}^{O} \hat{i}_{C\_Pk}(s)}{1/Z_{Vsys}(s) + 1/Z_{Csys}(s)}, \tag{1}$$

$$\hat{v}_{bus}(s) = \frac{\left(\sum_{i=1}^{M} \hat{v}_{V\_i}(s) + Z_{Vsys}(s)\left(\sum_{j=1}^{N} \hat{i}_{C\_Lj}(s) + \sum_{k=1}^{O} \hat{i}_{C\_Pk}(s)\right)\right)}{1 + Z_{Vsys}(s)/Z_{Csys}(s)}. \tag{4}$$

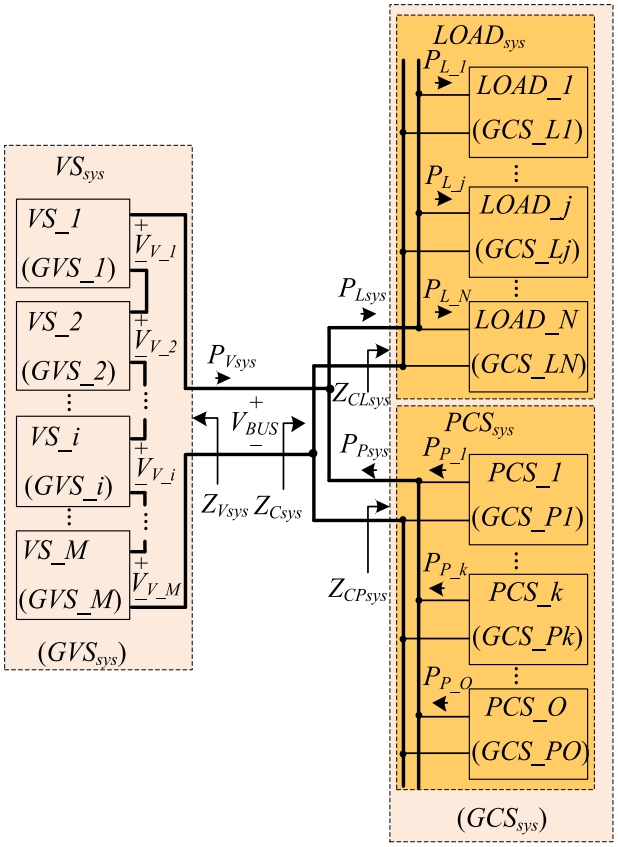

FIGURE 3. Map between the constant-power-source-involved and cascaded-type DC DPS and its small-signal model.

establish the map between the modules and their small-signal models shown as Figure 3. GVS_i models the module-level voltage source VS_i, and GVS_{sys} is the model of the system-level voltage source VS_{sys}. GCS_Lj models the module-level load $LOAD\_j$, and GCS_Pk models the module-level constant power source PCS_k. GCS_{sys} is the model of the parallel of $LOAD_{sys}$, and PCS_{sys}.

Thus, one can derive the capacity conservation equations and the power conservation equations as

$$\begin{cases} E_{sys} = E_{Vsys} + E_{Psys} = E_{Lsys} = \sum_{j=1}^{N} E_{L\_j} \\ P_{Vsys} + P_{Psys} = P_{Lsys} = \sum_{k=1}^{n} P_{L\_k} \\ E_{Psys} = \sum_{k=1}^{O} E_{P\_k} \\ P_{Psys} = \sum_{k=1}^{O} P_{P\_k}. \end{cases} \tag{6}$$

where E_{sys} is the capacity of the DC DPS, and E_{Vsys}, E_{Lsys}, E_{L_j}, E_{Psys}, and E_{P_k} are the capacities of VS_{sys}, $LOAD_{sys}$, $LOAD\_j$, PCS_{sys}, and PCS_k. P_{Vsys} is the power output by VS_{sys}, P_{Lsys} and P_{L_k} are the powers input to $LOAD_{sys}$ and $LOAD\_k$, and P_{Psys} and P_{P_k} are the powers output by PCS_{sys} and PCS_k.

Based on the theory in [20], the impedance specifications of the module-level constant power source PCS_k, the module-level load $LOAD\_j$, and the system-level voltage source VS_{sys} can be given directly as

$$\begin{cases} \left|Z_{Vsys}\right| < \frac{1}{2} \cdot (1-\epsilon) \cdot V_{BUS}^2 \cdot \left(E_{sys} + E_{Psys}\right)^{-1} \\ \left|Z_{C\_Lj}\right| \geq (1-\epsilon) \cdot V_{BUS}^2 \cdot E_{L\_j}^{-1}, \quad j = 1, 2, \ldots, N \\ \left|Z_{C\_Pk}\right| \geq (1-\epsilon) \cdot V_{BUS}^2 \cdot E_{P\_k}^{-1}, \quad k = 1, 2, \ldots, O, \end{cases} \tag{7}$$

where V_{BUS} is the nominal voltage of the DC bus, Z_{Vsys} is the port impedance of the system-level voltage source VS_{sys}, and Z_{C_Lj} and Z_{C_Pk} are the port impedances of the loads and constant power sources. ϵ is a constant in the range of (0, 1).

Here analyze how the impedance specifications in (7) guarantee the stability of a cascaded-type DC DPS. According to Middlebrook Criterion [23], if the open-loop gain $T_m(s) = Z_{Vsys}(s)/Z_{Csys}(s)$ defined in (5) has

$$\left|Z_{Vsys}(s)\right| < \left|Z_{Csys}(s)\right|, \tag{8}$$

the Nyquist curve of $T_m(s)$ will not encircle the point $(-1, j0)$. Considering the open-loop gain $T_m(s)$ has no right half plane (RHP) pole, the closed-loop transfer function $H(s) = 1/(1 + T_m(s))$ defined in (5) will have no RHP pole according to Nyquist Criterion, hence the cascaded-type DC DPS will be stable.

Considering the aforementioned Middlebrook Criterion, the key to the effectiveness of the impedance specifications proposed in (7) is how it makes the condition in (8) satisfied. To illustrated this, one can synthesize (3), (6) and (7), and study the relationship between $|Z_{Vsys}(s)|$ and $|Z_{Csys}(s)|$, which can be depicted as

$$\begin{aligned} &20\log\frac{\left|Z_{Vsys}\right|}{\left|Z_{Csys}\right|} \\ &= 20\log\left|Z_{Vsys}\right| - 20\log|Z_{Csys}| \\ &= 20\log\left|Z_{Vsys}\right| - 20\log|(\sum_{j=1}^{N} Z_{C\_Lj}^{-1} + \sum_{k=1}^{O} Z_{C\_Pk}^{-1})^{-1}| \\ &= 20\log\left|Z_{Vsys}\right| + 20\log|\sum_{j=1}^{N} Z_{C\_Lj}^{-1} + \sum_{k=1}^{O} Z_{C\_Pk}^{-1}| \\ &\leq 20\log\left|Z_{Vsys}\right| + 20\log(\sum_{j=1}^{N} |Z_{C\_Lj}^{-1}| + \sum_{k=1}^{O} |Z_{C\_Pk}^{-1}|) \\ &\leq 20\log\left|Z_{Vsys}\right| + 20\log(\sum_{j=1}^{N} \frac{E_{L\_j}}{(1-\epsilon)\, V_{BUS}^2} \\ &\qquad + \sum_{k=1}^{O} \frac{E_{P\_k}}{(1-\epsilon)\, V_{BUS}^2}) \\ &< 20\log\frac{1}{2}\frac{(1-\epsilon)\, V_{BUS}^2}{E_{sys} + E_{Psys}} + 20\log\frac{E_{sys} + E_{Psys}}{(1-\epsilon)\, V_{BUS}^2} = 20\log\frac{1}{2}, \end{aligned} \tag{9}$$

which means $\left|Z_{Vsys}(s)\right| < \left|Z_{Csys}(s)\right|/2$ and makes the condition in (8) satisfied, then the cascaded-type DC DPS will be stable.

According to the above analysis, the proposed impedance in (7) can guarantee the stability of a cascaded-type DC DPS. But analyzing the form of (7), one can find that the module-level loads and the constant power sources have been given their own decentralized impedance specifications, while the cascaded module-level voltage sources share

a centralized impedance specification, which is possessed by the system-level voltage source VS_{sys}. Therefore, one should decentralize the centralized impedance specification for VS_{sys} to the module-level voltage sources. If one defines the impedance specification for the module-level voltage source VS_i as

$$|Z_{V\_i}| < \frac{1}{2} \cdot \frac{(1-\epsilon) \cdot V_{BUS} \cdot V_{V\_i}}{E_{sys} + E_{Psys}}, \quad i = 1, 2, \ldots, M, \tag{10}$$

where V_{V_i} is the nominal voltage output by VS_i, and Z_{V_i} is the port impedance of VS_i.

Then

$$\begin{aligned} |Z_{Vsys}| &= |\sum_{i=1}^{M} Z_{V\_i}| \le \sum_{i=1}^{M} |Z_{V\_i}| \\ &< \sum_{i=1}^{M} \frac{1}{2} \cdot (1-\epsilon) \cdot V_{BUS} \cdot V_{V\_i} \cdot \left(E_{sys} + E_{Psys}\right)^{-1} \\ &\le \frac{1}{2} \cdot (1-\epsilon) \cdot V_{BUS}^2 \cdot \left(E_{sys} + E_{Psys}\right)^{-1}, \end{aligned} \tag{11}$$

and the impedance specification of VS_{sys} will be satisfied. In other word, (10) have decentralized the impedance specification for VS_{sys} to the module-level voltage sources. Thus, one can conclude the impedance specifications for the modules in the constant-power-source-involved and cascaded-type DC DPS as

$$\begin{cases} |Z_{V\_i}| < \frac{1}{2} \cdot \frac{(1-\epsilon) \cdot V_{BUS} \cdot V_{V\_i}}{E_{sys} + E_{Psys}}, & i = 1, 2, \ldots, M \\ |Z_{C\_Lj}| \ge (1-\epsilon) \cdot V_{BUS}^2 \cdot E_{L\_j}^{-1}, & j = 1, 2, \ldots, N \\ |Z_{C\_Pk}| \ge (1-\epsilon) \cdot V_{BUS}^2 \cdot E_{P\_k}^{-1}, & k = 1, 2, \ldots, O. \end{cases} \tag{12}$$

How the impedance specifications proposed in (12) guarantee the stability of a cascade-type DC DPS can be concluded as: (12) makes the impedance specifications in (7) satisfied according to (11), then (7) makes the condition in (8) satisfied according to (9), and (8) can guarantee the stability of a cascaded-type DC DPS according to Middlebrook Criterion.

By (12), the modules in the DC DPS have got decentralized impedance specifications that are independent to each other. Based on these impedance specifications, one can realize the independent and modular design of the modules in the constant-power-source-involved and cascaded-type DC DPS, as well one can guarantee the stability of the DC DPS.

III. CASE STUDY

A. SYSTEM STRUCTURE AND PARAMETER

For verifying the proposed method, this paper uses a hardware-in-loop testing platform to build a constant-power-source-involved and cascaded-type DC DPS shown as Figure 4. The nominal voltage of the DC bus is $V_{UBS} = 500$ V. The capacity of the cascaded-type DC DPS is $E_{sys} = 175$ kW. The cascaded-type DC DPS is formed by six modules: VS_1 and VS_2 are two cascaded voltage source modules; $LOAD\_1$, $LOAD\_2$, and $LOAD\_3$ are three paralleled load modules; and PCS_{sys} is a constant power source module.

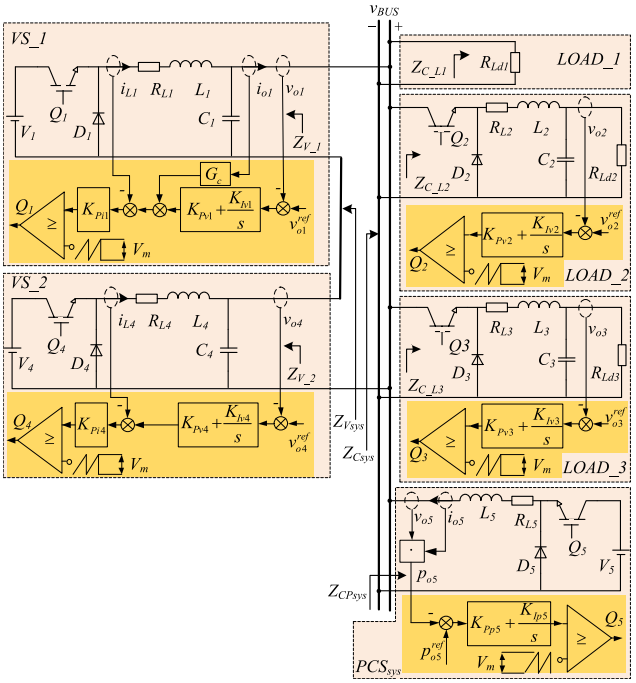

FIGURE 4. Topology of the simulated constant-power-source-involved and cascaded-type DC DPS.

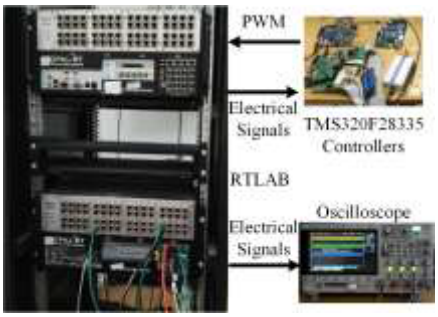

FIGURE 5. Hardware-in-loop testing platform.

The voltage source module VS_1 is regulated by its own output-voltage controller as well as VS_2, then the cascade of VS_1 and VS_2 is used to establish the voltage of the DC bus. The nominal voltage output by VS_1 is 300 V, while the nominal voltage output by VS_2 is 200 V. VS_1 equips a feed-forward compensation unit G_c to shape its port impedance based on the technology proposed in reference [24]. $LOAD\_1$ is a resistance with a capacity of $E_{L_1} = 25$kW. $LOAD\_2$ is a converter whose output voltage is tightly regulated, which acts as a constant power load with a capacity of $E_{L\_2} = 100$ kW. $LOAD\_3$ is similar to $LOAD\_2$ but the capacity is $E_{L_3} = 50$kW. PCS_{sys} is regulated by a power controller, which make it inject into the DC bus a constant power. Thus, it acts as a constant power source module.

The hardware-in-loop testing platform adopted by this paper is shown as Figure 5. In the testing platform, the power circuits of the cascaded-type DC DPS in Figure 4 are modeled in a RT-LAB, which is a real-time simulator. The control

TABLE 1. Parameters of the DC DPS.

Parameters	Value	Parameters	Value
V_1	600 V	R_{Ld3}	1.25 Ω
R_{L1}	1 mΩ	K_{Pv3}	2.20e-3
L_1	5 mH	K_{Iv3}	0.507
C_1	10000 μF	V_{o3}^{ref}	250 V
V_m	1 V	R_{Ld1}	10 Ω
K_{Pi1}	3.59e-2	V_4	400 V
K_{Pv1}	4.14	R_{L4}	1 mΩ
K_{Iv1}	304	L_4	8 mH
V_{o1}^{ref}	300 V	C_4	15000 μF
R_{L2}	1 mΩ	K_{Pi4}	8.38e-2
L_2	10 mH	K_{Pv4}	6.22
C_2	1000 μF	K_{Iv4}	439
R_{Ld2}	0.625 Ω	V_{o4}^{ref}	200 V
K_{Pv2}	7.79e-3	R_{L5}	1 mΩ
K_{Iv2}	0.534	L_5	10mH
V_{o2}^{ref}	250 V	V_5	1000 V
R_{L3}	1 mΩ	K_{Pp5}	6.28e-5
L_3	6.25 mH	K_{Ip5}	3.45e-3
C_3	500 μF	P_{o5}^{ref}	100 kW
ε	0.1		

algorithms are programmed in several TMS320F28335 DSP controllers. The controllers acquire electrical signals generated by the power circuit models in RT-LAB, and send PWM signals to RT-LAB to control the power circuit models. A telescope acquires electrical signals to record the testing waveforms.

This paper modularly designs all of the modules in the DC DPS. Besides, this paper makes each module of *VS*_2, *LOAD*_1, *LOAD*_2, *LOAD*_3, and PCS_{sys} satisfy its own decentralized impedance specification, while changes the port impedance of *VS*_1 for verifying its decentralized impedance specification in different conditions. The detailed parameters of the DC DPS are illustrated by TABLE 1. The upper-case variables are the steady-state components which correspond to the lower-case variables shown in Figure 4.

B. CASE I: CASCADED-VOLTAGE-SOURCES-MULTI-LOADS CASCADED-TYPE DC DPS

In this case, PCS_{sys} does not connect to the DC bus, which means that PCS_{sys} is not included in the DC DPS. Thus, the system is a cascaded-voltage-sources-multi-loads cascaded-type DC DPS. In this condition, the capacity of the DC DPS is $E_{Psys} = 0$kW. In the DC DPS, each power electronic converter works in continuous current mode, whose respective small-signal model has been given by reference [25]. As the formula of port impedance of each module in the DC DPS

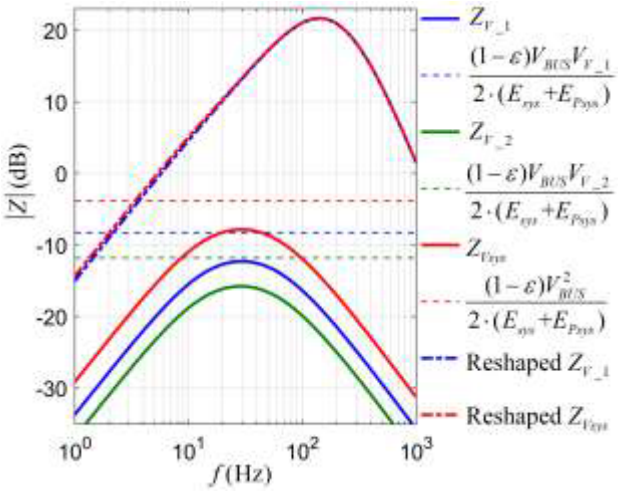

FIGURE 6. Amplitude-frequency characteristic curves of the voltage source modules and the decentralized impedance specifications in the cascaded-voltage-sources-multi-loads cascaded-type DC DPS.

can be referred to reference [20], this paper will plot the port impedance of a module directly.

In the cascaded-voltage-sources-multi-loads cascaded-type DC DPS, the amplitude-frequency characteristic of port impedance of *VS_1* as well as that of *VS_2* are illustrated in Figure 6. If G_C is 0, *VS*_1 satisfies its own decentralized impedance specification defined by (12), as well the same goes for *VS*_2, which causes that the system-level voltage source VS_{sys} obeys the decentralized impedance specification defined by (7). If

$$G_C = G_{C1} = \frac{2.4\times10^2 s^3 + 9.4\times10^5 s^2 + 4.1\times10^8 s + 3\times10^{10}}{2s^3 + 7.5\times10^3 s^2 + 9.5\times10^6 s + 4\times10^9}, \tag{13}$$

the port impedance of *VS*_1 will be changed, and $|Z_{V\_1}|$ will exceeds the limit given by (12). It causes that *VS*_1 does not obey its own port impedance specification.

Plot the Bode diagrams of Z_{Vsys} and Z_{Csys} shown as Figure 7. If G_C is 0, the system-level port impedance Z_{Vsys} satisfies its own specification as well as the system-level port impedance Z_{Csys}, then the cascaded-voltage-sources-multi-loads cascaded-type DC DPS is stable. If $G_C = G_{C1}$, $|Z_{Vsys}|$ is changed, does not satisfy its own specification, and crosses $|Z_{Csys}|$ at the frequency of 13 Hz. Besides, the phase difference $\varphi(T_m) = \varphi(Z_{Vsys}) - \varphi(Z_{Csys})$ at the frequency of 13 Hz exceeds 180°. As a consequence, the DC DPS will be unstable, and one will observe an oscillation of 13 Hz.

The result of hardware-in-loop test shown as Figure 8 corresponds well to the foregoing theoretical analysis. The oscilloscope shows the waveforms of the voltages v_{o1}, v_{o2}, v_{o3}, and v_{o4}. At state I, G_C is 0, and each module in the DC DPS satisfies its decentralized impedance specification defined in (12), which means that the condition of $|Z_{Vsys}(s)| < |Z_{Csys}(s)|$ is satisfied, and that the closed-loop transfer function $H(s)$

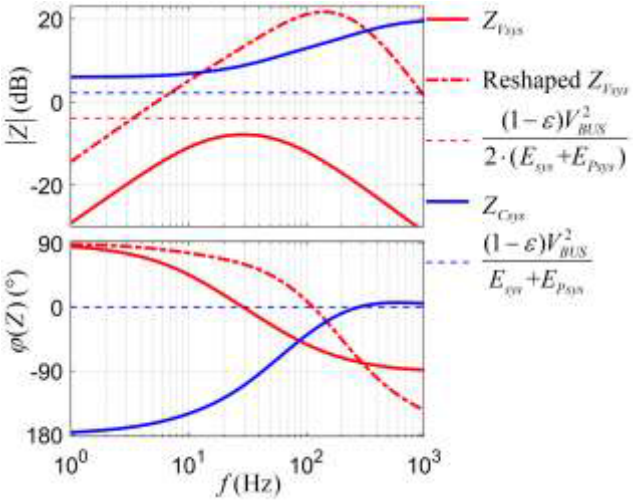

FIGURE 7. Bode diagrams of the system-level port impedances and the decentralized impedance specifications in the cascaded-voltage-sources-multi-loads cascaded-type DC DPS.

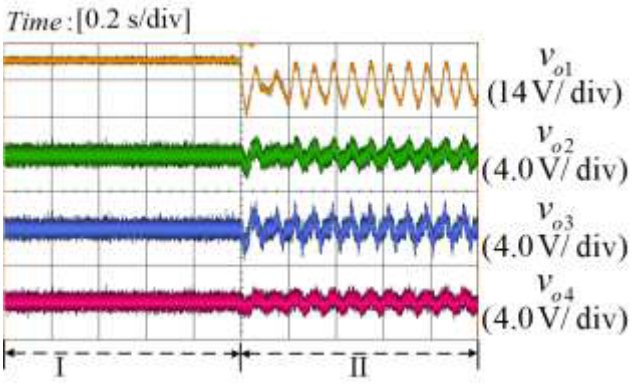

FIGURE 8. Hardware-in-loop test result of the cascaded-voltage-sources-multi-loads cascaded-type DC DPS.

has no right half plane (RHP) pole according to Middlebrook Criterion, thus the cascaded-voltage-sources-multi-loads cascaded-type DC DPS should be stable. As shown in stage I of Figure 8, all of the waveforms of the voltages v_{o1}, v_{o2}, v_{o3}, and v_{o4} are stable, which corresponds well to the theoretical analysis that the cascaded-voltage-sources-multi-loads cascaded-type DC DPS should be stable. At state II, G_C changes into G_{C1}, and VS_1 breaches its impedance specification defined in (12), and the amplitude of its impedance $|Z_{Vsys}|$ crosses $|Z_{Csys}|$ at the frequency of 13 Hz, where the phase difference $\varphi(T_m) = \varphi(Z_{Vsys}) - \varphi(Z_{Csys})$ exceeds 180°. Thus, according to Nyquist Criterion, the cascaded-voltage-sources-multi-loads DC DPS should be unstable, and one should observe an oscillation of 13 Hz. As shown in

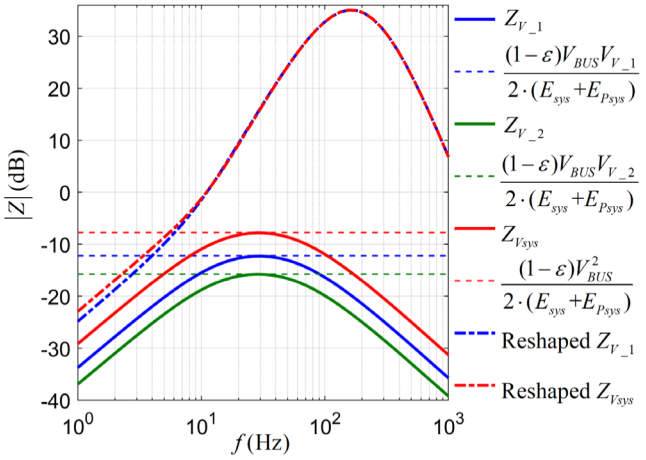

FIGURE 9. Amplitude-frequency characteristic curves of the voltage source modules and the decentralized impedance specifications in the constant-power-source-involved and cascaded-type DC DPS.

stage II of Figure 8, all of the waveforms of the voltages v_{o1}, v_{o2}, v_{o3}, and v_{o4} are unstable, and oscillations of about 13 Hz occur, which corresponds well to the analysis of theory.

To sum up, the waveforms in stage I of Figure 8 verify that the impedance specifications proposed by this paper can ensure the stability of a cascaded-voltage-sources-multi-loads cascaded-type DC DPS, while waveforms in stage II of Figure 8 verify that the theory basis of the proposed method is reasonable.

C. CASE II: CONSTANT-POWER-SOURCE-INVOLVED AND CASCADED-TYPE DC DPS

In this case, PCS_{sys} is connected to the DC bus and is included into the cascaded-type DC DPS for verifying the proposed impedances specifications when a constant power source involved. The capacity of the constant power source PCS_{sys} is designed to $E_{Psys} = 100$kW.

In the constant-power-source-involved and cascaded-type DC DPS, the amplitude-frequency characteristic curve of port impedance of VS_1 as well as of VS_2 are drawn in Figure 9. If G_C is 0, VS_1 satisfies the impedance specification in (12), VS_2 satisfies its own impedance specification at the same time, hereby VS_{sys} obeys the port impedance specification. If (14), as shown at the bottom of the page.

$|Z_{Vsys}|$ will be reshaped and do not satisfy the respective specification in (12).

The Bode diagrams of Z_{Vsys} and Z_{Csys} are plotted in Figure 10. If G_C is 0, the decentralized specification of Z_{Vsys} will be satisfied as well as that of Z_{Csys}, and the stability of the constant-power-source-involved and cascaded-type DC DPS should be ensured. If $G_C = G_{C2}$, $|Z_{Vsys}|$ will overlap

$$G_C = G_{C2} = \frac{1.5\times10^6 s^4 + 5.9\times10^9 s^3 + 2.8\times10^{12} s^2 + 2.7\times10^{14} s + 5.8\times10^{15}}{s^5 + 6.2\times10^3 s^4 + 1.6\times10^7 s^3 + 2\times10^{10} s^2 + 1.2\times10^{13} s + 3.2\times10^{15}}, \tag{14}$$

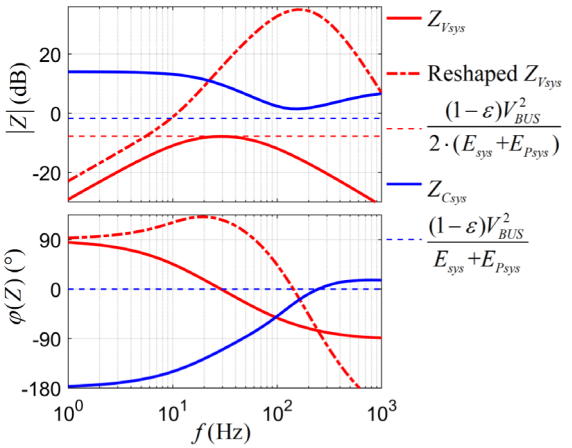

FIGURE 10. Bode diagrams of the system-level port impedances and the decentralized impedance specifications in the constant-power-source-involved and cascaded-type DC DPS.

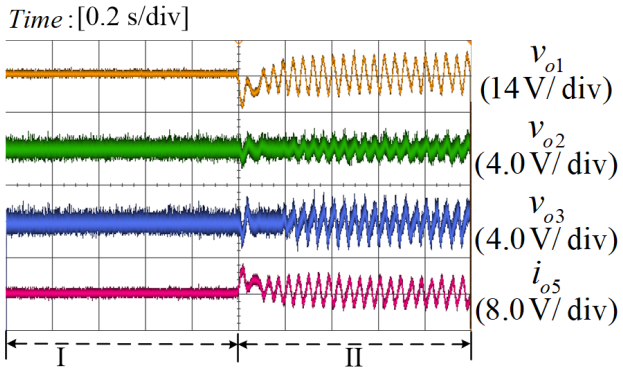

FIGURE 11. Hardware-in-loop test result of the constant-power-source-involved and cascaded-type DC DPS.

with $|Z_{Csys}|$ at the frequency of 22 Hz, where $\varphi(T_m) = \varphi(Z_{Vsys}) - \varphi(Z_{Csys})$ exceeds 180 °. Thus, an oscillation of 22 Hz will occur.

Figure 11 shows the hardware-in-loop test result of this case, where the waveforms of v_{o1}, v_{o2}, v_{o3}, and i_{o5} are recorded. At sate I, G_C is 0, all of the modules in the DPS satisfy the decentralized impedance specifications defined in (12), which means that the condition of $|Z_{Vsys}(s)| < |Z_{Csys}(s)|$ is satisfied, and that the closed-loop transfer function $H(s)$ has no right half plane (RHP) pole according to Middlebrook Criterion, and the constant-power-source-involved and cascaded-type DC DPS should be stable. As shown in stage I of Figure 11, all of the waveforms of v_{o1}, v_{o2}, v_{o3}, and i_{o5} are stable, which corresponds well to the theoretical analysis that the constant-power-source-involved and cascaded-type DC DPS should be stable. At state II, G_C is G_{C2}, VS_1 no longer obeys the decentralized impedance specification defined in (12), and the amplitude of its impedance $|Z_{Vsys}|$ crosses $|Z_{Csys}|$ at the frequency of 22 Hz, where the phase difference $\varphi(T_m) = \varphi(Z_{Vsys}) - \varphi(Z_{Csys})$ exceeds 180°. Thus, according to Nyquist Criterion, the constant-power-source-involved and cascaded-type DC DPS should be unstable, and one should observe an oscillation of 22 Hz. As shown in stage II of Figure 11, all of the waveforms of v_{o1}, v_{o2}, v_{o3}, and i_{o5} are unstable, and oscillations of about 22 Hz are stimulated as the theoretical prediction.

To sum up, the waveforms in stage I of Figure 11 testifies that the impedance specifications of this paper is able to ensure the stability of a constant-power-source-involved and cascaded-type DC DPS, while the waveforms in stage II of Figure 11 verify the rationality of the theory foundation.

IV. CONCLUSION

To ensure the stability of a constant-power-source-involved and cascaded-type DC DPS, this paper defines a time-invariant and decentralized impedance specification for each module in the DC DPS. By the proposed method, one can realize the modular design of the modules in the DC DPS, as well one can guarantee the stability of the DC DPS. The reasonability of the proposed method is illustrated by theoretical analyses, which is further verified by hardware-in-loop tests.

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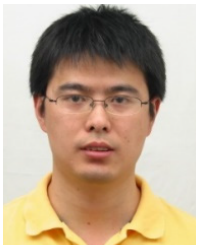

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