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Investigation of a Transistor Clamped T-Type Multilevel H-Bridge Inverter With Inverted Double Reference Single Carrier PWM Technique for Renewable Energy Applications

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ABSTRACT The Multilevel inverters (MLIs) are a new breed of power electronics converters. They are primarily used for the conversion of dc power to ac power. The two-level inverters are conventionally used to obtain ac power, but it requires operating the switches under very high switching frequency. Besides, the two-level inverter necessitates the use of LC filters with the switches operating under high *dv/dt* stress. The MLIs offer the advantage of utilizing several dc voltage sources to generate a stepped ac waveform with the proper arrangement of switches. Investigation of a Transistor Clamped T Type H-Bridge Multilevel Inverter (TC-TT-HB-MLI) with Inverted Double Reference Single Carrier PWM Technique (IDRSCPWM) for Renewable Energy Applications are discussed in this paper. A PV source is taken as an input to the TC-TT-HB-MLI. For different modulation indices like 0.85, 1 and 1.25, the FFT analysis is performed and presented, which corresponds to the variations in the irradiations from solar energy. A single unit of the TC-TT-HB-MLI is extended to a generalized MLI structure named Generalized Transistor Clamped T-Type H-Bridge Multilevel Inverter (GTC-TT-HB-MLI). The significant benefits of GTC-TT-HB-MLI are the multiple numbers of reductions in the switch count, and driver circuit counts for a higher number of MLI levels. Fast Fourier Transform (FFT) analysis is carried out on the MLI output to calculate the total harmonics distortion (THD). The experimental verification is performed using SPARTAN 3E-XCS250E; the gate signals are generated and provided to the switches.

INDEX TERMS Multilevel inverter topology, high switching frequency, double reference, single carrier, pulse width modulation scheme, total harmonics distortion.

I. INTRODUCTION

Ultimatum for energy is getting incremented every day, which is also resulting in an increased requirement of energy generation. Renewable sources are seen as an alternative to the fossil fuel-based non-renewable energy sources. The overexploitation of these sources to meet our daily requirements have put it in a degraded state. Hence there is rapid development in the research to extract power from alternate sources such as PV, wind, tidal, etc. Among them,

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the energy extracted from photovoltaic systems plays a vital role. The energy extracted from a photovoltaic system (PV system) is DC in nature. The DC nature of power from the PV panel is required to be converted into AC power to meet the domestic and industrial power needs. For this, power inverters play a significant role [1]–[10]. Two-level inverters are operated under very high switching frequency, resulting in high dv/dt of output voltage, increased heating up of the switches and higher electromagnetic interferences (EMI) [11], [12]. The multilevel inverters can overcome the drawbacks associated with the two-level inverters in many ways.

With a higher number of MLI levels, a nearly sinusoidal waveform is attained. As the number of MLI levels increase, the THD present in the ac output is reduced. The multilevel inverters can maximize the power and minimize the harmonic contents in the output AC voltage side [13], [14]. The modulation scheme serves the purpose by proper switching on and off the power switches. Diode Clamped MLI, flying capacitor MLI, and Cascaded H-Bridge MLI are three conventional multilevel inverter topologies [15]–[33]. Multilevel inverters are widely used in renewable energy applications, static reactive power compensators and adjustable speed drives [30], [35]–[38].

Diode Clamped MLI (DC-MLI) and Flying Capacitor MLI (FC-MLI) have problems like voltage balancing and dynamic voltage sharing at higher output levels. Thus, among the conventional MLI topologies cascaded H-Bridge configuration is widely accepted due to their modular structure and fault-tolerant capability [34]. The switching pulses for multilevel inverters can be generated by using various modulation techniques. Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), and Selective Harmonic Elimination (SHE-PWM) are the most used modulation techniques [30], [37]–[42]. Further SPWM technique is classified as Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) and Phase Shifted techniques (PS).

A single H-bridge cell generates only a three-level output. A high switching frequency modulation scheme can be employed to generate the MLI output. However, the harmonics distortion in the three-level H-bridge is still high. To improve the THD, the levels in the H-bridge can be increased by cascading several single H-bridge units to achieve a higher number of levels. However, this leads to an increase in the number of switches and gate driver circuits. A better solution is to improve the single H-bridge circuit to generate a five-level output with the use of two additional switches as against four additional switches in case of cascaded H-bridge circuit [43]. Similar work was carried out in the T-type MLI, where a predictive model controller was used in combination with a PI controller which creates a robust control algorithm [44]. In [45], and improved high switching frequency modulation scheme was employed to reduce the THD of the five-level T-type MLI. The work had utilized multi-referenced and dual-carriers to generate the gate pulses. Apart from the implementation of the conventional T-type topology for various applications and modulation schemes, it has also been extended to other MLI topologies. One such hybrid topology is the combination of T-type MLI with cross-connected MLI topology to achieve a higher number of levels with an increase in the number of switches [46]. In [47], a cross switched T-type MLI topology is proposed. Multiple T-type topologies with half-bridge configurations are interconnected with each other to generate a higher number of levels. But as the full-bridge configuration is not used, this topology is not suitable as a single unit which will generate only a three-level output for a Module Integrated Converter (MIC). In [48], a similar half-bridge configuration for a T-type inverter is used for electric vehicle application. The work results in only a three-level output for a bidirectional converter configuration.

The Transistor Clamped T-Type H-Bridge Multilevel Inverter (TC-TT-HB-MLI) is investigated in this paper with Inverted Double Reference Single Carrier PWM Technique (IDRSCPWM) for Renewable Energy Applications and different modulation index. The TC-TT-HB-MLI topology is a modification over the existing T-type topology with a reduced number of switches. The reduction in the number of switches is very much evident with the generalized version of the TC-TT-HB-MLI for a higher number of levels. The TC-TT-HB-MLI topology is highly suitable for photovoltaic applications. The TC-TT-HB-MLI is operated for different variations in the modulation index, which corresponds to the variations in the insolation level from the sun.

In section II, the working principle of the TC-TT-HB-MLI is given. Also, Fourier Series (FS) analysis of multilevel waveform is discussed in detail to calculate the magnitude of harmonics. In Section-III, experimental results and observations for different modulation index are discussed in detail. Section-IV deals with the extension of TC-TT-HB-MLI and comparison of MLI topologies. The conclusion is given in section-V.

II. FIVE-LEVEL TRANSISTOR CLAMPED T-TYPE H-BRIDGE MLI (TC-TT-HB-MLI)

The power circuit of TC-TT-HB-MLI is shown in Fig. 1(a). The power circuit of a five-level Transistor Clamped T-Type H-Bridge Multilevel Inverter (TC-TT-HB-MLI) consists of H-Bridge inverter and an auxiliary circuit. The auxiliary circuit comprised of a power MOSFET switch. The capacitors used 'C_1' *and* 'C_2' act as two input capacitors, share the input voltage is an equal magnitude of $V_{in}/2$. The five-level magnitudes are V_{in}, V_{in} /2, 0, $-V_{in}/2$, and $-V_{in}$. These different magnitudes are obtained proper sequence of the gate pulses to the switches. With the help of five semiconductor switches, the TC-TT-HB-MLI achieves a five-level output. The H-bridge at the end of the MLI topology offers the positive and negative polarity to generate a complete ac waveform.

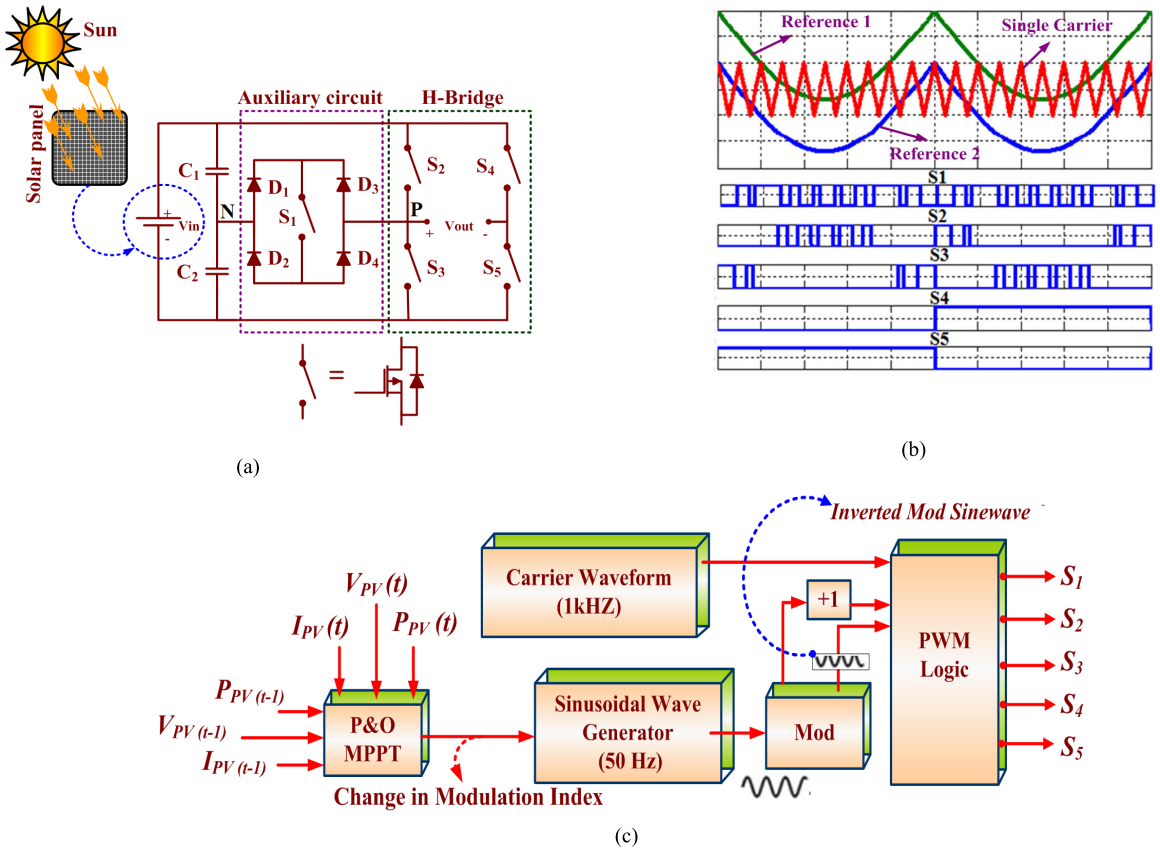

FIGURE 1. (a) Power circuit of five-level TC-TT-HB-MLI (b) Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM) Technique (c) Control logic for Inverted Double Reference Single Carrier Pulse Width Modulation (IDRSCPWM).

A. INVERTED DOUBLE REFERENCE SINGLE CARRIER PULSE WIDTH MODULATION (IDRSCPWM) TECHNIQUE AND MPPT

Fig. 1(b) represents the control logic of the IDRSCPWM technique. Fig. 1(c) depicts the control logic block diagram to obtain PWM pulses for switches of the TC-TT-HB-MLI. The control logic of TC-TT-HB-MLI consists of a Sinusoidal Pulse generator, Modulus Block (Mod), carrier waveform, positive biasing block, PWM Logic block along with maximum power point tracking (MPPT) controller. There is a small amount of loss (losses include semiconductor and conversion loss) while converts photovoltaic energy into electrical energy. Maximum Power Point (MPP) illustrates the maximum power (Product of V_{PP} and I_{PP} where V_{PP} and I_{PP} is the voltage and current at which maximum power is achieved) of Photovoltaic (PV) device. The use of Maximum Power Point Tracking (MPPT) is necessary and compulsory to make sure the output power of the photovoltaic device is maximum (*Pmax*) because the power depends on light, temperature and environmental condition [49]–[52]. To utilize input supply (V_{in}) maximum MPPT is necessary to transfer power to the inverter system. When the photovoltaic voltage (V_{PV}) decreases then photovoltaic current (I_{PV}) will ultimately increase and vice-versa. Maximum power point (MPP) is needed to position by any tracking algorithm because MPP depends upon temperature, irradiance and other environmental parameters [49]–[52]. Furthermore, its position is changed dynamically when these parameters are varied.

Load resistance should be necessary and compulsory match with good possible output resistance ($R_{MPP} = V_{MPP}/I_{MPP}$) to achieve maximum power transfer [52]. The curve of current-voltage (*I-V*) and power-voltage (*P-V*) is depicted in Fig. 2(a). In an inverter system, the Maximum Power Point is tracked by a varying duty cycle of DC-DC converter before feeding power to the inverter or by varying directly modulation index PWM of the inverter system. Several MPPT algorithms are addressed to track the MPP of the photovoltaic system [49]–[53]. An idea to control the modulation index of the controlled signal of the TC-TT-HB-MLI is explained in Fig. 2(b)-2(d).

Consequently, maximum power from the photovoltaic module is extracted by operating inverter near to MPP by varying modulation index (*m*). In this modulation technique two inverted references, one with an offset value added equal to the amplitude of the carrier is compared with the single triangular carrier to obtain the pulses for the power switches S_1-S_3. The switches S_4 and S_5 are operated with a line frequency of 50 Hz. Using equation (1), the modulation index to operate the MLI topology is designed. Where *'Am'* is the amplitude of the reference wave, and *'Ac'* is the amplitude of the triangular carrier wave. The modes of operation of the

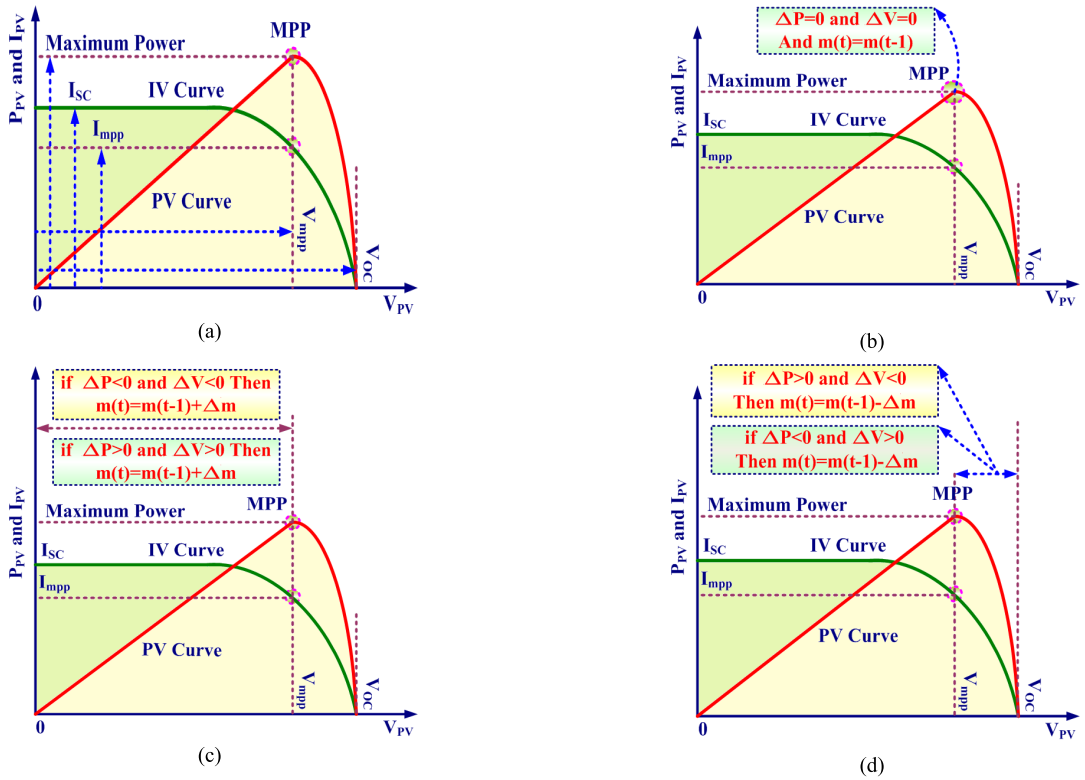

FIGURE 2. (a) P-V and I-V characteristic (a) curve of photovoltaic (PV) inverter system (b) MPPT condition when $\Delta P = 0$ and $\Delta V = 0$ (c) MPPT condition when $\Delta P < 0$, $\Delta V < 0$ and $\Delta P > 0$, $\Delta V > 0$ (d) MPPT condition when $\Delta P > 0$, $\Delta V < 0$ and $\Delta P < 0$, $\Delta V > 0$.

TABLE 1. Modes of operation of TC-TT-HB-MLI.

V_o	S_1	S_2	S_3	S_4	S_5	Voltage across switches				
						V_{PV} (Aux. switch)	S_2	S_3	S_4	S_5
V_{in}	OFF	ON	OFF	OFF	ON	$V_{in}/2$	0	V_{in}	V_{in}	0
$V_{in}/2$	ON	OFF	OFF	OFF	ON	0	$V_{in}/2$	$V_{in}/2$	V_{in}	0
0	OFF	OFF	ON	OFF	ON	$-V_{in}/2$	V_{in}	0	V_{in}	0
0	OFF	ON	OFF	ON	OFF	$V_{in}/2$	0	V_{in}	0	V_{in}
$-V_{in}/2$	ON	OFF	OFF	ON	OFF	0	$V_{in}/2$	$V_{in}/2$	0	V_{in}
$-V_{in}$	ON	OFF	ON	ON	OFF	$-V_{in}/2$	V_{in}	0	0	V_{in}

TC-TT-HB-MLI is shown in Table 1.

$$m = \frac{A_m}{2A_c} \tag{1}$$

$$\left.\begin{aligned} v(t) &= a_v + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_o t) + b_n \sin(2\pi n f_o t) \\ a_v &= \frac{1}{T}\int_{to}^{to+T} v(t)dt, \\ a_n &= \frac{2}{T}\int_{to}^{to+T} v(t)\cos(2\pi n f_o t)dt, \\ b_n &= \frac{2}{T}\int_{to}^{to+T} v(t)\sin(2\pi n f_o t)dt, \end{aligned}\right\} \tag{2}$$

For odd symmetry,

$$\left.\begin{aligned} v(t) &= -v(-t) \\ a_v &= 0, \\ a_n &= 0 \ \ for \ \ all \ \ n \\ b_n &= \frac{4}{T}\int_{0}^{T/2} v(t)\sin(2\pi n f_o t)dt, \end{aligned}\right\} \tag{3}$$

Using Fourier Series, it is possible, characterize periodic function $v(t)$ by infinite addition of cosine and sine functions which are harmonics related [54], [55].

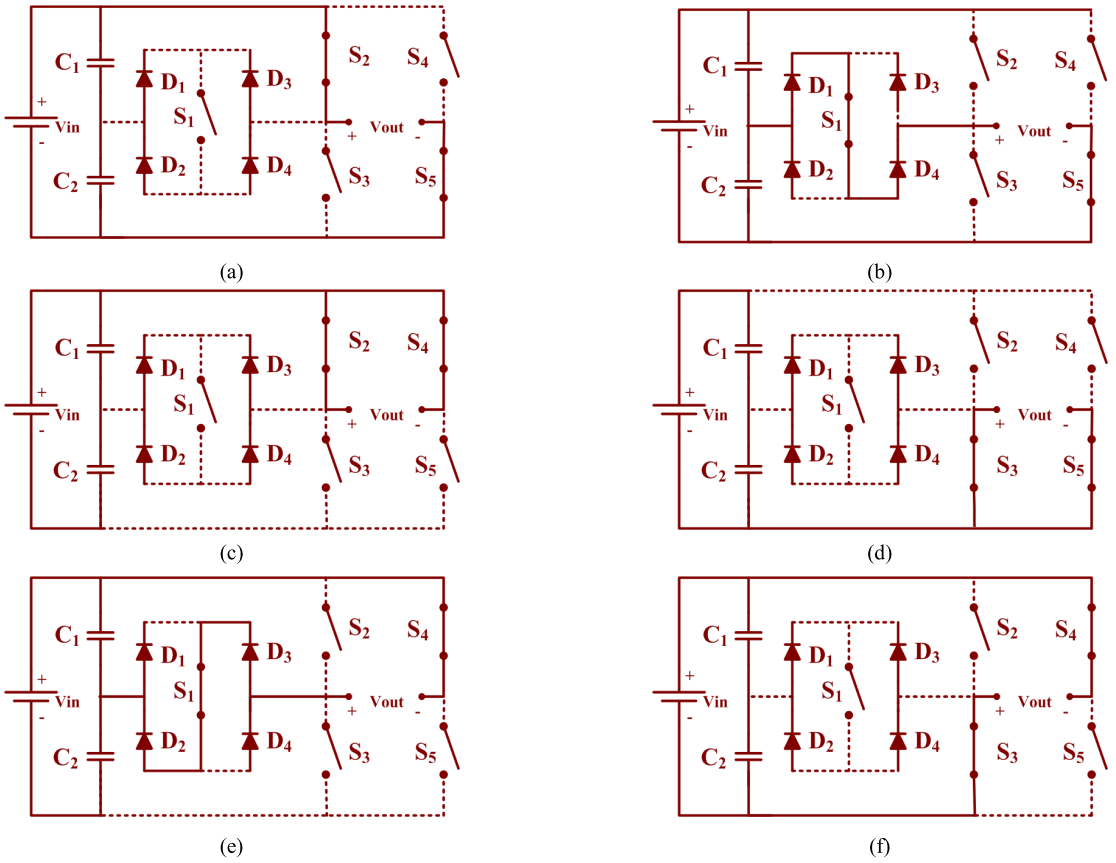

FIGURE 3. Working modes of transistor clamped T-Type H-Bridge multilevel inverter (TC-TT-HB-MLI) (a) LevelV_{in} (b) Level$V_{in}/2$(c) Level zero (d) Level zero (e) Level–$V_{in}/2$(f) Level–V_{in}.

For half-wave symmetry,

$$\left.\begin{aligned} &v(t) = -v(t - T/2)\\ &a_v = 0\\ &a_n = 0,\ for\ n\ even\\ &a_n = \frac{4}{T}\int_0^{T/2} v(t)\cos(2\pi n f_o t)dt,\ for\ n\ odd\\ &b_n = 0,\ for\ n\ even\\ &b_n = \frac{4}{T}\int_0^{T/2} v(t)\sin(2\pi n f_o t)dt,\ for\ n\ odd \end{aligned}\right\} \quad (4)$$

For odd quarter-wave symmetry (with both odd and half-wave symmetry),

$$\left.\begin{aligned} &a_v = 0\\ &a_n = 0,\ for\ \text{all}\ n\\ &b_n = 0,\ for\ n\ even\\ &b_n = \frac{8}{T}\int_0^{T/4} v(t)\sin(2\pi n f_o t)dt,\ for\ n\ odd \end{aligned}\right\} \quad (5)$$

It is possible to write the equation of harmonics in terms of switching angles of the multilevel inverter by using Fourier Series (FS). The output of Multilevel Inverter (MLI) is odd quarter-wave symmetry (the combination of odd and half-wave symmetry), thus for MLI output coefficient is,

$$b_n = \frac{4}{\pi}\int_0^{2\pi/4} v(\frac{\omega t}{2\pi f_o})\sin(n\omega_o t)d\omega t \quad (6)$$

For simplicity, let us consider voltage across each capacitor is V_{in} and θ_1, θ_2, θ_3,.. are switching angles. It is possible to calculate the magnitude of harmonics by using equation (1) to (7).

$$\left.\begin{aligned} b_n &= \frac{4}{\pi}[\int_{\theta_1}^{\theta_2} V_{in}\sin(n\omega t)d(\omega t)\\ &+ \int_{\theta_2}^{\theta_3} 2V_{in}\sin(n\omega t)d(\omega t) + \int_{\theta_3}^{\theta_4} 3V_{in}\sin(n\omega t)d(\omega t) + \cdots\cdots]\\ &= \frac{4}{\pi n}V_{in}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cdots\cdots] \end{aligned}\right\} \quad (7)$$

B. WORKING MODE OF TC-TT-HB-MLI

The various operating modes of the TC-TT-HB-MLI circuit is discussed in this section. The Fig. 3(a) shows the mode

of operation to generate the output voltage V_{in}. The switches S_2 and S_5 are switched ON to obtain the input voltage at the output. From Fig. 3(b), it can be observed that the switching ON the switches S_1 and S_5 generated an output voltage of $V_{in}/2$. A zero-level output is obtained by turning on the switches S_2 and S_4. It is represented in Fig. 3(c). The zero-level output is continued in Fig. 3(d) where the switches S_3 and S_5 are switched ON. It offers a balanced switching of the power switches during zero-level. The negative voltage $-V_{in}/2$ is generated by switching ON S_1 and S_4, as shown in Fig. 3(e). Fig. 3(f) represents the last level $-V_{in}$ is generated by switching ON S_3 and S_4.

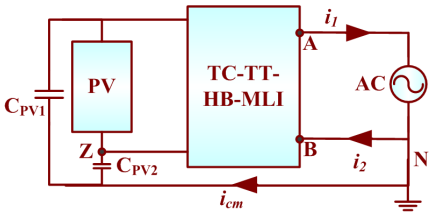

FIGURE 4. Common mode voltage model of the proposed converter model.

C. COMMON MODE VOLTAGE (CMV) ANALYSIS

Fig. 4 shows the Common Mode Voltage (CMV) of the proposed model. The CMV model consists of two stray capacitances from the PV panel C_{PV1} and C_{PV2}, a common point "Z" and a common mode current (i_{cm}) [56]. The common mode current is the difference of current i_1 and i_2. The common mode voltage (VCM) and common mode current (i_{cm}) are given by,

$$V_{CM} = \frac{V_{AZ} + V_{BZ}}{2} \tag{8}$$

$$i_{CM} = i_1 - i_2 \tag{9}$$

Based on (8)-(9), Table 2 is summarized, which shows the common mode voltages for different modes of operations.

TABLE 2. CMV analysis of the TC-TT-HB-MLI.

Level	V_{AZ}	V_{BZ}	V_{CM}
V_{in}	V_{PV}	0	$V_{PV}/2$
$V_{in}/2$	$V_{PV}/2$	0	$V_{PV}/4$
Zero	V_{PV}	V_{PV}	V_{PV}
Zero	0	0	0
$-V_{in}$	$V_{PV}/2$	V_{PV}	$3V_{PV}/2$
$-V_{in}/2$	0	V_{PV}	$V_{PV}/2$

* V_{PV} is the PV voltage

III. EXPERIMENTAL RESULTS AND DISCUSSION

The IDRSCPWM switching logic for the power switches of the TC-TT-HB-MLI is implemented with the help of SPARTAN-3E XCS250E FPGA trainer kit. The clock frequency of the processor is 20MHz. The family architecture of Spartan-3E is composed of the following fundamental blocks:

1. The "Input/Output Blocks (IOBs)" is responsible for collecting the data as input. After carrying out the desired operation, the output block is active to generate signals.
2. The data storage is carried out by "Block RAM" of 18-kbit memory.
3. A variety of logical operation is carried out by the "Configurable Logic Blocks (CLBs)" in the form of latches and flip flops.
4. The "Multiplier Block performs the signal multiplication".
5. "Digital Clock Manager (DCM)" provides the reference for carrying out the various process such as dividing, delaying and phase-shifting of clock signals.

The input for the experiment is taken from PV panels. In peak times each panel can provide a maximum voltage ranging from 32V-33V. For the implementation of a transistor clamped H-Bridge MLI four PV panels are connected in series. The experiment is conducted for modulation indices 0.85, 1 and 1.25 with R and RL-Load. The output results in each case are obtained and investigated with the help of Fluke-43B power quality analyzer. Table 3 specifies the hardware specification details of the TC-TT-HB-MLI.

TABLE 3. Experimental hardware specifications.

Parameters	Specifications
Input Voltage (Vin)	4 PV Panels (Each of 32V, Internal Series Resistance, Rs=0.4ohm, Reference solar irradiation=1000W/m^2, Tref= 25^{o}C, Voc=39.5V, Isc=2.06A)
Capacitors(C_1-C_2)	2200uF
Switching frequency(fs)	1kHz
Power resistor	100Ω,5A (Maximum rating)
Inductor	12mH
MOSFET	IRFP460
Fast Diode	DPG10I400PA
MOSFET Driver IC	TLP250

The experimental output is shown in Fig. 5(a) and Fig. 5(b) for an under-modulation case of m = 0.85 with R-load. It is observed that for R-load obtained power is 114W, 114VA, 8VAR with the 79.7V and 1.442A. The experimental output is shown in Fig. 5(c) and Fig. 5(d) for an under-modulation case of m = 0.85 with RL-load. It is observed that for RL-load obtained power is 104W, 108VA, 31VAR with the 80.1V and 1.343A. For the same under-modulation case, the individual fundamental component of voltage and current is obtained R-load is represented in Fig. 5(e) and Fig. 5(f). It was observed that the fundamental voltage is 78.9V, 49.98 Hz with 32.4% THD. It is also observed that the fundamental current is 1.426A, 49.98 Hz with 32.0% THD. For the same under-modulation case, the individual fundamental component of voltage and current is obtained with RL-load is shown in Fig. 5(g) and Fig. 5(h). It was observed that the fundamental voltage is 79.3V, 49.98 Hz with

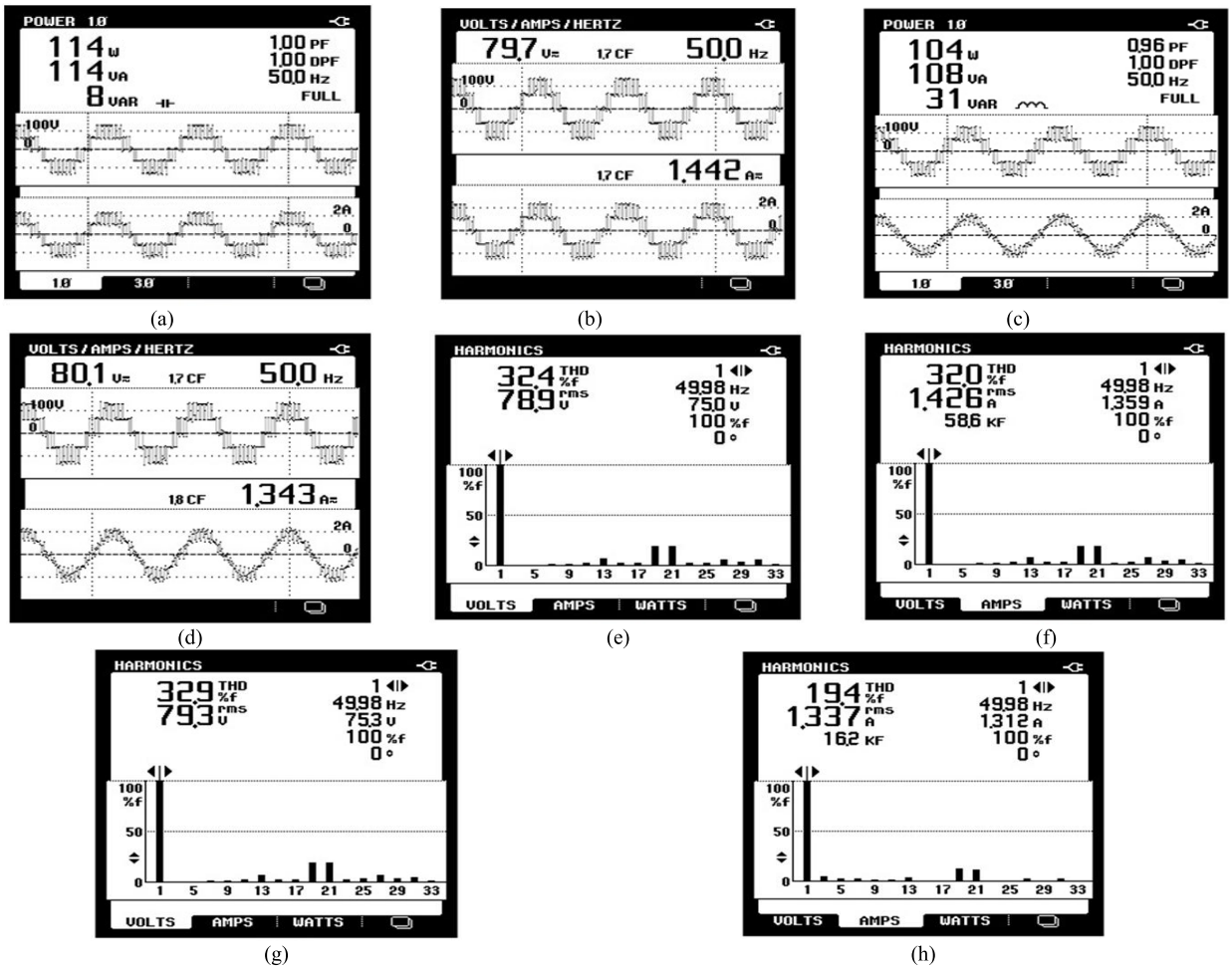

FIGURE 5. Experimental results (a) Output power of TC-TT-HB-MLI for m = 0.85 with R-load. (b) Output voltage and current of TC-TT-HB-MLI for m = 0.85 with R-load. (c) Output power of TC-TT-HB-MLI for m = 0.85 with RL-load (d) Output voltage and current of TC-TT-HB-MLI for m = 0.85 with RL-load (e) 1st harmonics (voltage) or fundamental for m = 0.85 with R-Load. (f) 1st harmonics (current) or fundamental for m = 0.85 with R-load. (g) 1st harmonics (voltage) or fundamental for m = 0.85 with RL-load. (h) 1st harmonics (current) or fundamental for m = 0.85 with RL-load.

32.9% THD. It is also observed that the fundamental current is 1.337A, 49.98 Hz with 19.4% THD.

Fig. 6(a) and Fig. 6(b) shows the output power, output voltage and output current for a modulation index of m = 1 (Unity Modulation) with R-load, respectively. It is observed that for R-load obtained power is 152W, 152VA, 10VAR with the 91.6V and 1.654A. Fig. 6(c) and Fig. 6(d) shows the output power, output voltage and output current for a modulation index of m = 1 (Unity Modulation) with RL-load respectively. It is observed that for RL-load obtained power is 142W, 146VA, 33VAR with the 92.0V and 1.577A. A separately fundamental component of voltage and current is obtained for a modulation index m = 1 and R-load as shown in Fig. 6(e) and Fig. 6(f). It is observed that the fundamental voltage is 91.0V, 49.98 Hz with 22.6% THD. It is also observed that the fundamental current is 1.638A, 49.98 Hz with 22.5% THD. The separately fundamental component of voltage and current is obtained for a modulation index m = 0.85 with RL-load is shown in Fig. 6(g) and Fig. 6(h). It is observed that the fundamental voltage is 91.2V, 49.98 Hz with 23.6% THD. It is also observed that the fundamental current is 1.574A, 49.98 Hz with 13.7% THD.

Fig. 7(a) and Fig. 7(b) shows the output power, output voltage and output current for a modulation index of m = 1.25 (Over Modulation) with R-load respectively. It is observed that for R-load obtained power is 183W, 183VA, 9VAR with the 100.8V and 1.821A. Fig. 7(c) and Fig. 7(d) shows the output power, output voltage and output current for a modulation index of m = 1.25 (Over Modulation) with RL-load respectively. It is observed that for RL-load obtained power is 177W, 180VA, 33VAR with the 101.7Vand 1.769A. Fig. 7(e) shows the fundamental voltage component while Fig. 7(f) shows the fundamental current component with R-load. The modulation index set for this purpose is m = 1.25. It is observed that the fundamental voltage is 100.1V, 49.98 Hz with 18.2% THD. It is also observed that the fundamental current is 1.805A, 49.98 Hz with 18.0% THD. Fig. 7(g) fundamental voltage while Fig. 7(h) shows the fundamental

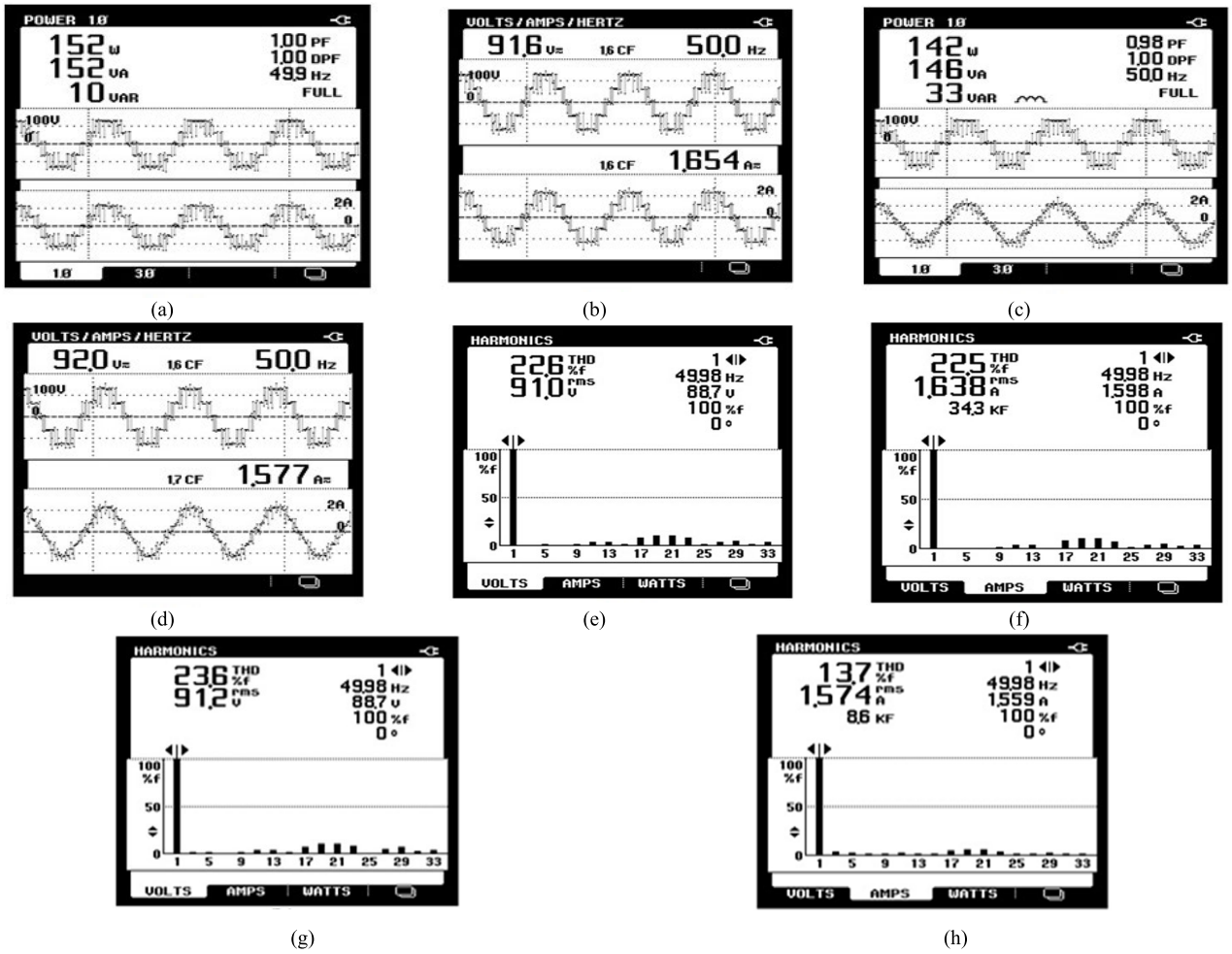

FIGURE 6. Experimental results (a) Output power of TC-TT-HB-MLI for m = 1 with R-load. (b) Output voltage and current of TC-TT-HB-MLI for m = 1 with R-load. (c) The output power of TC-TT-HB-MLI for m = 1 with RL-load (d) Output voltage and current of TC-TT-HB-MLI for m = 1 with RL-load (e) 1st harmonics (voltage) or fundamental for m = 1 with R-Load. (f) 1st harmonics (current) or fundamental for m = 1 with R-Load. (g) 1st harmonics (voltage) or fundamental for m = 1 with RL-load. (h) 1st harmonics (current) or fundamental for m = 1 with RL-load.

TABLE 4. Experimentally observed voltage and current THD.

Modulation Index	R Load		RL Load	
	Voltage THD	Current THD	Voltage THD	Current THD
0.85	32.4	32	32.9	19.4
1	22.6	22.5	23.6	13.7
1.25	18.2	18	18.5	12.5

current component with RL-load. It is observed that the fundamental voltage is 101.1V, 49.98 Hz with 18.5% THD. It is also observed that the fundamental current is 1.760A, 49.98 Hz with 12.5% THD.

The obtained THD results are summarized in Table 4. The graphical analysis is done based on the results obtained from the power quality analyzer (Fluke 43B). Henceforth, the THD, and odd harmonics of both the current and voltage of TC-TT-HB-MLI is performed for modulation indices in 0.85, 1 and 1.25 with R and RL-load. Fig. 8(a) and Fig. 8(b) show the voltage, and current harmonic spectrum analysis with R-load is graphically represented. Fig. 8(c) and Fig. 8(d) show the graph study of voltage and current harmonic spectrum of TC-TT-HB-MLI with RL-load, respectively. Fig. 8(e) and Fig. 8(f) show the Total Harmonic Distortions of both voltage and current of TC-TT-HB-MLI for modulation indices of 0.85, 1 and 1.25 with R and RL load respectively. From the observations, it is found that: The THD content of over modulated (m = 1.25) condition is low for TC-TT-HB-MLI but their odd harmonics (3^{rd}, 5^{th}, 7^{th}, 9^{th}) contents are higher compared to m = 0.85 and m = 1. Using the same input DC supply the over modulated condition can produce more output voltage compared to unity modulated and under modulated condition. TC-TT-HB-MLI can produce

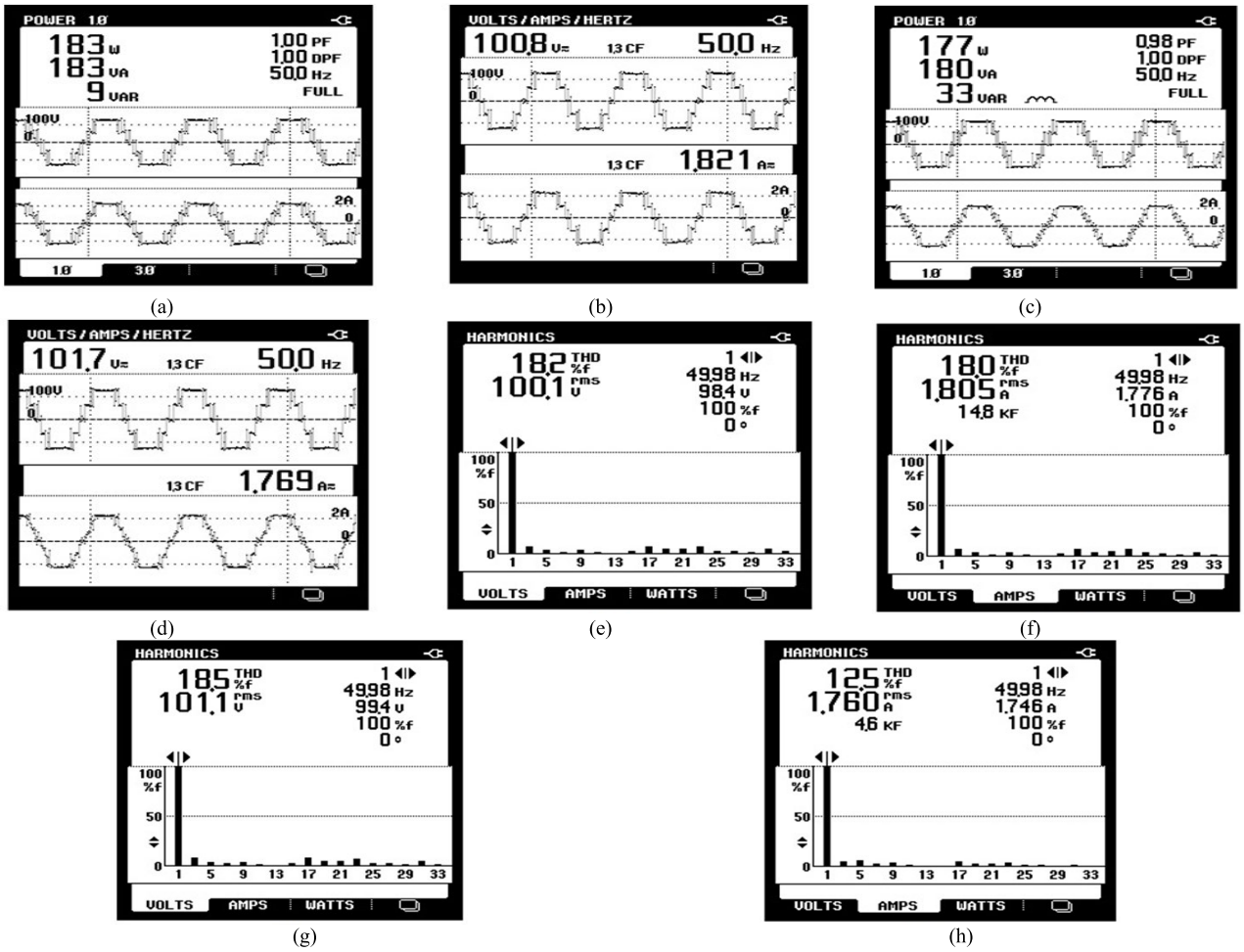

FIGURE 7. Experimental results (a) Output power of TC-TT-HB-MLI for m = 1.25 with R-load. (b) Output voltage and current of TC-TT-HB-MLI for m = 1.25 with R-load. (c) The output power of TC-TT-HB-MLI for m = 1.25 with RL-load (d) Output voltage and current of TC-TT-HB-MLI for m = 1.25 with RL-load (e) 1^{st} harmonics (voltage) or fundamental for m = 1.25 with R-Load. (f) 1^{st} harmonics (current) or fundamental for m = 1.25 with R-Load. (g) 1^{st} harmonics (voltage) or fundamental for m = 1.25 with R-Load. (h) 1^{st} harmonics (current) or fundamental for m = 1.25 with R-Load.

TABLE 5. Experimental results for varying irradiation conditions on TC-TT-HB-MLI.

Solar irradiation (W/m2)	Modulation Index	R-Load					RL-Load				
		rms voltage (V)	rms current (A)	Voltage THD (%)	Current THD (%)	Power Generated (W)	rms voltage (V)	rms current (A)	Voltage THD (%)	Current THD (%)	Power Generated (W)
1000	1.25	100	1.80	18.2	18.0	183	101	1.76	18.5	12.5	177
850	1	91	1.64	22.6	22.5	152	91.2	1.57	23.6	13.7	142
750	0.85	78.9	1.43	32.4	32.0	114	79.3	1.38	32.9	19.4	104

a five-level output with five power switches, whereas conventional cascaded CHB-MLI requires eight power switches, thereby reducing the power circuit complexity.

Table 5 shows the consolidated experimental results for varying irradiation conditions on TC-TT-HB-MLI for R and RL load. As observed from the table, for different irradiation conditions, the modulation index varied from a maximum of 1.25 corresponding to 1000 W/m^2. With a decrease in the solar irradiation condition, the modulation index decreases, which results in a lower output rms voltage, rms current and power generated.

IV. EXTENSION AND GENERALIZED STRUCTURE OF TC-TT-HB-MLI AND COMPARISON

In this section, the extension of TC-TT-HB-MLI named as Generalized TC-TT-HB-MLI (GTC-TT-HB-MLI) is explained, and it is also compared with conventional and recently addressed proposed Multilevel Inverter (MLI).

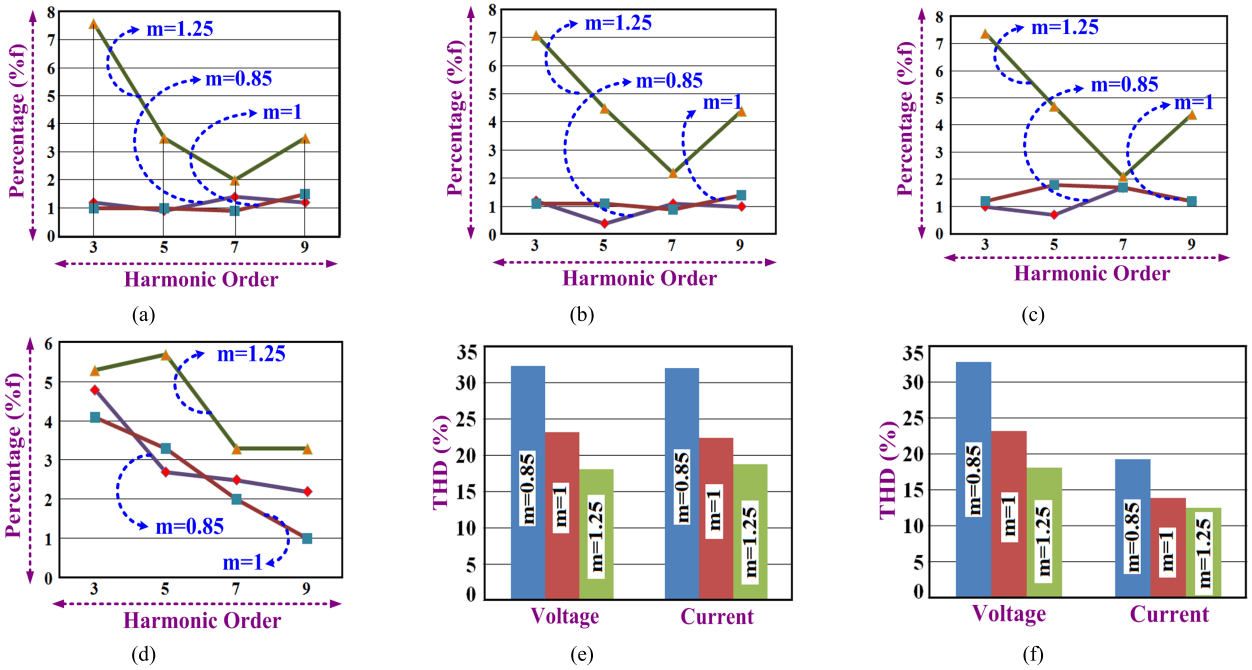

FIGURE 8. Performance (a) Voltage harmonic spectrum analysis with R-Load (b) Current harmonic spectrum analysis with R-Load (c) Voltage harmonic spectrum analysis with RL-load (d) Current harmonic spectrum analysis with RL-load (e) Voltage and Current THD analysis with R-Load (f) Voltage and Current THD analysis with RL-load.

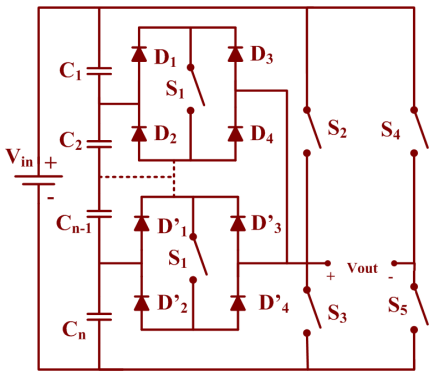

FIGURE 9. Extension and Generalized Transistor Clamped T-Type H-Bridge Multilevel Inverter (G TC-TT-HB-MLI).

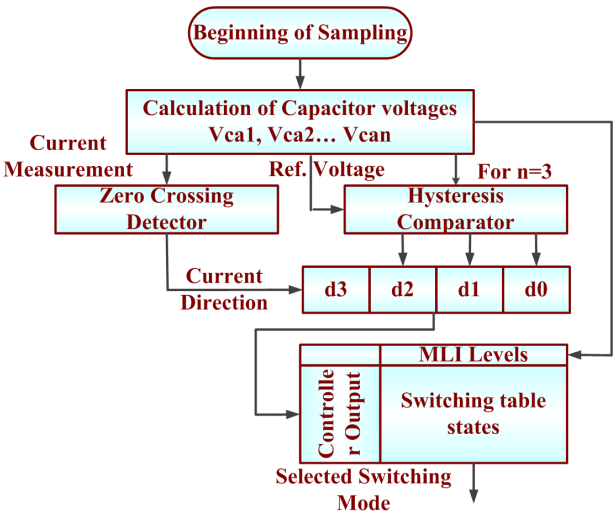

FIGURE 10. Capacitor voltage balancing algorithm for GTC-TT-HB-MLI.

Fig. 9 shows the generalized structure of the TC-TT-HB-MLI for N-Level. For extend the TC-TT-HB-MLI circuit additional, each stage required one controlled switch and four uncontrolled devices along with the capacitor. The GTC-TT-HB-MLI can generate any number of MLI levels with the cascaded operation of TC-TT-HB-MLI with proper capacitor balancing algorithm. For this purpose, for any specific level of GTC-TT-HB-MLI, it is necessary to take into account all the possible switching modes for achieving a particular MLI level. Depending upon the state of charge of the capacitors of each TC-TT-HB-MLI module, the suitable switching mode of all the possible modes can be selected so that the capacitor charging and discharging is balanced. Fig. 10 shows the capacitor voltage balancing algorithm where the status of capacitor charges is taken into account in the first step [57]. This is followed by measuring the current direction to decide upon the positive or negative mode of operation. A hysteresis comparator algorithm is utilized where a reference voltage for each capacitor is set to compare the actual voltage and decide upon the duty cycle of the power switches to charge or discharge the capacitor.

Conventional MLI consist of Diode Clamped Multilevel inverter (DC-MLI), Flying capacitor Multilevel Inverter (FC-MLI) and Cascaded Bridge Multilevel Inverter

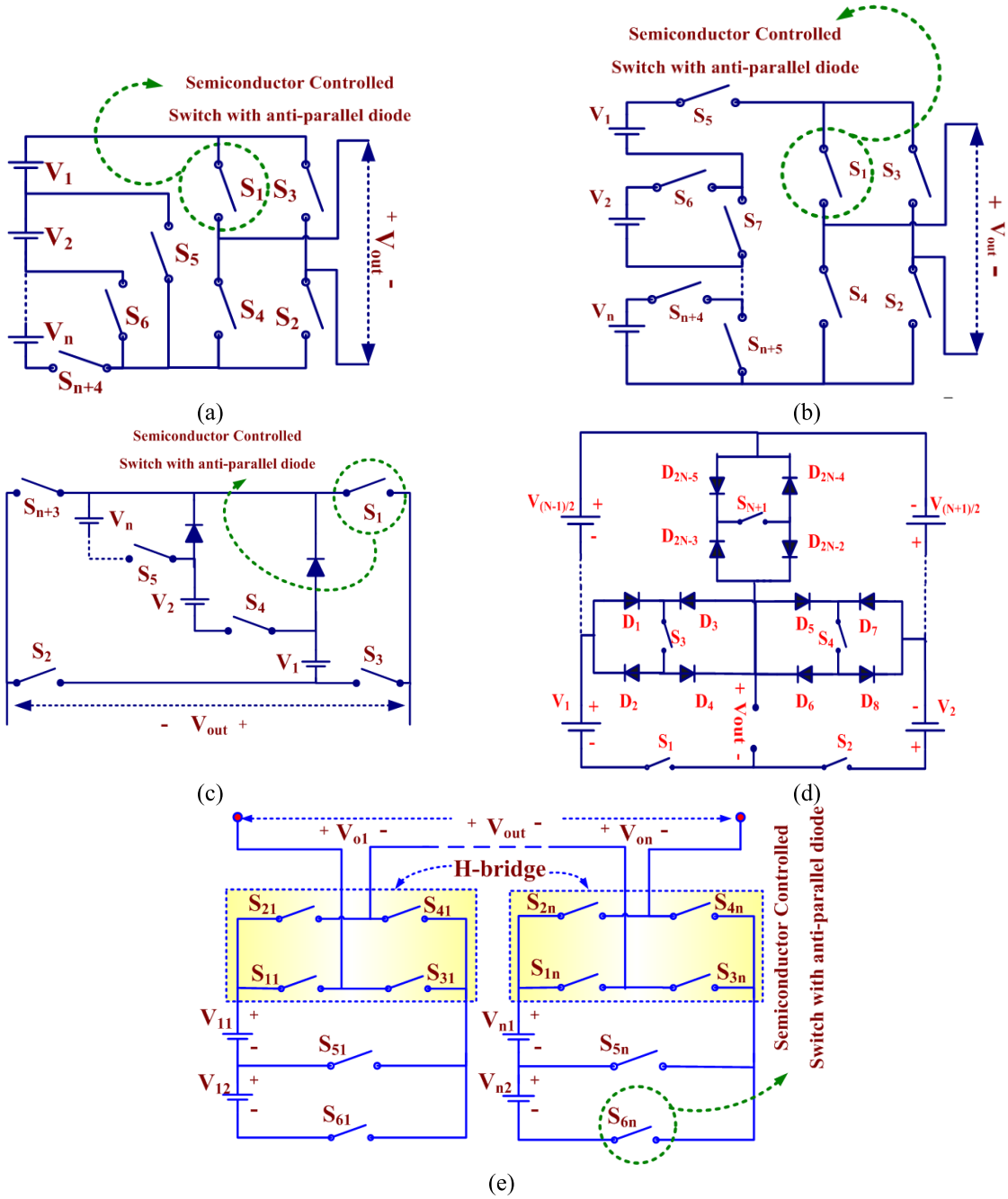

FIGURE 11. Recently addressed multilevel inverter structure (a) MLI proposed in [60] (b) MLI proposed in [61] (c) MLI proposed in [62] (d) MLI proposed in [63] (e) MLI proposed in [64].

(Cascaded MLI or CHB-MLI) [58], [59]. Numerous MLI are addressed in the literature based on the cascaded structure and arrangement of switches [60]–[67]. In [60], [61], seven-level Inverter is proposed with seven and nine switches, respectively. These both structures extended to generate the number of levels by adding n number of sources and additional switches, as shown in Fig. 11(a) and Fig. 11(b). Inverter depicted in Fig. 11(a) required one switch and an additional one voltage source to extend one stage of power circuit (or to add two levels in the output). Similarly, inverter depicted in Fig. 11(b) required two switch and additional one voltage source to extend one stage of the circuit (or to add two levels in the output). In [62], a nine-level inverter is proposed using seven switches, and extended multilevel structure of this inverter is shown in Fig. 11(c). Inverter depicted in Fig. 11(c) required one switch, one diode and additional one voltage source to extend one stage of the circuit (or to add two levels in the output). In [63], a new Multilevel Inverter (MLI) structure is proposed using fewer numbers of switches and its power circuit shown in Fig. 11(d). The noticeable feature of this inverter is that it only generates 3, 7, 11, 15, 19.... number of levels. Inverter depicted in Fig. 11(d) required two

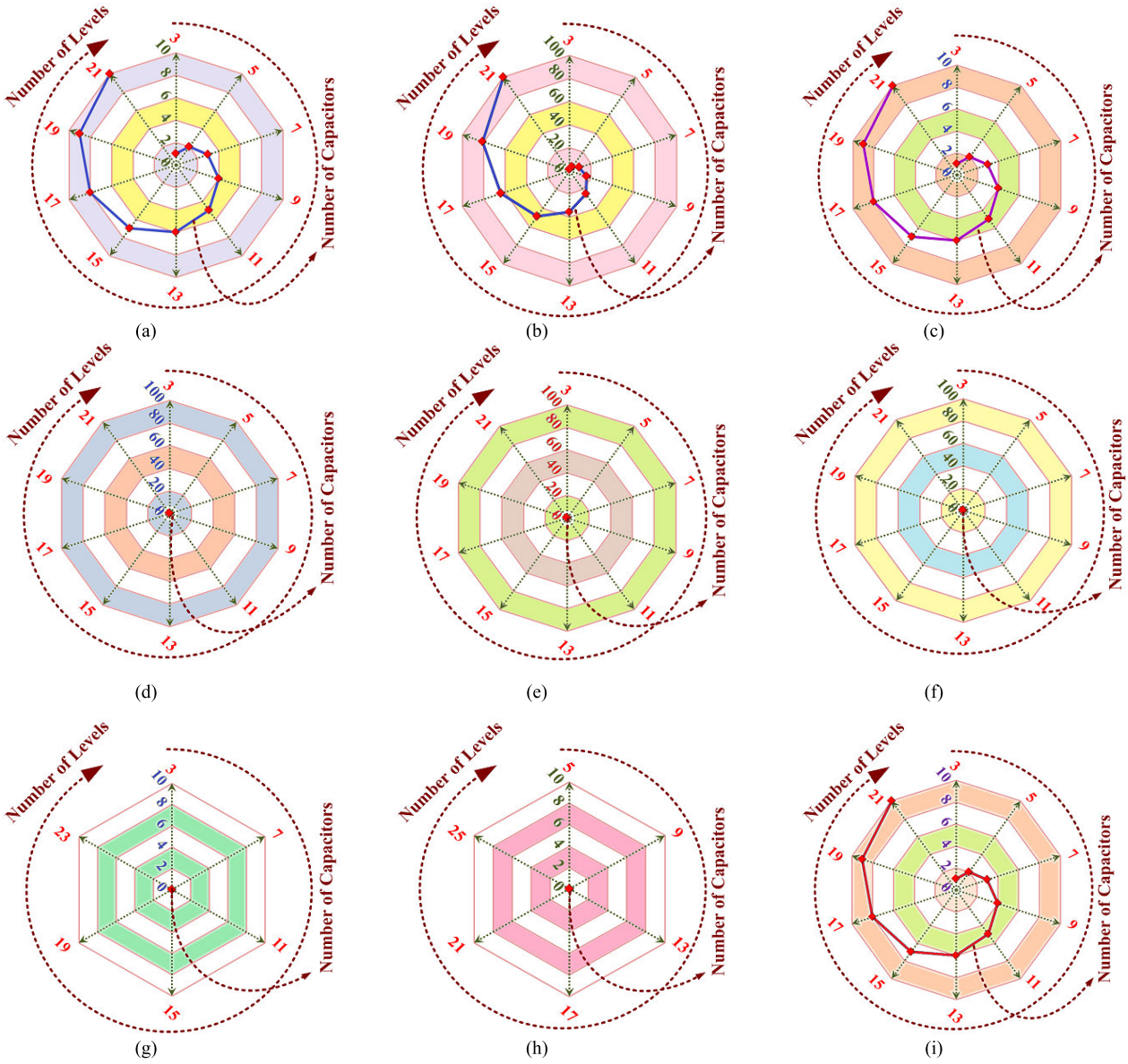

FIGURE 12. Requirement of number of capacitors for Multilevel Inverter (MLI) (a) Diode Clamped MLI or (DC-MLI) (b) Flying Capacitor MLI or (FC-MLI) (c) Cascaded MLI or (CHB-MLI) (d) MLI shown in Figure 11(a) [60] (e) MLI shown in Figure 11(b) [61] (f) MLI shown in Figure 11(c) [62] (g) MLI shown in Figure 11(d) [63] (h) MLI shown in Figure 11(e) [64] (i) GTC-TT-HB-MLI.

switches, eight diodes and additional two voltage sources to extend one stage of the circuit (or to add four levels in the output). In [64], a new cascaded Multilevel Inverter (MLI) is proposed by cascading new primary cell, which consists of additional switches and power circuit of the inverter is shown in Fig. 11(e). The noticeable feature of this inverter is that it only generates 5, 9, 13, 17, 21.... number of levels. For extend this topology (or to add four levels in the output), additional six switches with anti-parallel diodes and two sources are required. In Fig. 12(a)-(i), the requirement of number of capacitors to design conventional MLI, recently addressed MLI [62]–[67] and GTC-TT-HB-MLI is shown graphically as radar plot. First, it is observed that the Flying Capacitor Multilevel Inverter (FC-MLI) required the number of capacitors compared to all discussed multilevel inverter (MLI). Second, it is observed that there is no requirement of the number of capacitors for recently addressed and discussed MLI. Third, it is also observed that GTC-TT-HB-MLI, diode clamped MLI, and conventional cascaded MLI required the same number of capacitors.

In Fig. 13(a)-(i), the requirement of number of diodes to design conventional MLI, recently addressed MLI [62]–[67] and GTC-TT-HB-MLI is shown graphically as radar plot. First, it is observed that Diode Clamped MLI (DC-MLI) required the number of diodes compared to all discussed multilevel inverters. Second, it is also observed that Flying Capacitor MLI (FC-MLI) and conventional cascaded MLI required the same number of diodes. Third, it is

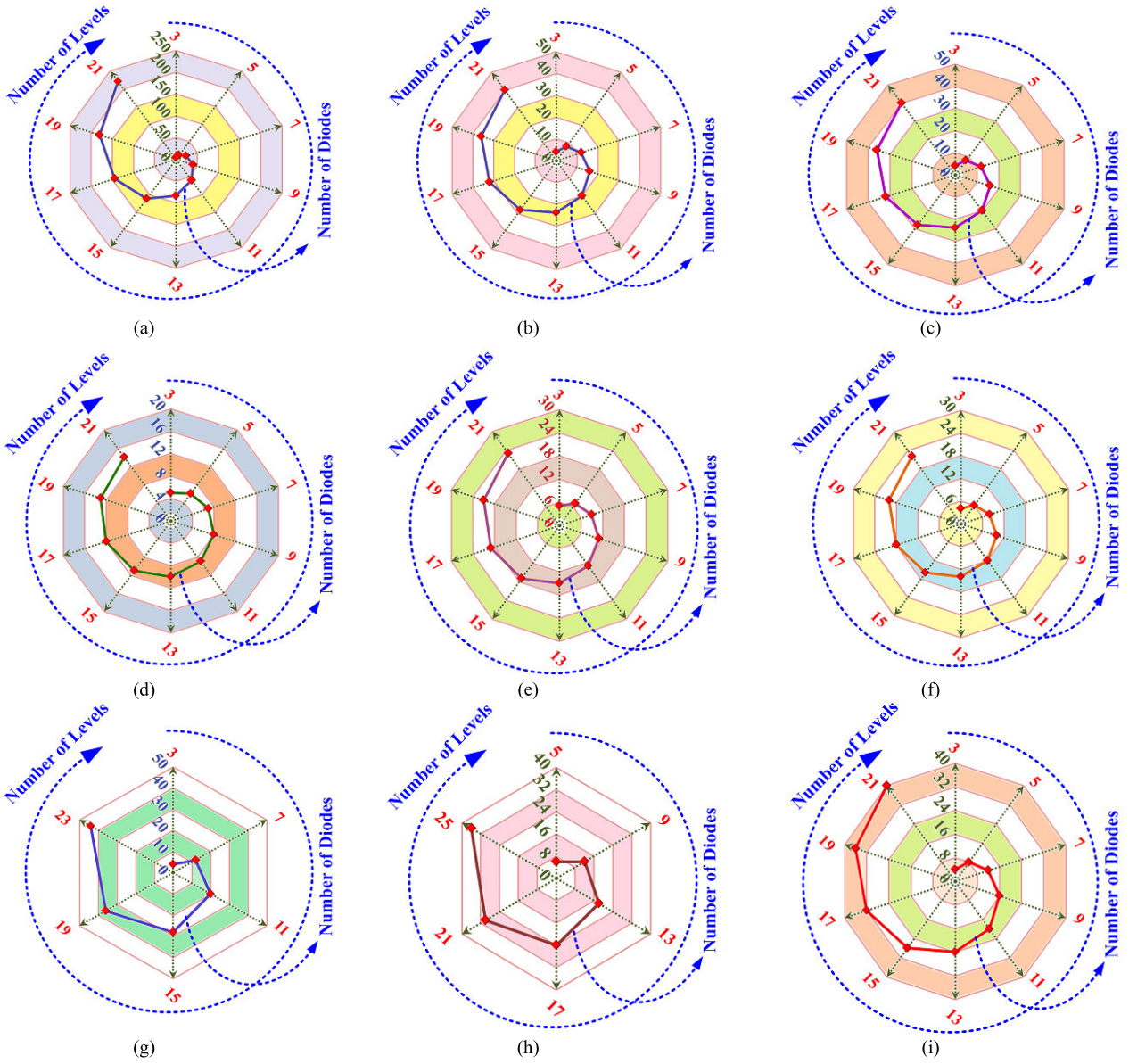

FIGURE 13. Requirement of number of diodes for Multilevel Inverter (MLI) (a) Diode Clamped MLI or (DC-MLI) (b) Flying Capacitor MLI or (FC-MLI) (c) Cascaded MLI or (CHB-MLI) (d) MLI shown in Figure 11(a) [60] (e) MLI shown in Figure 11(b) [61] (f) MLI shown in Figure 11(c) [62] (g) MLI shown in Figure 11(d) [63] (h) MLI shown in Figure 11(e) [64] (i) GTC-TT-HB-MLI.

observed that recently addressed MLI and GTC-TT-HB-MLI required fewer diode count in comparison to conventional MLI recently addressed MLI in [63].

In Fig. 14(a)-(i), the requirement of the number of switches to design conventional MLI, recently addressed MLI [62]–[64], [66], [67] and GTC-TT-HB-MLI is shown graphically like a radar plot. The first and foremost observation is that the GTC-TT-HB-MLI required relatively fewer switches count as compared to the conventional MLI topologies. The second observation is the equal number of components count for all the conventional MLI topologies. The third observation is the fewer switch count requirement by the GTC-TT-HB-MLI in comparison to the recently proposed MLI [62]–[67].

In Fig. 15(a), GTC-TT-HB-MLI is compared with conventional MLI (DC-MLI, FC-MLI, and CHB-MLI). In comparison to a CHB-MLI, the GTC-TT-HB-MLI required a fewer number of sources. The GTC-TT-HB-MLI, DC-MLI and FC-MLI required single source to generate any required MLI levels, but the magnitude of each level equals Vin/N. Moreover, the peak level voltage is equal to the magnitude of that single source. In Fig. 15(b), GTC-TT-HB-MLI is compared with recently addressed MLI [60]–[64]. With a smaller number of components, the GTC-TT-HB-MLI topology is observed better than the recently developed MLI topologies. In Table 6, the requirements of components are tabulated for conventional, recently addressed [60]–[64] and GTC-TT-HB-MLI; where N is the number

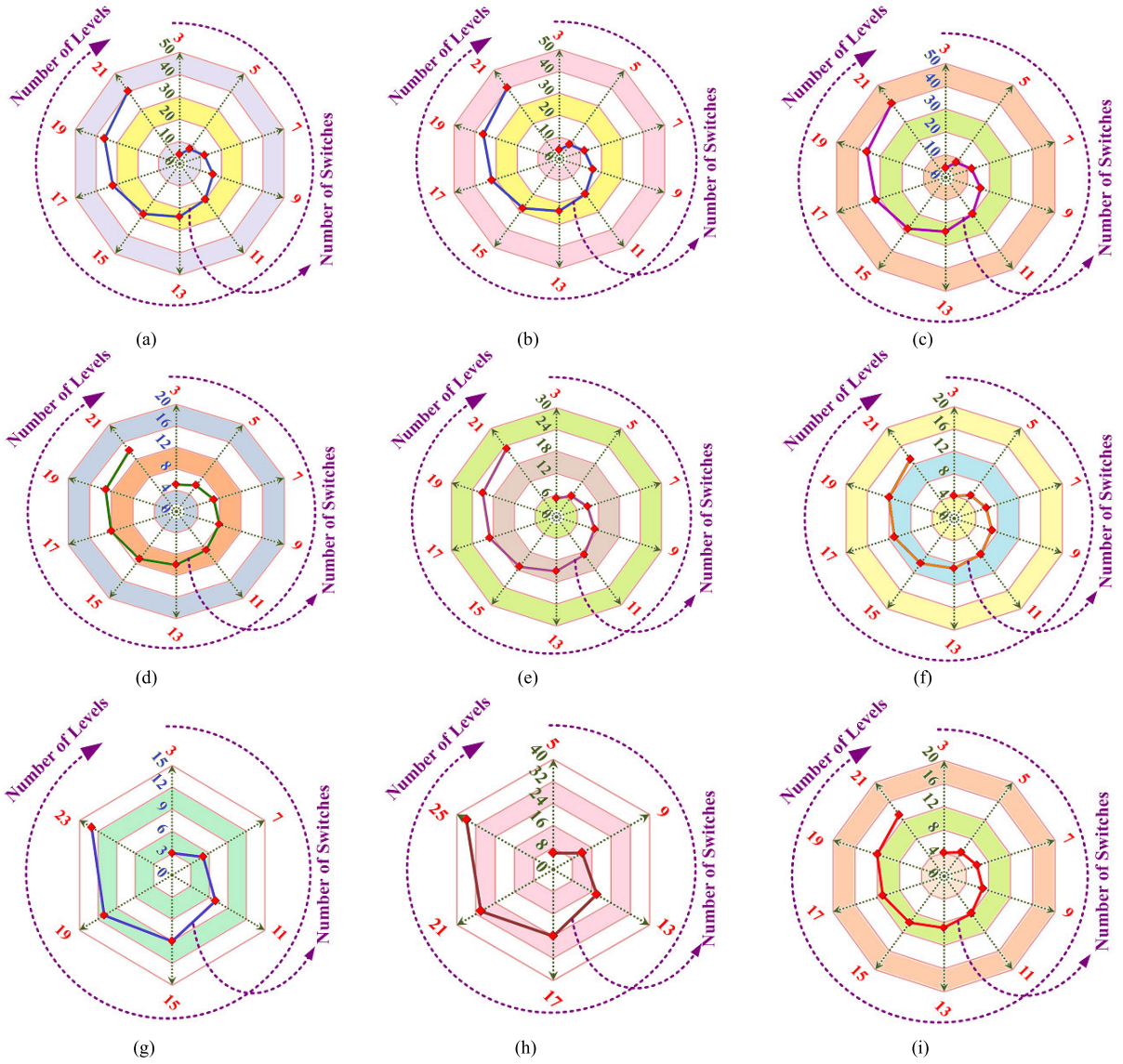

FIGURE 14. Requirement of number of switches for Multilevel Inverter (MLI) (a) Diode Clamped MLI or (DC-MLI) (b) Flying Capacitor MLI or (FC-MLI) (c) Cascaded MLI or (CHB-MLI) (d) MLI shown in Figure 11(a) [60] (e) MLI shown in Figure 11(b) [61] (f) MLI shown in Figure 11(c) [62] (g) MLI shown in Figure 11(d) [63] (h) MLI shown in Figure 11(e) [64] (i) GTC-TT-HB-MLI.

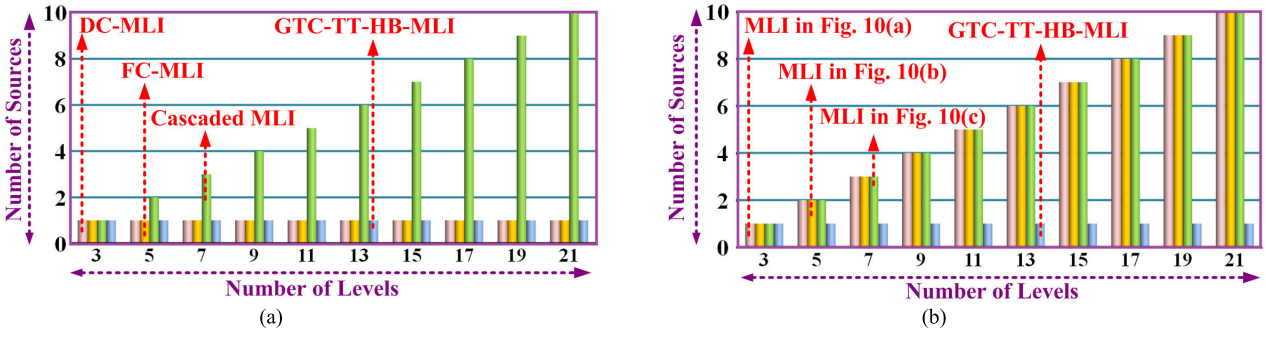

FIGURE 15. (a) Comparison of GTC-TT-HB-MLI with conventional MLI (b) Comparison of GTC-TT-HB-MLI with recently addressed MLI.

of levels. It is observed that in overall, GTC-TT-HB-MLI required a smaller number of components, and hence the circuit of GTC-TT-HB-MLI is cheaper and has less conduction loss.

V. CONCLUSION

A Transistor Clamped T-Type H-Bridge MLI (TC-TT-HB-MLI) was investigated with Inverted Double Reference Single Carrier PWM (IDRSCPWM) technique at differ-

TABLE 6. The requirement of number of capacitors, diodes, switches and source to design MLI structures.

Multilevel Inverter (MLI)	Number of capacitors	Number of diodes	Number of Switches	Number of sources
DC-MLI	0.5(N-1)	$0.5(N^2-1)$	2(N-1)	1
FC-MLI	$0.25(N-1)^2$	2(N-1)	2(N-1)	1
Cascaded MLI	0.5(N-1)	2(N-1)	2(N-1)	0.5(N-1)
MLI shown in Fig. 9(a)	0	0.5(N+7)	0.5(N+7)	0.5(N-1)
MLI shown in Fig. 9(b)	0	N+2	N+2	0.5(N-1)
MLI shown in Fig. 9(c)	0	N+1	0.5(N+5)	0.5(N-1)
MLI shown in Fig. 9(d)	0	2(N-1), N=3, 7, 11...	0.5(N+3), N=3, 7, 11…..	0.5(N+1)
MLI shown in Fig. 9(e)	0	1.5(N-1), N=5, 9, 13…..	1.5(N-1), N=5, 9, 13…..	0.5(N-1)
GTC-TT-HB-MLI	0.5(N-1)	2(N-1)	0.5(N+5)	1

ent modulation index for renewable energy application. Five-level PWM was achieved using an inverted double reference and single-carrier pulse signals; thus, the complexity of control logic was reduced. Fourier Series (FC) equations are discussed in detail to calculate the magnitude of harmonics. The applicability of PV input to the TC-TT-HB-MLI topology, a detailed study of the harmonic spectrum of the TC-TT-HB-MLI was done for modulation indices 0.85, 1 and 1.25 with R and RL load using Fluke-43B power quality analyzer. The extension of the TC-TT-HB-MLI was compared with conventional and recently addressed MLI considering the number of the capacitor, diodes, switches, sources and comparison was graphically shown by radar plot. TC-TT-HB-MLI required fewer component counts in comparison to recently addressed MLI and conventional MLIs. Experimental results proved the real-time justification of the TC-TT-HB-MLI topology with the presented modulation scheme.

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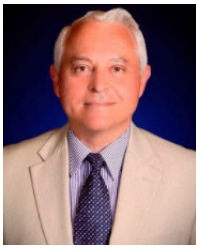

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