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An X/Ku Dual-Band Switch-Free Reconfigurable GaAs LNA MMIC Based on Coupled Line

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ABSTRACT This article presents an X/Ku dual-band switch-free reconfigurable GaAs low-noise amplifier (LNA) realized by inter-stage and output-stage coupled lines. This article is the first switch-free reconfigurable LNA design in the coupled lines structure. After amplified by the broadband drive stage, the input signal is divided into two parallel single-band stages (consists of a high-band stage and a low-band stage) by the proposed inter-stage coupled line. Two split-band signals are combined by the proposed output-stage coupled line into the output port after amplified by the single-band stages. The proposed coupled lines are also included in LNA matching networks. Dual-band operation of the proposed reconfigurable LNA is designed in a 0.15- μ m E-mode GaAs pHEMT process. The fabricated LNA features small-signal gains of 25-25.2/20.1-28 dB, noise figure (NF) of 1.28-1.41/1.23-1.51 dB, and output 1-dB compression point of 0.5-1.7/2.2-5 dBm over 8-10/12-20 GHz, while consuming 76/91 mA of dc current, with a size of 2.0 × 1.8 mm².

INDEX TERMS Coupled line, gallium arsenide (GaAs), low-noise amplifier (LNA), monolithic microwave integrated circuit (MMIC), multi-band.

I. INTRODUCTION

As one of the most critical active components, low noise amplifiers (LNAs) are highly demanded in modern active phased array systems such as multi-standard and multi-band transceivers [1]. To expand the dynamic range and improve the sensitivity of a receiver system, we expect to achieve low noise figure (NF), reasonable gain, high linearity as well as low power consumption for LNAs, which further introduces challenges on LNAs design [2]. In recent decades, extensive researches have been carried out on wideband LNAs. Distributed amplifier (DA) topology is most promising to be applied in an ultra-wideband LNA design [3]–[8]. Unfortunately, DA is not preferable in many situations for its relatively high NF, large chip size, and low unity gain [2]. Many other bandwidth enhancement techniques have also been presented in [9]-[15]. These proposed techniques can extend the bandwidth but also lead to the degradation of other RF performance [13]. Furthermore, the sensitivity of a receiver system with wideband LNAs may degrade significantly because the wideband LNAs amplify the desired signals as well as unwanted signals simultaneously.

Another approach to developing wideband receiver systems with good interference rejection is using reconfigurable LNAs. Many multi-band amplifiers configurations have been presented in the literature [16]-[22]. In [16], a 1.9-2.4 GHz reconfigurable LNA with a continuous tunable input matching network is proposed by utilizing tunable inductors. [17] reports a 2.4-5.4 GHz reconfigurable LNA with a broadband input stage and a band-selective stage using a multi-tap switching inductor and varactors. A reconfigurable multimode LNA employing a switched multi-tap transformer in the input matching network has been proposed in [18]. However, the tunable inductors, varactors, and RF switches mentioned above usually need extra power supplies and cannot be easily implemented at high frequencies for its associated loss. A 6-18 GHz switchless dual-band, dual-mode power amplifier (PA) has been reported in [19] using a coupled-line-based diplexer, which is similar to the coupled lines used in this article.

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In this article, an X/Ku dual-band switch-free reconfigurable LNA is presented. The reconfigurable feature is realized by the inter-stage and output-stage coupled lines, which are also included in the LNA matching networks. The proposed reconfigurable LNA has been fabricated using WIN 0.15- μ m enhancement-mode (E-mode) GaAs process. The die area of the proposed MMIC LNA is 2.0 × 1.8 mm², including all RF and DC power pads. With the frequency reconfigurable capability, the LNA exhibits 25-25.2/20.1-28 dB small-signal gain, 1.28-1.41/1.23-1.5 dB NF, and output 1-dB compression point of 0.5-1.7/2.2-5 dBm over 8-10/12-20 GHz.

This article is organized as follows. Section II introduces the theoretical analysis and reconfigurable mechanism of the proposed microstrip coupled lines. Section III presents the detailed circuit design of the proposed reconfigurable LNA. Measurement results of the proposed reconfigurable LNA are presented in Section IV, followed by a conclusion in Section V.

II. THEORETICAL ANALYSIS OF THE PROPOSED COUPLED LINES

The reconfigurable feature of the proposed dual-band LNA is realized by the inter-stage and output-stage coupled lines. To better understand the mechanism of the dual-band operation of the proposed coupled lines, an analysis of a conventional coupled microstrip line is introduced. Such a line is shown in Fig. 1(a).

In a conventional coupled line structure, the load impedance Z_{load} is assumed to be identical to the characteristic impedance Z_0 of the coupled-line. In this case, the output voltage of the coupled port (port 3) and through port (port 2) as a function of the input voltage V_{in} can be given as [23]:

$$V_{through} = V_{in} \cdot \frac{\sqrt{1 - K^2}}{\sqrt{1 - K^2}\cos\theta + j\sin\theta} = T \cdot V_{in} \quad (1)$$

$$V_{coupled} = V_{in} \cdot \frac{jK\sin\theta}{\sqrt{1 - K^2}\cos\theta + j\sin\theta} = C \cdot V_{in} \quad (2)$$

where

$$T = \frac{\sqrt{1 - K^2}}{\sqrt{1 - K^2}\cos\theta + j\sin\theta}$$
$$C = \frac{jK\sin\theta}{\sqrt{1 - K^2}\cos\theta + j\sin\theta}$$

Voltage coupling factor of port 3 as a function of the coupling coefficient, K and electrical length, θ can be given by:

$$20 \lg |C| = 20 \lg \left| \frac{jK\sin\theta}{\sqrt{1 - K^2\cos\theta + j\sin\theta}} \right|$$
(3)

K is the coupling coefficient of the coupled line, and θ is the electrical length of the coupled line. From (1) and (2), we can see that at very low frequencies or very short line length ($\theta \ll \pi/2$), virtually all input power is transmitted to port 2, with none being coupled to port 3. For $\theta = \pi/2$, the first maximum coupled power transmitted to port 3 is







FIGURE 2. Coupled power of coupled line A.

shown in Fig. 2. For K = 0.7, we can see that the maximum coupled power is approximately -3 dB with a long-coupled line ($\theta = \pi/2$). For this reason, the conventional coupled line structure in Fig. 1(a) may not be applicable in the proposed LNA.

A modified structure of the coupled line is shown in Fig. 1(b). The isolated port (port 4) is grounded. For ideal



FIGURE 3. Coupled power of the proposed coupled line B for high-band operation.

high-band frequencies operation, the shunt capacitance C_1 at the through port (port 2) performs a short circuit. For the low-band frequencies operation, the shunt capacitance C_1 is absorbed in the input impedance matching network of the low-band LNA. The output signal at the through port is reflected with a 180° phase shift and enters the coupled line again. Then the signal is coupled to the isolated port and reflected with a 180° phase shift and comes out of the coupled port (port 3) with the original coupled signal eventually. The output voltage of isolated port (port 4) and coupled port (port 3) as a function of the input voltage V_{in} can be given by:

$$V_4^- = C \cdot V_2^+ = C \cdot \Gamma \cdot V_2^- = C \cdot \Gamma \cdot T \cdot V_{in}$$
(4)
$$V_4^- = C \cdot V_2 + T \cdot V_2^+ = C \cdot V_2 + T \cdot \Gamma \cdot V_2^-$$

$$= C \cdot V_{in} + C \cdot T^2 \cdot V_{in}$$
(5)

Coupled power of port 3 as a function of the coupling coefficient, K and electrical length, θ can be given by:

$$20 \lg \left| \frac{V_3^-}{V_{in}} \right| = 20 \lg \left| C + C \cdot T^2 \right| \tag{6}$$

In (5), we can see that the eventually coupled signal coming out of the coupled port consists of two parts: $C \cdot V_{in}$ and $C \cdot T^2 \cdot V_{in}$. The phase difference between the two parts is identical to the double electrical length of the coupled line. As shown in Fig. 3, when the electrical length of the coupled line is $\lambda/4$, the phase difference between two parts of the coupled power is 180°, then the minimum coupled power is obtained.

Fig. 3 illustrates the coupled power in port 3 of the coupled line shown in Fig. 1(b) according to *K*, coupling coefficient of the coupled line. For a definite *K*, a maximum coupled power can be obtained when the coupled line has a $30^{\circ} \sim 45^{\circ}$ or $135^{\circ} \sim 150^{\circ}$ electrical length. When K = 0.7, the maximum coupled power can be obtained is approximately -4 dB and is not sufficient to be used in the inter-stage of the LNA. The reason for the insufficient coupled power lies in the phase difference between $C \cdot V_{in}$ and $C \cdot T^2 \cdot V_{in}$, the two parts of the coupled power. To tackle this problem, we added a shunt capacitance C_2 to the isolated port to make up for the phase difference between two parts of the coupled power.

Another possible inter-stage coupled line structure is shown in Fig. 1(c). In this structure, the coupled port



FIGURE 4. (a) Coupled power of the proposed coupled line C according to different coupling coefficients for high band operation. (b) Coupled power of the proposed coupled line C according to different electrical length for high band operation.

(port 3) is grounded, and coupled power comes out of the isolated port. The output voltage of port 3 and port 4 as a function of the input voltage V_{in} can be given by:

$$V_{3}^{-} = C \cdot V_{1}^{+} = C \cdot V_{in}$$

$$V_{4}^{-} = V_{3}^{+} \cdot T + V_{2}^{+} \cdot C$$

$$= C \cdot T \cdot \Gamma \cdot V_{in} + C \cdot T \cdot \Gamma \cdot V_{in}$$

$$= -2 \cdot C \cdot T \cdot V_{in}$$
(8)

For ideal high-band frequencies operation, the through port (port 2) and coupled port (port 3) perform short circuits. The output signal at the through port is reflected with a 180° phase shift, enters the coupled line, and comes out of the isolated port (port 4). The coupled signal at the coupled port is reflected with a 180° phase shift, and comes out of the isolated port finally. From (8), we can see that the eventual signal at the isolated port consists of two parts: output signal at the through port and coupled signal at the coupled port. Moreover, the two parts are in phase.

The output coupled power of port 4 as a function of the coupling coefficient, K and electrical length, θ is given by:

$$20 \lg \left| \frac{V_4^-}{V_{in}} \right| = 20 \lg \left| \frac{2K\sqrt{1 - K^2}\sin\theta}{1 - K^2\cos^2\theta} \right| \tag{9}$$

Specially, for $\theta = 90^{\circ}$, coupled power can be given by:

$$20 \lg \left| \frac{V_4^-}{V_{in}} \right| = 20 \lg \left(2K\sqrt{1 - K^2} \right)$$
(10)

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FIGURE 5. Inter-stage coupled line B.



Fig. 4(a) and Fig. 4(b) demonstrate the coupled power of the coupled line C shown in Fig. 1(c) according to different coupling coefficient, K and electrical length, θ of the coupled line. From Fig. 4(a), for a constant θ , we can see that the coupled power increases to the peak and then decreases as K increases. When θ rises, the value of K needed to achieve the maximum coupled power is smaller. For K is 0.58, the maximum coupled power can be obtained is approximately -0.35 dB when θ is 90°.

Fig. 5(a) is a circuit schematic of the proposed coupled line B. The length of the coupled line is 600 μ m with 30° ~ 40° electrical length over 12-18 GHz. Width and space are 7 μ m and 5 μ m with K, the coupling coefficient is 0.58, approximately. A shunt capacitance of $C_2 = 173$ fF is added to the isolated port to increase coupled power. Fig. 5(b) shows the simulation results of the proposed coupled line. Over 14-20 GHz, simulation results show that coupled power is approximately -2 dB, which is about 3 dB higher than analytical results shown in Fig. 3 due to the elimination of the phase difference between the two coupled power paths. Thus, the proposed coupled line shown in Fig. 5 can be applied in the inter-stage of the reconfigurable LNA.

Fig. 6(a) is a circuit schematic of the proposed coupled line C in Fig. 1(c). Length, width, and space between coupled lines in Fig. 1(b) and (c) are identical. A shunt capacitance of $C_3 = 0.3$ pF is added to the isolated port to increase coupled power. Fig. 6(b) shows the simulation results of the proposed coupled line C. Simulation results show that coupled power is approximately -1.8 dB over 12-18 GHz. It can be found that the coupled power of the two coupled lines shown



FIGURE 7. Output-stage coupled line.



FIGURE 8. Topology of the proposed reconfigurable LNA.

in Fig. 1(b) and (c) is comparable. Considering the convenience of layout, coupled line B showed in Fig. 1(b) is finally chosen as the inter-stage coupled line.

Schematic and simulation results of the output-stage coupled line are presented in Fig. 7(a) and (b). It's a symmetric structure of the inter-stage coupled line B with optimized C_2 and width of the coupled line. Insertion loss is less than 2 dB over 8-12 /14-20 GHz.

III. CIRCUIT DESIGN

The topology of the proposed dual-band switch-free reconfigurable LNA is shown in Fig. 8. The LNA consists of a broadband drive stage, single-band stages (high-band stage and low-band stage), and inter-stage/output-stage coupled-lines. All transistors in the proposed LNA are designed in commonsource (CS) architectures. Inductive source degeneration is used to achieve simultaneous NF and impedance matching [24]. Moreover, source inductance can help improve the stability of a transistor. The inductances are implemented via long bent transmission lines to achieve a compact chip area at the cost of a little more insertion loss. Instead of quarterwave long transformers which are usually used as bias circuits to block RF signal, narrow long bent transmission lines and bypass capacitors are used as bias circuits of the proposed LNA to behave as short circuits within the design bandwidth and reduce chip area. Circuit designs of the broadband drivestage and single-band stages are detailed as follows.

A. DESIGN OF THE BROADBAND DRIVE STAGE

The broadband drive stage plays a decisive role in the input matching and noise performance of the reconfigurable LNA. Inductive source degeneration is used to bring the optimum impedance for minimum NF close to the complex conjugate of input impedance. Therefore low NF and input impedance matching can be guaranteed simultaneously. Broadband input matching operation is achieved based on



FIGURE 9. Simulated performance of the broadband drive stage.



FIGURE 10. Simulated performance of the high-band stage.

 π -type networks. The broadband drive stage is composed of two cascaded CS 4 × 50 μ m transistors. The two transistors are biased at low noise region and operate at V_{ds1} of 2.5 V, V_{gs1} of 0.6 V with drain current I_{ds1} of 60 mA. Fig. 9 illustrates simulation results of the broadband drive stage. The broadband drive stage exhibits a small-signal gain of 11-23 dB, a noise figure of 0.8-1.0 dB, reverse isolation of 20-35 dB with input and output reflection coefficient less than -10 dB from 8-20 GHz.

B. DESIGN OF THE TWO SINGLE-BAND LNAS

From the simulation results of the broadband drive stage, it can be found that gain variation is 12 dB from 8 to 20 GHz. In order to maintain good gain flatness in all-band mode operation, the high-band stage consists of two transistors and the low-band stage consists of one transistor. Transistors size used in high-band and low-band stages is $2 \times 50 \ \mu$ m. Transistors are operated at V_{ds2}/V_{ds3} of 2.5 V, V_{gs2}/V_{gs3} of 0.6 V with drain current I_{ds2}/I_{ds3} of 31/15.8 mA. Fig. 10 presents simulation results of the high-band stage. The high-band stage exhibits a 15 dB small-signal gain, a noise figure of 1.0-2.0 dB, reverse isolation larger than 25 dB with input and output reflection coefficient less than -5 dB from 14-20 GHz. Simulation results of the low-band stage are shown in Fig. 11. The low-band stage presents a small-signal gain of 7-8 dB, a noise figure of 1.0-1.6 dB, reverse isolation larger than 15 dB from 8-12 GHz.

Even though every transistor is unconditionally stable, instabilities may still occur due to possible oscillation loops in the complex structure of the multi-device amplifier or due to the device's nonlinear behavior. Therefore, A R-C resistive



FIGURE 11. Simulated performance of the low-band stage.

TABLE 1. Drain voltages states of single-band transistors.

Band	V _{d2}	V _{d3}	Total current		
8-10 GHz	2.5 V	0 V	76 mA		
12-20 GHz	0 V	2.5 V	91 mA		
8-20 GHz	2.5 V	2.5 V	107 mA		

TABLE 2. Main parameters of reconfigurable LNA.

Q1	Q2	Q3	Q4	Q5
4×50 μm	4×50 μm	2×50 μm	2×50 μm	2×50 μm
W1	L _{s1}	L _{s2}	L _{s3}	L _{s4}
10 µm	210 µm	300 µm	150 μm	150 μm
L _{s5}	L ₁	L_2	L_3	L_4
300 µm	1150 μm	900 µm	1710 µm	990 µm
L_5	L_6	L ₇	L_8	L9
1060 µm	1230 µm	740 µm	850 μm	540 µm
L ₁₀	L ₁₁	L ₁₂		
880 µm	960 µm	980 µm		

feedback at the gate and drain of transistor Q_4 and a resistor of 6 Ω at the output port are used to improve the stability of the LNA.

Table 1 lists a summary of total dc drain current in multi-mode operation and drain voltages states of singleband transistors that are used to realize switch-free dual-band operation. Fig. 12 presents the complete schematic of the proposed dual-band reconfigurable LNA with parameters of key devices are listed in Table 2.

IV. MEASUREMENT RESULTS

The proposed LNA is fabricated in WIN Semiconductor 0.15- μ m E-mode GaAs pHEMT process. The thickness of the substrate is 100 μ m. Fig. 13 shows a micrograph of the LNA with a compact 2 × 1.8 mm² chip size, including all RF and dc power pads. The LNA is measured by on-wafer probing at RF pads, and the dc biases of the LNA are connected to an external circuit via 25- μ m diameter gold bond wires. The LNA is measured by the Cascade Microtech probe station, Summit 11000B-M. S parameters and noise performance are measured on-wafer by Agilent E5071C network analyzer and Agilent N8975B noise figure analyzer.

TABLE 3. Comparison with other single-band, wideband and multi-mode LNAs.

Reference	Freq(GHz)	NF(dB)	Gain(dB)	OP1(dBm)	P _{DC} (mW)	Area(mm ²)	FOM	Tech	
[25]	8-10	1.1-1.3	22-24	2.5@10GHz	32.8	0.46	19.9	180 nm SiGe	
[26]	14-18	2.4-3.2	18-18.6	N/A	730	2.2	N/A	0.25 µm GaN	
[24]	3-10	2.5-4.5	18-21	N/A	30	1.8	N/A	180 nm SiGe	
[27]	0.1-23	2.7-4	27.4	6.7-8.6	336	1.36	2.22	0.15 µm GaAs	
[28]	10/24	5.3/10.4	25.3/12.1	N/A	12	1.14	N/A	130 nm CMOS	
[29]	21.5/36	4.3/4.3	15.7/15.7	-8.6/-10.1	73.8	0.69	0.14/0.17	180 nm SiGe	
[21]	28/60	2.8/3.35	16.2/15	4.2/8	8.2/21	0.1	68.6/87.1	130 nm SiGe	
[30]	8-12	1.5-2.8	18	N/A	72	1.2	N/A	0.25 μm pHEMT	
	12-18	3.4-4.4	20						
This Work	8-10	1.28-1.41	25-25.2	0.5-1.7	190	190	2.6	3.7	0.15 um CoAs
	12-20	1.23-1.51	20.1-28	2.2-5	227.5	3.6	16.8	0.15 µm GaAs	



FIGURE 12. Schematic of the proposed reconfigurable LNA.



FIGURE 13. Micrograph of the proposed LNA.

A. S-PARAMETERS AND NF MEASUREMENT

Fig. 14 presents the measured and simulated S-parameters and NF of the proposed LNA in dual-band mode. At dual-band mode from $8\sim20$ GHz, the LNA achieves a small-signal gain of 21.6-28.4 dB, NF of 1-1.5 dB, input and output returnloss are better than 8 dB.



FIGURE 14. Measured (solid line) and simulated (dashed line) S-parameters and NF of the proposed LNA in dual-band mode.

By turning off transistors of Q_3 and Q_4 shown in Fig. 12, the LNA operates in low-band mode from $8 \sim 10$ GHz. Fig. 15 gives the measured and simulated S-parameters,



FIGURE 15. Measured (solid line) and simulated (dashed line) S-parameters and NF of the proposed LNA in low-band mode.



FIGURE 16. Measured (solid line) and simulated (dashed line) S-parameters and NF of the proposed LNA in high-band mode.



FIGURE 17. Measured and simulated OP1dB of the proposed LNA.

and the LNA achieves a small-signal gain of 25-25.2 dB, NF of 1.28-1.41 dB, input and output return-loss are greater than 10 dB.

When the transistor of Q_5 shown in Fig. 12 is turned off, the LNA operates in high-band mode from $12\sim20$ GHz. Fig. 16 gives the measured and simulated S-parameters and NF. LNA achieves a small-signal gain of 20.1-28 dB, NF of 1.23-1.51 dB, input and output return-loss are better than 10 dB.

B. OP1dB MEASUREMENT

Simulated and measured OP1dB of the LNA operating in different modes is shown in Fig. 17. The measured OP1dB from $8 \sim 10$ GHz is 0.5-1.7 dBm. The measured OP1dB from 12-20 GHz is 2.2-5 dBm.

Table 3 compares the performance of the proposed dualband switch-free reconfigurable LNA with other state-of-theart single-band, wideband and multi-mode LNAs. The LNA presented in this article is the first switch-free reconfigurable LNA based on coupled lines. It can be found that NF of the proposed LNA is much lower than that of other reported wideband and multi-mode LNAs. Moreover, performance of the proposed LNA in different operation bands is comparable with that of the corresponding single-band LNAs. The definition of figure of merit (FOM) can be written by:

$$FOM = \frac{Gain[abs] \cdot OP1[mW] \cdot Freq[GHz]}{P_{DC}[mW] \cdot (NF - 1)[abs]}$$
(11)

V. CONCLUSION

A switch-free dual-band LNA operating in 8-10 and 12-20 GHz band is demonstrated and fabricated in a 0.15- μ m E-mode GaAs process. To obtain frequency reconfigurable capabilities, we theoretically analyzed and developed coupled lines in the inter-stage and output-stage. The input dual-band signals are divided into single-band amplifiers by the inter-stage coupler and combined into output port by the output-stage coupler. The unit transistor of the proposed LNA is designed in common-source (CS) architecture and uses source degeneration inductors to obtain low noise and input matching simultaneously. The 3.6 mm² chip exhibits a measured small signal gain of 25-25.2 dB with 1.28-1.41 dB noise figure in 8-10 GHz and a measured small signal gain of 20.1-28 dB with 1.23-1.51 dB noise figure in 12-20 GHz. Measurement results show that the proposed switch-free reconfigurable LNA can be applied in modern multi-mode receiver systems.

REFERENCES

- J. Hu, K. Ma, S. Mou, and F. Meng, "A seven-octave broadband LNA MMIC using bandwidth extension techniques and improved active load," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 10, pp. 3150–3161, Oct. 2018.
- [2] M. Moezzi and M. S. Bakhtiar, "Wideband LNA using active inductor with multiple feed-forward noise reduction paths," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 1069–1078, Apr. 2012.
- [3] G. Nikandish and A. Medi, "Unilateralization of MMIC distributed amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3041–3052, Dec. 2014.
- [4] G. Nikandish and A. Medi, "A 40-GHz bandwidth tapered distributed LNA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1614–1618, Nov. 2018.
- [5] T. Kraemer, C. Meliani, F. J. Schmueckle, J. Wuerfl, and G. Traenkle, "Traveling-wave amplifiers in transferred substrate InP-HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 9, pp. 2114–2121, Sep. 2009.
- [6] C.-Y. Hsiao, T.-Y. Su, and S. S. H. Hsu, "CMOS distributed amplifiers using gate-drain transformer feedback technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2901–2910, Aug. 2013.
- [7] K. Fang and J. F. Buckwalter, "Efficient linear millimeter-wave distributed transceivers in CMOS SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 1, pp. 295–307, Jan. 2019.
- [8] K. W. Kobayashi, D. Denninghoff, and D. Miller, "A novel 100 MHz-45 GHz input-termination-less distributed amplifier design with lowfrequency low-noise and high linearity implemented with a 6 inch 0.15 μ m GaN-SiC wafer process technology," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2017–2026, Sep. 2016.

- [9] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 548–552, Feb. 2005.
- [10] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, Nov. 2006.
- [11] D. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.
- [12] V. Bhagavatula and J. C. Rudell, "Analysis and design of a transformerfeedback-based wideband receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1347–1358, Mar. 2013.
- [13] G. Nikandish and A. Medi, "Transformer-feedback interstage bandwidth enhancement for MMIC multistage amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 441–448, Feb. 2015.
- [14] M. P. van der Heijden, L. C. N. de Vreede, and J. N. Burghartz, "On the design of unilateral dual-loop feedback low-noise amplifiers with simultaneous noise, impedance, and IIP3 match," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1727–1736, Oct. 2004.
- [15] L. Wu, H. F. Leung, and H. C. Luong, "Design and analysis of CMOS LNAs with transformer feedback for wideband input matching and noise cancellation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1626–1635, Jun. 2017.
- [16] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS lownoise amplifier with reconfigurable input matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1054–1062, May 2009.
- [17] C.-T. Fu, C.-L. Ko, C.-N. Kuo, and Y.-Z. Juang, "A 2.4–5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 2754–2763, Dec. 2008.
- [18] X. Yu and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1236–1246, Mar. 2013.
- [19] K. Choi, H. Park, M. Kim, J. Kim, and Y. Kwon, "A 6–18-GHz switchless reconfigurable dual-band dual-mode PA MMIC using coupled-linebased diplexer," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5685–5695, Jun. 2018.
- [20] N. M. Neihart, J. Brown, and X. Yu, "A dual-band 2.45/6 GHz CMOS LNA utilizing a dual-resonant transformer-based matching network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1743–1751, Aug. 2012.
- [21] A. A. Nawaz, J. D. Albrecht, and A. C. Ulusoy, "A Ka/V band-switchable LNA with 2.8/3.4 dB noise figure," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 10, pp. 662–664, Oct. 2019.
- [22] A. Ç. Ulusoy, T. Purtova, B. Tillack, H. Schumacher, and M. Kaynak, "24 to 79 GHz frequency band reconfigurable LNA," *Electron. Lett.*, vol. 48, no. 25, pp. 1598–1600, Dec. 2012.
- [23] D. M. Pozar, *Microwave Engineering*, 3rd ed. Hoboken, NJ, USA: Wiley, 2005.
- [24] A. Ismail and A. A. Abidi, "A 3–10-GHz low-noise amplifier with wideband LC-ladder matching network," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.
- [25] T. Kanar and G. M. Rebeiz, "X- and K-band SiGe HBT LNAs with 1.2- and 2.2-dB mean noise figures," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2381–2389, Oct. 2014.
- [26] F. Guo and Z. Yao, "Design of a Ku-band AlGaN/GaN low noise amplifier," in *Proc. 3rd Asia–Pacific Conf. Antennas Propag.*, Jul. 2014, pp. 1406–1408.
- [27] J. Hu, K. Ma, S. Mou, and F. Meng, "Analysis and design of a 0.1–23 GHz LNA MMIC using frequency-dependent feedback," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 9, pp. 1517–1521, Sep. 2019.

- [28] K.-A. Hsieh, H.-S. Wu, K.-H. Tsai, and C.-K. C. Tzuang, "A dualband 10/24-GHz amplifier design incorporating dual-frequency complex load matching," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1649–1657, Jun. 2012.
- [29] J. Lee and C. Nguyen, "A K-/Ka-band concurrent dual-band singleended input to differential output low-noise amplifier employing a novel transformer feedback dual-band load," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2679–2690, Sep. 2018.
- [30] M. He, Y. Peng, and B. Li, "A reconfigurable low noise amplifier for X/Ku band," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, Chengdu, China, May 2018, pp. 1–3.



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