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TFET-Based Voltage Detector: Proposal and Investigation

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ABSTRACT In this paper, a tunnel field-effect transistor (TFET)-based voltage detector is proposed and its electrical characteristics are investigated using technology computer-aided design (TCAD) simulation. The operating principle of the proposed voltage detector is explained and possible applications in electrical overstress (EOS) and electrostatic discharge (ESD) protection are explored. Moreover, the impact of the key parameters on device performance is also discussed. The simulation results show that the proposed TFET-based voltage detector has a low leakage current and high detection sensitivity under EOS events compared to traditional diode-based detectors. With an additional nMOSFET capacitor, the proposed circuit can also be used for ESD protection.

INDEX TERMS Band-to-band tunneling (BTBT), electrical overstress (EOS), electrostatic discharge (ESD), tunnel field-effect transistor (TFET), voltage detector.

I. INTRODUCTION

Tunnel field-effect transistors (TFETs) employ electric field control of band-to-band tunneling (BTBT) as the current gating mechanism, which enables them to achieve sub-threshold swings smaller than 60 mV/dec at room temperature [1]–[4]. However, silicon TFETs have low driving abilities compared to conventional metal-oxide-semiconductor FETs (MOSFETs), which restricts the use of these devices in practical applications. Fortunately, silicon TFETs are compatible with conventional complementary metal-oxide-semiconductor (CMOS) technology, which allows the design of hybrid TFET-MOSFET circuits [5]–[8].

Electrical overstress (EOS) protection and electrostatic discharge (ESD) are two important issues for integrated circuits (ICs) [9]–[11]. Recently, several studies have investigated the ESD characteristics of TFETs and proposed a hybrid TFET-MOSFET-based whole-chip ESD protection network [12]–[16]. However, the results showed that the TFETs could not conduct high-amplitude currents when used as a single protection device.

Resistor-capacitor (RC) networks are widely used to distinguish ESD events from normal power-up events. However, it is not realistic to use on-chip RC networks to detect EOS events since they have much longer current rise times (generally over 10 μs). Therefore, a voltage detector consisting of a diode string and a resistor is often used [9]–[11]. However, the detection sensitivity and the leakage current of diode-based voltage detectors should be improved. In this paper, a new TFET-based voltage detector is proposed and its application in detecting EOS and ESD events is investigated. The simulation results demonstrate that the proposed voltage detector has high sensitivity to high V_{DD} voltages, low leakage current and small layout area compared to conventional solutions.

II. TFET-BASED VOLTAGE DETECTOR

A. PRINCIPLE OF THE TFET-BASED VOLTAGE DETECTOR

Figs. 1 (a) and (b) show the schematics of a traditional diode-based [9], [10] and the proposed TFET-based voltage detectors, respectively. A p^+/n-well diode string is used in the diode-based voltage detector, while only one conventional point TFET is used in the proposed detector. The traditional diode-based voltage detector is formed by a diode string and a resistor R. When the V_{DD} voltage exceeds the threshold voltage (V_{th}) of the diode string, the voltage detector conducts and causes a voltage drop across R. As a result, V_{Detect_Diode} becomes lower than V_{DD}, indicating that the

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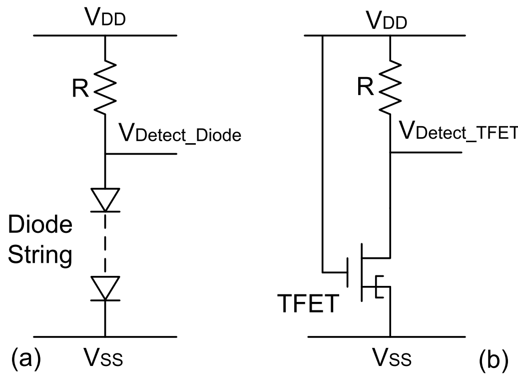

FIGURE 1. Schematics of (a) traditional diode-based voltage detector [9], [10] and (b) the proposed TFET-based voltage detector.

high voltage on V_{DD} is captured. The operating principle of the proposed TFET-based voltage detector is similar to that of the traditional diode-based approach. The gate of the TFET is connected to V_{DD}, forming a "normally-on" structure. Since the tunneling probability of silicon TFETs is low and a relatively high gate work function is applied, the BTBT is weak enough under normal operating voltages (below 1 V) and the leakage current can be controlled [3], [4], [17], [18]. When V_{DD} is high enough, the TFET conducts, the BTBT current flows through R and a detection signal V_{Detect_TFET} is generated.

B. STRUCTURE OF THE TFET-BASED VOLTAGE DETECTOR

The TFET used in the proposed detector is a traditional point TFET with the following key parameters. The lengths of the active and the gate regions are 200 nm and 100 nm, respectively. The junction depth is 50 nm, and a SiO2 film with a thickness of 0.6 nm is used as a gate dielectric. The gate metal work function (ϕTFET) is 5 eV and the resistance of R is 20 kΩ. The doping concentrations of p^+, n^+, p-well, and p-sub regions are 10^{20}, 10^{20}, 10^{17}, and 10^{16} cm^{-3}, respectively.

Since the driving current of the TFET is relatively low, the width of the TFET is increased in the proposed design to enhance the detection sensitivity. This can be implemented by increasing the finger number of TFET in the layout design. In this work, detectors with 2-, 3-, and 4-finger TFETs are investigated. Figs. 2 (a), (b) and (c) show the cross-sectional views of voltage detectors based on a diode string, a single finger TFET, and a 4-finger TFET, respectively. It is clear that the equivalent width of the TFET in Fig. 2 (c) is 4 times that of the single finger TFET. For diode-based voltage detectors, more diodes mean a lower leakage current, but also a higher Vth [19]. For ICs with an operating voltage of 1 V, three diodes are usually used in commercial products to balance the two factors [20]. Thus, three diodes are also used in this work. The lengths of the active regions and the doping concentrations of the diodes are the same as those of the TFET. It should be mentioned that a TFET drawn in multi-finger style can save layout area since some active regions are shared among fingers. It can be seen from Fig. 2 that even a 4-finger TFET has a smaller layout area compared with the 3-diode string.

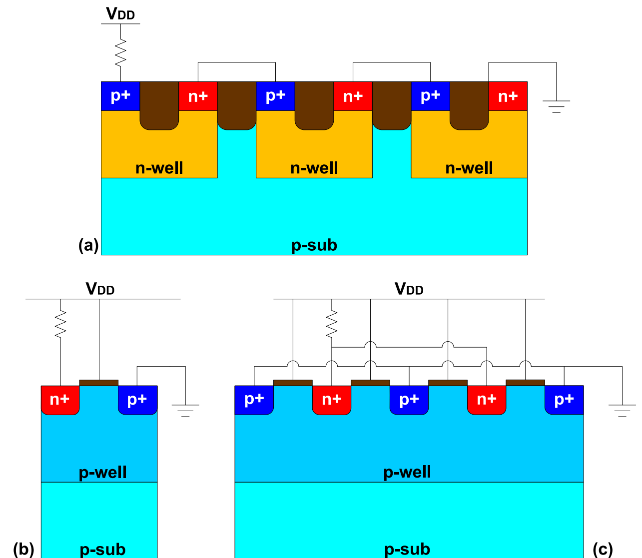

FIGURE 2. Cross sectional views of voltage detectors used in the simulations based on (a) a 3-diode string, (b) a single finger TFET and (c) a 4-finger TFET (not to scale).

C. TCAD METHODOLOGY AND SIMULATION OF THE TFET

Simulations were carried out using the Synopsys Sentaurus simulator. A dynamic non-local BTBT model was used to capture the BTBT phenomenon. Moreover, band-gap narrowing and doping-dependent Shockley-Read-Hall recombination models were also used. Since the voltage detector is used to detect the high V_{DD} voltage, the Van Overstraeten-de Man model was employed to calculate avalanche generation. In addition, the high-field saturation mobility model was also enabled. The calibration of the DC characteristics of the TFET used in this work was performed by matching the simulation results with the experimental data reported in [14]. Fig. 3 (a) shows the calibrated transfer characteristics using the experimental data. It can be seen from the figure that a good match between the experimental data and the simulated characteristics is obtained with less than 10% error.

As mentioned above, the TFET used in the voltage detector has a high gate metal work function, ensuring low leakage current (I_{Leak_TFET}). Interestingly, I_{Leak_TFET} in this work is the ON-state current of a TFET in normal application, namely the drain-source current when both the drain-source voltage (V_{ds}) and the gate-source voltage (V_{gs}) are equal to V_{DD}. Fig. 3 (b) shows the transfer curves of the TFET used in this work with different V_{ds} values. With a proper gate metal work function (5 eV) and a V_{DD} of 1 V, an I_{Leak_TFET} of 2.1×10^{-13} A/μm is obtained, which means that the voltage detector introduces a low leakage current. The ambipolar conduction is observed in the transfer curves, and the drain-source current is on the order of 10^{-9} A/μm when V_{gs} is 0 V. However, this will not result in extra leakage current since the gate is tied to V_{DD} in the proposed voltage detector.

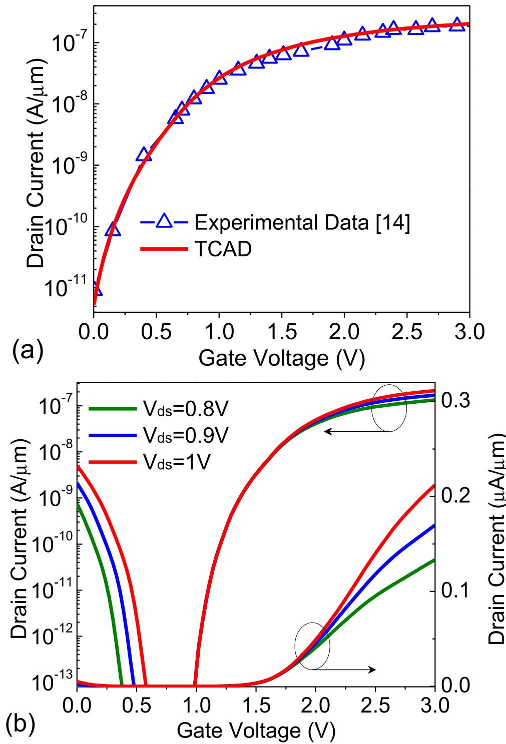

FIGURE 3. (a) Calibrated transfer characteristics using the experimental data from [14]. The curves are shifted so that the gate voltage where the drain-source current is $\sim 10^{-11}$ A/μm is at the origin. (b) Transfer curves of the TFET used in the voltage detector under different values of drain-source voltage (V_{ds}).

III. SIMULATION RESULTS OF THE TFET-BASED VOLTAGE DETECTOR

A. TURN-ON CHARACTERISTIC

DC simulations of both the TFET and 3-diode-based voltage detectors were carried out. V_{DD} was swept from 0 to 3 V and the results are shown in Fig. 4. It can be seen from the figure that the V_{Detect_TFET} is 1.83, 1.56, and 1.39 V for the 2-, 3-, and 4-finger TFETs, respectively, at $V_{DD} = 3$ V. In contrast, V_{Detect_Diode} is significantly higher than V_{Detect_TFET} with a value of 2.09 V. On the other hand, with the 2-, 3-, and 4-finger TFETs, V_{Detect_TFET} departs from V_{DD} when V_{DD} is 1.97, 1.86, and 1.80 V, respectively, while it is 2.01 V for V_{Detect_Diode} (the departure point is defined as the value of V_{DD} when V_{Detect_TFET} or V_{Detect_Diode} is 100 mV lower than V_{DD}). These results indicate that the sensitivity of the proposed TFET-based voltage detector is higher than that of the 3-diode based detector. The better detection performance of the proposed detector can be explained as follows. The TFET-based voltage detector is essentially a resistor-based inverter (or like a common-source amplifier). When V_{DD} exceeds the detector's Vth, the "output" signal (V_{Detect_TFET}) decreases with the increase in the "input" signal (V_{gs}), whereas V_{Detect_Diode} always increases with an increase in V_{DD}. Thus, a larger voltage drop across the resistor R will be obtained in the TFET-based voltage detector under the same V_{DD} value compared with that in the diode-based detector. Increasing the value of R can also enhance the detection sensitivity; however, it will also significantly increase the layout area.

It should be mentioned that it is extremely difficult to enhance the trigger sensitivity of the diode-based voltage detector effectively by enlarging the diode size. Even if the width of each diode is increased 10 times, V_{Detect_Diode} is only reduced by 0.1 V when V_{DD} is 3 V.

B. LEAKAGE CURRENT

Fig. 5 shows the leakage currents of the TFET-based and diode-based voltage detectors under different temperatures. It can be seen that the leakage current of the proposed TFET-based voltage detector is lower than that of the 3-diode-based detector. At 25 °C, both the TFET and the diode string have low leakage currents. However, the TFET has much better temperature stability than the diode string. Generally, when the temperature rises from 25 to 125 °C, the drain-source current of a Si-TFET at a certain bias increases by less than an order of magnitude, whereas, it can increase by several orders of magnitude for the diode string [19], [21]. This is mainly attributed to the conduction of the parasitic bipolar junction transistor, which is regarded as the Darlington Effect. In this work, I_{Leak_TFET} rises from 2.1×10^{-13} to 5.8×10^{-11} A/μm with a V_{DD} of 1 V, whereas, the current for the diode string rises from 8.5×10^{-13} to 9.6×10^{-9}

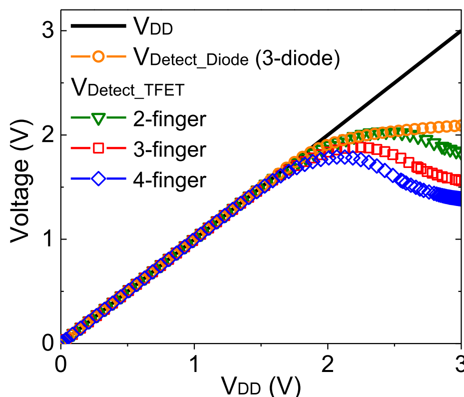

FIGURE 4. DC simulation results of node voltages of TFET and 3-diode-based voltage detectors.

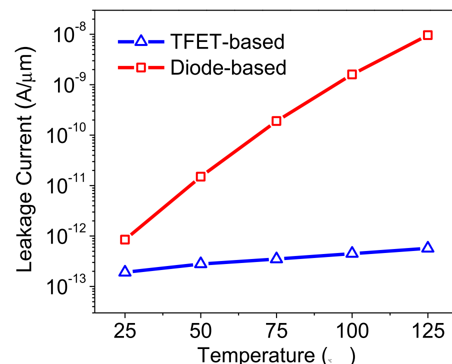

FIGURE 5. Leakage currents of TFET-based and diode-based voltage detectors under different temperatures.

A/μm, as shown in Fig. 5. Thus, the low leakage current is a significant advantage of the proposed TFET-based voltage detector.

C. EFFECT OF IMPACT IONIZATION

As mentioned before, the proposed TFET-based voltage detector is designed to detect a high V_{DD} voltage, thus the device will operate in high electric-field condition and impact ionization must be considered. Figs. 6 (a) and (b) show the contour plots of BTBT and impact ionization generation rates near the source/channel junction with a V_{DD} of 3 V, while Fig. 6 (c) shows the generation rates extracted at 0.5 nm below the Si/oxide interface. It can be seen that although the impact ionization generation rate is lower than the BTBT rate, it will affect the detection signal. DC simulation results comparing the detection signals with and without impact ionization model are shown in Fig. 7. Without impact ionization model, V_{Detect_TFET} increases by 0.2, 0.05 and 0.03 V for the 2-, 3- and 4-finger TFETs, respectively, when V_{DD} is 3 V and the corresponding departure points increase by 0.17, 0.1 and 0.07 V, respectively.

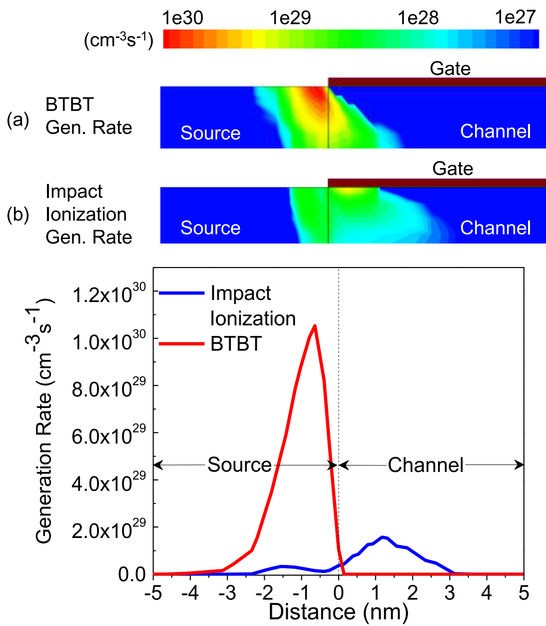

FIGURE 6. BTBT and impact ionization generation rates near the source/channel junction with a V_{DD} of 3 V, extracted at 0.5 nm below the Si/oxide interface.

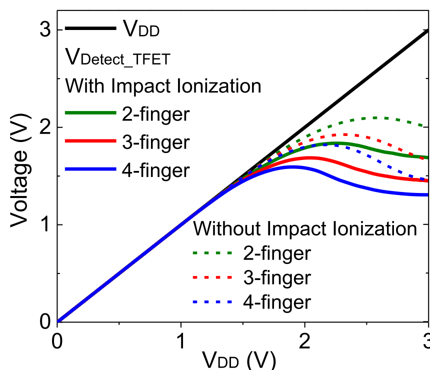

FIGURE 7. DC simulation results of node voltages with and without impact ionization.

IV. EOS AND ESD PROTECTION CIRCUITS WITH TFET-BASED VOLTAGE DETECTOR

A. PRINCIPLE OF THE PROPOSED EOS PROTECTION CIRCUIT

Figs. 8 (a) and (b) shows the schematics of EOS protection circuits with the traditional diode-based [9], [10] and the proposed TFET-based voltage detectors, respectively. Both protection circuits are composed of a voltage detector, a trigger pMOSFET, and a silicon-controlled rectifier (SCR) device. For the TFET-based protection circuit, during an EOS event, the high V_{DD} voltage exceeds the Vth of the diode string and enables the conduction of the voltage detector. V_{Detect_TFET} becomes lower than V_{DD}, the pMOSFET is turned on and a current is injected into the substrate of the SCR, which turns on the SCR to discharge the EOS current. Under the normal operating conditions, V_{DD} is low and the TFET does not conduct, no current flows through R and V_{Detect_TFET} is tied to V_{DD}. Thus, the pMOSFET and the SCR will not turn on. The operating principle of the diode-based voltage detector is similar to that of the TFET-based approach.

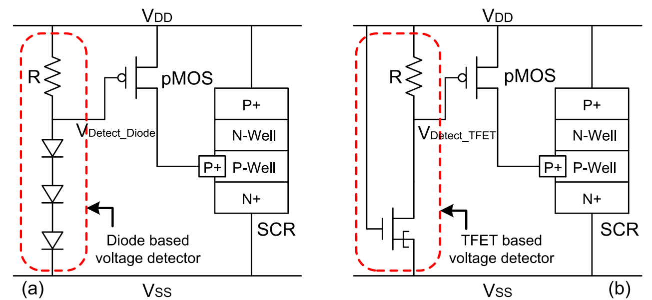

FIGURE 8. Schematics of EOS protection circuits with (a) traditional diode-based voltage detector [9], [10] and (b) the proposed TFET-based voltage detector.

Fig. 9 shows the cross-sectional view of the EOS protection circuit with the proposed TFET-based voltage detector, where all the devices (TFET, pMOSFET, SCR) have the same widths. A 2-finger TFET is shown as an example.

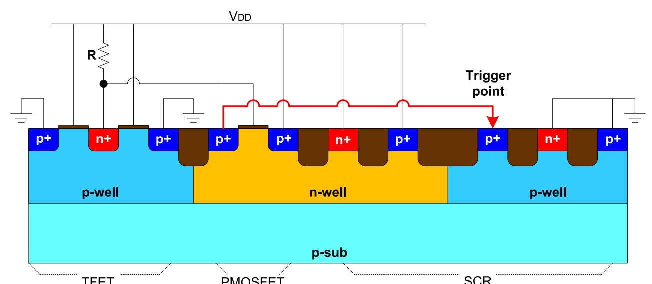

FIGURE 9. Cross sectional view of EOS protection circuit with the proposed TFET-based voltage detector (not to scale).

B. PROPOSED PROTECTION CIRCUIT UNDER EOS EVENT

The characteristics of the proposed TFET-based protection circuit were investigated. The simulation conditions were similar with that used in [11], i.e. an EOS-like pulse is applied to V_{DD} when the IC is under normal operating condition ($V_{DD} = 1$ V). V_{DD} rises from 1 V to 3 V in 8 μs and causes the conduction of the protection circuit. The simulation results are shown in Fig. 10. It can be seen from the figure that for the protection circuits with 2-, 3-, and 4-finger TFETs, the total currents increase sharply when V_{DD} rises to 2.75, 2.59, and 2.48 V, respectively (the corresponding V_{DD} value is defined as the trigger voltage), indicating that the SCR is fully turned on in all three cases. On the other hand, the trigger voltage for the diode-based protection circuit is 2.84 V. Fig. 11 shows the current density contour plots before and after the SCR is turned on. The main current components before the SCR is turned on are from the TFET and the pMOSFET, indicating that both the TFET and the pMOSFET are conducting and a trigger current is injected into the SCR. After the SCR is turned on ($V_{DD} = 2.8$ V), the main current component is from the SCR. In contrast, the trigger voltage of the 3-diode based protection circuit is 2.86 V, which is significantly higher than that of the proposed TFET-based protection circuit.

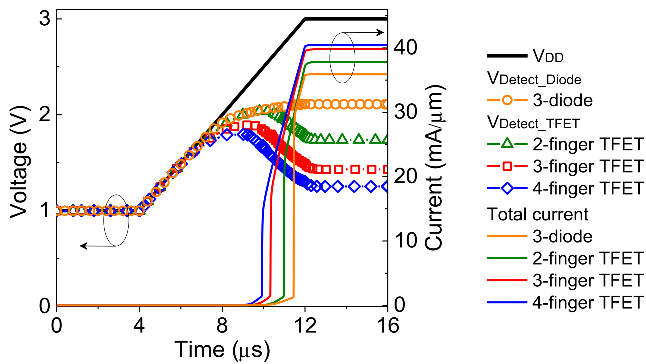

FIGURE 10. Node voltages and total currents of different protection circuits under EOS-like simulation.

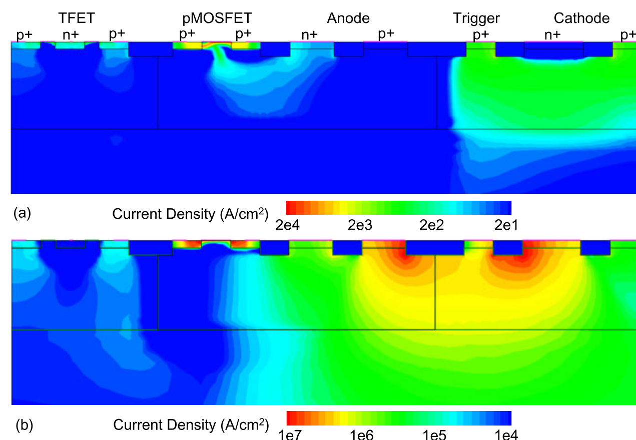

FIGURE 11. Contour plots of current density (a) before and (b) after the SCR is turned on.

Another advantage of the proposed TFET-based protection circuit is that the discharging capability is increased, as the total currents are 37.8, 39.8, and 40.4 mA/μm with 2-, 3-, and 4-finger TFETs, respectively, when V_{DD} is 3 V, while for the diode-based circuit, the total current is 36 mA/μm. This is mainly because the pMOSFET in the proposed circuit has a larger V_{gs}, so it discharges more current and also enhances the positive feedback regeneration of the SCR.

C. PROPOSED PROTECTION CIRCUIT UNDER ESD EVENT

An ESD event can be regarded as a kind of EOS event. However, both the current rise time and the discharge duration of ESD events are much shorter than those of typical EOS events such as a surge. The typical current rise time of a human body model (HBM) ESD event is 10 ns, whereas it is 8 μs for a surge event [9]. This difference will result in detection performance degradation of the proposed TFET-based voltage detector. The transmission line pulsing (TLP) method is widely used for ESD measurement and simulation. In this work, a current waveform with 10 ns rise time and 100 ns pulse width is applied to V_{DD} to simulate the HBM event, in similarity to previous works [12], [14]. The thermo-dynamic model was used to calculate the heat generation in the ESD event.

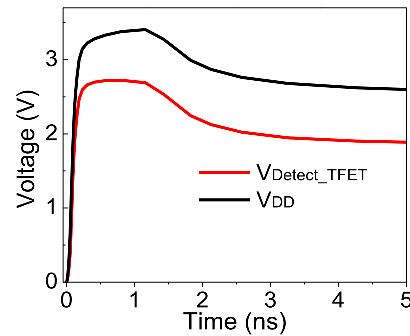

FIGURE 12. Transient node voltages of the proposed TFET-based EOS protection circuit in the first 5 ns under TLP simulation with a current amplitude of 10 mA/μm.

The transient node voltages of the proposed TFET-based EOS protection circuit (Fig. 8 (b)) in the first 5 ns under TLP simulation are shown in Fig. 12. In this section, a 2-finger TFET was used in the simulation. It can be seen that V_{DD} increases to ~3.4 V in the first 1.2 ns, while V_{Detect_TFET} is ~2.6 V. The difference between V_{DD} and V_{Detect_TFET} is significantly smaller than that in the EOS simulation. This phenomenon can be explained as follows. When the gate voltage of a TFET increases, an inversion layer is formed and connects the drain region to the lower surface of the gate oxide, as shown in Fig. 13 [22]. Thus, the gate capacitance (C_g) mainly consists of the gate-drain capacitance (C_{gd}). Under the ESD event, when the current is injected into the device, the gate voltage rises quickly and the coupling effect of C_{gd} increases the potential of the drain region. This

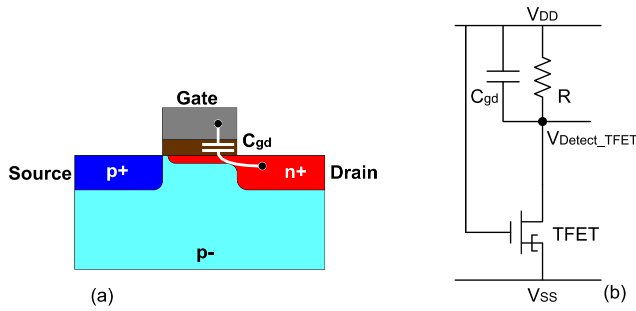

FIGURE 13. (a) Under inversion bias (high V_{gs} and high V_{ds}), asymmetric partitioning of gate capacitance is observed in a TFET, (b) the corresponding equivalent circuit.

opposes the reduction in V_{Detect_TFET} caused by the BTBT current, and in turn degrades the detection sensitivity.

In order to enhance the detection performance under an ESD event, an nMOSFET capacitor with 50 nm gate length and a width the same as the SCR and TFET was added to the proposed TFET-based ESD/EOS protection circuit, as shown in Fig. 14. In this condition, the nMOSFET capacitor counteracts the coupling effect of the induced C_{gd}. The simulation results are shown in Fig. 15. It can be seen from Fig. 15 (a) that in the first 5 ns, the V_{DD} in the ESD/EOS protection circuit is significantly lower than that in the EOS protection circuit, indicating that the ESD detection performance is enhanced with the addition of the nMOSFET capacitor. At this time, the main physical mechanism of the TFET-based ESD/EOS protection circuit is the capacitance coupling rather than BTBT generation at the initial time. Therefore, the proposed circuit in Fig. 14 is suitable for both EOS and ESD protection circuits, and the main physical mechanisms for detection are BTBT and capacitance coupling, respectively. It should be noted that the introduction of the nMOSFET capacitor has no impact on EOS event detection. This is because the size of the nMOSFET capacitor is very small, the equivalent RC time constant is correspondingly small, and the EOS event has a much longer rise time. The V_{DD} in the diode-based protection circuit shows a trend similar to that in the TFET-based ESD/EOS protection circuit. This is because the diode-based voltage detector is also influenced by the coupling effect.

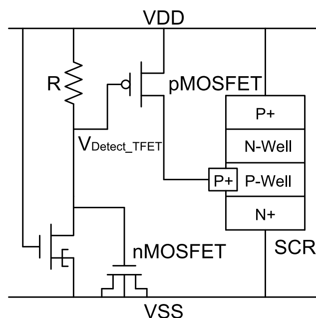

FIGURE 14. Schematic of TFET-based ESD/EOS protection circuit with additional nMOSFET capacitor.

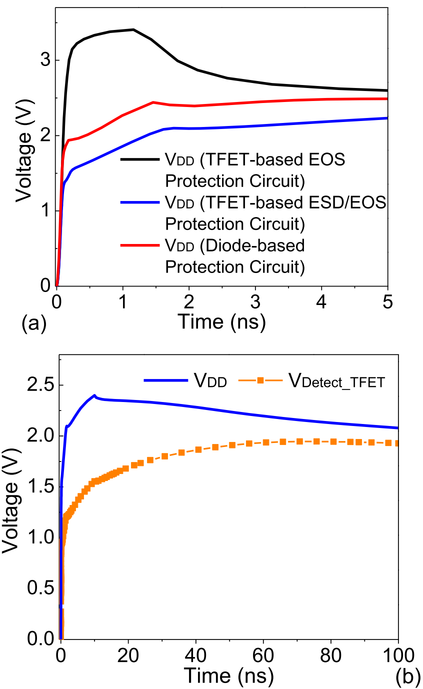

FIGURE 15. Node voltages under TLP simulation with a current amplitude of 10 mA/μm. (a) Comparison of V_{DD} values between the three circuits in the first 5 ns and (b) V_{DD} and V_{Detect_TFET} values in TFET-based ESD/EOS protection circuit (Fig. 14) in the entire TLP duration.

Fig. 15 (b) shows the node voltage waveforms of the ESD/EOS protection circuit in the entire 100 ns TLP simulation. The experimental results show that the gate oxide breakdown voltage of the advanced bulk MOSFET under 100 ns TLP test is over 3 V [23], indicating that the proposed circuit can protect the devices. V_{DD} first rises to about 2.4 V at 10 ns, and then gradually falls. However, V_{Detect_TFET} is very low (less than $\sim$1.55 V) in the first 10 ns and shows a rising trend until 70 ns. This also verifies that the coupling effect plays an important role in the voltage detector at the initial time. When the capacitors are gradually charged, V_{Detect_TFET} gradually increases.

Since capacitance coupling is the main detection mechanism of the proposed TFET-based ESD/EOS protection circuit under an ESD event, the impact of a fast power-up event is also considered. The capacitance coupling-based (namely, the RC-based) ESD protection circuit may be turned on due to a fast V_{DD} variation, causing leakage current and even a latch-up issue [24]. A voltage waveform with 100 ns rise time and 1 V amplitude was applied to V_{DD} to mimic the fast power-up event. The node voltages and the current of the proposed TFET-based ESD / EOS protection circuit in a fast power-up event simulation are shown in Fig. 16. It can be seen from the figure that V_{Detect_TFET} is slightly lower than V_{DD} during the ramping stage, mainly due to the coupling effect. However, such a small difference between V_{Detect_TFET} and V_{DD} cannot turn on the pMOSFET, and no significant leakage current is generated. On the other hand, since the holding voltage of the normal SCR device is higher than 1 V

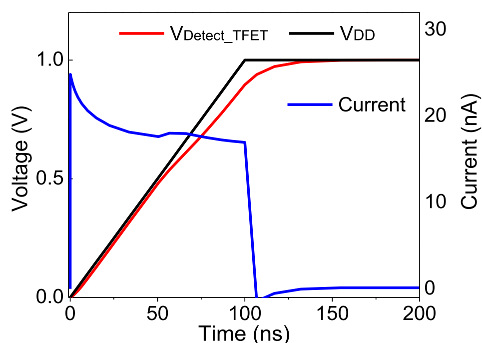

FIGURE 16. Node voltages and current of the proposed TFET-based ESD/EOS protection circuit in a fast power-up event simulation.

(operating voltage), the risk of a latch-up being induced by the fast power-up event can be ignored [25].

A thermal analysis of the proposed circuit under TLP simulation was also conducted. Fig. 17 shows the waveforms of V_{DD} and maximal lattice temperature during the TLP simulations with different current amplitudes. The lowest gate oxide breakdown voltages of thin oxide nMOSFETs in advanced technologies under 100 ns TLP tests are around 3 V [25]. It can be seen from Fig. 17 that the V_{DD} values are generally lower than 3 V. Thus, it is expected that the devices in the proposed circuit are free from oxide breakdown under TLP tests.

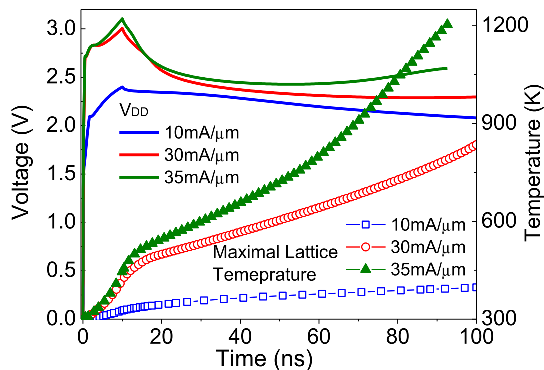

FIGURE 17. The waveforms of V_{DD} and maximal lattice temperature during the TLP simulations with different current amplitudes.

The failure temperature is considered to be 1200 K in the simulation. It can be seen that when the current amplitude is not more than 30 mA/μm, the maximal lattice temperature is lower than 1200 K for the whole TLP duration. However, when the current amplitude increases to 35 mA/μm, the maximal lattice temperature reaches 1200 K at 92 ns and the simulation terminates, since thermal failure occurs.

Generally, the hot spot appears where the current density is the highest. Figures 18 (a) and (b) show the contour plots of the lattice temperature at 1 ns and 100 ns under a 30 mA/μm TLP simulation, respectively. At 1 ns, the pMOSFET is first turned on and the hot spot appears. At 100 ns, the hot spot appears at the parasitic npn bipolar junction transistor (BJT) since the SCR is fully turned on and most of the current flows from the npn BJT to ground.

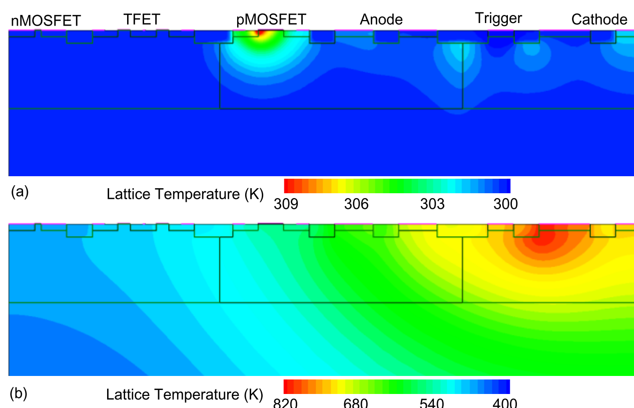

FIGURE 18. Contour plots of lattice temperature at (a) 1 ns and (b) 100 ns under a 30 mA/μm TLP simulation.

V. CONCLUSION

In this paper, a new voltage detector consisting of a TFET and a resistor is proposed. The new proposed TFET-based voltage detector has a lower leakage current, higher detection sensitivity, and smaller layout area compared to conventional diode-based voltage detectors. The simulation results demonstrate that when used for EOS protection, the proposed voltage detector can quickly turn on an SCR device and enhance the discharging capability. However, for ESD protection, an additional capacitor is required to enhance the detection performance of the proposed voltage detector.

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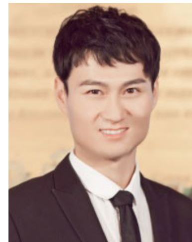

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