Parallel-Type Asymmetric Memristive Diode-Bridge Emulator and Its Induced Asymmetric Attractor

YI YE [ID], (Graduate Student Member, IEEE), JIE ZHOU, (Graduate Student Member, IEEE),
QUAN XU [ID], (Member, IEEE), MO CHEN [ID], (Member, IEEE),
AND HUAGAN WU [ID], (Member, IEEE)
School of Microelectronics and Control Engineering, Changzhou University, Changzhou 213164, China
Corresponding author: Huagan Wu (wuhg@cczu.edu.cn)

ABSTRACT Symmetry brings beauty, while asymmetry is the general law of nature. This paper reports a novel parallel-type asymmetric memristive diode-bridge (AMDB) emulator, which is implemented by an unbalance diode-bridge linked with a RC filter. Following the voltage constraints of the unbalance diode-bridge, the mathematical model of the parallel-type AMDB emulator is established. Thereafter, the asymmetric property of the hysteresis loops is demonstrated by the numerical simulations and confirmed by the hardware experiments. Furthermore, by importing the parallel-type AMDB emulator into the classical Chua's circuit, a novel memristive Chua's circuit is proposed, so that the asymmetric double-scroll chaotic attractor, asymmetric coexisting single-scroll chaotic attractors, and asymmetric coexisting limit cycles can be revealed herein. The parallel-type AMDB emulator enriches the types of memristor emulators and it can mimic the asymmetric property of the physical memristor device.

INDEX TERMS Asymmetry, parallel-type AMDB emulator, asymmetric attractor, Chua's circuit.

I. INTRODUCTION

Memristor, known as the fourth circuit element, is a dazzling star in electronic circuit fundamentals [1], [2]. Its nano-scale property makes the device occupy exceedingly small layout area in IC application [3], the non-volatile property makes it be well received in neuromorphic circuit and informatics processing [4]–[7], and the nonlinearity property makes it contribute to the generation of abundant and complex dynamical behaviors in memristive chaotic circuits [8]–[12]. Unfortunately, for the difficulty of its fabrication, the physical memristor device is inconvenient to acquire through regular purchasing channels. For the convenience of scientific research, numerous mathematical models [13]–[15], PSpice models [16] and analog circuit emulators [17]–[20] were reported for equivalently implementing the characteristics of various memristors in the past few years. Among those, the memristive diode-bridge emulator [8], [10] is greatly welcomed because of the simple structure, no grounded limitation, easy circuit access and so on.

In general, the diode-bridge circuit has a symmetrical structure with four diode bridge arms. Thus, the pre-existing memristive diode-bridge emulators just exhibit the symmetric hysteresis loops pinched at the origin [8], [20], [21]. However, the physical memristor device usually possesses the asymmetric hysteresis loops [2], [22]. The influence of symmetric-breaking phenomenon on the dynamical systems has attracted much attention [23]–[27]. Recently, Kengne et al took the antiparallel semiconductor diodes pair as an asymmetric nonlinear emulator, upon which various asymmetry-induced dynamical behaviors were revealed in several asymmetric chaotic circuits [28]–[31]. Inspired by this, a series-type asymmetric memristive diode-bridge (AMDB) emulator was newly proposed by inserting an extra diode into the first bridge arm of diode-bridge circuit [32]. Based on the series-type AMDB emulator, two asymmetric memristor-based jerk circuits were constructed. Since there is only one zero equilibrium, these two asymmetric memristor-based jerk circuits only generated the single-scroll attractors with the relatively

The associate editor coordinating the review of this manuscript and approving it for publication was Norbert Herencsar [ID].

simple dynamics, resulting in that the asymmetry of attractor topologies could not be presented perfectly. Meanwhile, it can be found that the asymmetry property can be enhanced when inserting more diodes into two symmetric bridge arms in series. However, the forward voltage required for the bridge arm will be enlarged. In this way, a much larger input voltage should be applied in its application circuit, which extremely limits the circuit applications of series-type AMDB emulator.

To solve this issue, a novel parallel-type AMDB emulator is proposed in this paper. The rest of the paper is arranged as follows. In Section II, the circuit structure and mathematical model of the parallel-type AMDB emulator is proposed, and the voltage constrains of the unbalance diode-bridge are verified. Afterwards, the volt-ampere curve of the proposed parallel-type AMDB emulator is demonstrated by the numerical simulations and confirmed by the hardware experiments. In Section III, a parallel-type AMDB emulator-based Chua's circuit is established and some asymmetric chaotic attractors and limit cycles are perfectly embodied by the numerical simulations and the hardware experiments. The end is some discussions and conclusions.

II. CIRCUIT STRUCTURE AND MATHEMATICAL MODEL

The memristive diode-bridge emulators, consisting of a symmetric diode-bridge and a RC filter, can exhibit the symmetric hysteresis loops pinched at the origin [21]. To mimic the asymmetric hysteresis loops appeared in physical memristor devices [2], [22], two diode parallel arrays are introduced into the first and third branches to obtain asymmetric property, as shown in Fig. 1. Each diode parallel array has m diodes connected in parallel, which is marked as DPA in Fig. 1. The parameter m is a positive integer. Thus, the branches B_1 and B_3 are different from the branches B_2 and B_4, rusting in the construction of unbalance diode-bridge. In this paper, such an analog discrete components-based memristor emulator is called as a parallel-type AMDB emulator.

A. MATHEMATICAL MODEL

Denote i_{Dk}, i_{Dl}, and i as the currents flowing through the diode D_k, diode parallel array DPA$_l$, and parallel-type AMDB emulator, respectively. And denote v_{Dk}, v_{Dl}, and v as the voltages across D_k, DPA$_l$, and AMDB emulator, respectively. All the diodes have identical model parameters I_S (reverse saturation current), n (emission coefficient), and V_T (thermal voltage). Then, the constitutive relations of the diode D_k and diode parallel array DPA$_l$ can be unified as

$$i_{Dk} = I_S(e^{2\xi v_{Dk}} - 1), \tag{1}$$

and

$$i_{Dl} = mI_S(e^{2\xi v_{Dk}} - 1), \tag{2}$$

respectively, where $k = 11, \ldots, 1m, 2, 31, \ldots, 3m$, and 4, $l = 1, 3, \xi = 1/(2nV_T)$.

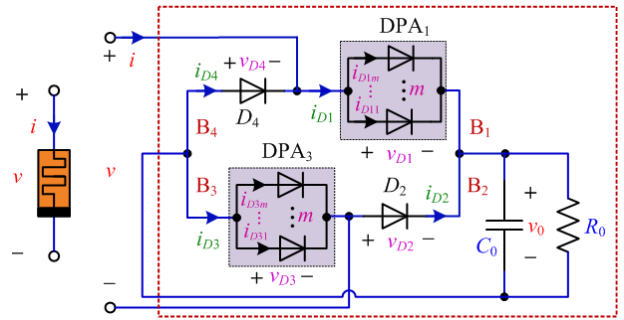There exist two conditional identities for the voltages across two pairs of the parallel bridge arms (the branches

FIGURE 1. Circuit schematic of the parallel-type AMDB emulator.

B_1, B_3, and the branches B_2, B_4). In other word, the voltages satisfy the following constrains

$$v_{D1} = v_{D3}, \quad v_{D2} = v_{D4}, \tag{3}$$

The two voltage constraints are the key to derive the mathematical model of the parallel-type AMDB emulator, which will be confirmed in the next part.

According to Kirchhoff's voltage law, for the circuit loop of DPA$_1$, C_0, DPA$_3$ and input voltage source, one can obtain

$$v_{D1} + v_{D3} = v - v_0, \tag{4}$$

and for another circuit loop of D_2, C_0, D_4 and input voltage source, there yields

$$v_{D2} + v_{D4} = -v - v_0, \tag{5}$$

Based on Kirchhoff's current law, for the nodes linked with the branches B_1, B_4, and the branches B_2, B_3, we can get the following equations

$$i = i_{D1} - i_{D4} = i_{D3} - i_{D2}, \tag{6}$$

and for the node linked with the branches B_1, B_2, we can get

$$i_{D1} + i_{D2} = C_0 \frac{dv_0}{dt} + \frac{v_0}{R_0}. \tag{7}$$

Substituting (3) into (4) and (5), there yields

$$2v_{D1} = 2v_{D3} = v - v_0, \tag{8}$$
$$2v_{D2} = 2v_{D4} = -v - v_0. \tag{9}$$

According to the constitutive relations of D_k and DPA$_l$ in (1) and (2), the equations given in (6) and (7) can be rewritten as

$$i = I_S(me^{2\xi v_{D3}} - e^{2\xi v_{D2}} - m + 1), \tag{10}$$
$$\frac{dv_0}{dt} = \frac{I_S(me^{2\xi v_{D3}} + e^{2\xi v_{D2}} - m - 1)}{C_0} - \frac{v_0}{R_0 C_0}. \tag{11}$$

Substituting (8) and (9) into (10) and (11), the above equations can be organized as

$$i = G(v_0, v)v$$
$$= I_S[me^{\xi(v-v_0)} - e^{-\xi(v+v_0)} - m + 1], \tag{12a}$$
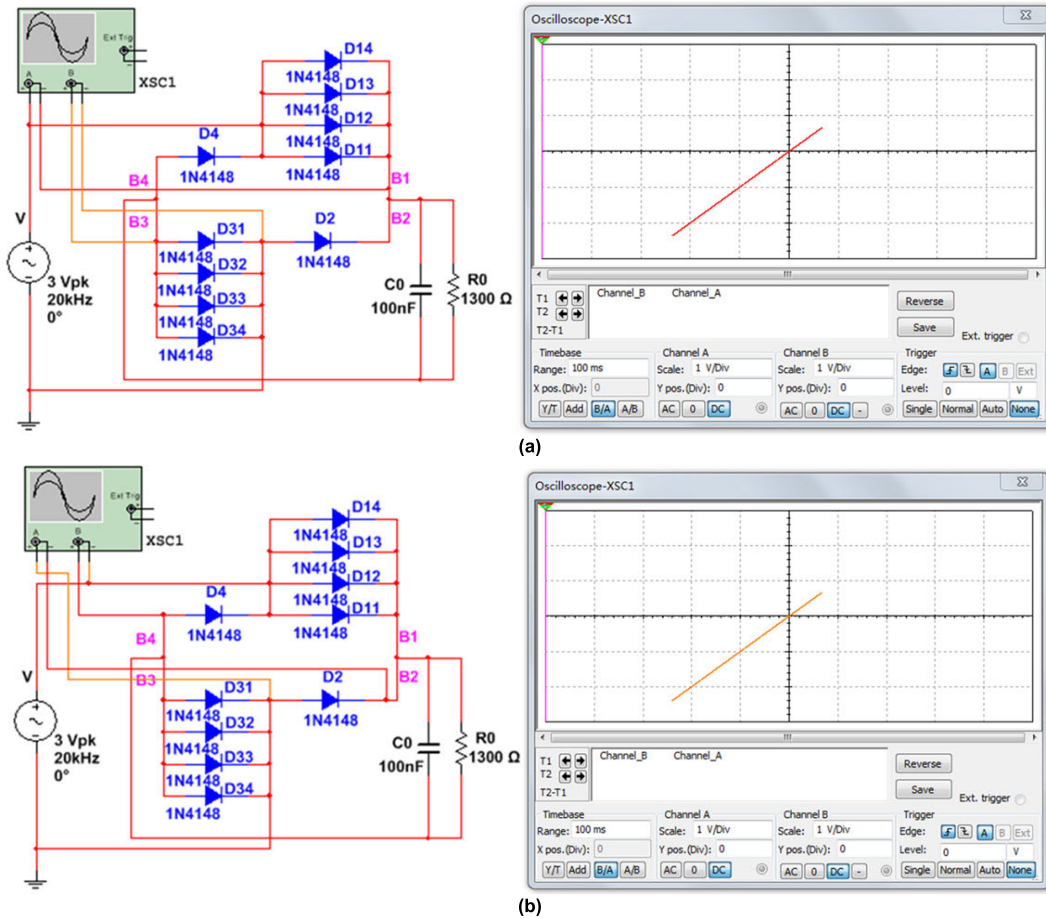$$\frac{dv_0}{dt} = g(v_0, v)$$

FIGURE 2. Multisim simulation analysis for the parallel-type AMDB emulator with $m = 4$ when applying $V = 3\sin(40000\pi t)$, (a) the voltage constraint of branches B_1 and B_3, (b) the voltage constraint of branches B_2 and B_4.
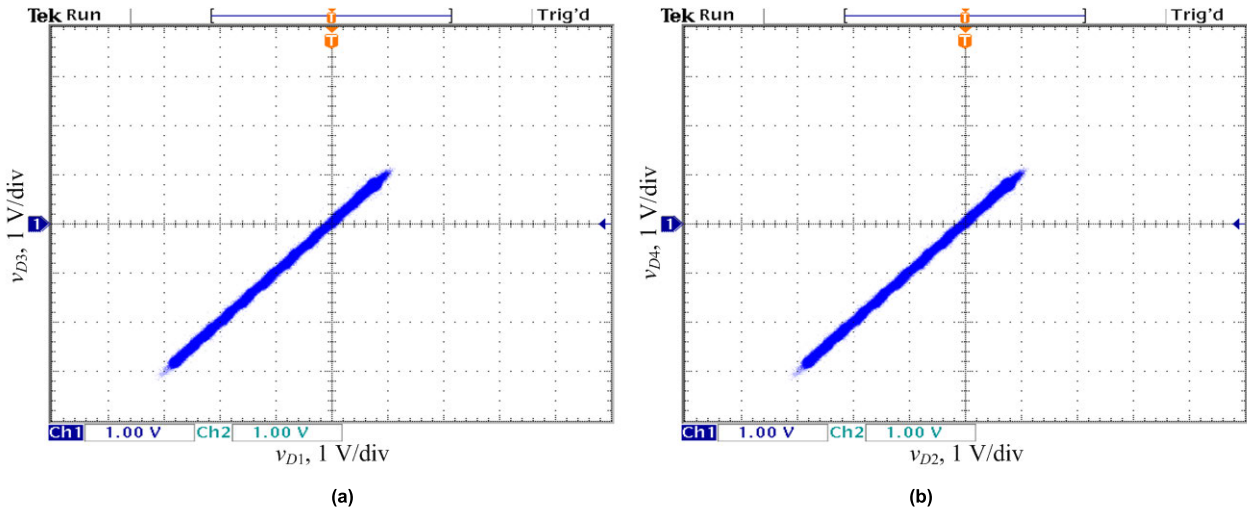

FIGURE 3. Experimental synchronous lines of the parallel-type AMDB emulator with $m = 4$ when applying $V = 3\sin(40000\pi t)$, (a) the voltage constraint of $v_{D1} = v_{D3}$, (b) the voltage constraint of $v_{D2} = v_{D4}$.

$$= \frac{I_S[me^{\xi(v-v_0)} + e^{-\xi(v+v_0)} - m - 1]}{C_0} - \frac{v_0}{R_0 C_0}.$$

$$(12b)$$

Therefore, the proposed parallel-type AMDB emulator in Fig. 1 can be described by (12), which accords with the definition of an extended memristor in [33].
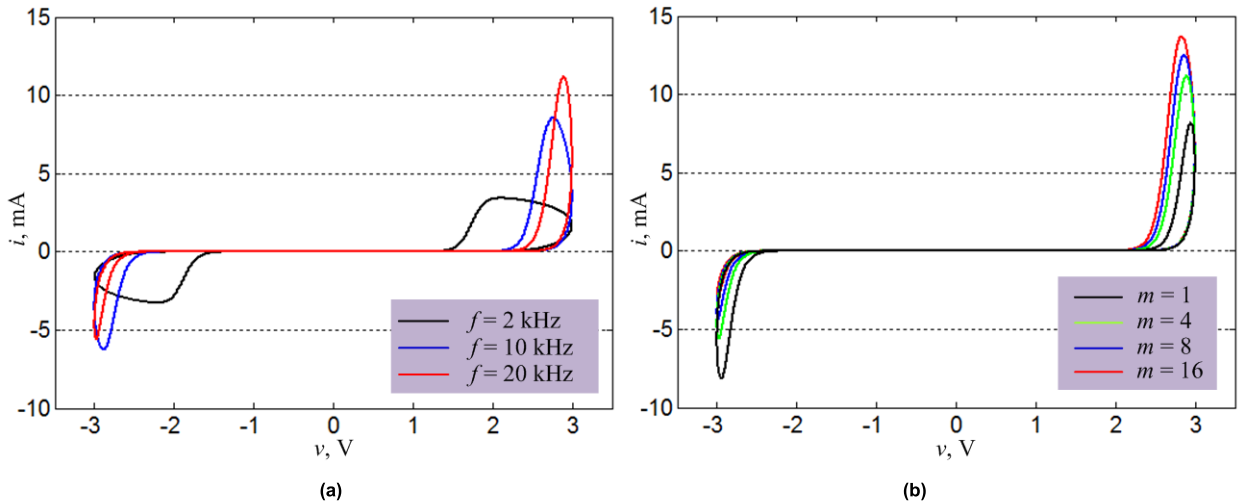
FIGURE 4. Numerical simulated hysteresis loops for the parallel-type AMDB emulator with $R_0 = 1.3$ kΩ and $C_0 = 100$ nF, (a) $m = 4$, $f = 2$ kHz, 10 kHz and 20 kHz; (b) $f = 20$ kHz, $m = 1$, 4, 8 and 16.

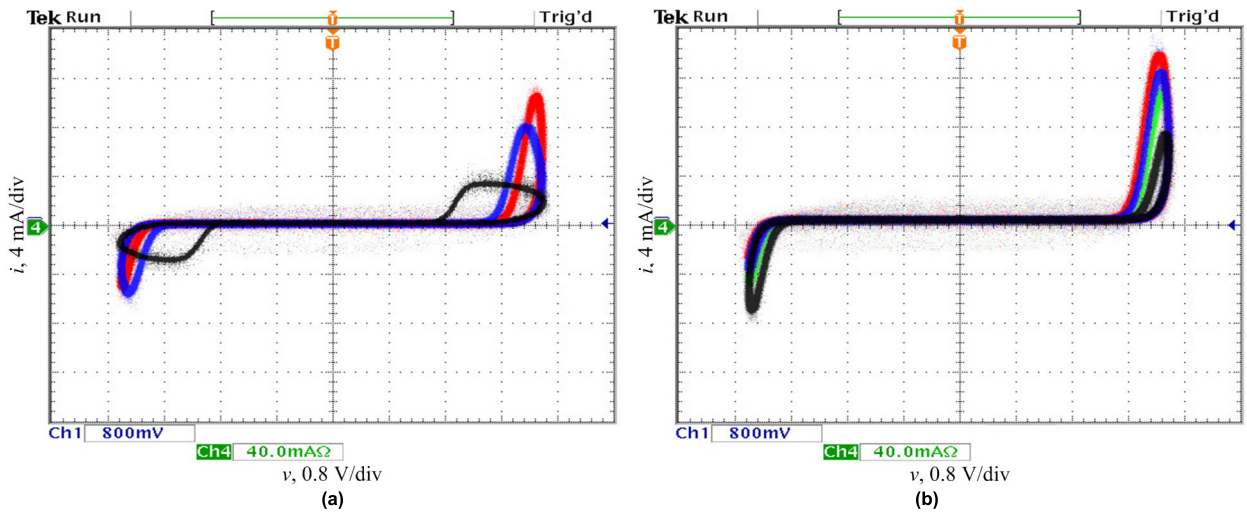**FIGURE 5.** Experimental captured hysteresis loops for the parallel-type AMDB emulator with $R_0 = 1.3$ kΩ and $C_0 = 100$ nF, (a) $m = 4$, $f = 2$ kHz, 10 kHz and 20 kHz; (b) $f = 20$ kHz, $m = 1$, 4, 8 and 16. Note that the output signal in Ch4 is enlarged by 10 times of the captured current i.
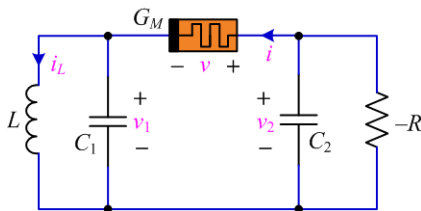

FIGURE 6. Parallel-type AMDB emulator-based Chua's circuit.

In fact, once the symmetry of the diode-bridge is broken by connecting some diodes in parallel to one or two bridge arms, an asymmetric memristive diode-bridge emulator is established. Here, we just present a typical case that an equal number of diodes are connected in parallel to the first and third bridge arms. Thus, the yielded mathematical model can be relatively simple.

B. CONFIRMATION OF VOLTAGE CONSTRAIN

The voltage constraints in (3) are the key fundamental for constructing mathematical model (12). Take the parallel-type AMDB emulator with $m = 4$, $R_0 = 1.3$ kΩ and $C_0 = 100$ nF as an example. Multisim simulations and hardware experiments are used to verify the correctness of the voltage constrains in (3).

Firstly, Multisim simulation circuit of the parallel-type AMDB emulator is built, consisting of ten 1N4148 diodes, one capacitor and one resistor. The AC voltage source is used to provide the periodic stimulus, and its peak voltage and frequency are set as 3 V and 20 kHz, respectively. Ociloscope XSC1 set as X-Y mode is utilized to capture the electrical signals. The screenshots of the simulation circuit and oscilloscope interactive interface are shown in Fig. 2. The observation objects in Fig. 2(a) are the terminal voltages of branches B_1 and B_3, whereas those in Fig. 2(b) are the terminal voltages of branches B_2 and B_4. The simulated
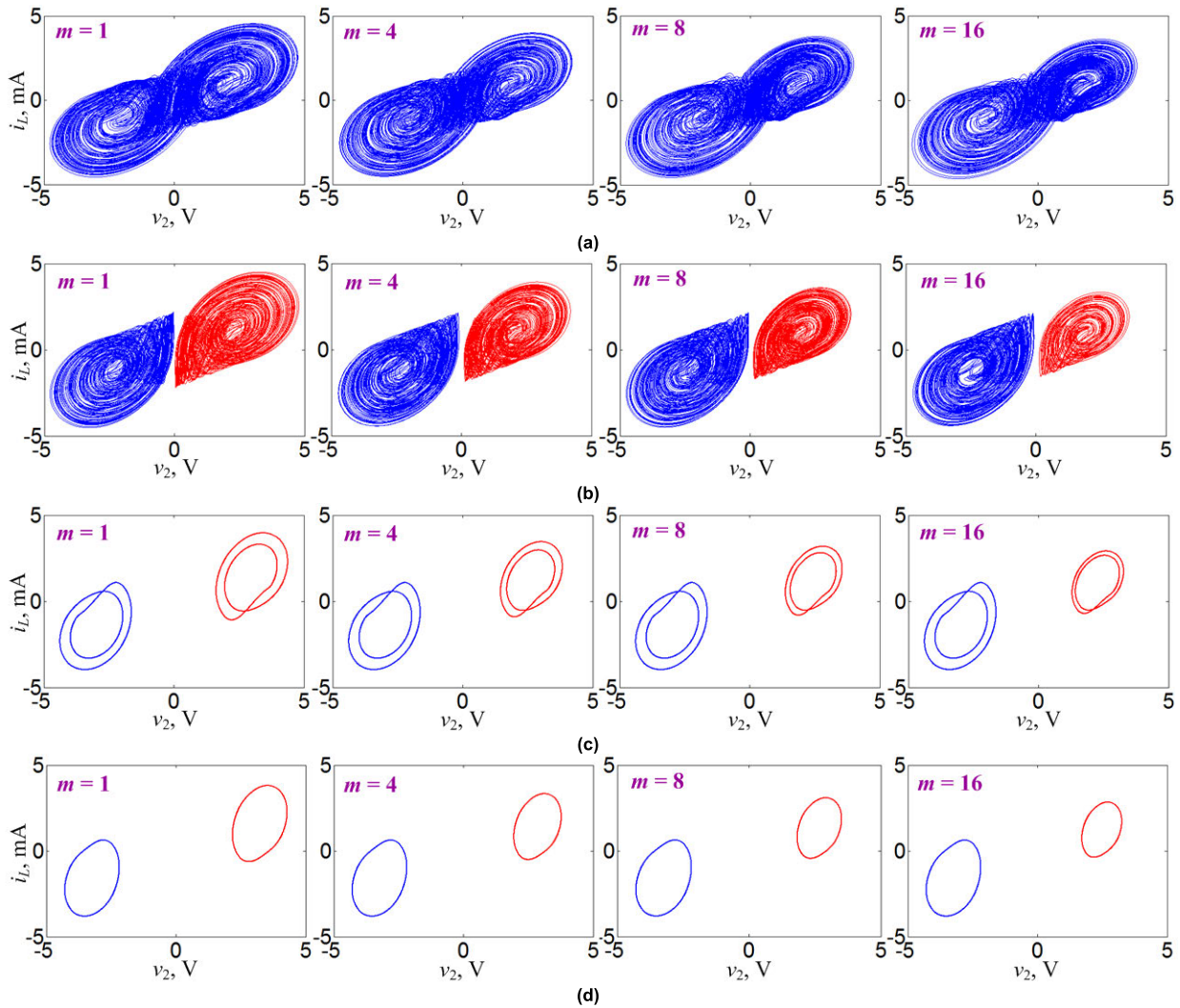
FIGURE 7. Topological evolutions of different types of attractors with m increasing from 1, to 4, to 8, and to 16. (a) double-scroll chaotic attractors under $C_2 = 15$ nF; (b) coexisting single-scroll chaotic attractors under $C_2 = 20$ nF; (c) coexisting period-2 limit cycles under $C_2 = 34$ nF; (d) coexisting period-1 limit cycles under $C_2 = 45$ nF. The blue and red attractors are initiated from $(-1$ nV, 0 V, 0 V, 0 V) and (1 nV, 0 V, 0 V, 0 V), respectively.
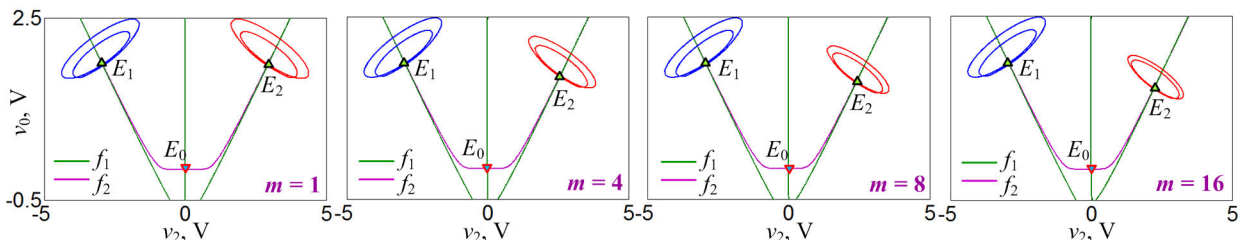
FIGURE 8. Equilibrium points fixed by the function curve intersections and phase portraits ($C_2 = 34$ nF) of system (13) with m increasing from 1, to 4, to 8, and to 16 in the v_2-v_0 plane. The blue and red attractors are initiated from $(-1$ nV, 0 V, 0 V, 0 V) and (1 nV, 0 V, 0 V, 0 V), respectively.

synchronous lines indicate that the two pairs of observed electrical signals are in complete synchronization.

Secondly, the physical hardware circuit is also welded and tested. Tektronix AFG3022 function generator is employed to provide the AC voltage source and Tektronix TDS 3034C is used to capture the experimental plots. Different from the Multisim simulation, two additional subtraction circuits are needed to detect the branch voltages, which can reduce the influence of voltage probes on the hardware circuit. Each subtraction circuit is composed of four 2 MΩ resistors and one AD711JN operational amplifier. The experimental results of the synchronous lines are shown in Fig. 3, which are consistent with the Multisim simulation plots in Fig. 2.

After the Multisim simulations and the hardware experiments, one can draw a conclusion that the voltage constrains in (3) are correct. Thus, the derived mathematical model in (12) is credible. Besides, from Figs. 2(a) and 3(a), one can notice that the forward voltages of the diode-bridge arms B_1 and B_3 are about 0.7 V. Addtionally, these voltages remain unchanged when m changes. As a result, the DPA in the parallel-type AMDB emulator can be constructed by much more diodes, without the limitation of forward voltage. However, for the series-type AMDB emulator reported in [32], when increasing the numerber of diodes, the forward voltage increases by multiplier. From this aspect, the parallel-type AMDB emulator is much better than the series-type AMDB emulator.

C. ASYMMETRIC HYSTERESIS LOOP

Pinched hysteresis loop is the fingerprint of a memristor under periodic stimulus [33]. When the parallel-type AMDB emulator is excited by an AC voltage source $V = 3\sin(2\pi ft)$, its volt-ampere curves in different parameters are plotted in Fig. 4. The RC filter with $R_0 = 1.3$ kΩ, $C_0 = 100$ nF is selected, and the 1N4148 diode with $I_S = 5.84$ nA, $n = 1.94$, $V_T = 26$ mV is used.

In Fig. 4(a), the parameter m is fixed as 4, and the frequency f is set to 2 kHz, 10 kHz, and 20 kHz, respectively. It can be seen that each volt-ampere curve is pinched at the origin, implying the current will vanish when the applied AC voltage vanishes. When increasing the frequency, the lobe area of the volt-ampere curve decreases, but the difference between the peak current and valley current increases. In short, with the increase of f, the asymmetry of hysteresis loop becomes remarkable. In Fig. 4(b), f is fixed as 20 kHz, and m is set to 1, 4, 8 and 16, respectively. With the increase of m, the left lobe area becomes smaller and smaller, whereas the right lobe area gets bigger and bigger. That is to say the differences between the peak currents and valley currents are gradually enhanced when increasing the parameter m. As can be seen, with the frequency evolution, the parallel-type AMDB emulator can exhibit the asymmetric hysteresis loops pinched at the origin ($G(v_0, 0) \neq \infty$). This implies that the parallel-type AMDB emulator belongs to the extended memristor but without non-volatile property [33].

Also, the hardware experiments for the pinched hysteresis loops are completed according to Fig. 1. The corresponding results are plotted in Fig. 5. Tektronix TCP213A current probe is used to detect the port currents of the parallel-type AMDB emulator. For better visual effect, the test wire is wound around the current probe ten turns, i.e., the output signal in Ch4 (40 mAΩ/div) is enlarged by 10 times of the test current i (4 mA/div). The experimental results in Fig. 5 match well with the numerical results in Fig. 4.

III. PARALLEL-TYPE AMDB EMULATOR-BASED CHUA'S CIRCUIT

Chua's diode is a nonlinear resistor. It is the key element for achieving chaotic oscillations in Chua's circuit. Generally,

TABLE 1. Realization of the non-standard capacitor.

Theoretical value	Tantalum capacitors in parallel	Measured value
15 nF	Two 10 nF capacitors	15.5 nF
20 nF	One 10 nF and five 1 nF capacitors	20.2 nF
34 nF	One 10 nF and one 22 nF capacitors	29.5 nF
45 nF	One 47 nF capacitor	42.7 nF
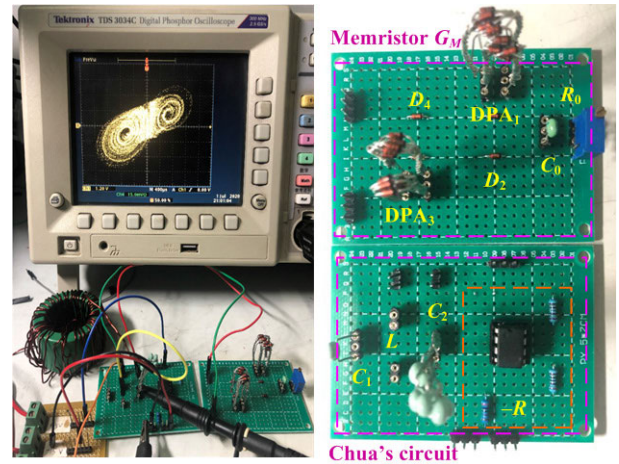
FIGURE 9. Hardware breadboard of the asymmetric memristor-based Chua's circuit and the experimentally captured asymmetric double-scroll chaotic attractor.

Chua's circuit can generate symmetric double-scroll attractors, symmetric coexisting single-scroll attractors, or symmetric multi-scroll attractors [34]–[38]. In this part, the parallel-type AMDB emulator-based Chua's circuit is taken as an example to explore the dynamical effect of asymmetric nonlinearity.

A. MEMRISTIVE CIRCUIT AND ITS ATTRACTORS

To demonstrate the dynamical effect of asymmetric nonlinearity, an asymmetric memristor-based Chua's circuit is constructed using a parallel-type AMDB emulator to couple a passive LC network and an active RC filter, as shown in Fig. 6. The voltages v_1, v_2 across the capacitors C_1 and C_2, and the current i_L flowing through the inductor L are chosen as the state variables. Together with the inner state variable v_0 of the parallel-type AMDB emulator G_M, there are four state variables, namely, v_1, v_2, i_L and v_0.

Based on the mathematical model of the parallel-type AMDB emulator, when applying Kirchhoff's law to the asymmetric memristor-based Chua's circuit in Fig. 6, the circuit state equations can be described as

$$C_1 \frac{dv_1}{dt} = I_S[me^{\xi(v-v_0)} - e^{-\xi(v+v_0)} - m + 1] - i_L,$$

$$C_2 \frac{dv_2}{dt} = \frac{v_2}{R} - I_S[me^{\xi(v-v_0)} - e^{-\xi(v+v_0)} - m + 1],$$
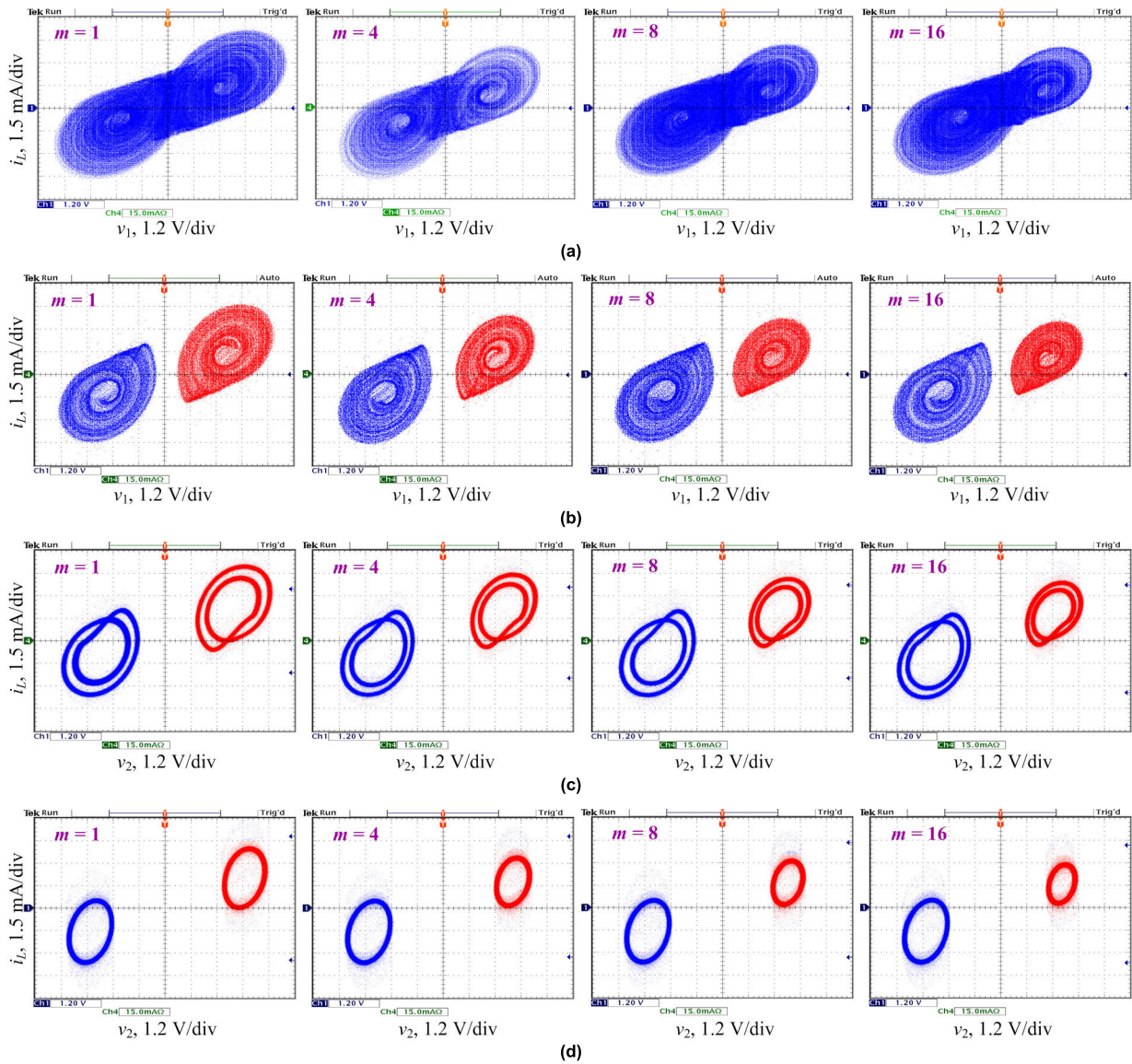
FIGURE 10. Experimental results of the phase plots with different C_2 (a) double-scroll chaotic attractors, $C_2 = 15.5$ nF, (b) coexisting single-scroll chaotic attractors, $C_2 = 20.2$ nF; (c) coexisting period-2 limit cycles, $C_2 = 29.5$ nF; (d) coexisting period-1 limit cycles, $C_2 = 42.7$ nF.

$$C_0 \frac{dv_0}{dt} = I_S[me^{\xi(v-v_0)} + e^{-\xi(v+v_0)} - m - 1] - \frac{v_0}{R_0},$$

$$L \frac{di_L}{dt} = v_1, \tag{13}$$

where $v = v_2 - v_1$. Seen from (13), all the nonlinear terms are related to the parallel-type AMDB emulator. It means that the parallel-type AMDB emulator has a great influence on the attractor topologies of system (13). This influence can be revealed by MATLAB numerical simulations based on (13), in which the circuit parameters are fixed as $C_1 = 10$ nF, $L = 20$ mH, $R = 2$ kΩ, $R_0 = 1.3$ kΩ, and $C_0 = 100$ nF, and the other two parameters, C_2 and m, are taken as the controllable parameters.

For fixed $C_2 = 15$ nF, set m to 1, 4, 8 and 16, respectively. System (13) generates double-scroll chaotic attrac-

tors, as shown in Fig. 7(a). Similarly, by adjusting C_2 to 20 nF, to 34 nF, to 45 nF, system (13) can generate three different types of attractors, including coexisting single-scroll chaotic attractors, coexisting period-2 and period-1 limit cycles, as plotted in Figs. 7(b)-(d). In Fig. 7, the blue and red attractors are initiated from $(-1$ nV, 0 V, 0 V, 0 V) and (1 nV, 0 V, 0 V, 0 V), respectively. Note that the nonzero initial value is used to provide a weak perturbation for the autonomous system (13).

Obviously, from the phase plots in the first column ($m = 1$) in Fig. 7, it can be seen that the left- and right-scroll attractors are symmetric about the origin. By contrast, from the second column ($m = 4$), third column ($m = 8$), and fourth column ($m = 16$), it can be found that the right-scroll attractors become smaller and smaller. Therefore, the difference

between the right- and left-scroll attractors is becoming more and more apparent. One can also find that this evolution is consistent with that of the asymmetric hysteresis loops exhibited by the parallel-type AMDB emulator.

B. EQUILIBRIUM POINT ANSLYSIS

For the parallel-type AMDB emulator-based Chua's system, the equilibrium point is expressed as $E = (0, \tilde{v}_2, \tilde{v}_0, \tilde{i}_L)$, in which $\tilde{i}_L = I_S[me^{\xi(\tilde{v}_2 - \tilde{v}_0)} - e^{-\xi(\tilde{v}_2 + \tilde{v}_0)} - m + 1]$, and $\tilde{v}_2$ and $\tilde{v}_0$ can be obtained by solving the following equations

$$f_1 = -me^{\xi(\tilde{v}_2 - \tilde{v}_0)} + e^{-\xi(\tilde{v}_2 + \tilde{v}_0)} + m - 1 + \frac{\tilde{v}_2}{RI_S} = 0,$$

$$f_2 = me^{\xi(\tilde{v}_2 - \tilde{v}_0)} + e^{-\xi(\tilde{v}_2 + \tilde{v}_0)} - m - 1 - \frac{\tilde{v}_0}{R_0 I_S} = 0. \quad (14)$$

As can be seen, the equilibrium point E has no connection with the capacitance C_2. Take the asymmetric coexisting limit cycles at $C_2 = 34$ nF as examples to explain the equilibrium point evolutions with m increasing.

By using the graphical method, the equilibrium points fixed by the function curve intersections and phase portraits with different m in the v_2-v_0 plane are depicted in Fig.8. MATLAB function 'ezplot' is employed to plot the curves of f_1 and f_2. As can be clearly seen, system (13) has one zero equilibrium point E_0 and two non-zero equilibrium points E_1 and E_2. The coexisting period-2 limit cycles are generated around E_1 or E_2. With m increasing, E_0 and E_1 keep unchanged, while E_2 gradually glides along the f_2 in the first quadrant. As a result, the asymmetric limit cycle pairs are thereby coexisted.

C. EXPERIMENTAL RESULTS

Based on one chip of AD711JN operational amplifier, one inductance coil and some other discrete components, the hardware breadboard of the asymmetric memristor-based Chua's circuit is fabricated, as shown in Fig. 9. The inductance coil is measured as 18.3 mH with the parasitic resistance 2 Ω. An AD711JN operational amplifier is employed to realize the negative resistor $-R$. And the non-standard capacitances of C_2 are obtained byparalleling several tantalum capacitors, as listed in Tab. 1. Tektronix TDS 3034C with Tektronix TCP213A current probe is used to capture the experimental results of the phase plots. The results are displayed in Fig. 10, which are in good agreement with the numerical ones given in Fig. 7. It is noticed that the coexisting left- or right-attractor is emerged by switching the power on and off repeatedly.

IV. CONCLUSION

This paper reported a novel parallel-type AMDB emulator implemented by an asymmetric diode-bridge cascaded with a RC filter. The mathematical modeling, Multisim circuit analyses, MATLAB numerical simulations, and breadboard hardware experiments were executed. The parallel-type AMDB emulator, inexpensive and easy to be physically fabricated with the on-the-shelf components, was confirmed to behave

the pinched property of physical memristor device. In addition, the parallel-type AMDB emulator-based Chua's circuit was taken as an example. Due to the existence of asymmetric nonlinearity, the equilibrium points of memristive Chua's circuit are asymmetrically distributed in the phase space, resulting in the appearance of different types of asymmetric attractors. Of course, the dynamical mechanism is more complex and interesting, which will be studied in our next work.

DATA AVAILABILITY

The data used to support the findings of this study are available from the corresponding author upon request.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

[1] L. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.
[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found?" *Nature*, vol. 453, pp. 80–83, May 2008.
[3] Y. Babacan and F. Kaçar, "Floating memristor emulator with subthreshold region," *Anal. Integr. Circuits Signal Process.*, vol. 90, no. 2, pp. 471–475, Feb. 2017.
[4] I. Vourkas, D. Stathis, G. C. Sirakoulis, and S. Hamdioui, "Alternative architectures toward reliable memristive crossbar memories," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 1, pp. 206–217, Jan. 2016.
[5] S. Xiao, X. Xie, S. Wen, Z. Zeng, T. Huang, and J. Jiang, "GST-memristor-based online learning neural networks," *Neurocomputing*, vol. 272, pp. 677–682, Jan. 2018.
[6] T. Chen, L. Wang, and S. Duan, "Implementation of circuit for reconfigurable memristive chaotic neural network and its application in associative memory," *Neurocomputing*, vol. 380, pp. 36–42, Mar. 2020.
[7] H. Bao, A. Hu, W. Liu, and B. Bao, "Hidden bursting firings and bifurcation mechanisms in memristive neuron model with threshold electromagnetic induction," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 31, no. 2, pp. 502–511, Feb. 2020.
[8] H. Wu, Y. Ye, M. Chen, Q. Xu, and B. Bao, "Extremely slow passages in low-pass filter-based memristive oscillator," *Nonlinear Dyn.*, vol. 97, no. 4, pp. 2339–2353, Jul. 2019.
[9] H. G. Wu, Y. Ye, B. C. Bao, M. Chen, and Q. Xu, "Memristor initial boosting behaviors in a two-memristor-based hyperchaotic system," *Chaos, Solitons Fractals*, vol. 121, pp. 178–185, Apr. 2019.
[10] Q. Xu, Q. Zhang, B. Bao, and Y. Hu, "Non-autonomous second-order memristive chaotic circuit," *IEEE Access*, vol. 5, pp. 21039–21045, Jul. 2017.
[11] Z. Li, C. Zhou, and M. Wang, "Symmetrical coexisting attractors and extreme multistability induced by memristor operating configurations in SC-CNN," *AEU—Int. J. Electron. Commun.*, vol. 100, pp. 127–137, Feb. 2019.
[12] Z. Wen, Z. Li, and X. Li, "Bursting dynamics in parametrically driven memristive jerk system," *Chin. J. Phys.*, vol. 66, pp. 327–334, Aug. 2020, doi: 10.1016/j.cjph.2020.04.009.
[13] H. Lin, C. Wang, Q. Hong, and Y. Sun, "A multi-stable memristor and its application in a neural network," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, early access, Jun. 8, 2020, doi: 10.1109/TCSII.2020.3000492.
[14] Y. Dong, G. Wang, G. Chen, Y. Shen, and J. Ying, "A bistable nonvolatile locally-active memristor and its complex dynamics," *Commun. Nonlinear Sci. Numer. Simul.*, vol. 84, May 2020, Art. no. 105203.
[15] H. Wu, Y. Ye, M. Chen, Q. Xu, and B. Bao, "Periodically switched memristor initial boosting behaviors in memristive hypogenetic jerk system," *IEEE Access*, vol. 7, pp. 145022–145029, Oct. 2019.
[16] M. Nigus Getachew, R. Priyadarshini, and R. M. Mehra, "SPICE model of HP-memristor using PWL window function for neuromorphic system design application," *Mater. Today, Proc.*, Feb. 2020, doi: 10.1016/j.matpr.2020.01.540.
[17] A. G. Alharbi, M. E. Fouda, Z. J. Khalifa, and M. H. Chowdhury, "Electrical nonlinearity emulation technique for current-controlled memristive devices," *IEEE Access*, vol. 5, pp. 5399–5409, 2017.

[18] V. K. Sharma, M. S. Ansari, and T. Parveen, "Tunable memristor emulator using Off-The-Shelf components," *Procedia Comput. Sci.*, vol. 171, pp. 1064–1073, 2020.

[19] A. Yesil, "A new grounded memristor emulator based on MOSFET-C," *AEU - Int. J. Electron. Commun.*, vol. 91, pp. 143–149, Jul. 2018.

[20] Q. Xu, Q. L. Zhang, H. Qian, H. G. Wu, and B. C. Bao, "Crisis-induced coexisting multiple attractors in a second-order nonautonomous memristive diode bridge-based circuit," *Int. J. Circuit Theory Appl.*, vol. 46, no. 10, pp. 1917–1927, May 2018.

[21] B. Bao, J. Yu, F. Hu, and Z. Liu, "Generalized memristor consisting of diode bridge with first order parallel RC filter," *Int. J. Bifurcation Chaos*, vol. 24, no. 11, Nov. 2014, Art. no. 1450143.

[22] L. Minati, L. V. Gambuzza, W. J. Thio, J. C. Sprott, and M. Frasca, "A chaotic circuit based on a physical memristor," *Chaos, Solitons Fractals*, vol. 138, Sep. 2020, Art. no. 109990.

[23] J. Kengne, R. L. T. Mogue, T. F. Fozin, and A. N. K. Telem, "Effects of symmetric and asymmetric nonlinearity on the dynamics of a novel chaotic jerk circuit: Coexisting multiple attractors, period doubling reversals, crisis, and offset boosting," *Chaos, Solitons Fractals*, vol. 121, pp. 63–84, Apr. 2019.

[24] J. Gu, C. Li, Y. Chen, H. H. C. Iu, and T. Lei, "A conditional symmetric memristive system with infinitely many chaotic attractors," *IEEE Access*, vol. 8, pp. 12394–12401, 2020.

[25] S. R. Bishop, A. Sofroniou, and P. Shi, "Symmetry-breaking in the response of the parametrically excited pendulum model," *Chaos, Solit. Fractals*, vol. 25, no. 2, pp. 264–277, Jul. 2005.

[26] H. Cao, J. M. Seoane, and M. A. F. Sanjuán, "Symmetry-breaking analysis for the general Helmholtz–Duffing oscillator," *Chaos, Solitons Fractals*, vol. 34, no. 2, pp. 197–212, Oct. 2007.

[27] M. Heinrich, T. Dahms, V. Flunkert, S. W. Teitsworth, and E. Schöll, "Symmetry-breaking transitions in networks of nonlinear circuit elements," *New J. Phys.*, vol. 12, no. 11, Nov. 2010, Art. no. 113030.

[28] L. Kamdjeu Kengne, H. T. Kamdem Tagne, A. N. Kengnou Telem, J. R. Mboupda Pone, and J. Kengne, "A broken symmetry approach for the modeling and analysis of antiparallel diodes-based chaotic circuits: A case study," *Anal. Integr. Circuits Signal Process.*, vol. 104, no. 2, pp. 205–227, May 2020.

[29] L. Kamdjeu Kengne, J. Kengne, N. A. Kengnou Telem, J. R. Mboupda Pone, and H. T. Kamdem Tagne, "Asymmetry-induced dynamics for a class of diode-based chaotic circuits: A case study," *J. Circuits, Syst. Comput.*, Jul. 2020, doi: 10.1142/s0218126621500778.

[30] L. K. Kengne, H. T. K. Tagne, J. R. M. Pone, and J. Kengne, "Dynamics, control and symmetry-breaking aspects of a new chaotic jerk system and its circuit implementation," *Eur. Phys. J. Plus*, vol. 135, no. 3, pp. 1–28, Mar. 2020.

[31] L. K. Kengne, J. R. M. Pone, H. T. K. Tagne, and J. Kengne, "Dynamics, control and symmetry breaking aspects of a single opamp-based autonomous LC oscillator," *AEU-Int. J. Electron. Commun.*, vol. 118, p. 53146, May 2020.

[32] M. Hua, S. Yang, Q. Xu, M. Chen, H. Wu, and B. Bao, "Forward and reverse asymmetric memristor-based jerk circuits," *AEU—Int. J. Electron. Commun.*, vol. 123, Aug. 2020, Art. no. 153294.

[33] L. O. Chua, "If it's pinched it's a memristor," *Semicond. Sci. Technol.*, vol. 29, no. 10, p. 104001, 2014.

[34] R. Barboza and L. O. Chua, "The four-element Chua'S circuit," *Int. J. Bifurcation Chaos*, vol. 18, no. 4, pp. 943–955, Apr. 2008.

[35] K. Rajagopal, S. Kacar, Z. Wei, P. Duraisamy, T. Kifle, and A. Karthikeyan, "Dynamical investigation and chaotic associated behaviors of memristor Chua's circuit with a non-ideal voltage-controlled memristor and its application to voice encryption," *AEU—Int. J. Electron. Commun.*, vol. 107, pp. 183–191, Jul. 2019.

[36] M. Chen, M. Sun, H. Bao, Y. Hu, and B. Bao, "Flux–Charge analysis of Two-Memristor-Based Chua's circuit: Dimensionality decreasing model for detecting extreme multistability," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 2197–2206, Mar. 2020.

[37] N. Wang, C. Li, H. Bao, M. Chen, and B. Bao, "Generating multiscroll Chua's attractors via simplified piecewise-linear Chua's diode," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4767–4779, Dec. 2019.

[38] Q. Xu, Y. Lin, B. Bao, and M. Chen, "Multiple attractors in a non-ideal active voltage-controlled memristor based Chua's circuit," *Chaos, Solitons Fractals*, vol. 83, pp. 186–200, Feb. 2016.

YI YE (Graduate Student Member, IEEE) received the B.S. degree in electronic information engineering from the Changzhou Institute of Technology, Changzhou, China, in 2017. He is currently pursuing the M.S. degree in electronic circuits and systems with Changzhou University. His research interests include analysis and implementation of memristor equivalent circuits, and memristive and chaotic systems.
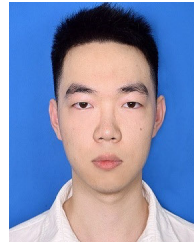
JIE ZHOU (Graduate Student Member, IEEE) received the B.S. degree in electronic science and technology from the Xuzhou Institute of Technology, Xuzhou, China, in 2019. He is currently pursuing the M.S. degree in electronic circuits and systems with Changzhou University. His research interests include analysis and implementation of memristor equivalent circuits, and memristive and chaotic systems.

QUAN XU (Member, IEEE) was born in Lianyungang, China, in 1983. He received the B.S. degree in physics from the Huaiyin Teachers College in 2005, and the M.S. and Ph.D. degrees in optical engineering from the University of Electronics Science and Technology of China in 2011.

Since 2011, he has been a Lecturer with Changzhou University, China, where he is currently an Associate Professor. He has authored more than 30 articles and holds more than ten inventions. His research interests include memristor and its applications, and memristive neuromorphic circuits.

MO CHEN (Member, IEEE) received the B.S. degree in information engineering, and the M.S. and Ph.D. degrees in electromagnetic field and microwave technology from Southeast University, Nanjing, China, in 2003, 2006, and 2009, respectively. From March 2009 to July 2013, she was a Lecturer with Southeast University. She is currently an Associate Professor with the School of Information Science and Engineering, Changzhou University, Changzhou, China. Her research interests include memristor and its application circuits, and other nonlinear circuits and systems.

HUAGAN WU (Member, IEEE) received the B.S. degree in electrical information engineering and automation from the Jiangsu University of Technology, Changzhou, China, in 2010, and the M.S. and Ph.D. degrees in information and communication engineering from the Nanjing University of Science and Technology, Nanjing, China, in 2015.

She is currently a Lecturer with the School of Information Science and Engineering, Changzhou University, Changzhou. Her research interests include memristor and its application circuits, and other nonlinear circuits and systems.

● ● ●