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Model Predictive Current Control for Fault-Tolerant Bidirectional Voltage Source Converter With Open Circuit Fault and Unbalanced Grid Voltage

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ABSTRACT To improve the fault-tolerant operation capability of bidirectional voltage source converter (BVSC), an improved model predictive current control (IMPCC) for fault-tolerant BVSC, is proposed with balanced DC-link capacitor voltage under unbalanced grid voltage. The proposed method can maintain continuous operation even if power device faults and unbalanced grid voltage faults occur together. A current predictive model of the fault-tolerant BVSC is established. By using grid voltages and 90° lagging signals in the $\alpha\beta$ stationary coordinate system, the reference current calculation method is designed for BVSC to eliminate power ripple under unbalanced grid voltage, which can avoid the complex positive and negative sequence extraction. DC-link split capacitor voltage balancing is achieved by the improved cost function. Based on the current predictive model and improved cost function, the optimal space voltage vectors are selected for fault-tolerant BVSC. Compared to the existing predictive methods, the proposed IMPCC can balance DC-link capacitor voltage and eliminate the power ripples for fault-tolerant BVSC under unbalanced grid with simple implementation. The experimental results validate the effectiveness of the proposed control scheme.

INDEX TERMS Bidirectional voltage source converter, fault-tolerant, open circuit faults, unbalanced grid voltage, predictive current control.

I. INTRODUCTION

The main goal of the fault-tolerant power converter is to work continuously even with reduced performance when converter faults occur during normal operation. Due to the increasing use of grid-connected systems, such as photovoltaic panels, wind energy, and batteries, the reliability and fault-tolerant capability of a bidirectional voltage source converter (BVSC) has become an urgent issue for hybrid microgrid [1]–[4]. The reliability of power converter is influenced by many factors, such as operation environment, hardware, and software design, packaging, etc. According to [1], more than 80% of converter faults are caused by switching devices faults, including open circuit, short circuit, and gate driver signal faults. Therefore, it has significant meaning to study the fault-tolerant capability of BVSC to improve the fault-tolerant capability of the power conversion system.

To enhance the fault-tolerant capability of power converters, fault-tolerant topologies and control schemes have been developed. Different fault-tolerant applications have been studied, including pulse width modulation (PWM) rectifier, and renewable power generation [5]–[8]. The three-phase four-switch (TPFS) converter topology which is a fault-tolerant topology of a three-phase six-switch (TPSS) converter, can maintain continuous operation with switching devices open circuit faults in a phase leg. The control schemes of TPFS are classified into two categories: modulation based linear control and nonlinear control. The vector

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PWM strategy for TPFS inverters can select three or four vectors by space vector modulation. These fault-tolerant methods of the TPFS converter rely on the PWM control method [8], [9], which needs coordinates transformation and modulation module with complex algorithms. Furthermore, these methods for TPFS are all for the conditions of a balanced grid and do not consider unbalanced grid voltage.

The unbalanced grid voltage is a common fault because of unbalanced three-phase loads. The unbalanced grid voltage will increase the total harmonic distortion (THD) of grid-connected currents and power ripples [10], [11]. A unified model of voltage source converter and control scheme with multi-frequency proportional-resonant is proposed to improve the performance under unbalanced grid conditions in [12]. An improved model predictive direct power control (MPDPC) for PWM rectifiers is proposed in [13]. However, these methods require the phase-locked loop (PLL), positive and negative sequence extraction. In the traditional PWM control, the positive and negative sequences of voltage and current are separated [14] where the calculations of control methods are significant and complex.

Direct power control (DPC) selects the optimal voltage vector directly from the limited vectors, which has a fast dynamic response [15], [16]. A nonlinear sliding mode DPC is proposed for a voltage source converter to simplify the system design and enhance the transient performance without an extra current loop [17]. The DPC switching patterns are investigated in detail, and a hysteresis controller is proposed to eliminate the active power steady-state error [18]. However, this research only focuses on the control schemes of the TPSS converter. Hence, it is necessary to study the control strategy for the fault-tolerant BVSC under dual fault conditions to enhance the fault-tolerant capability.

Model predictive control (MPC) can keep flexible control for different variables and constraints. The optimal voltage vectors are achieved by MPC [19]–[33]. Compared to modulation based linear control techniques, Park transformation, sequence extraction, and PLL are not needed in MPC. As a result, the calculation amount can be significantly reduced. MPC scheme can be used both in TPSS [26]–[28] and TPFS converter [29], [31]. A multi-vector model predictive power control is proposed to minimize power ripple and achieve capacitor voltage balancing control [29]. However, these studies only consider balanced grid conditions. If the grid voltages are unbalanced, the current harmonics and power ripples will increase significantly, which needs to be studied in depth

In this paper, an improved model predictive current control (IMPCC) method is proposed for fault-tolerant BVSC to reduce current harmonic distortion and power ripples under the conditions of switch open circuit and unbalanced grid voltages. The proposed method provides high reliability for the bidirectional power conversion. Experimental comparisons between the proposed and conventional methods are presented to verify the performance of the proposed control scheme. When the phase leg faults and unbalanced grid conditions occur, the fault-tolerant BVSC can keep continuous operation, which improves the reliability of the bidirectional power conversion.

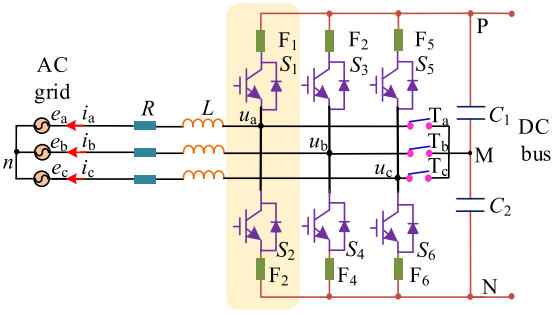

FIGURE 1. The fault-tolerant topology of BVSC.

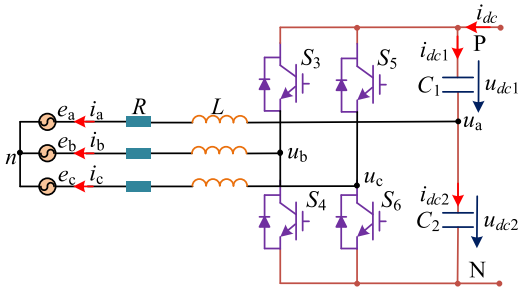

FIGURE 2. Three-phase four-switch fault-tolerant topology with phase leg a fault.

II. NONREDUNDANT FAULT-TOLERANT BVSC MODEL

In this paper, the control scheme of BVSC with an open circuit or short circuit faults of power devices in a phase leg is studied. Usually, the fast fuse devices are connected in series with the power devices. The short circuit faults can be converted to open circuit faults once the fusible element opens. The topology of nonredundant fault-tolerant BVSC is shown in Fig. 1. The midpoint M of the dc-link split capacitor is connected with the corresponding grid phase with additional bidirectional switches (T_a, T_b, T_c), such as TRIACS or IGBT with a diode rectifier bridge. When an open circuit or short circuit faults occur, the fast fuse will be opened and the bidirectional switch will be conducted to replace the faulted leg [1]. When there is a switch fault in phase leg a, the reconstructed fault-tolerant BVSC is shown in Fig. 2.

According to Kirchhoff's law, the voltage equation of the fault-tolerant converter in *abc* coordinates system can be expressed by:

$$L\frac{di_{abc}}{dt} + Ri_{abc} = u_{abc} - e_{abc} \tag{1}$$

where u_{abc}, i_{abc}, e_{abc} are the converter output voltages, grid-connected currents, and grid voltages, respectively.

After Clark transformation of (1), the state equation in the $\alpha\beta$ coordinates can be obtained as:

$$L\frac{di_{\alpha\beta}}{dt} + Ri_{\alpha\beta} = u_{\alpha\beta} - e_{\alpha\beta} \tag{2}$$

where $i_{\alpha\beta}$, $u_{\alpha\beta}$, $e_{\alpha\beta}$ are the grid-connected current, converter output voltage, and grid voltage, respectively.

The switch fault may occur in phases a, b, or c. With different fault conditions, the switching states $S_i (i = a, b, c)$ are defined as:

$$S_a = \begin{cases} 1 & \text{if } S_1 \text{ is on and } S_2 \text{ is off} \\ 0 & \text{if } S_1 \text{ is off and } S_2 \text{ is on} \end{cases} \tag{3}$$

$$S_b = \begin{cases} 1 & \text{if } S_3 \text{ is on and } S_4 \text{ is off} \\ 0 & \text{if } S_3 \text{ is off and } S_4 \text{ is on} \end{cases} \tag{4}$$

$$S_c = \begin{cases} 1 & \text{if } S_5 \text{ is on and } S_6 \text{ is off} \\ 0 & \text{if } S_5 \text{ is off and } S_6 \text{ is on} \end{cases} \tag{5}$$

In Fig. 2, when the phase a leg has faults, the faulty phase is connected to the dc-link mid-point. S_b and S_c can be controlled. The output voltage of fault-tolerant BVSC is expressed by switching states as [6]:

$$\begin{cases} uan = \dfrac{u_{dc1}}{3}(-S_b - S_c) + \dfrac{u_{dc2}}{3}(2 - S_b - S_c) \\ ubn = \dfrac{u_{dc1}}{3}(2S_b - S_c) + \dfrac{u_{dc2}}{3}(2S_b - S_c - 1) \\ ucn = \dfrac{u_{dc1}}{3}(2S_c - S_b) + \dfrac{u_{dc2}}{3}(2S_c - S_b - 1) \end{cases} \tag{6}$$

where u_{dc1}, u_{dc2} are voltages of dc-link split capacitor C_1 and C_2, respectively. u_{an}, u_{bn}, u_{cn} present the output voltages of BVSC.

Different from the conventional BVSC, in Fig.2, there are only four voltage vectors (0 0), (0 1), (1 0), (1 1) for fault-tolerant BVSC.

Assuming the sampling period is defined as T_s, the derivative of grid-connected currents can be expressed as:

$$\frac{di_{\alpha\beta}}{dt} = \frac{i_{\alpha\beta}(k+1) - i_{\alpha\beta}(k)}{T_s} \tag{7}$$

Simplifying (2), the discrete equation can be expressed as follows:

$$i_{\alpha\beta}(k+1) = \frac{T_S\left(u_{\alpha\beta}(k) - e_{\alpha\beta}(k)\right)}{L} + \left(1 - \frac{RT_s}{L}\right) i_{\alpha\beta}(k) \tag{8}$$

where $i_{\alpha\beta}(k)$, $u_{\alpha\beta}(k)$, $e_{\alpha\beta}(k)$ are the $\alpha\beta$ components of the grid-connected current, output voltage and grid voltage at k^{th} sampling instant. $i_{\alpha\beta}(k+1)$ is the predictive current in the $\alpha\beta$ coordinate of the $(k+1)^{\text{th}}$ sampling time.

III. POWER MATHEMATICAL MODEL UNDER UNBALANCED GRID VOLTAGE

The positive and negative sequence components of grid voltages and currents under unbalanced grid voltage can be obtained as follows:

$$\begin{cases} e = \left(e_d^+ + je_q^+\right) e^{j\omega t} + \left(e_d^- + je_q^-\right) e^{-j\omega t} \\ i = \left(i_d^+ + ji_q^+\right) e^{j\omega t} + \left(i_d^- + ji_q^-\right) e^{-j\omega t} \end{cases} \tag{9}$$

where e_{dq}^+, e_{dq}^-, i_{dq}^+, i_{dq}^- are the positive and negative sequence components of the grid voltage and current, respectively. ω is the angular frequency of grid voltage. According to instantaneous power theory, the grid side power of converter can be expressed as:

$$S_g = P_g + jQ_g \tag{10}$$

$$\begin{cases} P_g = p_{av}^g + p_{c2}^g \cos(2\omega t) + p_{s2}^g \sin(2\omega t) \\ Q_g = q_{av}^g + q_{c2}^g \cos(2\omega t) + q_{s2}^g \sin(2\omega t) \\ p_{av}^g = e_d^+ i_d^+ + e_q^+ i_q^+ + e_d^- i_d^- + e_q^- i_q^- \\ p_{c2}^g = e_d^+ i_d^- + e_q^+ i_q^- + e_d^- i_d^+ + e_q^- i_q^+ \\ p_{s2}^g = e_d^+ i_q^- - e_q^+ i_d^- + e_d^- i_q^+ - e_q^- i_d^+ \\ q_{av}^g = e_q^+ i_d^+ - e_d^+ i_q^+ + e_q^- i_d^- - e_d^- i_q^- \\ q_{c2}^g = e_q^+ i_d^- - e_d^+ i_q^- + e_q^- i_d^+ - e_d^- i_q^+ \\ q_{s2}^g = e_d^+ i_d^- + e_q^+ i_q^- - e_d^- i_d^+ - e_q^- i_q^+ \end{cases} \tag{11}$$

where p_{av}^g, q_{av}^g, p_{c2}^g, p_{s2}^g, q_{c2}^g, q_{s2}^g are the average values and power ripples of active power P_g and reactive power Q_g.

To avoid using a sequential extraction procedure, the grid voltage vector $\boldsymbol{e}$, current vector $\boldsymbol{i}$ and their quadrature signals e', i' with lagging 90° are used. Then the positive and negative sequence components can be expressed by:

$$\begin{bmatrix} e_{dq}^+ \\ e_{dq}^- \\ i_{dq}^+ \\ i_{dq}^- \end{bmatrix} = \frac{1}{2} \begin{bmatrix} e^{-j\omega t} & je^{-j\omega t} & 0 & 0 \\ e^{j\omega t} & -je^{j\omega t} & 0 & 0 \\ 0 & 0 & e^{-j\omega t} & je^{-j\omega t} \\ 0 & 0 & e^{j\omega t} & -je^{j\omega t} \end{bmatrix} \times \begin{bmatrix} e_\alpha + je_\beta \\ e'_\alpha + je'_\beta \\ i_\alpha + ji_\beta \\ i'_\alpha + ji'_\beta \end{bmatrix} \tag{12}$$

Based on (12) and (11), output active power and reactive power can be expressed as follows:

$$\begin{cases} p_{av}^g = \dfrac{1}{2}(i_\alpha e_\alpha + i_\beta e_\beta + i'_\alpha e'_\alpha + i'_\beta e'_\beta) \\ q_{av}^g = \dfrac{1}{2}(i_\alpha e_\beta - i_\beta e_\alpha + i'_\alpha e'_\beta - i'_\beta e'_\alpha) \\ p_{c2}^g = \dfrac{1}{2}\begin{bmatrix} \left(i_\alpha e_\alpha + i_\beta e_\beta - i'_\alpha e'_\alpha - i'_\beta e'_\beta\right)\cos(2\omega t) \\ + \left(i_\alpha e'_\alpha + i_\beta e'_\beta + i'_\alpha e_\alpha + i'_\beta e_\beta\right)\sin(2\omega t) \end{bmatrix} \\ p_{s2}^g = \dfrac{1}{2}\begin{bmatrix} -\left(i_\alpha e'_\alpha + i_\beta e'_\beta + i'_\alpha e_\alpha + i'_\beta e_\beta\right)\cos(2\omega t) \\ + \left(i_\alpha e_\alpha + i_\beta e_\beta - i'_\alpha e'_\alpha - i'_\beta e'_\beta\right)\sin(2\omega t) \end{bmatrix} \\ q_{c2}^g = \dfrac{1}{2}\begin{bmatrix} \left(i_\alpha e_\beta - i_\beta e_\alpha - i'_\alpha e'_\beta + i'_\beta e'_\alpha\right)\cos(2\omega t) \\ + \left(i_\alpha e'_\beta - i_\beta e'_\alpha + i'_\alpha e_\beta - i'_\beta e_\alpha\right)\sin(2\omega t) \end{bmatrix} \\ q_{s2}^g = \dfrac{1}{2}\begin{bmatrix} -\left(i_\alpha e'_\beta - i_\beta e'_\alpha + i'_\alpha e_\beta - i'_\beta e_\alpha\right)\cos(2\omega t) \\ + \left(i_\alpha e_\beta - i_\beta e_\alpha - i'_\alpha e'_\beta + i'_\beta e'_\alpha\right)\sin(2\omega t) \end{bmatrix} \end{cases} \tag{13}$$

where e_α, e_β, e'_α, e'_β, i_α, i_β, i'_α, i'_β are grid voltage, current, and the 90° lagging signals, where the sequence extraction and PLL are not needed.

IV. MPC METHOD UNDER UNBALANCED GRID VOLTAGE CONDITIONS

This paper proposed an IMPCC method for fault-tolerant BVSC, which achieved DC-link capacitor voltage balancing, the current THD reduction and the elimination of reactive power ripples.

A. DC-LINK SPLIT CAPACITOR VOLTAGE BALANCE CONTROL

The capacitors C_1 and C_2 are in series connected in Fig. 1, where the values are the same. The capacitor voltages are obtained by:

$$\begin{cases} u_{dc1} = \dfrac{u_{dc}}{2} + \dfrac{1}{2C}\displaystyle\int_k^{k+1} i_a dt + \dfrac{u_{dc1}(k) - u_{dc2}(k)}{2} \\ u_{dc2} = \dfrac{u_{dc}}{2} - \dfrac{1}{2C}\displaystyle\int_k^{k+1} i_a dt - \dfrac{u_{dc1}(k) - u_{dc2}(k)}{2} \end{cases} \tag{14}$$

where $u_{dc1}(k)$, $u_{dc2}(k)$ are the voltage of C_1 and C_2 at k^{th} sampling instant, respectively.

The capacitor voltage u_{dc2} fluctuates around the $u_{dc}/2$ with offset $\Delta u_{dc}/2$. To reduce the voltage offset of the midpoint, a dc bias current $\bar{i}_a$ is designed to inject into the faulty phase current i_a. Then the voltage offset of DC-link midpoint can be expressed as:

$$\begin{aligned} \Delta u_{dc} &= u_{dc1} - u_{dc2} \\ &= \frac{1}{C}\int_k^{k+1} (i_a + \bar{i}_a)dt + [u_{dc1}(k) - u_{dc2}(k)] \end{aligned} \tag{15}$$

For the sinusoidal current $i_a = I_m sin(\omega t)$, the average value of midpoint offset of capacitor voltages can be obtained as.

$$\Delta \bar{u}_{dc} = \frac{1}{C}\int_k^{k+1} \bar{i}_a dt \tag{16}$$

A low-pass filter is used to obtain the average value of dc voltage offset. Then the dc bias current $\bar{i}_a$ is obtained by a proportional controller of midpoint voltage offset.

$$\bar{i}_a = \mathrm{k}_v \Delta \bar{u}_{dc} \tag{17}$$

where k_v is the proportional coefficient. Hence, the bias current in $\alpha\beta$ stationary frame can be obtained as:

$$\begin{bmatrix} \bar{i}_{\alpha ref} \\ \bar{i}_{\beta ref} \end{bmatrix} = \begin{bmatrix} \sqrt{\dfrac{2}{3}}\bar{i}_a \\ 0 \end{bmatrix} \tag{18}$$

B. REFERENCE CURRENT CALCULATION OF REGULATING ACTIVE POWER WITH RIPPLE ELIMINATION

Under unbalanced grid voltage conditions, the output power contains power ripple, as shown in (13). With different control objectives, the reference current i^*_{ref} can be obtained. If the control purpose is to regulate the active power with ripple elimination, the ripples p^g_{c2} and p^g_{s2} in the formula (13) are 0. Then the following equation is obtained.

$$\begin{cases} p^g_{av} = P_{ref} \\ q^g_{av} = Qref \\ i_\alpha e_\alpha + i_\beta e_\beta - i'_\alpha e'_\alpha - i'_\beta e'_\beta = 0 \\ i_\alpha e'_\alpha + i_\beta e'_\beta + i'_\alpha e_\alpha + i'_\beta e_\beta = 0 \end{cases} \tag{19}$$

The current reference values $i^p_{\alpha ref}$, $i^p_{\beta \mathrm{ref}}$ in $\alpha\beta$ frame for eliminating active power ripples can be obtained by:

$$\begin{cases} i^p_{\alpha ref} = \dfrac{\mathrm{P}_{ref} e'_\beta}{e_\alpha e'_\beta - e'_\alpha e_\beta} + \dfrac{2Q_{ref} e_\beta}{e^2_\alpha + e^2_\beta + e'^2_\beta + e'^2_\alpha} \\ i^p_{\beta \mathrm{ref}} = \dfrac{-P_{ref} e'_\alpha}{e_\alpha e'_\beta - e'_\alpha e_\beta} - \dfrac{2Q_{ref} e_\alpha}{e^2_\alpha + e^2_\beta + e'^2_\beta + e'^2_\alpha} \end{cases} \tag{20}$$

C. REFERENCE CURRENT CALCULATION OF REGULATING REACTIVE POWER WITH RIPPLE ELIMINATION

In this part, the control objective is constant reactive power generation with ripple elimination under unbalanced grid voltage conditions. Then the power ripple q^g_{c2}, and q^g_{s2} in (13) are 0. To achieve reactive power stable control, it is equivalent to solving the following equations:

$$\begin{cases} p^g_{av} = P_{ref} \\ q^g_{av} = Qref \\ i_\alpha e_\beta - i_\beta e_\alpha - i'_\alpha e'_\beta + i'_\beta e'_\alpha = 0 \\ i_\alpha e'_\beta - i_\beta e'_\alpha + i'_\alpha e_\beta - i'_\beta e_\alpha = 0 \end{cases} \tag{21}$$

The reference current value $i_{\alpha ref}$, $i_{\beta \alpha ref}$ in $\alpha\beta$ frame for eliminating reactive power ripple can be obtained as:

$$\begin{cases} i^q_{\alpha ref} = \dfrac{2P_{ref} e_\alpha}{e^2_\alpha + e^2_\beta + e'^2_\alpha + e'^2_\beta} - \dfrac{Q_{ref} e'_\alpha}{e_\alpha e'_\beta - e'_\alpha e_\beta} \\ i^q_{\beta \mathrm{ref}} = \dfrac{2P_{ref} e_\beta}{e^2_\alpha + e^2_\beta + e'^2_\alpha + e'^2_\beta} - \dfrac{Q_{ref} e'_\beta}{e_\alpha e'_\beta - e'_\alpha e_\beta} \end{cases} \tag{22}$$

According to (18), (20) and (22), the reference current for the cost function can be expressed by:

$$\begin{cases} i^*_{\alpha ref} = k_p i^p_{\alpha ref} + k_q i^q_{\alpha ref} + \bar{i}_{\alpha ref} \\ i^*_{\beta ref} = k_p i^p_{\beta ref} + k_q i^q_{\beta ref} + \bar{i}_{\beta ref} \end{cases} \tag{23}$$

where k_p, k_q are the coefficients with different control objectives. When the control objective is to eliminate power ripples of active power, then k_p is 1 and k_q is 0. When the control purpose is to eliminate the reactive power ripple elimination, k_p is 0 and k_q is 1. Therefore, with the proposed method, active or reactive power oscillations can be eliminated, not simultaneously.

Equations (20) and (22) are reference current values for different control objectives. According to the control objective, the corresponding coefficients k_p, k_q are determined and the control algorithm can be implemented.

TABLE 1. System parameters of fault tolerant BVSC

Symbol	System Parameters	Values
u_{dc}	DC-link voltage	400 V
C_1, C_2	Capacitance	1000 μF
L	Filter inductance	5 mH
R	Line resistance	0.2 Ω
e	AC power line voltage	190 V
f	AC power frequency	60Hz
T	Transformer	Y-Y, 190 V/75V, 5 kVA
f_{samp}	Sampling frequency	20 kHz

D. COST FUNCTION WITH DELAY COMPENSATION

The goal of model predictive current control is to make the output current track the reference current. With the sampling signal of The predictive output currents of BVSC at $(k+1)^{\text{th}}$ instant can be obtained by using formula (8) with different voltage vectors, grid-connected currents, and voltages at k^{th} sampling instant. To select the optimal voltage vector, the cost function g is designed to compare all the predictive current values of four different voltage vectors. The voltage vector which makes the cost function minimum is the optimal vector at the next instant.

There is usually a time delay between the optimal voltage vector and the applied voltage vector for a digital implementation, which influences the dynamic and static performance of the control system [30]. To compensate this time delay in digital control, the cost function considering the time delay compensation is designed by the square sum of the error value between the predictive current $i(k+2)$, reference current shown in formula (23) as:

$$g = \left[k_p i^p_{\alpha ref} + k_q i^q_{\alpha ref} + \bar{i}_{\alpha ref} - i_\alpha(k+2)\right]^2 + \left[k_p i^p_{\beta ref} + k_q i^q_{\beta ref} + \bar{i}_{\beta ref} - i_\beta(k+2)\right]^2 \quad (24)$$

The predictive current at $(k+2)^{\text{th}}$ sampling period can be obtained by predictive value at $(k+1)^{\text{th}}$ instant as:

$$i_{\alpha\beta}(k+2) = \frac{T_S\left[u_{\alpha\beta}(k+1) - e_{\alpha\beta}\right]}{L} + \left(1 - \frac{RT_s}{L}\right) \times i_{\alpha\beta}(k+1) \quad (25)$$

The MPC structure of fault-tolerant BVSC is shown in Fig. 3. The grid voltage and current e_{abc}, i_{abc} can be acquired by signal sampling circuits. After Clarke's transformation, $e_{\alpha\beta}$, $i_{\alpha\beta}$ can be obtained. Predictive function (8) and (20) calculate the current predictive values $i_\alpha(k+1)$, $i_\beta(k+1)$, $i_\alpha(k+2)$, $i_\beta(k+2)$. With the reference currents (23) and predictive values, the optimal voltage vector is obtained by the cost function (24). Then the switching states which minimize the cost function are selected and applied at the next instant to achieve the control of fault-tolerant BVSC.

V. EXPERIMENT VERIFICATION

An experimental setup consisting of a TI TMS320F28335 controller board and fault-tolerant BVSC shown in Fig. 4 has been built to verify the performance of the proposed control scheme. The experimental parameters are shown in Table 1. Experimental results have been recorded by the YOKOGAWA DLM4000 series mixed signal oscilloscope. The power quality analyzer Fluke 435II is used to measure the current THD and negative current unbalance (NCU). DC power source APL-II has been used to provide stable DC power. The AMETEK MX-30 ac programmable power supply emulates the unbalanced grid voltage. A comparison of experimental tests of both BVSC and fault-tolerant BVSC, have been realized in different operating modes. In each experimental test, the three-phase six-switch converter (traditional BVSC) is first used and then the three-phase four-switch converter (fault-tolerant BVSC) is applied. The experimental results of current THD, negative current unbalance, dc split capacitor voltage deviation, and power ripples are analyzed and compared in detail.

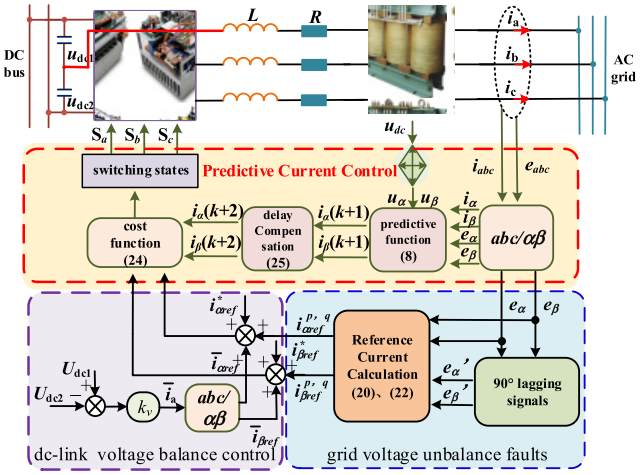

FIGURE 3. Block diagram of predictive current control structure for fault-tolerant BVSC with the unbalanced grid.

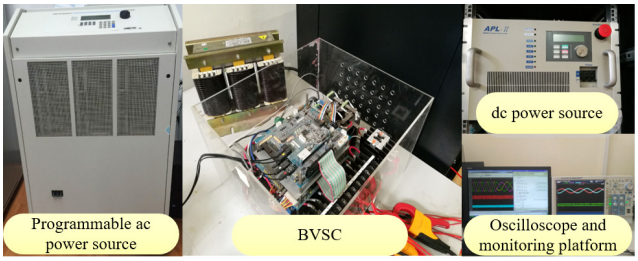

FIGURE 4. Experimental setup of fault-tolerant BVSC.

A. EXPERIMENTAL RESULTS FOR FAULT-TOLERANT BVSC WITH OPEN CIRCUIT FAULT

Fig. 5 shows the steady-state experimental results of traditional BVSC, fault-tolerant BVSC with MPCC and the proposed IMPCC when switch open circuit faults occur in phase a. The converter works in inverter mode and outputs inductive reactive power. The reference currents are obtained under $P_{ref} = 1000$ W, $Q_{ref} = -1000$Var. Fig. 5(a) shows the experimental results with traditional BVSC. When the switch fault of phase a occurs, it can be seen that the current is

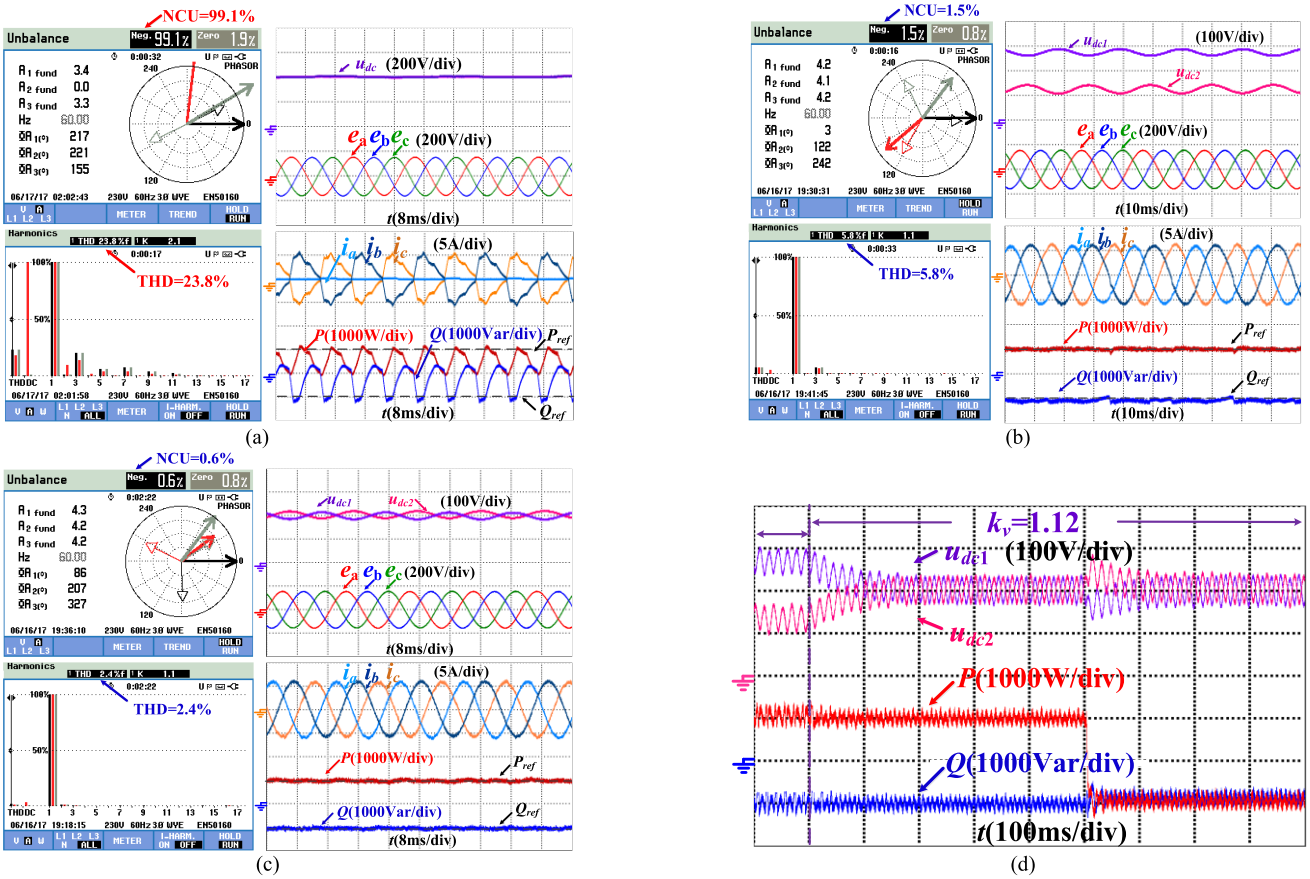

FIGURE 5. Experimental results for switching device open-circuit faults of phase a, (a) BVSC (b) fault-tolerant BVSC (c) fault-tolerant BVSC with proposed control scheme (d) dc-link capacitor voltages.

seriously distorted. The current THD is up to 23.8% and NCU of three-phase currents reaches 99.1%. The output active power of converter fluctuates from 0 to 1100 W and reactive power varies between 200 and −1100 Var, which indicates that the three-phase six-switch BSVC cannot work properly in inverter mode with open-circuit faults. Fig. 5(b) shows that the fault-tolerant converter with MPCC has a lower current THD of 5.8%, and the NCU is reduced to 1.5%. The output power is stable. Although the current THD is larger than the grid requirement, the fault-tolerant converter can work continuously after switch faults. However, the dc-link voltages u_{dc1} and u_{dc2} are unbalanced with u_{dc1} larger than the rating value. The lifetime of capacitor C_1 will be reduced. It is prone to causing secondary faults to the power converter for electrolytic capacitor over-voltage operation.

Using the proposed IMPCC, the experimental results are shown in Fig. 5(c). The grid-connected currents are sinusoidal with 2.4% THD, 0.6% NCU and the output power is stable. Besides, balanced dc-link split capacitor voltages are achieved, which will reduce the possibility of the secondary faults of capacitor C_1. Experimental results show that when switch open circuit faults occur, the fault-tolerant BVSC can work continuously and meet the grid requirements with the proposed IMPCC method. Besides, the balance control of the dc-link capacitor voltage is achieved.

To verify the performance of the dc-link capacitor voltage control, tests are carried out under different conditions. In Fig. 5(d), before 0.1 s, dc-link voltage balance control is not used and k_v is 0. The capacitor voltages u_{dc1} and u_{dc2} are not balanced. At 0.1 s, the coefficient k_v changes to 1.12. The dc bias current is injected into phase a. The deviation of the u_{dc1} and u_{dc2} is becoming smaller, and balanced control is achieved. At 0.6 s, the reference power is stepped from $P_{ref} = 1000$ W to $P_{ref} = -1000$ W. The fault-tolerant BVSC works from the inverter mode to rectifier mode. The dc-link capacitor voltage keeps balanced during the transition. The experimental results verify the effectiveness of the dc-link balance control scheme during both steady-state and dynamic performance.

B. EXPERIMENTAL RESULTS FOR FAULT-TOLERANT BVSC WITH OPEN CIRCUIT FAULT AND UNBALANCED GRID VOLTAGE

Fig. 6 shows the dynamic experimental results of MPCC and IMPCC for the fault-tolerant BVSC in the transition between inverter and rectifier modes with leg faults under a single-phase unbalanced grid voltages. The voltage of phase b sags to 70% of the rated value. The reference current is obtained under initial power $P_{ref} = 1000$ W, $Q_{ref} = -1000$ Var. At 0.04 s, P_{ref} changes from 1000W to −1000 W and the

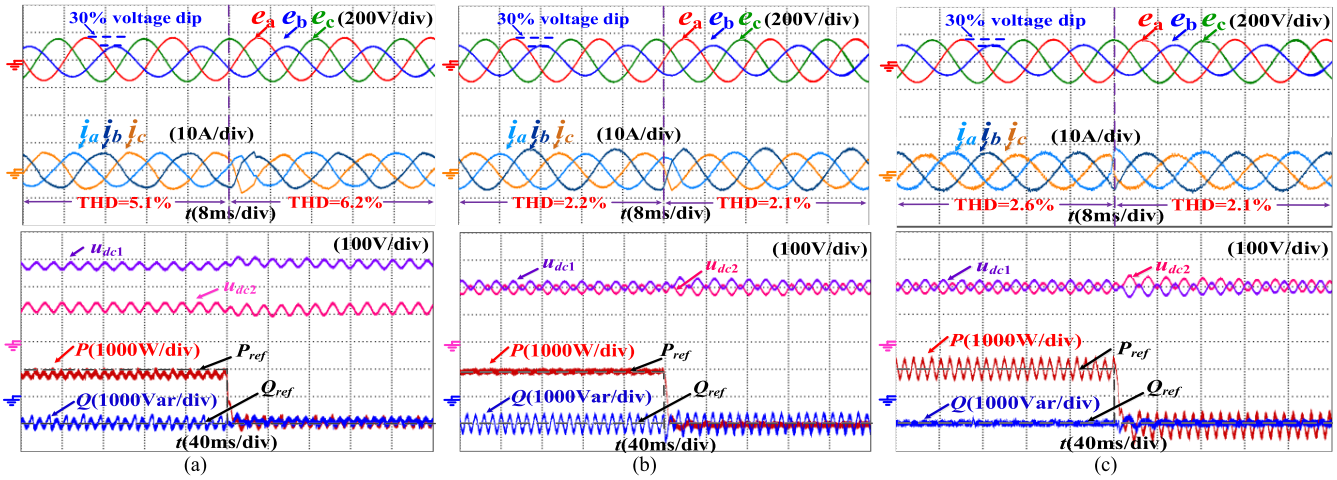

FIGURE 6. Experimental results for fault-tolerant converter with open circuit fault and single-phase unbalanced grid voltage, using (a) MPCC (b) the proposed IMPCC scheme with active power ripple elimination, (c) the proposed IMPCC scheme with reactive power ripple elimination.

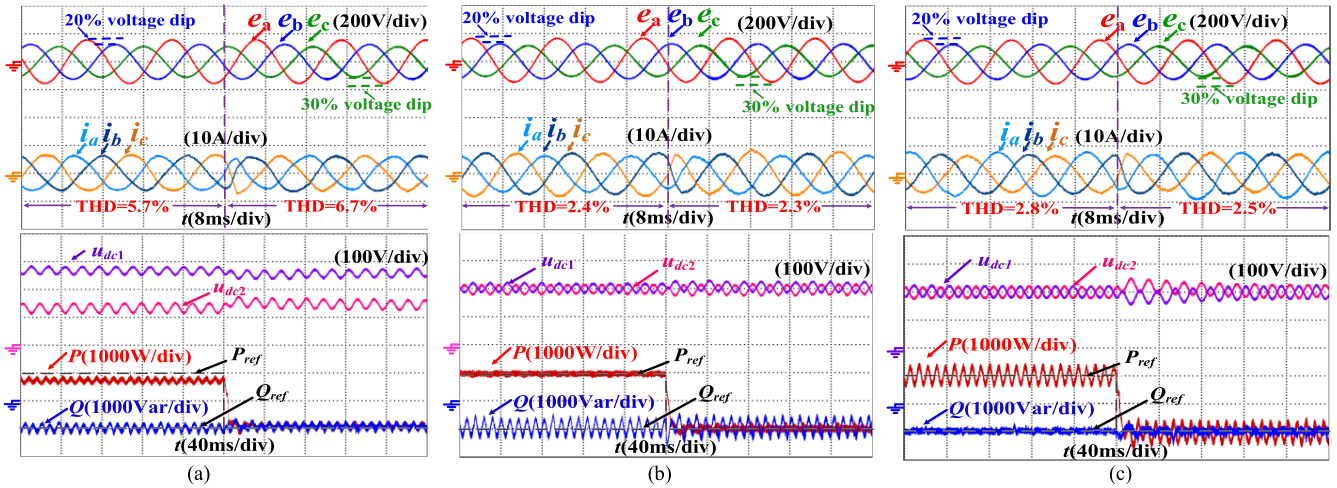

FIGURE 7. Experimental results for a fault-tolerant converter with open circuit fault and three-phase unbalanced grid voltage, using (a) MPCC (b) the proposed IMPCC scheme with active power ripple elimination, (c) the proposed IMPCC scheme with reactive power ripple elimination.

fault-tolerant BVSC works in rectifier mode. The waveforms include three-phase voltage and current, active power and reactive power.

Fig. 6(a) shows the results of conventional MPCC with fault-tolerant BVSC. The current THD is up to 5.1% in inverter mode and 6.2% in rectifier mode. The active power and reactive power contain twice line frequency power ripples. The active power ripple P_{rip} is 437.5 W and the reactive power ripple Q_{rip} is 600 Var. The dc-link voltage u_{dc1} and u_{dc2} are unbalanced. The capacitor C_1 operates in overvoltage conditions, and the lifetime will be reduced. Fig. 6(b) and (c) show the results of the proposed IMPCC with active power and reactive power ripple elimination, respectively. In Fig. 6 (b) and (c), P_{rip} is 157 W, 690 W and Q_{rip} are 610 Var, 184 Var, respectively. The power ripples have been significantly reduced. First, with the proposed method, the dc-link voltage balance control is achieved under both open circuit fault and single-phase unbalance grid. Second, power ripples are reduced under the proposed method. Inactive power ripple elimination mode, the active power ripple is reduced by 28.1%. The reactive power ripple is reduced by 41.6% with reactive power elimination control. The output power can be controlled stable with less ripple. Third, with active power ripple elimination, the current THD is reduced to 2.2% in inverter mode and 2.1 % in rectifier mode. With reactive power ripple elimination, the current THD drops to 2.6% and 2.1%, respectively.

When three-phase unbalanced grid voltages and switch open circuit faults occur, the dynamic responses of fault-tolerant BVSC with MPCC and IMPCC are also investigated. Fig. 7 shows the experimental results under the voltages of phase b and phase c sag to 80% and 70% of the rated voltage value, respectively. The started reference power $P_{ref} = 1000$ W, $Q_{ref} = -1000$ Var. The fault-tolerant BVSC works in inverter mode and generates capacitive reactive power. Then P_{ref} steps from 1000 W to -1000 W, the converter is switched to operate in rectifier mode.

As shown in Fig. 7(a), the current under the conventional MPCC has a large number of harmonic components, and current THD is 5.7% before active power changing and 6.7% after that. But there are power ripples in both active and reactive power. The converter under the proposed IMPCC has better performance in Fig. 7(b) and (c). In Fig. 7(b), under proposed IMPCC to reduce active power ripples, the grid-connected currents are sinusoidal, and the THD drops to 2.4% before active power changing and 2.3% after that. P_{rip} is reduced from 423 W to 162 W. In Fig.7(c), with reactive power ripple elimination, the reactive power is stable, and the THD of grid-connected current drops to 2.8% in inverter mode and 2.5% in rectifier mode. Q_{rip} is reduced from 730 Var to 165 Var. The dc-link voltage is balanced during the transition from the inverter mode to the rectifier mode. For fault-tolerant BVSC, the twice line frequency power ripples are eliminated by the proposed method. The ripples of the active power or reactive power are reduced by 26.1% and 56.5% for active or reactive power ripples elimination, respectively. The power quality is improved under switch faults and unbalanced grid voltages conditions. Although the power ripples of the fault-tolerant BVSC are still larger than traditional TPSS converter, it can continuously operate under fault conditions.

Fig.6 and 7 show that the fault-tolerant BVSC can operate continuously by the proposed IMPCC, even if the switch open circuit faults and unbalanced grid voltage occur together. The voltage balance control of dc-link split capacitors can be achieved. Based on experimental comparison results, the fault-tolerant BVSC under the proposed IMPCC scheme has a better performance compared to the traditional MPCC, which ensures continuous operation of the converter and validate the proposed control scheme.

VI. CONCLUSION

For reliable and safe operation of the bidirectional ac/dc power conversion, this paper proposes an IMPCC scheme for fault-tolerant BVSC to keep balanced dc-link capacitor voltage, reduce power ripples and current harmonics, which enhances the fault-tolerant operation capability under open-circuit fault and unbalanced grid voltage.

First, the space voltage vectors and the central point of dc-link voltage offsets for fault-tolerant BVSC are analyzed with different phase leg fault conditions. The influence caused by the unbalanced dc-link split capacitor voltage is also investigated. Second, to reduce the power ripple and grid-connected current THD, the reference currents are calculated by using grid voltages and their 90° lagging signals in the $\alpha\beta$ stationary coordinates. Compared to the traditional MPCC, the proposed IMPCC improves fault-tolerant capacity and the power quality with less current distortion and power ripples. Under both single-phase and three-phase unbalanced grid voltages, IMPCC keeps the grid-connected current sinusoidal. The twice line frequency ripples of active power or reactive power are eliminated with the proposed method for different control objectives. Finally, an improved reference current calculation method is designed to achieve dc-link split capacitor voltage balancing. Under the unbalanced grid voltage and switch open circuit fault conditions, the fault-tolerant BVSC can operate continuously with the proposed control scheme, which enhances the reliability of the bidirectional power conversion.

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