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Transient Modeling Method for Faulty DC Microgrid Considering Control Effect of DC/AC and DC/DC Converters

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ABSTRACT The accurate transient modeling of faulty DC microgrids is the basis of fault detection, fault location and fault isolation. AC/DC and DC/DC converters keeps their normal control strategies until the fault is detected. However, in existing researches, the influence of the control effect of converters is normally being ignored in the transient characteristics of DC microgrids. This omission reduces the accuracy of the faulty transient model. Thus, this paper proposes a transient modeling method for faulty DC microgrid considering control effect of different DC/AC and DC/DC converters. Firstly, the transient characteristics of different converters (including voltage source converter, boost circuit, bidirectional chopper circuit and buck circuit) are analyzed. And then, the faulty transient model of ring-type DC microgrid is established. Furthermore, the correctness of proposed modeling method is verified by comparing with the Control-hardware-in-loop (CHIL) test system. The results show that the proposed method can not only improve the accuracy of transient analysis of faulty DC microgrid, but also enhance the calculation efficiency.

INDEX TERMS DC microgrid, faulty transient modeling, control effect, converter.

I. INTRODUCTION

The DC microgrid, which belongs to DC distribution system, is a promising concept in power system [1]. Compared with traditional AC distribution grids, DC microgrids have two unique advantages: 1) There is no concept of ''phase'' in DC microgrids, which means that the phase synchronization does not need to be considered when AC distributed renewable energies (DERs) are connected [2]; 2) Using DC microgrids to connect with DC devices (such as photovoltaic (PV), energy storage (ES)) can reduce the use of power electronic switches, which makes the distribution systems more efficient and economical [3]. Thus, DC microgrids have been widely used in isolated islands power supply [4], [5], distributed generators (DG) connection [6], [7], asynchronous AC grid interconnection [8], urban power supply [9], electric vehicle [10], [11] and data centers [12], etc. However, DC fault protection has become a great challenge for DC microgrids [13].

Fault detection, fault isolation and fault location are the three basic elements of fault protection. Accurate transient modeling of the faulty DC microgrid is helpful for the selection of the threshold in fault detection [14] and the selection of the parameters of protection devices in fault isolation [15]. Meanwhile, to achieve fault location, the faulty currents obtained by the transient modeling can be used as reference signals to compare with the sampled signals [16]. Therefore, the transient modeling of faulty DC microgrids is the key to provide the analysis basis of fault detection, fault location and fault isolation. The fault characteristic analysis of DC microgrids can be divided into transient analysis for system structures and transient analysis for AC/DC or DC/DC converters.

The system structures of DC microgrids include radial structure, ring structure and mesh structure [17]. The topologies of radial structure are simple. And each line is decoupled. Thus, the fault loops of radial structure can be regarded as resistance-inductance (RL) loops composed of short circuit fault resistance, faulty line resistance and faulty line inductance [18], [19]. In the ring structure, there are two paths between the fault point and any node. Reference [20] disconnects the ring structure from the position, where farthest from the fault point. The simplified ring structure is equivalent to a radial structure centered on the fault point. The complexity

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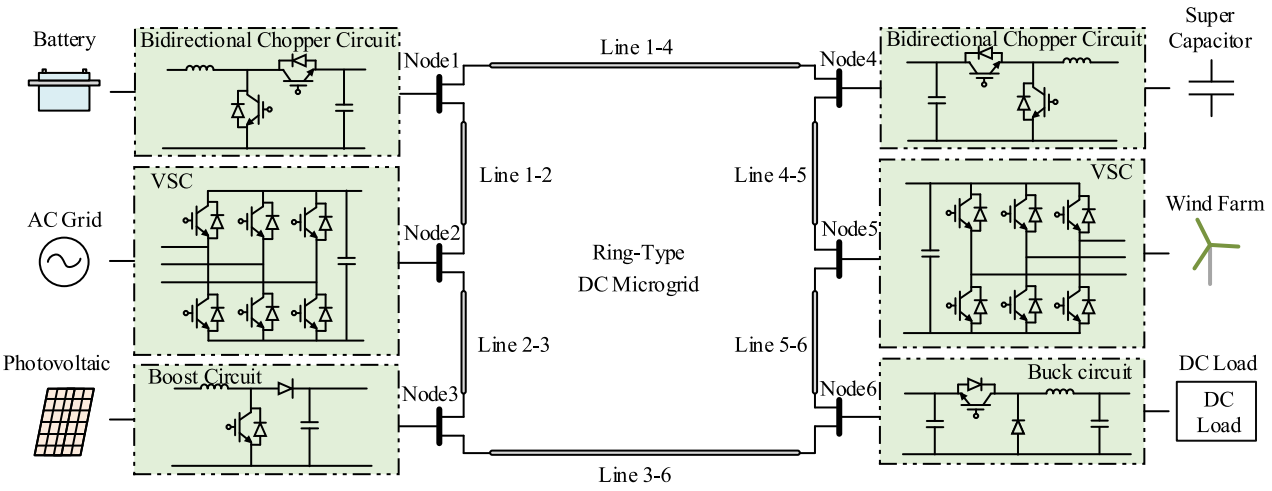

FIGURE 1. Schematic of a ring-type DC microgrid with distributed energy access.

of the mesh structure is the highest, since the lines are coupled with each other. In [21], the matrix expressions of the lines currents in the mesh structure are derived. Furthermore, to make the matrix solvable, the Dijkstra's path algorithm is used to eliminate the virtual nodes in the matrix. In [15], the Kirchhoff voltage and current equations in the mesh-type DC microgrid are given in the form of difference equations. And the lines currents are iterated automatically. In summary, the transient characteristics of various system structures have been analyzed. Also, accurate transient models have been established.

Voltage source converters (VSCs) and various DC/DC converters are the most commonly used converters in DC microgrids. Firstly, as analyzed in [18]–[22], the transient current being injected from VSCs can be divided into three parts: 1) The discharge current of DC-link capacitor of VSCs; 2) The discharge current provided by the line inductance through the freewheeling diode in VSCs; 3) Short circuit current provided by the AC system through the freewheeling diode in VSCs. Unlike VSCs, there are various DC/DC converter topologies connected with different control objects. The numerical analysis for a DC microgrid with PV was derived in [23]. The results show that the contribution of PV to faults cannot be neglected. Bidirectional chopper circuit is normally used to connect with an ES in DC microgrid [24]. The analysis in [24] shows that the ES contributes to faults when the ground faults occur. The equivalent circuits at different stages of DC/DC converters connected with PV and ES were established in [25]. Moreover, comprehensive comparisons among them have also been investigated. Overall, there have existing researches on the transient modeling of converters in the faulty situation. However, the currents being injected from converters were ignored during the period from fault occurrence to fault detection in previous researches, which reduces the accuracy of fault transient model.

The period from fault occurrence to fault detection is the most important stage on fault transient analysis. And depending on the severity of fault, the time scale of this period ranges from a few milliseconds to tens of milliseconds. For better performance on fault detection, location and isolation, it is necessary to consider the contribution of currents being injected from converters. Since the fault is not detected, the switches in converters are not blocked at this period. And the control systems keep the normal control strategy at this period. To figure out the contribution of fault current being injected from converters, it is necessary to analyze the control effect of converters on the fault transient characteristic.

Under this situation, the transient modeling and analysis of power electronic converters in faulty DC microgrids are accomplished in this paper. The main contributions of this paper can be described as following: 1) The transient responses of power electronic converters (VSC, boost circuit, buck circuit and bidirectional chopper circuit) are modelled and analyzed; 2) A transient modeling method for faulty ring-type DC microgrids is proposed. In addition, the proposed method can be implemented by computer automatically and applied in fault detection, fault location and other situations easily.

The rest of this paper is organized as follows: Section II presents the transient fault analysis problem for DC microgrids; Section III analyzes the transient characteristics of DC/AC converter and DC/DC converter in a faulty ring-type DC microgrid; The numerical analysis of the error between the transient calculation model and the Control-hardware-in-loop (CHIL) test system is completed in Section IV; Section V draws the conclusion.

II. PROBLEM STATEMENT

A. RING-TYPE DC MICROGRID WITH DISTRIBUTED ENERGIES ACCESS

The classic ring-type DC microgrids connected with the distributed energies is taken as the case study in this paper. The schematic of the ring-type DC microgrid is shown in Fig. 1.

This system connects to a variety of AC units and DC units. The AC grid and wind farm (WD) are AC units connected to the DC microgrids by VSCs. While, the PV, battery, super capacitor and DC load are DC units connected to the DC microgrids by various DC/DC converters (including boost circuit, buck circuit and bidirectional chopper circuit).

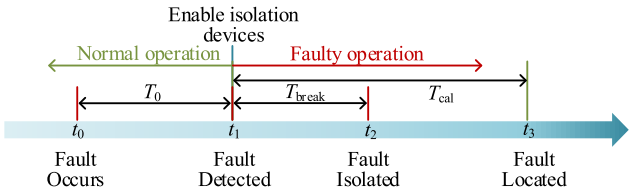

FIGURE 2. Post-fault process in a DC microgrid.

B. POST-FAULT PROCESS OF THE DC MICROGRID

Fault detection, fault isolation and fault location are the three basic elements of fault protection. And the moments of fault detection, fault isolation, fault location is shown in Fig. 2. Assuming that a fault occurs at t_0. Firstly, the fault will be detected at t_1 by the fault detection devices. Once the fault is detected, the fault isolation devices will be enabled and the switches in converters will be blocked immediately. The fault isolation devices will isolate faulty line at t_2 to ensure the normal operation of other healthy lines. While the fault position will be located at t_3 to ensure the fault be repaired timely. The accurate transient modeling of the DC microgrid during the period from fault occurrence to fault detection is helpful for the selection of the threshold in fault detection and the selection of the parameters of isolation devices. Meanwhile, the faulty currents and nodes voltages obtained by the transient modeling can be used as reference signals compared with the sampled signals in fault location. The use in fault detection and fault location can be found in [26]. While, the use for the selection of parameters of isolation devices can be found in [27].

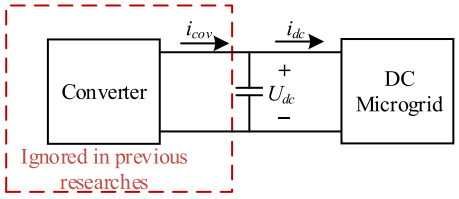

FIGURE 3. Relationship between DC microgrid and converter.

The control systems in converters will keep their normal control strategies during the period from fault occurrence to fault detection. And the control systems affect the changes of the currents i_{cov} being injected from converters. However, as shown in Fig. 3, the currents i_{cov} are ignored during the period from fault occurrence to fault detection in previous researches [18]–[25], which will reduce the accuracy of fault transient analysis. Thus, it is necessary to establish a transient calculation model that considers the currents i_{cov}, which are related to the effect of control systems in different converters.

III. TRANSIENT ANALYSIS OF FAULTY DC MICROGRID

The transient characteristic of converters is analyzed in this section. Firstly, the transient models of each converter are established. Secondly, to analyze the accuracy of the transient models of converters in a whole DC microgrid, the transient model of each converter is combined to achieve the transient model of the ring-type DC microgrid.

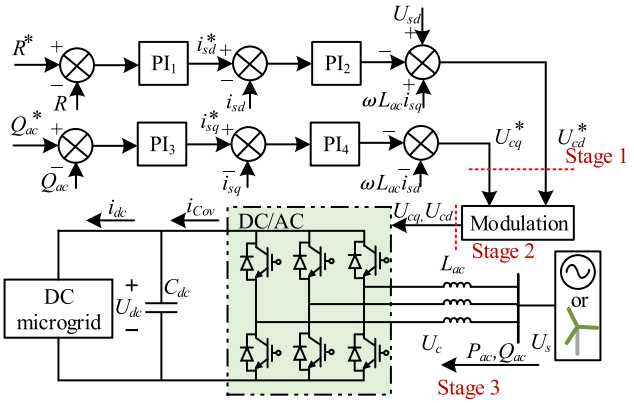

FIGURE 4. The topology and control diagram of VSC.

A. MODEL OF AC/DC CONVERTERS IN FAULTY DC MICROGRID

VSC normally works as DC/AC converter to connect with AC grids or WFs in DC microgrids. The topology and control diagram of VSC is shown in Fig. 4. DC-link voltage control is used in VSC, which connects with AC grids, to stabilize DC-link voltage. While active power control is used in VSC, which connects with WFs, to regulate active power. Moreover, the double closed loop control with PI controllers is the commonly control method used in VSC.

The transient analysis of VSC is divided into three stages. The first stage is the establishment of the relationship between output (reference voltage of AC side, which defines as U_{cd}^* and U_{cq}^*) and input (including DC-link voltage U_{dc}, active power P_{ac}, reactive power Q_{ac}, current of AC side i_s and voltage of AC side U_s) in control system. The second stage is the establishment of the relationship between output (modulation current of VSC, which defines as U_{cd} and U_{cq}) and input (U_{cd}^* and U_{cq}^*) in modulation. The third stage is the establishment of the relationship between output (P_{ac}, Q_{ac}, i_s and injection current i_{cov}) and input (U_{cd} and U_{cq}) in hardware circuit.

The first stage: the output U_{cd}^* and U_{cq}^* in difference form can be expressed as:

$$\begin{cases} U_{cd}^*(k) = u_{cd1}(k) + u_{cd2}(k) + u_{cd3}(k) \\ U_{cq}^*(k) = u_{cq1}(k) + u_{cq2}(k) + u_{cq3}(k) \end{cases} \quad (1)$$

where

$$\begin{cases} u_{cd1}(k) = -K_{p1}\cdot K_{p2}\cdot[\dfrac{\tau_{i1}\tau_{i2}c^2+(\tau_{i1}+\tau_{i2})c+1}{\tau_{i1}\tau_{i2}c^2} \\ \qquad \cdot(R^*-R(k)) \\ +\dfrac{2-2\tau_{i1}\tau_{i2}c^2}{\tau_{i1}\tau_{i2}c^2}\cdot(R^*-R(k-1)) \\ \qquad +\dfrac{\tau_{i1}\tau_{i2}c^2-(\tau_{i1}+\tau_{i2})c+1}{\tau_{i1}\tau_{i2}c^2}\cdot \\ (R^*-R(k-2))]+2u_{cd1}(k-1)-u_{cd1}(k-2) \\ u_{cd2}(k) = K_{p2}\cdot[\dfrac{1+c\tau_{i2}}{c\tau_{i2}}\cdot i_{sd}(k)+\dfrac{1-c\tau_{i2}}{c\tau_{i2}} \\ \qquad \cdot i_{sd}(k-1)]+u_{cd2}(k-1) \\ u_{cd3}(k) = U_s(k)+\omega L_{ac}i_{sq}(k) \end{cases} \tag{2}$$

$$\begin{cases} u_{cq1}(k) = -K_{p3}\cdot K_{p4}\cdot[\dfrac{\tau_{i3}\tau_{i4}c^2+(\tau_{i3}+\tau_{i4})c+1}{\tau_{i3}\tau_{i4}c^2} \\ \qquad \cdot(Q^*_{ac}-Q_{ac}(k)) \\ +\dfrac{2-2\tau_{i3}\tau_{i4}c^2}{\tau_{i3}\tau_{i4}c^2}\cdot(Q^*_{ac}-Q_{ac}(k-1)) \\ \qquad +\dfrac{\tau_{i3}\tau_{i4}c^2-(\tau_{i3}+\tau_{i4})c+1}{\tau_{i3}\tau_{i4}c^2}\cdot \\ (Q^*_{ac}-Q_{ac}(k-2))]+2u_{cq1}(k-1)-u_{cq1}(k-2) \\ u_{cq2}(k) = K_{p4}\cdot[\dfrac{1+c\tau_{i4}}{c\tau_{i4}}\cdot i_{sq}(k)+\dfrac{1-c\tau_{i4}}{c\tau_{i4}}\cdot i_{sq}(k-1)] \\ \qquad +u_{cq2}(k-1) \\ u_{cq3}(k) = -\omega L_{ac}i_{sd}(k) \end{cases} \tag{3}$$

where $Kp\alpha$ and $\tau i\alpha$ are proportional coefficients and integral time constants of PI controller α, R stands for P_{ac} in active power control, R stands for U_{dc} in DC-link voltage control, $c = 2/T_s$, T_s is sample time, ω is AC frequency, L_{ac} is inductance of AC lines.

The second stage: since the modulation of the VSC maybe saturate after fault, the output (U_{cd}, U_{cq}) of modulation is not equal to input (U^*_{cd}, U^*_{cq}) after $U^*_c > U_{dc}/\sqrt{3}$. Thus, in the second stage, the output U^*_{cd} and U^*_{cq} in difference form can be expressed as:

$$\begin{cases} U_{cd}(k) = \dfrac{U_{dc}(k)}{\sqrt{3}}\cdot\dfrac{U^*_{cd}(k)}{\sqrt{(U^*_{cd}(k))^2+(U^*_{cq}(k))^2}} \\ U_{cq}(k) = \dfrac{U_{dc}(k)}{\sqrt{3}}\cdot\dfrac{U^*_{cq}(k)}{\sqrt{(U^*_{cd}(k))^2+(U^*_{cq}(k))^2}} \end{cases} \tag{4}$$

The third stage: the expressions of P_{ac}, Q_{ac}, i_d, i_q and i_{cov} can be expressed as (5) according to [28]:

$$\begin{cases} P_{ac}(k+1) = U_{sd}(k)\cdot i_{sd}(k) \\ Q_{ac}(k+1) = -U_{sd}(k)\cdot i_{sq}(k) \\ i_{sd}(k+1) = i_{sd}(k)+\dfrac{\Delta T}{L_{ac}} \\ \qquad [\omega L_{ac}i_{sq}(k)+U_{sd}(k)-U_{cd}(k)] \\ i_{sq}(k+1) = i_{sq}(k)+\dfrac{\Delta T}{L_{ac}}[-\omega L_{ac}i_{sd}(k)-U_{cq}(k)] \\ i_{cov}(k+1) = \dfrac{U_{cd}(k)\cdot i_{sd}(k)+U_{cq}(k)\cdot i_{sq}(k)}{U_{dc}(k)} \end{cases} \tag{5}$$

Through the iteration calculation of (1), (4) and (5), the changes of state variables in VSC before fault detection can be calculated.

B. MODEL OF DC/DC CONVERTERS IN FAULTY DC MICROGRID

Unlike VSC, there are various topologies of DC/DC converters connected with different objects. This Part analyzes the transient characteristics of PV, ES (battery and super capacitor) and DC load. Meanwhile, the transient characteristics of converters corresponding to the DC units are also analyzed.

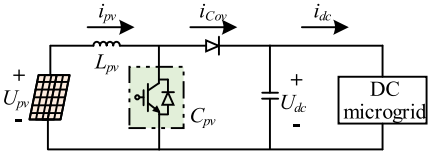

FIGURE 5. The topologies of boost circuit.

1) PHOTOVOLTAICS AND ITS CONVERTERS

Boost circuit is normally worked as DC/DC converter in DC microgrid to connect with PVs. The topologies of boost circuit are shown in Fig. 5. To maximize PV power transmission, Incremental conductance method, which is a popular maximum power point tracking (MPPT) method, is used as the control strategy of boost circuit. The description of incremental conductance method can be found in [29].

The characteristic of PV can be expressed as:

$$i_{pv} = N_p\cdot I_p - N_p\cdot I_0\left[e^{\frac{q\left(u_{pv}+i_{pv}\cdot R_s\right)}{N_s\cdot AKT}}-1\right]-\frac{u_{pv}+i_{pv}\cdot R_s}{R_{sh}} \tag{6}$$

where I_p is the short circuit current of PV, I_0 is the reverse saturation current of diode, R_s and R_{sh} are series and parallel internal resistances, q is elementary charge, A is the quality factor of diode, K is Boltzmann constant, T is temperature, N_s and N_p are the number of series and parallel photovoltaic cells.

According to (6), the ratio of the rate of the change of current di_{pv} and voltage dU_{pv} can be expressed as:

$$\frac{di_{pv}(k+1)}{dU_{pv}(k+1)} = \frac{\left(-\dfrac{qN_pI_0}{N_sAKT}\cdot e^{\frac{q\left(U_{pv}(k)+R_s\cdot i_{pv}(k)\right)}{N_s\cdot AKT}}-\dfrac{1}{R_{sh}}\right)}{\left(1+\dfrac{R_s}{R_{sh}}+\dfrac{qN_pI_0R_s}{N_sAKT}\cdot e^{\frac{q\left(U_{pv}(k)+R_s\cdot i_{pv}(k)\right)}{N_s\cdot AKT}}\right)} \tag{7}$$

The DC-link voltage U_{dc} decreases immediately after fault occurs. Because the transient characteristics of U_{dc} changes rapidly, and the regulation of closed-loop of MTTP has hysteresis, U_{pv} will drop along with U_{dc}. According to the I-U curve of a single PV cell shown in Fig. 6, the working point of the PV system shifts to the left. Therefore, a constant current source is used to replace the output current of PV. Finally,

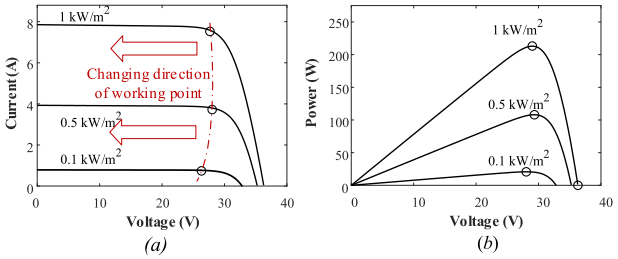

FIGURE 6. *I-U* and *P-V* characteristic curve of PVs: *a*) *I-U* characteristic curve, *b*)*P-V* characteristic curve.

i_{pv} and U_{pv} can be expressed as:

$$\begin{cases} i_{pv}(k+1) \approx i_{pv}(0) \\ U_{pv}(k+1) = U_{dc}(k) \cdot \left(1 - g_{pv}(k)\right) \end{cases} \tag{8}$$

where U_{dc} is the DC-link voltage, g_{pv} is the duty cycle of IGBT.

And the change of duty cycle g_{pv} can be expressed as:

$$\begin{cases} g_{pv}(k+1) = g_{pv}(k) + \Delta g_{pv} \text{ if} \dfrac{di_{pv}}{dU_{pv}} + \dfrac{i_{pv}}{U_{pv}} < 0 \\ g_{pv}(k+1) = g_{pv}(k) - \Delta g_{pv} \text{ if} \dfrac{di_{pv}}{dU_{pv}} + \dfrac{i_{pv}}{U_{pv}} > 0 \end{cases} \tag{9}$$

where the constant value Δg_{pv} is the rate of change in duty cycle. Because the step size of the change of duty cycle has little influence on efficiency [30], fixed step size is used for the change of duty cycle.

Moreover, when the control system of boost circuit is saturated, g_{pv} needs to be modified by:

$$g_{pv}(k) = \begin{cases} g_{pv\max}, & \text{if } g_{pv}(k) > g_{pv\max} \\ g_{pv\min}, & \text{if } g_{pv}(k) < g_{pv\min} \end{cases} \tag{10}$$

The expressions of variables in PV and its converters can be expressed as:

$$\begin{cases} i_{pv}(k+1) = i_{pv}(k) \\ i_{cov}(k+1) = \left(1 - g_{pv}(k)\right) \cdot i_{pv}(k) \end{cases} \tag{11}$$

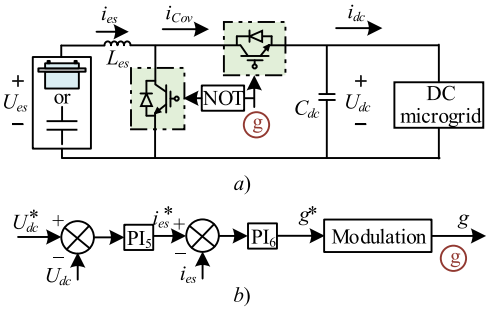

FIGURE 7. The topology and control diagram of bidirectional chopper circuit.

2) ENERGY STORAGE AND ITS CONVERTERS

The bidirectional chopper circuit is normally worked as DC/DC converter to connect with ESs in DC microgrids. The topology of bidirectional chopper circuit is shown as Fig. 7 *a*). DC-link voltage control is normally used in bidirectional chopper circuit to stabilize DC-link voltage. And the control diagram is shown as Fig. 7 *b*). Batteries and super capacitors are two complementary ESs. The batteries have high energy density but have slow power regulation speed. In contrast, the super capacitors have fast power regulation speed but have low energy density.

Since the life of batteries decreases as the number of charges and discharges increases, the high frequency component of inputs is generally filtered out in the control system of batteries. Because the short circuit fault is a high frequency power fluctuation, the output of control system for battery is considered unchanged from fault occurrence to fault detection. Thus, the expression of i_{cov} can be expressed as:

$$i_{cov}(k+1) = i_{cov}(k) + \frac{g_{bt}(k) \cdot [U_{bt}(0) - g_{bt}(k) U_{dc}(k)]}{L_{bt}} \cdot \Delta T \tag{12}$$

where g_{bt} is the output of control system, U_{bt} is the voltage of battery, L_{bt} is the inductance of DC line.

The power regulation speed of super capacitors is fast. Once a fault occurs in DC microgrid, the super capacitor injects power immediately to suppress the dropping of DC-link voltage. The transient analysis of bidirectional chopper circuit for super capacitors is similar to the transient analysis of VSC and also can be divided into three stages.

The first stage is the establishment of the relationship between output g_s^* and input (U_{dc} and i_{st}) in control system. The expression of g_s^* can be expressed as:

$$g_s^*(k) = g_{s1}(k) + g_{s2}(k) \tag{13}$$

where

$$\begin{cases} g_{s1}(k) = K_{p5} \cdot K_{p6} \cdot [\dfrac{\tau_{i5}\tau_{i6}c^2 + (\tau_{i5}+\tau_{i6})c + 1}{\tau_{i5}\tau_{i6}c^2} \\ \qquad \cdot (U^*_{dc} - U_{dc}(k)) \\ + \dfrac{2 - 2\tau_{i5}\tau_{i6}c^2}{\tau_{i5}\tau_{i6}c^2} \cdot (U^*_{dc} - U_{dc}(k-1)) \\ \qquad + \dfrac{\tau_{i5}\tau_{i6}c^2 - (\tau_{i5}+\tau_{i6})c + 1}{\tau_{i5}\tau_{i6}c^2} \cdot \\ (U^*_{dc} - U_{dc}(k-2))] + 2g_{s1}(k-1) - g_{s1}(k-2) \\ g_{s2}(k) = -K_{p6} \cdot [\dfrac{1+c\tau_{i6}}{c\tau_{i6}} \cdot i_{sc}(k) + \dfrac{1-c\tau_{i6}}{c\tau_{i6}} \cdot i_{sc}(k-1)] \\ \qquad + g_{s2}(k-1) \end{cases} \tag{14}$$

where $Kp\alpha$ and $\tau i\alpha$ are proportional coefficients and integral time constants of PI controller α, $c = 2/T_s$, T_s is sample time.

The second stage is the establishment of the relationship between output g_s and input g_s^* in modulation. The expression of g_s can be expressed as:

$$g_s(k) = \begin{cases} g_{s\max}, & \text{if } g_s^*(k) > g_{s\max} \\ g_s^*(k), & \text{if } g_{s\max} \geq g_s^*(k) > g_{s\min} \\ g_{s\min}, & \text{if } g_s^*(k) \leq g_{s\min} \end{cases} \tag{15}$$

The third stage is establishment of the relationship between output (U_{sc}, i_{sc} and i_{cov}) and input g in hardware circuit. The expressions of those above variables can be expressed as:

$$\begin{cases} U_{sc}(k+1) = U_{sc}(k) - \dfrac{\Delta T}{C_{sc}} \cdot i_{sc}(k) \\ i_{sc}(k+1) = i_{sc}(k) + \dfrac{\Delta T}{L_{sc}}[U_{sc}(k) - g_s(k) \cdot U_{dc}(k)] \\ i_{cov}(k+1) = g_s(k) \cdot i_{sc}(k) \end{cases} \tag{16}$$

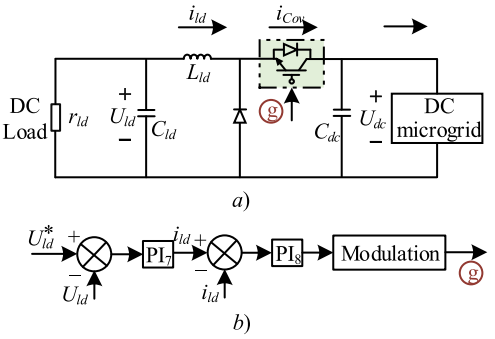

FIGURE 8. The topology and control diagram of buck circuit: *a*) topology of buck circuit, *b*) control diagram of buck circuit.

3) DC LOAD AND ITS CONVERTERS

Buck circuit is normally worked as DC/DC converter in DC microgrid to connect with DC load. The topology and control diagram of buck circuit is shown in Fig. 8. DC-link voltage control is normally used to stabilize voltage U_{ld} of DC load.

Similar to the derivation of bidirectional chopper circuit for super capacitors, the transient analysis of buck circuit for DC loads can also be divided into three stages.

The first stage is the establishment of the relationship between output g_l^* and input (U_{dc} and i_{st}) in control system. The expression of g_l^* can be expressed as:

$$g_l^*(k) = g_{l1}(k) + g_{l2}(k) \tag{17}$$

where

$$\begin{cases} g_{l1}(k) = K_{p7} \cdot K_{p8} \cdot [\dfrac{\tau_{i7}\tau_{i8}c^2 + (\tau_{i7} + \tau_{i8})c + 1}{\tau_{i7}\tau_{i8}c^2} \\ \qquad \cdot (U_{ld}^* - U_{ld}(k)) \\ + \dfrac{2 - 2\tau_{i7}\tau_{i8}c^2}{\tau_{i7}\tau_{i8}c^2} \cdot (U_{ld}^* - U_{ld}(k-1)) \\ \qquad + \dfrac{\tau_{i7}\tau_{i8}c^2 - (\tau_{i7} + \tau_{i8})c + 1}{\tau_{i7}\tau_{i8}c^2} \cdot \\ (U_{ld}^* - U_{ld}(k-2))] + 2g_{l1}(k-1) - g_{l1}(k-2) \\ g_{l2}(k) = -K_{p8} \cdot [\dfrac{1 + c\tau_{i8}}{c\tau_{i8}} \cdot i_{ld}(k) + \dfrac{1 - c\tau_{i8}}{c\tau_{i8}} \\ \qquad \cdot i_{ld}(k-1)] + g_{l2}(k-1) \end{cases} \tag{18}$$

where $Kp\alpha$ and $\tau i\alpha$ are proportional coefficients and integral time constants of PI controller α, $c = 2/T_s$, T_s is sample time, U_{ld} is the voltage of DC load, i_{ld} is the current of DC load.

The second stage is the establishment of the relationship between output g_l and input g_l^* in modulation. The expression of g can be expressed as:

$$g_l(k) = \begin{cases} g_{l\max}, & \text{if } g_l^*(k) > g_{l\max} \\ g_l^*(k), & \text{if } g_{l\max} \geq g_l^*(k) > g_{l\min} \\ g_{l\min}, & \text{if } g_l^*(k) \leq g_{l\min} \end{cases} \tag{19}$$

The third stage is the establishment of the relationship between output (U_{ld}, i_{ld} and i_{cov}) and input g_l in hardware circuit. The expressions of those above variables can be expressed as:

$$\begin{cases} U_{ld}(k+1) = U_{ld}(k) + \dfrac{\Delta T}{C_{ld}} \cdot [U_{ld}(k)/r_{ld} - i_{ld}(k)] \\ i_{ld}(k+1) = i_{ld}(k) + \dfrac{\Delta T}{L_{ld}}[U_{ld}(k) - g_l(k) \cdot U_{dc}(k)] \\ i_{cov}(k+1) = g_l(k) \cdot i_{ld}(k) \end{cases} \tag{20}$$

C. TRANSIENT ANALYSIS OF FAULTY DC MICROGRID

According to [27], there are only two kinds of variables (nodes voltages and lines currents) in system structures of DC microgrids. And the difference expressions of nodes voltages and lines currents can be expressed as:

$$\begin{cases} u_i(k+1) = u_i(k) + \dfrac{i_{cov\_i}(k) - \sum_{k=1}^{N} i_{ik}(k)}{C_i} \cdot \Delta T \\ i_l(k+1) = i_l(k) + \dfrac{u_a(k) - u_b(k) - i_l(k) \cdot R_l}{L_l} \cdot \Delta T \end{cases} \tag{21}$$

where u_i is the voltage of node i, i_l is the current of line l, i_{ik} is the current from node i to node k, i_{cov_i} is the current from converter of node i, C_i is the capacitance of node i, R_l and L_l are the resistance and inductance of line l.

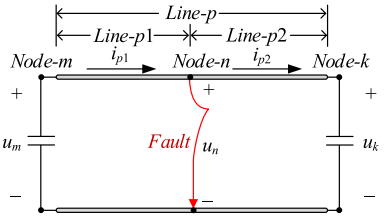

FIGURE 9. Faulty line in DC microgrid.

Taking pole-to-pole short circuit fault as an example and supposing a fault occurs on line p. The faulty line is shown in Fig. 9. A faulty node n and two DC lines p_1, p_2 are denoted following the occurrence of the fault. The voltage of node n and currents of lines p_1, p_2 can be expressed as (22). The difference expressions of other nodes voltages and lines currents still use (21).

$$\begin{cases} u_n(k+1) = \left(i_{p1}(k) - i_{p2}(k)\right) \cdot R_{fault} \\ i_{p1}(k+1) = i_{p1}(k) + \dfrac{u_m(k) - u_n(k) - i_{p1}(k) \cdot R_{p1}}{L_{p1}} \cdot \Delta T \\ i_{p2}(k+1) = i_{p2}(k) + \dfrac{u_n(k) - u_k(k) - i_{p2}(k) \cdot R_{p2}}{L_{p2}} \cdot \Delta T \end{cases} \tag{22}$$

where u_n, u_m, u_k are the voltages of node n, m, k; i_{p1} and i_{p2} are the currents of line p_1 and p_2; R_{fault} is the fault resistance; R_{p1}, R_{p2} and L_{p1}, L_{p2} are the resistances and inductances of line p_1 and p_2. ΔT is the size of iteration step.

Based on the above analysis, the transient analysis process of a ring-type DC microgrid is iterated by three parts: transient modeling of AC units and their converters; transient modeling of DC units and their converters; and transient modeling of variables in system structures of DC microgrids. Finally, the process of transient analysis of a DC microgrid is shown as Fig. 10.

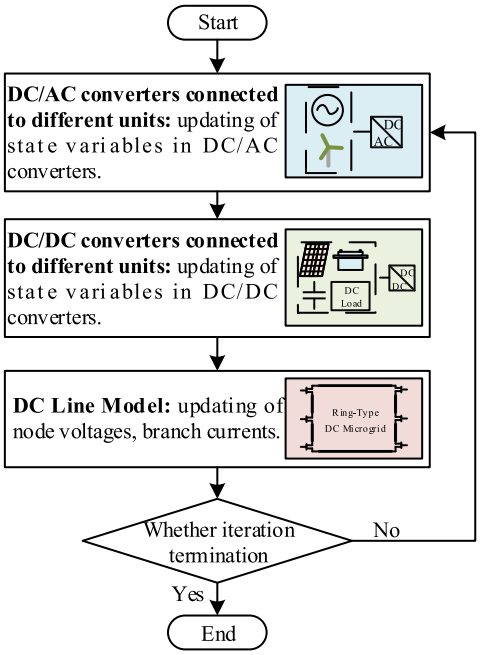

FIGURE 10. Transient analysis process of ring-type DC microgrid.

IV. NUMERICAL ANALYSIS

The transient calculation models are coded as M-code in Matlab. And the faulty DC microgrid is run in Typhoon 602+ CHIL test system. The accuracy of the transient calculation models is validated by the comparison with the CHIL test system. In addition, to decouple the analysis of each converter's modeling, the converters are connected to the ideal DC grid respectively. To verify the accuracy of converters' models in a whole DC microgrid, the converters are connected through a ring-type DC microgrid.

A. CONTROL-HARDWARE-IN-LOOP TEST SYSTEM

The experiment platform based on CHIL is shown as Fig. 11. Firstly, the experiment scenarios of DC microgrid are designed in CHIL platform of Typhoon 602+. And the time step of Typhoon 602+ is 1μs. Meanwhile, the control systems of various converters are implemented in TMS32028335DSP+ Spartan 6XC6SLX16FPGA control board and the modulation frequency is 10kHz.

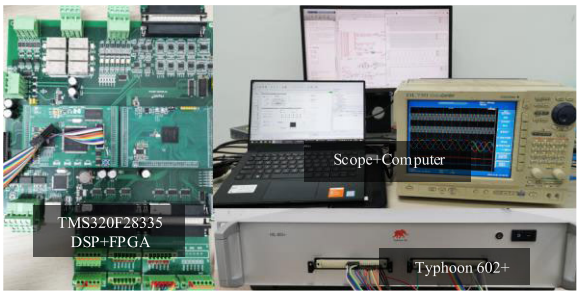

FIGURE 11. Experiment platform based on CHIL.

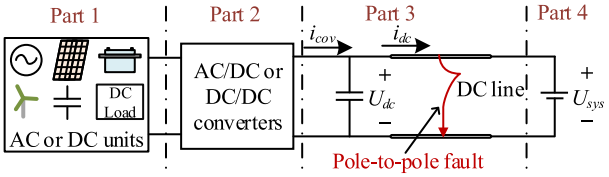

FIGURE 12. The Structure of Test System of AC/DC and DC/DC converters.

B. VALIDATION OF TRANSIENT MODELING OF CONVERTERS

1) STRUCTURE AND PARAMETERS OF TEST SYSTEM

The structure of test system of AC/DC and DC/DC converters are shown as Fig. 12. And the test system can be divided into four parts. Firstly, part 1 is the connected AC or DC units, including AC grid, WF, PV, ES (battery and super capacitor) and DC load. Secondly, part 2 is the converters corresponding to various units: AC grid uses VSC controlled by DC-link voltage control, and the voltage is set as 1000V; WF uses VSC controlled by active power control, and the output power is set as 100kW; PV uses boost circuit controlled by MPPT; ES uses bidirectional chopper circuit controlled by DC-link voltage control, and the voltage is set as 1000V; DC load uses buck circuit controlled by DC-link voltage control, and the voltage of DC load is set as 300V. Thirdly, part 3 includes the DC-link capacitor and DC line. The capacitance of capacitor is set as 8000μF. The length, resistance and inductance of DC line is set as 3km, 0.2Ω and 4mH. Finally, part 4 is a DC voltage source, which is used as an equivalent for the DC microgrid. And the voltage U_{sys} is set as 960V.

It is assumed that pole-to-pole faults occur at midpoint of DC line. And to simulate different fault degrees, the fault resistance takes the values of 1$\mu\Omega$, 1mΩ, 0.1Ω, 0.2Ω and 0.4Ω. And transients characteristics of this test system are analyzed through CHIL test system, calculation model proposed in this paper and calculation model ignoring i_{cov}. Moreover, the absolute error is used to compare the calculation results and CHIL results.

The errors of U_{dc} and i_{dc} are related to i_{cov}. However, the currents i_{cov} being injected from converters are ignored in previous researches [18]–[25]. Thus, the modeling method of ignoring the currents i_{cov} is used for comparison. And the structure of test system using pervious researches' modeling method is shown as Fig. 13.

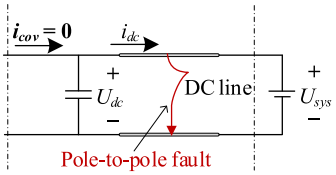

FIGURE 13. The structure of test system in pervious researches.

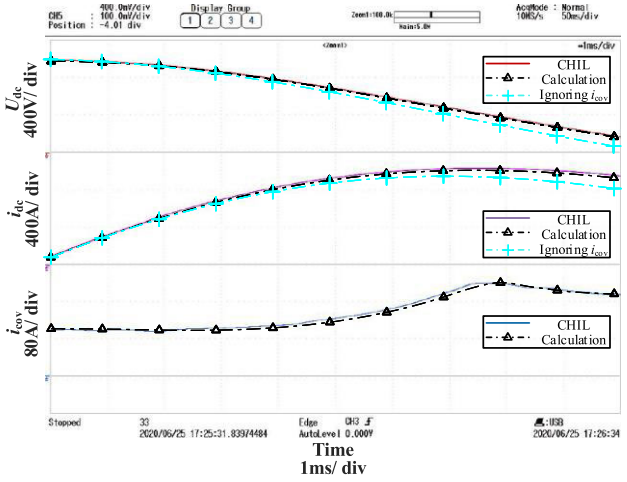

FIGURE 14. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

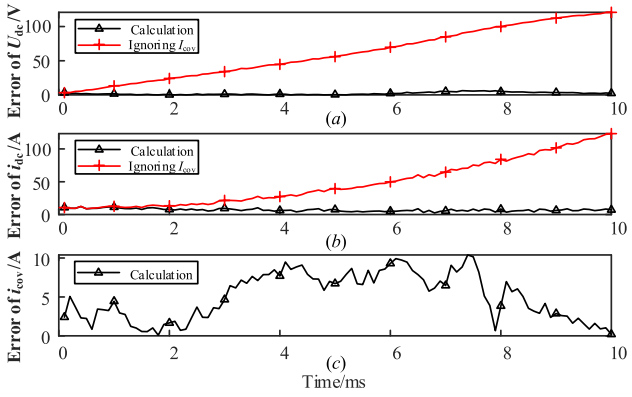

FIGURE 15. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

2) VALIDATION OF VSC CONNECTED WITH AC GIRD

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with AC grid are shown as Fig. 14. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 15. It can be found that i_{cov} obtained by calculation model is similar to i_{cov} obtained by CHIL. The current i_{cov} has the maximum error at the period from 3ms to 8ms. And the maximum error of i_{cov} is less than 10A. Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} by calculation method and CHIL are 10.87V and 11.07A. Otherwise, the errors of U_{dc} and i_{dc} will reach 124.98V and 126.57A when i_{cov} is not considered in calculation method.

TABLE 1. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	107.71	1.33	59.82	6.90	0.15	2.80
1mΩ	111.21	3.33	62.46	9.91	0.37	4.53
0.1Ω	124.98	2.67	63.99	10.87	1.07	4.68
0.2Ω	135.84	2.00	64.59	11.45	0.69	5.01
0.4Ω	147.67	2.00	65.54	17.28	0.63	6.10
The Error of i_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	128.77	0	46.64	9.92	0	3.87
1mΩ	131.57	0.15	45.54	8.47	0.09	2.90
0.1Ω	126.57	0.08	44.31	11.07	0.09	3.64
0.2Ω	120.13	0.18	42.86	12.97	0.08	4.00
0.4Ω	112.24	2.56	40.46	12.92	0.22	4.44

The more detailed error results under different fault resistances (1$\mu\Omega$, 1mΩ, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 1. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 107V and the average errors of U_{dc} are greater than 59V. The maximum errors of i_{dc} are greater than 112A, and the average errors of i_{dc} are greater than 40A. On the contrary, when the transient characteristics of VSC and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 18V and the average errors of U_{dc} are less than 6V. The maximum errors of i_{dc} are less than 13A, and the average errors of i_{dc} are less than 5A.

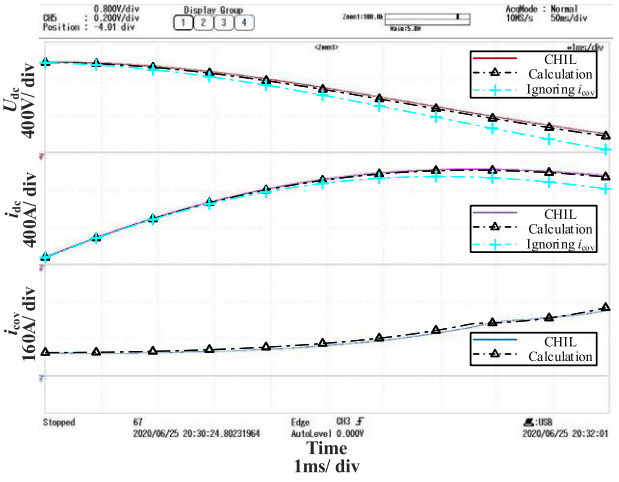

FIGURE 16. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

3) VALIDATION OF VSC CONNECTED WITH WF

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with WF are shown as Fig. 16. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 17. It can be found that the trend of i_{cov} calculated by the proposed method is similar

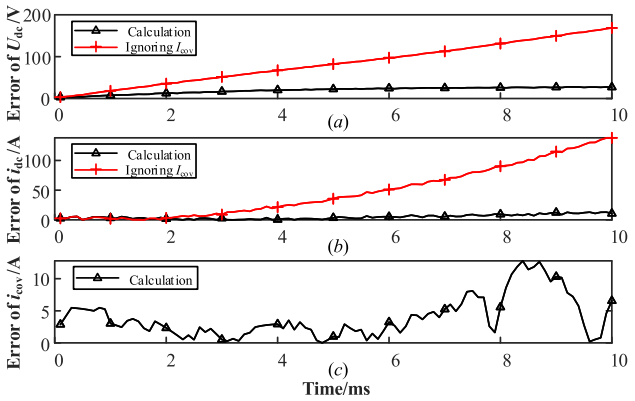

FIGURE 17. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

to that in CHIL test system. The error of i_{cov} is less than 5A within 7ms from fault occurs. And the maximum error of i_{cov} is less than 15A within 10ms from fault occurs. Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} are 27.78V and 14.39A. Otherwise, the errors of U_{dc} and i_{dc} will reach 167.98V and 138.91A when i_{cov} is not considered in calculation method.

The more detailed error results under different fault resistances ($1\mu\Omega$, $1m\Omega$, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 2. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 139V and the average errors of U_{dc} are greater than 74V. The maximum errors of i_{dc} are greater than 109A, and the average errors of i_{dc} are greater than 40A. On the contrary, when the transient characteristics of VSC and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 42V and the average errors of U_{dc} are less than 19V.The maximum errors of i_{dc} are less than 24A, and the average errors of i_{dc} are less than 11A.

TABLE 2. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	191.07	2.67	94.40	41.05	2.67	18.57
1mΩ	188.23	3.33	91.55	38.10	3.33	15.74
0.1Ω	167.98	3.33	83.83	27.78	3.33	12.80
0.2Ω	151.50	3.33	74.40	18.31	2.70	11.89
0.4Ω	139.67	3.33	75.06	18.92	3.33	15.06
The Error of i_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	154.43	0	49.56	23.10	0	10.92
1mΩ	154.20	2.43	49.36	17.01	0	7.94
0.1Ω	138.91	0.53	47.12	14.39	0	5.11
0.2Ω	124.80	13.18	50.00	19.47	2.61	9.52
0.4Ω	109.81	0.21	40.58	12.00	0.23	4.51

4) VALIDATION OF BOOST CIRCUIT CONNECTED WITH PV

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with PV are

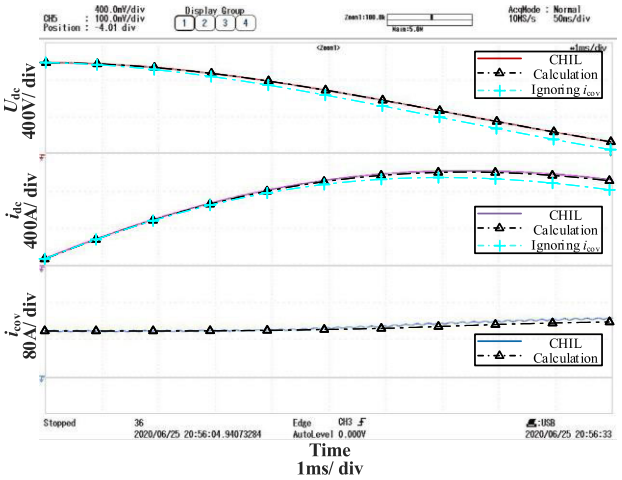

FIGURE 18. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

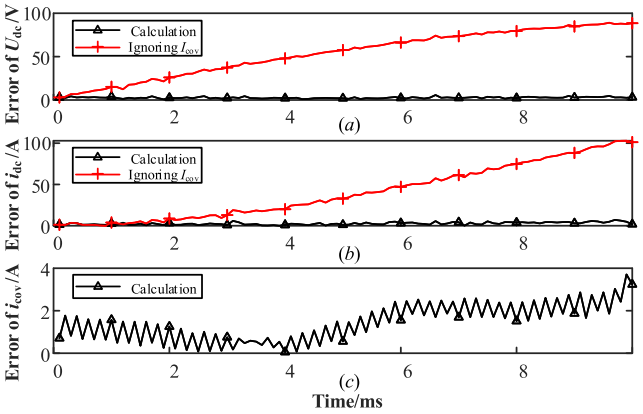

FIGURE 19. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

shown as Fig. 18. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 19. It can be found that ripples exist in i_{cov} obtained by CHIL, and the frequency is 5kHz. This is because the duty cycle in control system varies by a fixed step size. Since the boost circuit is simplified by mean value model, the ripples are not reflected in the proposed calculation model. Despite the ripples, the error is less than 4A within 10ms after fault occurs. Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} are 5.40V and 7.62A. Otherwise, the errors of U_{dc} and i_{dc} will reach 85.72V and 101.58A when i_{cov} is not considered in calculation method.

The detailed error results under different fault resistances ($1\mu\Omega$, $1m\Omega$, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 3. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 85V and the average errors of U_{dc} are greater than 50V. The maximum errors of i_{dc} are greater than 88A, and the average errors of i_{dc} are greater than 35A. On the contrary, when the transient characteristics of boost circuit and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 13V

TABLE 3. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	95.90	3.67	59.06	12.13	2.32	7.87
1mΩ	91.09	2.40	55.25	8.15	0.67	4.05
0.1Ω	85.72	3.00	50.28	5.40	0.05	1.93
0.2Ω	92.09	1.00	55.22	5.73	1.00	3.25
0.4Ω	92.93	2.33	55.11	6.06	0.71	2.57
The Error of i_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	117.43	0	41.57	13.77	0.16	6.40
1mΩ	112.87	0	41.88	8.86	0	2.99
0.1Ω	101.58	9.59	44.14	7.62	0.08	2.80
0.2Ω	101.46	0.18	38.65	6.83	0.03	2.52
0.4Ω	88.90	0.09	35.76	6.10	0.08	2.04

and the average errors of U_{dc} are less than 8V.The maximum errors of i_{dc} are less than 14A, and the average errors of i_{dc} are less than 7A.

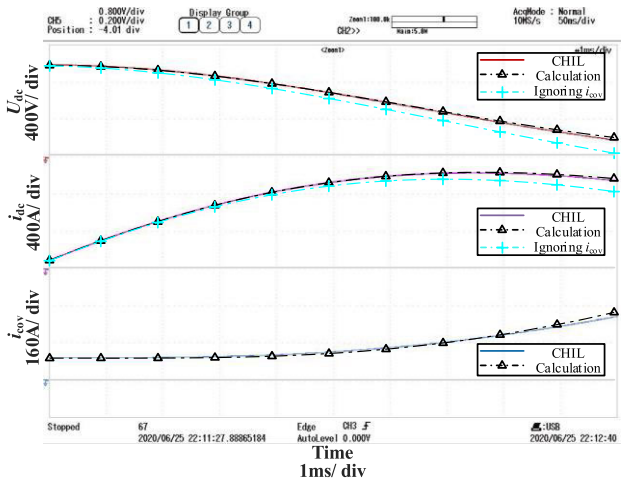

FIGURE 20. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

5) VALIDATION OF BIDIRECTIONAL CHOPPER CIRCUIT CONNECTED WITH ES

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with battery are shown as Fig. 20. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 21. Because the life of batteries decreases as the number of charges and discharges increases, the high frequency component of inputs is generally filtered out in the control system of batteries. The short circuit fault is a high frequency power fluctuation. Therefore, in the proposed calculation model, the output of control system for battery is considered unchanged from fault occurrence to fault detection. Although the approximate processing of control system results in a monotonic increase of i_{cov}'s error, the error is less than 10A within 10ms after

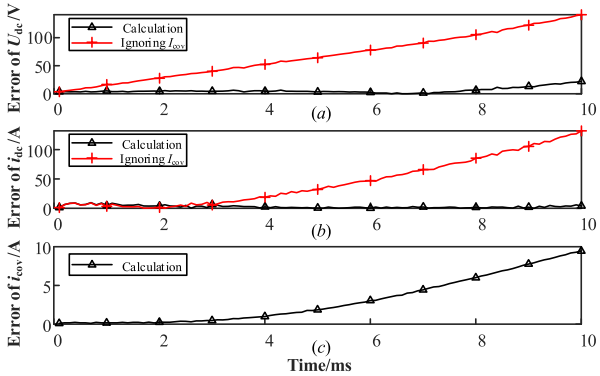

FIGURE 21. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

fault occurs Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} are 27.72V and 12.53A. Otherwise, the errors of U_{dc} and i_{dc} will reach 135.64V and 126.57A when i_{cov} is not considered in calculation method.

The detailed error results under different fault resistances (1$\mu\Omega$, 1mΩ, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 4. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 132V and the average errors of U_{dc} are greater than 61V. The maximum errors of i_{dc} are greater than 107A, and the average errors of i_{dc} are greater than 40A. On the contrary, when the transient characteristics of bidirectional chopper circuit and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 28V and the average errors of U_{dc} are less than 8V.The maximum errors of i_{dc} are less than 13A, and the average errors of i_{dc} are less than 7A.

TABLE 4. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	143.41	3.67	66.32	25.20	0.03	6.16
1mΩ	140.56	3.67	65.10	27.99	0.01	6.26
0.1Ω	135.64	2.33	61.56	27.72	0.07	7.51
0.2Ω	136.50	3.00	64.48	21.80	0	5.43
0.4Ω	132.01	3.00	63.56	18.34	0.01	4.70
The Error of i_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	143.43	0.66	47.93	7.38	0	2.07
1mΩ	137.85	1.23	49.06	10.93	0.16	3.21
0.1Ω	126.57	9.59	49.56	12.53	0.27	6.96
0.2Ω	117.51	0.30	43.29	10.63	0.13	2.44
0.4Ω	107.57	3.90	40.91	7.19	0.03	3.49

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with SC are shown as Fig. 22. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 23. It can be found that the trend of i_{cov} calculated by the proposed method is similar to that in CHIL test system. The maximum

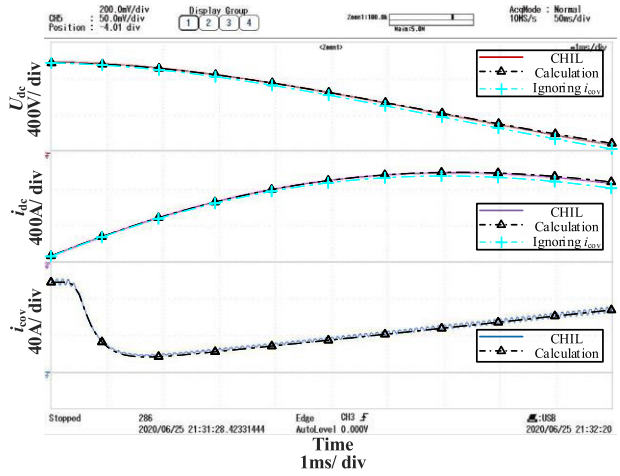

FIGURE 22. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

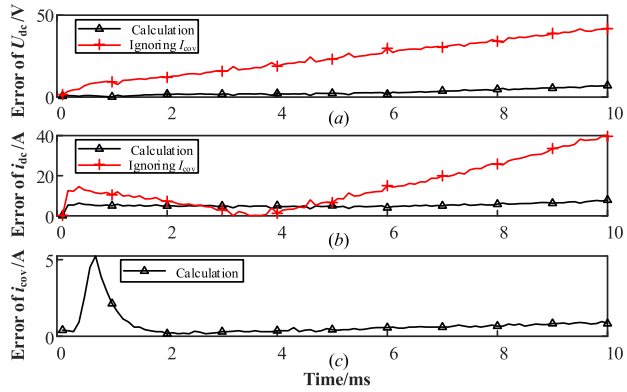

FIGURE 23. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

error of i_{cov} occurs within 1ms after fault occurs, and the value is less than 5A. The error of i_{cov} is reduced and maintained within 2A from 1ms to 10ms. Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} are 10.36V and 7.45A. Otherwise, the errors of U_{dc} and i_{dc} will reach 39.39V and 40.57A when i_{cov} is not considered in calculation method.

The detailed error results under different fault resistances ($1\mu\Omega$, $1m\Omega$, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 5. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 41V and the average errors of U_{dc} are greater than 19V. The maximum errors of i_{dc} are greater than 36A, and the average errors of i_{dc} are greater than 13A. On the contrary, when the transient characteristics of bidirectional chopper circuit and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 12V and the average errors of U_{dc} are less than 4V. The maximum errors of i_{dc} are less than 8A, and the average errors of i_{dc} are less than 3A.

6) VALIDATION OF BUCK CIRCUIT CONNECTED WITH DC LOAD

Taking the fault resistance of 0.1Ω as an example, the waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov} (filtered through 500Hz) of the test system connected with DC load are

TABLE 5. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault Resistance	Ignored Injected Current			Considering Control System		
	Max	Min	Avg	Max	Min	Avg
$1\mu\Omega$	72.74	0	20.45	10.14	0	3.81
$1m\Omega$	69.90	1.33	20.87	9.65	0.10	3.63
0.1Ω	39.39	2.66	20.82	10.36	0.02	3.71
0.2Ω	41.09	0.66	19.93	11.22	0.04	4.02
0.4Ω	45.67	1.33	23.12	10.01	0.01	3.28
The Error of i_{dc} under Different Fault Resistances						
Fault Resistance	Ignored Injected Current			Considering Control System		
	Max	Min	Avg	Max	Min	Avg
$1\mu\Omega$	44.77	0.04	15.47	7.40	0.11	2.34
$1m\Omega$	44.53	0.05	15.52	7.36	0	2.41
0.1Ω	40.57	0.06	14.61	7.45	0.33	2.49
0.2Ω	37.46	0.04	13.85	7.36	0.05	2.14
0.4Ω	36.98	0.33	14.56	6.36	0.11	2.69

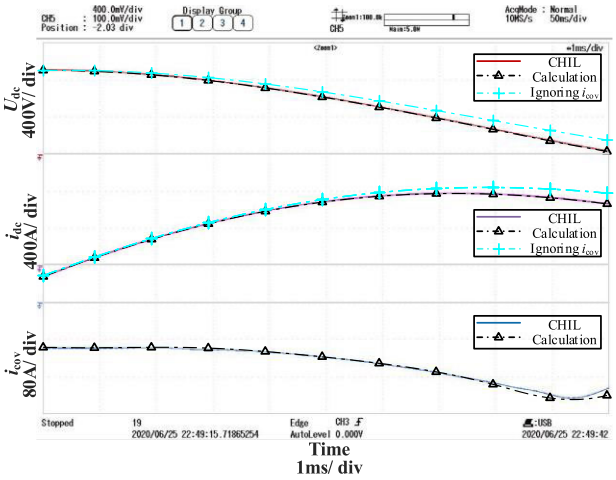

FIGURE 24. Waveform of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

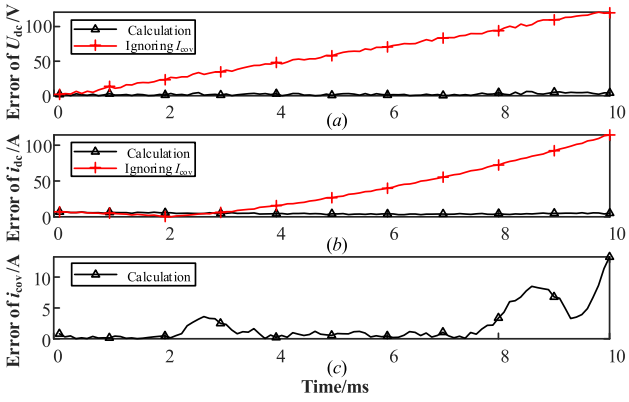

FIGURE 25. Error of DC-link voltage U_{dc}, line current i_{dc} and i_{cov}.

shown as Fig. 24. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 25. It can be found that the trend of i_{cov} calculated by the proposed method is similar to that in CHIL test system. The error of i_{cov} is less than 5A within 8ms from fault occurs. And the maximum error of i_{cov}

is less than 15A within 10ms from fault occurs. Furthermore, since i_{cov} is considered in the calculation of U_{dc} and i_{dc}, the maximum errors of U_{dc} and i_{dc} are 7.74V and 14.33A. Otherwise, the errors of U_{dc} and i_{dc} will reach 123.62V and 116.25A when i_{cov} is not considered in calculation method.

The detailed error results under different fault resistances ($1\mu\Omega$, $1m\Omega$, 0.1Ω, 0.2Ω and 0.4Ω) are shown in Table 6. When i_{cov} is not considered in calculation method, the maximum errors of U_{dc} are greater than 111V and the average errors of U_{dc} are greater than 57V. The maximum errors of i_{dc} are greater than 97A, and the average errors of i_{dc} are greater than 34A. On the contrary, when the transient characteristics of buck circuit and the corresponding injected current i_{cov} are considered, the maximum errors of U_{dc} are less than 8V and the average errors of U_{dc} are less than 5V.The maximum errors of i_{dc} are less than 13A, and the average errors of i_{dc} are less than 7A.

TABLE 6. The error of U_{dc} and i_{dc} under different fault resistances.

The Error of U_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	111.75	0.43	57.04	7.68	0.01	4.79
1mΩ	113.21	0.43	58.20	7.41	0.03	5.01
0.1Ω	123.62	0.44	62.78	7.74	0.20	3.10
0.2Ω	124.73	0.67	60.40	5.85	0.05	2.01
0.4Ω	118.39	0.45	58.89	6.99	0	1.58
The Error of i_{dc} under Different Fault Resistances						
Fault	Ignored Injected Current			Considering Control System		
Resistance	Max	Min	Avg	Max	Min	Avg
1μΩ	115.51	0.12	39.69	12.14	2.18	5.02
1mΩ	115.71	0.09	39.62	11.83	2.73	5.41
0.1Ω	116.25	0.15	38.55	14.33	2.38	6.97
0.2Ω	109.19	0.12	36.97	7.00	1.02	3.42
0.4Ω	97.60	0.38	34.13	5.33	0.18	2.17

7) COMPARISON OF TRANSIENT MODEL OF DIFFERENT CONVERTERS

The errors of U_{dc} and i_{dc} are related to i_{cov}. However, the currents i_{cov} being injected from converters are ignored in previous researches [18]–[25]. And i_{cov} is influenced by the control of converters. For example, the control target is DC-link voltage when converter connects to SC. To suppress the decrease of the DC-link voltage after fault occurs, the modulation ratio increases rapidly. This causes the drop of i_{cov}. Thus, the average errors of U_{dc} and i_{dc} are only 21.04V and 14.80A even if i_{cov} is ignored when converter connects to SC. On the contrary, the control target is selected as active power when converter connects to WF. The control reduces VSC's AC side voltage U_c to increase active power delivery, and i_{cov} increases continuously after the fault. As a result, the average errors of U_{dc} and i_{dc} reach 83.85V and 47.32A if i_{cov} is ignored when converter connects to WF. Compared with the previous researches which ignores the control effect of converters and injected current i_{cov}, the method proposed in this paper can always guarantee the calculation accuracy in the fault transient analysis.

C. VALIDATION OF TRANSIENT MODELING OF DC MICROGRID

1) PARAMETERS OF RING-TYPE DC MICROGRID

The ring-type DC microgrid shown in Fig. 1 is taken as the test system. The parameters and control targets of control systems in converters are the same as those in Part B, Section IV. In addition, both the bidirectional chopper circuits connect with ESs and the VSC connects with AC grid adopt DC-link voltage control. To prevent the conflicts of their control, the control systems in battery and SC only operate when the DC-link voltage is 50V away from 1000V (lower than 950V or higher than 1050V).

The circuit parameters of DC microgrid include DC-link capacitances, lines resistances and inductances. The DC-link capacitances of all converters are set as 8000μF. The resistances and inductances of lines are shown in Table 7. Moreover, the pole-to-pole faults are assumed to occur at midpoint of DC line. And the fault resistance is set as 0.1Ω.

TABLE 7. Resistances and inductances of DC lines.

Line	Resistance	Inductance	Line	Resistance	Inductance
1-2	0.20Ω	3.00mH	3-6	0.24Ω	3.60mH
1-4	0.05Ω	0.75mH	4-5	0.20Ω	3.00mH
2-3	0.25Ω	3.75mH	5-6	0.18Ω	2.70mH

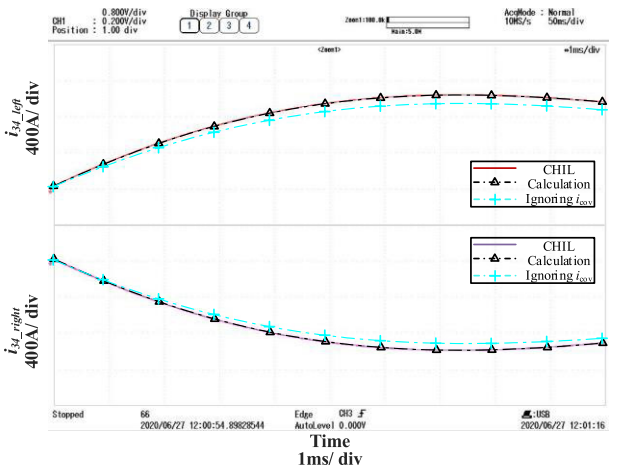

FIGURE 26. Waveform of currents on fault line 3-6.

2) CALCULATION ACCURACY

Taking the fault occurrence at the midpoint of line 3-6 as an example, the waveform of the currents i_{36_left} and i_{36_right} at fault line 3-6 are shown in Fig. 26. In addition, the currents calculated by the proposed method and currents calculated in the case of ignoring i_{cov} are also shown in Fig. 26. And the errors of the proposed calculation model and the calculation model ignoring i_{cov} compared with the CHIL test system are shown in Fig. 27.

It can be found that the trend of i_{36_left} and i_{36_right} calculated by the proposed method are the same as that in CHIL test system. And the maximum errors of i_{36_left} and i_{36_right} are

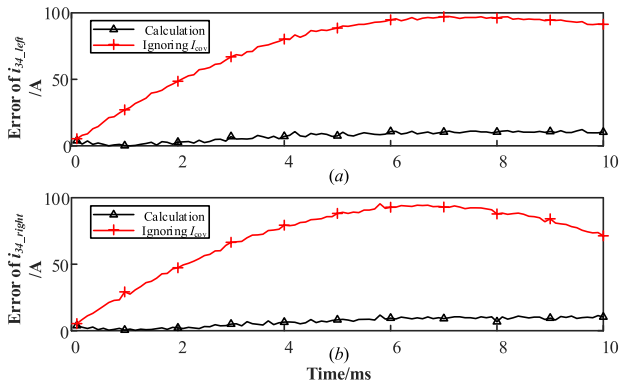

FIGURE 27. Error of currents on fault line 3-6.

12.22A and 11.74A respectively. On the contrary, the errors of i_{36_left} and i_{36_right} will reach 97.30A and 95.47A when i_{cov} is not considered.

The more detailed error results under different faulty conditions are shown in Table 8. It can be found that, after considering the i_{cov} that changes with the control systems, the errors of calculated fault currents are reduced. The average error decreased from 76.56A to 6.77A.

TABLE 8. The Error of currents of faulty DC lines under different faulty conditions.

Faulty Conditions		Left (unit: A)			Right (unit: A)		
		Max	Min	Avg	Max	Min	Avg
Line 1-2	left	102.24	0.67	79.87	12.23	0.55	7.94
	right	111.21	1.33	80.43	11.34	0.47	7.23
Line 1-4	left	120.23	6.31	89.32	10.35	0.17	6.45
	right	117.34	5.32	86.49	10.43	0.34	6.42
Line 2-3	left	101.43	3.48	67.67	9.88	0.08	6.52
	right	100.89	4.43	68.83	9.67	0.24	6.31
Line 3-6	left	97.30	5.33	74.57	12.22	0.05	7.20
	right	95.47	5.37	70.79	11.74	0.31	6.64
Line 4-5	left	112.3	5.23	75.35	9.67	0.53	6.35
	right	116.3	5.64	78.34	10.23	0.56	6.95
Line 5-6	left	107.8	3.56	72.42	9.45	0.23	6.77
	right	104.4	4.33	74.64	9.32	0.75	6.43

3) CALCULATION EFFICIENCY

Referring to the analysis method in [21], the calculation efficiency of the proposed calculation method is analyzed. Using PC with Intel(R) core(TM) i7-8700 CPU @3.20 GHz as the experiment platform. The proposed calculation model for the six-terminal ring-type DC microgrid is coded as M-code in Matlab 2018b. The transient characteristics of variables are analyzed, and the time range is 10ms after fault occurs. The time spent under calculation model is 4.23ms. On the other hand, the DC microgrid is also simulated by Matlab/Simulink with 1μs time step. The short-circuit fault occurred at t = 1.0 s, and we observe the simulation results from 1.0s to 1.01s (time range is also 10ms). The time spent under simulation is 2.45s. The comparison shows that the transient model proposed in this paper is over 413 times faster than simulation. This validates the proposed method can analyze the faulty DC microgrid efficiently.

TABLE 9. The time spending under calculation model and simulation.

Calculation model	Simulation	Speedup factor
4.23ms	2.45s	413.71

V. CONCLUSION

Through the analysis in this paper, it is proved that the control effect in converters has contributions on the fault transient characteristic of DC microgrid. Therefore, the influences of the control systems are being considered in the establishment of the transient calculation model in this paper. In detail, the transient characteristics of different converters (including voltage source converter, boost circuit, bidirectional chopper circuit and buck circuit) with different units (including AC grid, wind farm, photovoltaic, energy storage and DC load) are being analyzed. And then the transient model of ring-type DC microgrid, connecting with AC/DC units by different converters, is established. By comparison with the CHIL test system, the transient model proposed in paper improves the transient analysis accuracy significantly and enhances the computational efficiency.

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