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Fast-Settling Two-Stage Automatic Gain Control for Multi-Service Fibre-Wireless Fronthaul Systems

WEN LI[1,2], AIXIN CHEN[1], (Member, IEEE), XUEFENG WANG[2], TONGYUN LI[3], (Member, IEEE), RICHARD V. PENTY[3], (Senior Member, IEEE), AND XIAOBIN LIU[2]

[1]School of Electronic and information Engineering, Beihang University, Beijing 100191, China
[2]Beijing Institute of Aerospace Control Devices, Beijing 100094, China
[3]Electrical Division, Centre for Photonic Systems, Engineering Department, Cambridge University, Cambridge CB30FA, U.K.

Corresponding author: Wen Li (liwen5658@ buaa.edu.cn)

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ABSTRACT With the development of fast digitiser and digital signal processing techniques, wide-band digital radio-over-fiber (DRoF) based wireless fronthaul systems have been extensively studied as a way of offering multi-service wireless coverage. With data compression, the high digital data rate caused by digitisation can be reduced so as to minimise the infrastructure cost for last-mile cellular coverage. However, data compression always comes with the cost of a lower input power dynamic range. To overcome the issue, this paper proposes a novel fast-settling two-stage automatic gain control (FSS-AGC) algorithm, in which gain adjustment is carried out by a multi-threshold decision mechanism with a fast-settling time (within 2μ s), high stability and great accuracy. By introducing a novel gain control mechanism which simultaneously adjusts the gain in the digital and RF domains, the loss of dynamic range after compression is compensated. This algorithm is applied and demonstrated in a DRoF based digital distributed antenna system (DDAS) which supports all current cellular services from 3 Chinese mobile network operators (MNOs). The demonstration shows over 73dB dynamic range, with 40dB improvement compared with conventional links. Its promising properties and excellent performance enable its potential application in next-generation converged networks for Internet of things (IoT) and 5G services.

INDEX TERMS Automatic gain control, digital radio over fibre, settling time, dynamic range, gain control, 4G, 5G.

I. INTRODUCTION

With low cost, less chromatic dispersion, great flexibility and strong anti-interference, digital radio over fibre (DRoF) has been widely used in indoor signal distribution systems [1]–[3]. With the reuse of existing broadband high-speed optical network [4], long-distance transmission of RF signals can be achieved until the received signal strength goes below the sensitivity of the optical transceiver module in a low cost manner. As DRoF system lowers the infrastructure cost of wireless networks by supporting simultaneous transmission of multi-service RF signals as well as making use of existing network infrastructure and devices, it is increasingly preferred by mobile network operators (MNOs) for providing last-mile cellular coverage. DRoF based cloud radio access network (C-RAN) is widely deployed for 4G services [5]. However, the simultaneous transmission of multi-microwave and even multi-millimetre-wave signals leads to a rapid increase in the transmission rate of the link in the system, which demands expensive high-speed optical transceiver and fibre, especially when several commercial cellular bands from MNOs are required to be converged onto a single

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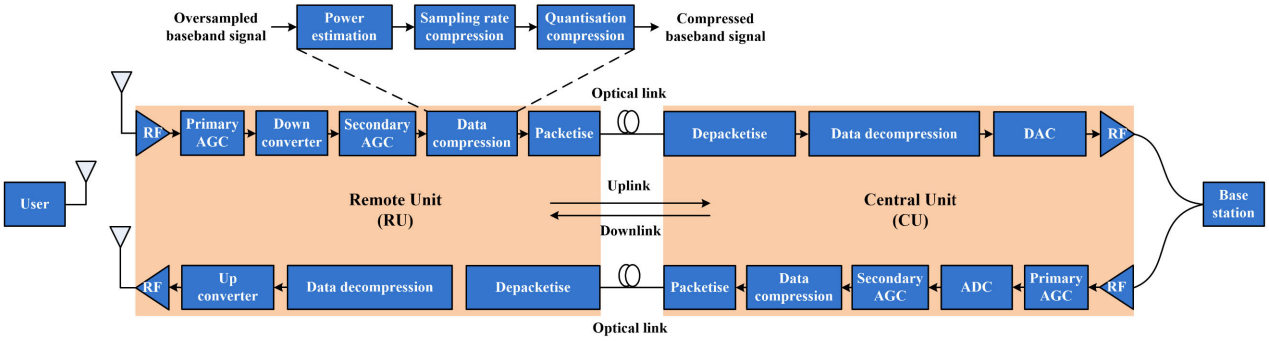


FIGURE 1. Block diagram of the DRoF transceiver system.

network infrastructure. Current common public radio interface (CPRI) requires a 1.2288Gbps link for a single 20MHz LTE signal [6]. The capacity requirement could be a few hundred Gbps for a multi-service system including several multiple input and multiple output (MIMO) based 5G services.

In fact, studies have been performed on the multi-service low-bit rate transmission system based on data compression algorithm allowing more services to be transmitted over a given link with limited capacity. In [7], the authors proposed a novel data compression algorithm which has shown a three-fold increase in data transmission efficiency compared with CPRI. In such a system, digital signal resampling and quantisation compression was performed so as to reduce the transmission data rate per service. However, the lossy compression technique also comes with the cost of reduced input power dynamic range and signal transmission performance [8]. Under the influence of communication distance variation and multipath effects over the uplink, the power of the RF signals transmitted by DRoF varies greatly. As a result, a wide input power dynamic range is desirable for the system [9], [10].

Conventionally, we use frontend analogue automatic gain control (AGC) to improve the input dynamic range [11] by automatically adjusting the gain applied on the input power. In this analogue AGC, power detection and gain control are performed using analogue loop-back or loop-forward circuit [12]–[14]. However, it suffers from low gain-control accuracy due to the limited control complexity implemented on analogue circuitry. Digital automatic gain control (DAGC) with digital control loop implemented on field programmable gate array (FPGA) or application specific integrated circuit (ASIC) is now more commonly used in wireless communication system designs to perform accurate gain estimation in the digital domain so that the system is more robust in terms of reconfigurability and flexibility [15], [16]. In [17], an improved multistage AGC for distribute antenna system (DAS) is presented. The system improves the dynamic range compared with the conventional low-cost optical transponder link. In [18], a fast DAGC with high accuracy for digital audio broadcasting (DAB) receivers is proposed. The algorithm is simplified with only shifting and comparing and it is easy to use. However, although the proposed DAGC can adjust the received signal within 0.5 ms timescale, it is still unable to meet the LTE requirements due to LTE's fast variation in signal level. In [19], a fast convergence two-stage AGC algorithm is proposed for a bluetooth low energy (BLE) compliant radio, while the gain tuning step is limited as the algorithm feeds the control signal to the analog chip. A feed-forward AGC algorithm proposed in [20], [21] focuses on making the most of ADC quantisation bits and maintaining stable peek-to-average ration (PAR). However, the accuracy and the stability of the system need to improve due to its open-loop structure. In [22], look-up-table method is used to control the gain of multistage RF devices accurately, which greatly improves the dynamic range of the system. However, several amplifier chips are needed for this approach, which increases hardware cost.

In this paper, a novel fast-settling two-stage Automatic Gain Control (FSS-AGC) algorithm for dynamic range enhancement in multi-service low-bit rate DRoF based digital distributed antenna system (DDAS) systems is proposed and studied. The proposed algorithm introduces a two-stage gain control loops which includes primary and secondary AGC loops. Besides, it adopts a multi-threshold comparing method in the control period. It seeks to improve the dynamic range of the DDAS system in a fast and stable way with data compression at the same time. Compared with the previous approach, the multi-service low-bit rate DDAS system with FSS-AGC improves the dynamic range by 40dB and increases the dynamic range to more than 74dB. Moreover, the demonstration shows that the error vector magnitude (EVM) performance of the system with the FSS-AGC is a lot better than that of the system with the single-stage AGC, implying that the signal transmitted through the low bit rate DRoF link with FSS-AGC can distort less. The simulation result also shows that its response time is less than 2μs with great stability and accuracy.

II. SYSTEM REQUIREMENT AND THE PROPOSED AGC ARCHITECTURE

Fig. 1 shows the block diagram of a single path of the multi-service DRoF system. For the uplink, a dipole omni-directional antenna is used to collect the RF signal from the users. The amplification stages are included to compensate

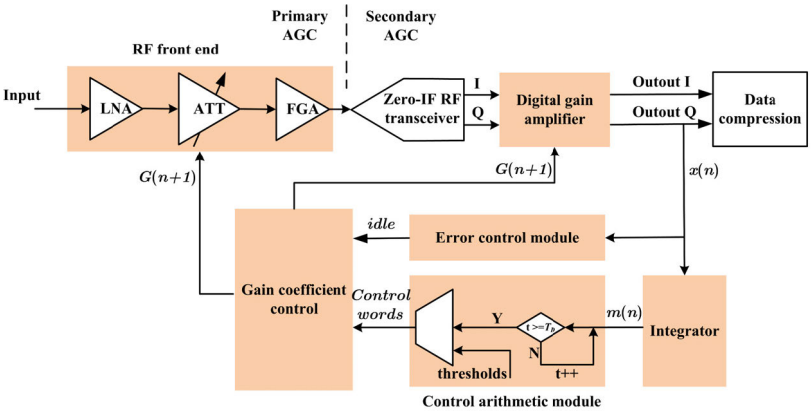


FIGURE 2. The principal block diagram of the FSS-AGC algorithm.

the wireless loss. The gain of the amplifier is adjusted dynamically by the primary AGC to regulate the RF power. The RF signal is then converted to a baseband waveform by a downconverter. Digital signal processing, including the secondary AGC and data compression, is carried out before the data symbols are packetised and transmitted to the central unit (CU) over a single model fibre (SMF). At the optical receiver, there is data decompression processing to reassemble the signal from the depacketised data symbols, and then the signal is converted back to the RF signal by an upconverter. The downlink operates in a similar manner, generating the RF signals from the CU and transporting them to the remote unit (RU) for signal coverage. However, the uplink of the system requires a larger dynamic range due to the unknown input power which depends on the wireless transmission distance between the user mobile station and the RU antenna. For this reason, we focus on the uplink performance in this paper.

In order to support low-bit rate multi-service transmission, as shown in Fig. 1, a data compression algorithm, which includes the sampling rate compression and the quantisation compression, is introduced in the system. Sampling rate compression is performed by down sampling of the IQ data stream at a lower clock rate with optimized sampling offsets [23]. Here, we remove the redundancy in sampling by filtering the signal with cutcoff frequency close to its highest spectral component at baseband. Moreover, quantisation compression is applied by removing the least significant bits (LSBs) and truncating the most significant bits (MSBs) in a nonlinear manner. However, the reduction of quantisation resolution causes the RF dynamic range of the system to drastically decrease. According to ADC theory, each effective number of bits (ENOB) decrease will worsen the signal-to-quantisation-noise (SQNR) of digitization by roughly 6dB. In this case, in order to maintain a wide input dynamic range of the system, the frontend AGC loop is placed before the data compression block to keep the level of the input digital signal within a certain range. In 4G LTE and 5G new radio (NR), orthogonal frequency division multiplexing (OFDM) technology is used to encode user channels on multiple resource blocks with different subcarrier frequencies. This will cause high peak-to-average power ratio (PAPR) which requires fast gain control and accurate gain estimation to accommodate a wider power range to achieve satisfactory Quality of Service (QoS).

Conventional DAGC performs gain estimation in the digital domain and then feed it back to the amplifier in the analogue path. In this system, we take advantage of the FPGA based digital processing circuit and use it to estimate the gain. This gain is fed into amplifiers located at both the analogue and digital frontend to perform accurate gain control and dynamic range enhancement simultaneously. To our knowledge, this is the first demonstration using the proposed two-stage AGC architecture which might create profound impact for future RF frontend designs in many applications.

III. DETAILED DESIGN

Fig. 2 shows the principal block diagram of the FSS-AGC algorithm. It consists of an integrator module, a control arithmetic module, an error control module, a gain coefficient control module and a digital amplifier module. The integrator module measures the power of the output baseband IQ signal which has been amplified by the FSS-AGC loop. The control arithmetic module compares the measured powers with the thresholds and then outputs control words. The adjusted gain values are calculated by the gain coefficient control module according to the control words, which are used to set the gain of the digital amplifier module or the RF frontend. The digital amplifier module is used to rescale the range of the baseband signal. The error control module is a detector to detect the power of the output signal in real time and prevent signal saturation. As shown in the block diagram, the algorithm mainly contains two stages, the primary AGC and the secondary AGC which are used to adjust the RF signal power and the baseband signal power to an ideal level respectively. In the uplink, the RF signal collected from antennas is fed into the RF frontend. The maximum input dynamic range of the system is primarily limited by the input dynamic range of the zero-IF RF transceiver module which performs the direct conversion of RF signals to baseband signals. As mentioned

in section 2, in order to keep the power of the RF signals within a certain range and enlarge the input dynamic range of the system, the primary AGC loop which controls the gain of the RF frontend is introduced before the zero-IF RF transceiver module. The secondary AGC control loop which controls the gain of the digital baseband signal is used before data compression and it seeks to make the most of the available quantisation bits by adjusting the baseband signal to a certain range. In this way, a nonlinear quantisation compression mechanism is applied to realize a higher data compression ratio.

A. INTEGRATOR MODULE

The proposed AGC is a feedback control algorithm. The power of the output signal needs to be measured before the gain is adjusted. A stable, accurate and fast power measurement method directly improves the stability and the timing response of the AGC. At present, moving average filter (MAF) is mostly used to measure the power of the digital signal. However, the length of the digital signal is the key factor affecting the timing response of the AGC. When the received signal power changes rapidly or the number of the digitized received signal bits is not enough, accurate measured results cannot be obtained and thus the limit cycle effect occurs [24]. In this paper, in order to measure the power of the received baseband signal with fast timing response and high stability, a backward discrete time integrator which takes the previous signal into consideration is depicted in

$$m(n) = m(n-1) + K \times 1/f_s \times x(n) \tag{1}$$

where m(n) represents the measured power of the current signal, m(n-1) represents the measured power of the previous signal, K is the coefficient which represents the effect of the new input on the output, f_s is the block sampling frequency and x(n) is the current received signal. A larger K reduces the response time of the output signal, but its stability is also reduced, causing the output signal to oscillate. As a result, a trade-off should be made between the timing response and the stability when we choose the K value.

B. CONTROL ARITHMETIC MODULE

Moreover, the algorithm adopts the method of threshold comparison in period to adjust the gain of the link. The control arithmetic module includes a counter and a threshold comparator, aiming to control the range of the output signal power between low-threshold (*low*) and high-threshold (*up*). A two-stage gain control loop will work when the measured power is out of range in a control period (T_D), which adjusts the gain of the system. We define a parameter *comp* to judge the power status, which is defined as

$$comp = \begin{cases} 0, & low \le m(n) \le up \\ 1, & others \end{cases} \tag{2}$$

In this design, the control arithmetic module will change its state to adjust the gain of the link if the number of times that *comp* appears as "1" in the T_D is greater than α, and then we set the gain adjustment idle (*tune*) as "1". Otherwise, the target gain remains the same and we set the *tune* as "0". In this way, the gain jitter that can be caused by signal instability will not happen. However, if the values of T_D and the decision factor (α) are too large, the judgment time will be too long, which will increase the response time of AGC. Moreover, the control arithmetic module adjusts the gain of the link only once in one T_D and adopts a step-by-step control method and the gain value is adjusted from small to large. In addition, the adjusting processing will not stop until the measured signal power is in the optimum range or the *tune* is "0" in the T_D. In the primary AGC control loop, the high-threshold (up_a) and the low-threshold (low_a) correspond to the maximum and minimum input power respectively within the zero-IF RF transceiver module input dynamic range. In the secondary AGC loop, the high-threshold (up_a) corresponds to the maximum value which (B-υ) quantisation bits can represent and the low-threshold (low_b) corresponds to the maximum value which σ quantisation bits can represent. Here, σ is the number of LSBs, B is the ADC's number of quantisation levels and υ is the number of MSBs.

TABLE 1. Signal level vs. gain control word in FSS-AGC.

Stage	Num	Measured power range	Gain control word
Primary AGC	1	larger than up_a	RF_ATT_1
	0	$low_a \sim up_a$	RF_Gain_0
	-1	$(10^{-1.05})\cdot low_a \sim low_a$	RF_Gain_1
	-2	smaller than $(10^{-1.05})\cdot low_a$	RF_Gain_2
Secondary AGC	7	larger than $(10^{3})\cdot up_b$	ATT_31~ATT_35
	6	$(10^{2.5})\cdot up_b \sim (10^{3})\cdot up_b$	ATT_26~ATT_30
	5	$(10^{2})\cdot up_b \sim (10^{2.5})\cdot up_b$	ATT_21~ATT_25
	4	$(10^{1.5})\cdot up_b \sim (10^{2})\cdot up_b$	ATT_16~ATT_20
	3	$(10^{1})\cdot up_b \sim (10^{1.5})\cdot up_b$	ATT_11~ATT_15
	2	$(10^{0.5})\cdot up_b \sim (10^{1})\cdot up_b$	ATT_6~ATT_10
	1	$up_b \sim (10^{0.5})\cdot up_b$	ATT_1~ATT_5
	0	$low_b \sim up_b$	Gain_0
	-1	$(10^{-0.5})\cdot low_b \sim low_b$	Gain_1~Gain_5
	-2	$(10^{-1})\cdot low_b \sim (10^{-0.5})\cdot low_b$	Gain_6~Gain_10
	-3	$(10^{-1.5})\cdot low_b \sim (10^{-1})\cdot low_b$	Gain_11~Gain_15
	-4	$(10^{-2})\cdot low_b \sim (10^{-1.5})\cdot low_b$	Gain_16~Gain_20
	-5	$(10^{-2.5})\cdot low_b \sim (10^{-2})\cdot low_b$	Gain_21~Gain_25
	-6	$(10^{-3})\cdot low_b \sim (10^{-2.5})\cdot low_b$	Gain_26~Gain_30
	-7	smaller than $(10^{-3})\cdot low_b$	Gain_31~Gain_35

What's more, unlike the conventional single threshold comparison, the algorithm uses a multi-threshold based comparison mechanism which reduces the number of gain adjustments. As Table 1 shows, in the primary AGC loop, the measured signal value range smaller than the low-threshold (low_a)

has been grouped into 2 levels. In the secondary AGC loop, the measured signal value range smaller than low_b has been grouped into 7 levels, and the measured signal value range higher than up_b has been grouped into 7 levels. Under a single threshold condition, for example, when $up_b \leq m^2(n) \leq 10^{0.5} \cdot up_b$, the gain adjustment process continues till the determination condition is not satisfied.

C. GAIN COEFFICIENT CONTROL MODULE

The value of the gain adjustment has a positive correlation with the logarithm of the signal strength error between the reference value (γ) and the measured signal power ($m(n)$), which can be written as below:

$$G(n+1) - G(0) = 10\mu(\lg(\gamma^2/m^2(n))) \tag{3}$$

where the left side is the value of the gain adjustment in dB format, μ is a self-defined coefficient which determines the speed of gain control, and the right side represents the ratio between the reference value and the measured signal power in dB format. Therefore, the updated gain value is calculated by the comparison result. In the secondary AGC control loop, when $\mu = 1$, $up_b = (10^1) \cdot \gamma^2$, we can get

$$G(n+1) - G(0) = -10 \lg 10 = -10dB \tag{4}$$

So when $m^2(n) \geq up_b$, the gain value of the system should be cut down by at least 10dB. The calculation method is the same when $m^2(n) \leq low_b$.

Furthermore, in a single threshold condition in the secondary AGC loop, for example, when $(10^{-0.5}) \cdot low_b < m^2(n) < low_b$, the gain is adjusted up to 5 times in order to keep the output signal power stable, requiring 5 gain control words to adjust the gain value of the digital amplifier module. Similarly, under a single threshold condition in the primary AGC loop, the gain of the RF frontend is adjusted by the gain coefficient control module only once. This method greatly reduces the settling time of the AGC in different power ranges of the input signal. The algorithm adopts the strategy of starting the primary AGC before the secondary AGC. Only when the control value of the primary AGC reaches the limit does the secondary AGC work. Therefore, we can determine that the maximum settling time of the two-stage AGC can be calculated in an ideal condition as

$$\begin{aligned} T_S &= T_{Sa} + T_{Sb} \\ &= 1/f_s \times T_D \times 1 + 1/f_s \times T_D \times 5 \end{aligned} \tag{5}$$

where f_s is the system clock, T_{Sa} and T_{Sb} are the maximum settling time of the primary AGC and the secondary AGC respectively.

D. ERROR CONTROL MODULE

Unlike traditional AGC with only an amplifying module, in the novel AGC algorithm the adjustment gain values are controlled by both the gain coefficient control module and the error control module. The error control module can reset the gain factor by determining whether the signal is saturated or not, which can cope with the abrupt changes of signals very well. Both the I and Q components can flag the signal saturation. Taking the I component as an example, if the output samples whose absolute values are larger than a certain threshold (V_{max}), we flag the signal as saturated and then output a signal (*idle*) as "1". Otherwise, we output the *idle* as "0". When the *idle* is "1", the adjusted gain values will be set as the initial values. In this case, the gain coefficient control module does not work. When the *idle* is "0", the gain coefficient control module works normally.

TABLE 2. Characteristics of the RF Frontend Module.

Module	Device number	Gain (dB)	P1dB(dBm)	IP3(dBm)
LNA	MGA-684P8	17.6	22	32.4
ATT	PE4302	-31.5~0	34	52
FGA	TQP3M9028	14.5	20.7	40

E. GAIN ADJUSTMENT MODULE

The received baseband signal is first passed through the integrator module and then the control arithmetic module under the system clock (f_s). In the gain coefficient control module, the gain adjustment value can be calculated according to the measured signal power range by (3). In the RU, the uplink gain of the RF frontend is mainly from a serial digitally-controlled attenuator (ATT) and a two-stage amplifier which includes a low-noise amplifier (LNA) and a fixed gain amplifier (FGA). In order to minimize the noise figure (NF) of the whole link, the LNA is placed in the first stage. The gain, P1dB and output third order intercept point (IP3) of the RF frontend devices are shown in Table 2. The PE4302 is a high linearity ATT covering a 31.5dB attenuation range in 0.5dB steps. We set the initial attenuation value of the ATT as 21dB. Therefore, the total gain of the RF front-end link can be adjusted by dynamically adjusting the attenuation value of the ATT. Compared with using variable gain amplifier (VGA) of the same gain range, the design can withstand high RF power, which avoids link saturation or even damage of senstitive analog devices. In the primary AGC loop, the gain adjustment ranges from -10.5dB to 21dB with the minimum gain step of 10.5dB, and the dynamic range can be increased by more than 30dB. In the digital gain amplifier module, in order to realize the function of gain adjustment function, the received baseband signal is multiplied by a gain coefficient, and then the multiplied signal is shifted according to the gain.

F. TWO-STAGE AGC

In the FSS-AGC algorithm, the primary AGC can not only realize a coarse gain adjustment of the RF frontend to enlarge the system dynamic range, but also avoid the saturation and hence damage to the zero-IF RF transceiver module. Besides, it improves the measurement range of the integrator module as well as the sensitivity of the AGC algorithm by adjusting the signal strength of the RF frontend. After the

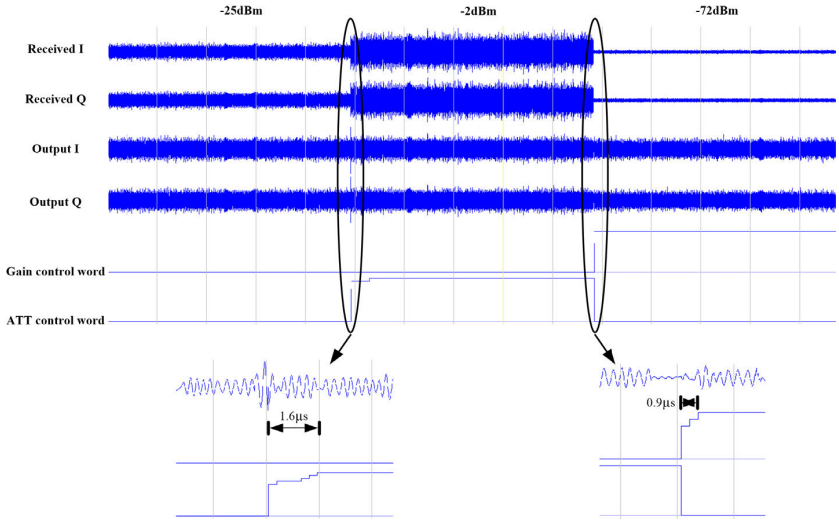


FIGURE 3. Simulation results of the FSS-AGC algorithm.

gain adjustment of the secondary AGC which is connected in series with the primary AGC, the system maintains the output baseband signal within a proper range, which makes it possible to do further data compression without degrading the input dynamic range performance.

Several key parameters, such as T_D, K and α, affect the response time and the stability of the system. In order to make the algorithm more flexible, the parameters can be changed to configurable registers. The proposed AGC circuits can be easily used for other wireless systems when the values of the registers are modified. Table 3 lists the parameters and descriptions of the FSS-AGC.

TABLE 3. FSS-AGC control parameter description.

Parameter	Description
f_s	System clock
K	coefficient of integrator module
T_D	control period
α	decision factor
V_{max}	threshold of saturation
γ	reference value
μ	self-defined parameter
σ	number of LSBs
B	quantisation bits of ADC
υ	number of MSBs
low_a	low-threshold of the primary AGC
up_a	high-threshold of the primary AGC
low_b	low-threshold of the secondary AGC
up_b	high-threshold of the secondary AGC

IV. HDL SIMULATION AND EXPERIMENTAL RESULTS

A. HDL SIMULATION RESULTS BASED ON FSS-AGC ALGORITHM

The improved FSS-AGC algorithm was implemented using Verilog HDL and simulated on the Xilinx Vivado 17 software where the loop timing response was analysed and verified. By taking a series of digitised LTE baseband signals with different power settings as input, the resultant waveforms can be analysed and displayed by Vivado integrated logic analyser (ILA) tool, as shown in Fig. 3. Considering the simulation speed and accuracy, we set the sample data depth of the ILA as 2^14 (16384) samples for each input. Based on the input dynamic range of the system, we concatenate 3 power levels ($-$2dBm, $-$25dBm and $-$72dBm) together to generate 49152 samples in total as displayed in the first two rows in Fig. 3. After the AGC is applied, the simulation results are shown in the following two rows labelled as output I and Q while the dynamic gain (Gain) and the attenuation adjustment values (ATT) are shown in the fifth and sixth rows respectively. As shown in Fig. 3, we can see that the proposed FSS-AGC algorithm can effectively adjust the gains of the system and keep the output signal power at a desired level in 1.6μs for the rising edge and 0.9μs for the falling edge as well as maintain the stability of the output signal at the same time. From the formula (3), we can see that the theoretical value of the loop settling time should be no more than 2μs. The simulation results are in agreement with the theoretical values, and the improved FSS-AGC algorithm has a fast reaction with a high stability at a sudden change of the input signals.

The implementation of the scheme is based on the XC7K325T type FPGA of the Kintex 7 series produced by Xilinx. The proposed FSS-AGC scheme implements digital gain adjustment by the bit shifting operation which does not require such complicated mathematical functions. Multiple modules are shared by the primary AGC and the secondary AGC, so the FSS-AGC does not increase resource utilization and implementation complexity compared with the single stage AGC. In our experiment, our AGC portion consumes 130 Adaptive Look-Up Tables (ALUT) and 102 Registers of hardware resource. It should be noted that the design in this paper is a high accurate control. If the requirement on accuracy is reduced, the number of control words will be

TABLE 4. Resampling compression parameters of each service.

Service number	Service standard	MNO	Uplink frequency band (MHz)	Bandwidth (MHz)	Sampling rate(Mbit/s)	Notes
1	GSM 900	China Mobile/ China Unicom	889-915	26	30.72	-
2	GSM 1800	China Mobile	1710-1735	25	25.6	LTE MIMO supported
3	TD-LTE (E)	China Mobile	2320-2370	50	51.2	LTE MIMO supported
4	GSM1800/LTE FDD 1.8G	China Unicom	1735-1765	30	30.72	LTE MIMO supported
5	WCDMA 2100	China Unicom	1940-1980	40	51.2	LTE MIMO supported
6	CDMA 800	China Telecom	820-835	15	15.36	-
7	LTE FDD 2.1G	China Telecom	1920-1940	20	25.6	-
8	LTE FDD 1.8G	China Telecom	1765-1785	20	25.6	LTE MIMO supported
9	IMT-2020 3.5G	China Telecom	3400-3500	20	25.6	
Total				411	465.92	

reduced and the use of hardware resources can be greatly reduced.

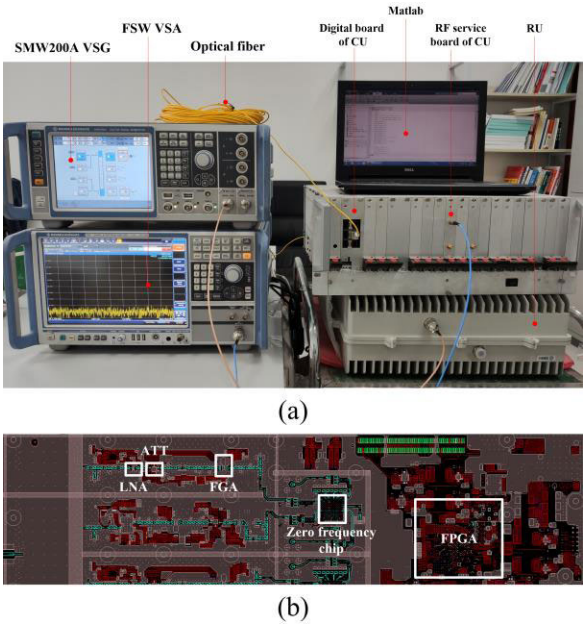


FIGURE 4. (a) FSS-AGC loop experimental setup (b) photograph of the specific PCB of the RU uplink.

B. EXPERIMENTAL RESULTS ON DROF SYSTEM

In order to verify the performance of the proposed FSS-AGC algorithm, the design is integrated into DRoF based DDAS which supports 14 RF services for indoor wireless coverage. The hardware board of the system has been designed and the measurement setup is shown in Fig. 4 (a). In the RU, an Analog Devices (ADI) AD9371 zero-IF RF transceiver module is used as upconverter and downconverter. A Xilinx Kintex 7 XC7K325T FPGA is used to process real-time digital signal including the data compression, the secondary AGC and packetization in the system. We use a Rhode and Schwarz (R&S) SMW200A vector signal generator (VSG) to generate the input signal, meanwhile the output is measured using the R&S FSW vector signal analysis (VSA). As shown in Table 4, 14 inputs of 9 cellular services from

TABLE 5. FSS-AGC control parameter description and configuration.

Parameter	Description	Value
f_s	System clock	153.6MHz
K	coefficient of integrator module	13107
T_D	control period	50
α	decision factor	36
V_{max}	threshold of saturation	5000
γ	reference value	160
μ	self-defined parameter	1
σ	number of LSBs	8
B	quantisation bits of ADC	16
υ	number of MSBs	0
low_a	low-threshold of the primary AGC	14
up_a	high-threshold of the primary AGC	1000
low_b	low-threshold of the secondary AGC	4
up_b	high-threshold of the secondary AGC	1000

the three Chinese MNOs are supported. The line transfer rate of the system without any signal processing is up to 34.4Gbps (= 14 × 16bit ×153.6M). We set the sampling rate compression parameters as shown in Table 4 and the quantisation compression parameters as follows, $\sigma = 0$, $\upsilon = 8$. The sampling rate has been down sampled by five times and quantisation bit is compressed by 2 times. The transmission data rate of the system is compressed to 7.4Gbps (=465.92M×8bit×2). Meanwhile, the RF frontend of each channel uses a single PE4302. As described in the section 3, based on statistics and analysis of the control procedure, the selected parameters of the FSS-AGC algorithm are listed in Table 5. The control words and the corresponding gain adjustment values are shown in Table 6. The FSS-AGC algorithm can be performed in both downlink and uplink of a low bit rate transmission system. Meanwhile, the uplink of the system requires a larger dynamic range due to the unknown input power. In this section, as FDD uplink signal is encoded by the LTE QPSK modulation scheme with large PAR, to demonstrate the algorithm performance in the worst case, an experimental test is carried out based on FDD uplink signal. Fig. 4 (b) shows a photograph of the specific

TABLE 6. FSS-AGC control words and corresponding gain adjustment values.

Control word	Gain adjustment value（dB）	Control word	Gain adjustment value（dB）	Control word	Gain adjustment value（dB）	Control word	Gain adjustment value（dB）
RF_ATT_1	-31.5	Gain_20	20	Gain_1	1	ATT_18	-18
RF_Gain_0	-21	Gain_19	19	Gain_0	0	ATT_19	-19
RF_Gain_1	-10.5	Gain_18	18	ATT_1	-1	ATT_20	-20
RF_Gain_2	0	Gain_17	17	ATT_2	-2	ATT_21	-21
Gain_35	35	Gain_16	16	ATT_3	-3	ATT_22	-22
Gain_34	34	Gain_15	15	ATT_4	-4	ATT_23	-23
Gain_33	33	Gain_14	14	ATT_5	-5	ATT_24	-24
Gain_32	32	Gain_13	13	ATT_6	-6	ATT_25	-25
Gain_31	31	Gain_12	12	ATT_7	-7	ATT_26	-26
Gain_30	30	Gain_11	11	ATT_8	-8	ATT_27	-27
Gain_29	29	Gain_10	10	ATT_9	-9	ATT_28	-28
Gain_28	28	Gain_9	9	ATT_10	-10	ATT_29	-29
Gain_27	27	Gain_8	8	ATT_11	-11	ATT_30	-30
Gain_26	26	Gain_7	7	ATT_12	-12	ATT_31	-31
Gain_25	25	Gain_6	6	ATT_13	-13	ATT_32	-32
Gain_24	24	Gain_5	5	ATT_14	-14	ATT_33	-33
Gain_23	23	Gain_4	4	ATT_15	-15	ATT_34	-34
Gain_22	22	Gain_3	3	ATT_16	-16	ATT_35	-35
Gain_21	21	Gain_2	2	ATT_17	-17		

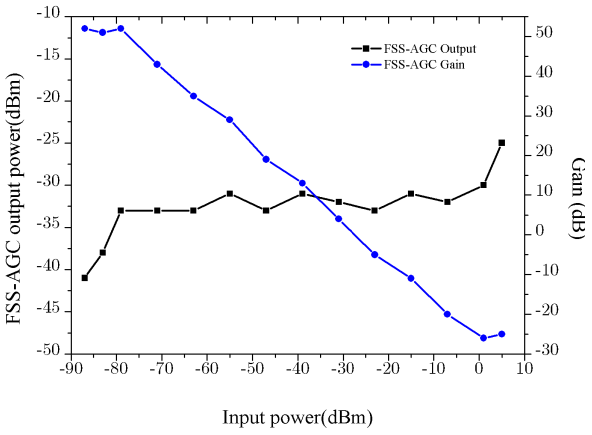


FIGURE 5. Measured output power and Gain vs. input power of FSS-AGC system.

printed circuit board (PCB) of the RU uplink which performs the AGC progress.

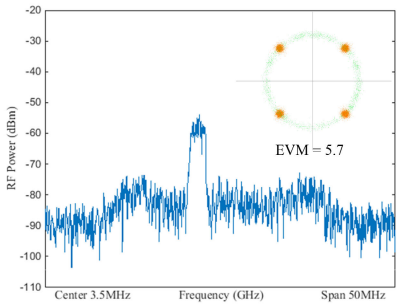
The measured FSS-AGC output power and the gain adjustment value results for the FDD 1800 uplink channel in the low bit rate DDAS system are shown in Fig. 5. With the introduction of FSS-AGC, the uplink performance of the system has been significantly improved. We can see that the FSS-AGC algorithm can track changes when the input power ranges from −72 to 2dBm. Beyond this range, the AGC cannot track any more and the system output follows its input in linear dB by dB behaviour.

In order to verify the improvement of signal transmission performance by FSS-AGC in the system, the received uplink signal centred at 3.5GHz of the IMT-2020 3.5G channel in the CU is measured. The recovered RF spectra and screenshot of the constellation plot when the input signal power at RU is set as −45dBm are shown in Fig. 6. It can be observed that the FSS-AGC will enhance the amplitude of the received LTE signal with the RF spectrum looking more clearly. Meanwhile, the constellation plot of the received signal after the gain adjustment by FSS-AGC was good which proves that the signal transmission quality has improved a lot if the FSS-AGC is introduced in the system.

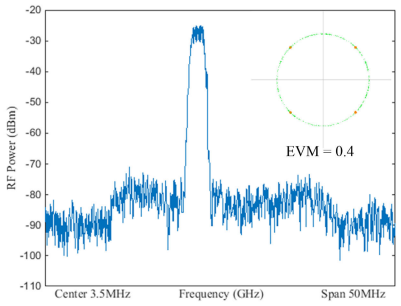
The EVM results of the FSS-AGC uplink system are shown in Fig. 7. For comparison, the corresponding results of the conventional low bit rate DDAS system without AGC and the improved case with a single-stage AGC (the primary AGC) after data compression are also included in Fig. 7. The output EVM for the LTE signal of the FSS-AGC low bit rate system is well below 5% which is specified by the 3rd generation partnership project (3GPP) for the input power range from −76 to −2dBm, corresponding to a dynamic range of 74 dB. Compared with the conventional DRoF link, the dynamic range has been improved by the FSS-AGC algorithm from less than 34dB to 74dB, an increase of 40dB without degrading the signal waveform quality. Besides, compared with that of the DRoF link with a single-stage AGC, the dynamic range of the FSS-AGC system has also been improved by 10dB. What's more, the EVM performance of the system with the FSS-AGC is a lot better than that of the system with the single-stage AGC, implying that the signal transmitted through the low bit rate DRoF link with FSS-AGC can distort less.

TABLE 7. Performance comparison and summary.

Index	[17]	[18]	[19]	[20]	[25]	[26]	This work
Gain range (dB)	23	-	84	20	-	22	40
Gain step (dB)	-	-	3	-	2	2	0.5
Settling time (μs)	-	500	8	-	16-32	<2.4	1.6
Gain control	Analogue	Digital	Analogue	Digital	Digital	Analogue	Digital
Type	Feed-forward	Feed-backward	Feed-backward	Feed-forward	Feed-backward	Feed-forward	Feed-backward



(a)



(b)

FIGURE 6. Recovered RF spectrum and constellation plot at the receiver-side. Conventional DRoF (b) DRoF with FSS-AGC.

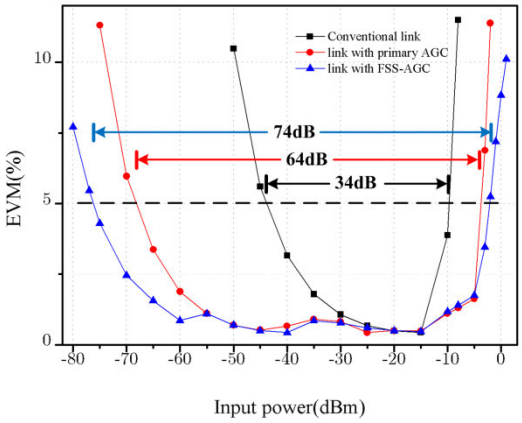


FIGURE 7. EVM performance for the FSS-AGC uplink system.

The performance of the presented AGC is summarized in Table 7, along with a comparison with other AGC loops. This work achieves a faster gain adjustment response, higher gain accuracy and wider gain adjustment range owing to the adoption of two-stage AGC architecture and multi-threshold comparing method.

V. CONCLUSION

In this paper, a novel two-stage FSS-AGC algorithm is proposed and demonstrated for the first time. It is able to make the most of quantisation bits while achieving fast timing response and maintaining great stability so that a highly efficient data compression algorithm can be introduced. Simulated results show that by adopting an effective periodic multi-threshold judgement method, the FSS-AGC algorithm can achieve an accurate stable gain adjustment with a fast timing response (with a short response time of less than $2\mu s$). An experiment is conducted to test the performance of the algorithm in low bit rate DRoF based DDAS. According to the experimental results, the two-stage AGC can improve the dynamic range of the low bit rate DRoF system by 40dB with a low distortion in steady state. This architecture can be well suited for a range of next generation wireless applications with stringent time requirements.

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WEN LI received the master's degree in electronic science and technology from Beihang University, Beijing, China, in 2014, where he is currently pursuing the Ph.D. degree in electronic science and technology.

Since 2014, he has been a Wireless Communication Engineer with the Beijing Institute of Aerospace Control Devices (BIACD), Beijing. He went to the University of Cambridge as a Visiting Scholar, in 2017 and 2018. His research interests include signal processing for wireless systems, multicarrier communications, and information theory.

AIXIN CHEN (Member, IEEE) received the Ph.D. degree in electromagnetic field and microwave technology from the University of Electronic Science and Technology of China, Chengdu, China, in 1999. From 2000 to 2002, he was a Postdoctoral Fellow with the School of Electronic Information and Engineering, Beihang University, Beijing, China, where he is currently a Professor. His research interests include antennas and electromagnetic compatibility.

XUEFENG WANG received the bachelor's degree from Wuhan University, Wuhan, China, in 1997, and the Ph.D. degree from the Chinese Academy of Sciences, Shanghai, China, in 2002. He has published more than 50 articles. He is currently the Director of the Beijing Institute of Aerospace Control Device. His research interests include fiber optics and optoelectronic sensors. He received the National Award, in 2010.

TONGYUN LI (Member, IEEE) received the B.Eng. degree in electronics and computer engineering from the University of Aberdeen, in 2007, and the Ph.D. degree in engineering from the University of Cambridge, in 2012.

He is currently a Research Associate with the Centre for Photonic Systems, Engineering Department, University of Cambridge. His research interests mainly include digital radio over fibre, in-building wireless systems, and next-generation wireless fronthaul systems.

RICHARD V. PENTY (Senior Member, IEEE) received the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1989.

He was a Science and Engineering Research Council Information Technology Fellow with the University of Cambridge, where he is currently Professor of photonics. He has held academic posts at the University of Bath, Bath, U.K., and the University of Bristol, Bristol, U.K. He is the author or a coauthor of more than 900 publications. He is a co-founder of Zinwave, PervasID, and eComm. His current research interests include high-speed optical communications systems, optical data communications, photonic integrated circuits, and radio over fibre. He is a Fellow of the Royal Academy of Engineering.

XIAOBIN LIU received the master's degree in control theory and control engineering from the Beijing Institute of Technology, Beijing, China, in 2006. Since 2006, he has been a Wireless Communication Engineer with the Beijing Institute of Aerospace Control Devices (BIACD), Beijing. He is currently the Director of the Communication System Division, Beijing Institute of Aerospace Control Device. His research interests include satellite communications and network of computer.