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Capacitance Multiplier Using Small Values of Multiplication Factors for Adjustability Extension and Parasitic Resistance Cancellation Technique

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ABSTRACT This paper presents a new concept of a capacitance multiplier using the topology of differential voltage buffer and current conveyor, where the capacitor is connected to the current input terminal. The presented topology overcomes the typical issue known from similar solutions, i.e. creation of an undesired lossy character of the impedance plot. The added feedback path in the structure serves for minimization of the serial parasitic resistance of the current input terminal as well as the output resistance of differential voltage buffer. The electronic driving of the current and voltage internal gains of the active elements allows the adjustment of the capacitance multiplication factor as well as readjustment of the overall capacitance structure between the lossy and lossless modes of operation. The adjustment of the multiplication factor intentionally targets low ranges of gains. Despite that the multiplication factor equals or is less than 1, the range of adjustability is very wide. Simple modifications of the proposed concept leading to the differential-mode operation and enhancement of the multiplication factor are shown and explored. They were experimentally tested in more than 2 decades, from 0.03 to 5.8 nF, and controlled by single DC voltage from 0.1 to 1.0 V. The outputs of experimental measurements meet with the PSpice simulations and confirm the design validity.

INDEX TERMS Adjustability, capacitance multiplication, current conveyor, current gain, differential voltage buffer, electronic tuning, multiplication factor adjustment, voltage gain.

I. INTRODUCTION

Electronically adjustable and tunable circuit applications are receiving a lot of attention in the fields of signal generation and signal processing. The adjustment of parameters of applications can be implemented especially by the utilization of various active elements (AEs) and devices with electronically adjustable internal parameters or inter-terminal transfers [1], [2]. Capacitance multipliers [2] are useful tools especially when the design requires a very high capacity values, but the used fabrication process or other reasons allow to achieve only a very small value of the physical capacitance (typically units or tens of pF due to the space limitations). Such a high value of capacity is obtained as a product of a small value of capacity and a quite large constant [3] (in principle based on the gains of the active circuitry). This constant is known as the multiplication (or multiplying) factor (MF). In some cases, its value can be intentionally varied thanks to active control (driving voltage or current influencing the final value) or, in simpler cases, passive way of tuning (implemented by a resistor value, for instance). The existing and widely applied principles of tuning target the increasing (boosted) value of MF. The upper limits of MF are given by the gain limits of the active circuitry (voltage gain, current gain, product of transconductance and resistance, or even joint impact of several types of gains). However, very high values of gain in the circuitry lead to issues with limitation of dynamics, nonlinear dependencies

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of gains on driving parameters, nonlinearities of the transfer responses (a necessity to process very low signal levels) as well as increased power consumption.

We have studied the features of recently reported solutions (see comparison in Table 1 where works [3]–[30] have been compared in detail). In accordance with some of these works, the MF (having a fixed value) should be as high as possible in ideal case. The following conclusions were established from the analysis of the works included in Table 1:

a) Existing solutions allow achieving very high ranges and values of MF, which obviously require very large ranges of driving parameters (bias currents, etc.) – [3], [4], [6], [9], [11]. Table 1 indicates this value as the capacity ratio – a case when equivalent capacity is tuned between maximal and minimal values. High values of gains lead to processing of very low signal levels [6], [11].
b) Despite of a wide change of capacity, the efficiency of adjustment is not high – [4], [6], [11].
c) In some circuits [5], [7], [9], [14], [17], [21], [24], [25], the number of needed passive elements is high.
d) In some cases [4], [8], [18], without any additional advantage, the number of active devices is also high. As described later, our concept uses additional active devices to obtain increased effectiveness of the adjustment.
e) The problem of serial small-signal parasitic resistances connected to the working floating capacitor is not solved in previous works [3], [5], [12]–[14], [19], [22], [23], [26]–[28], [30].
f) Electronic reconfiguration between lossy (having intentional zero of impedance frequency response) and lossless modes of operation is not possible in case of previous solutions.
g) Additional extension of the adjustability range of capacity is possible only in cases of active solutions with multiparameter adjustability (see [6]). Single parameter adjustable capacity multipliers [3]–[5], [9], [29] reach a large range of values of capacity only by very wide-range control of the used driving force.
h) All the reviewed solutions use an increasing value of gain (gain $\geq$ 1) to boost the MF. Our solution operates with attenuation and without boosting of MF (the maximal current gain is 1 – multiplication factor $\leq$ 1). By this method, electronic tunability is preserved as well as further features (discussed below), which can be useful in specific cases of applications. Small attenuation of the useful signal is typically more convenient for proper signal processing than its amplification.

Our work introduces different approaches to adjust the value of MF that does not exceed the value 1. Increasing the value of the capacity by MF is not the only possible way when tunable and adjustable application of the ''boosted'' capacitor is expected. Other possibility is presented in this paper. The results show that it is also very effective for tunable applications from the view of a wide range of adjustment of the value of the equivalent (multiplied) capacity but the gain(s) in the circuitry stay reasonable and low.

Different kinds of known solutions are based on a grounded capacitor (the multiplier boosts the capacity of the grounded element) [4], [6]–[11], [15]–[18], [20], [21], [24], [25], [29]. However, the number of topologies using a floating capacitor is also significant [3], [5], [12]–[14], [19], [22], [23], [26]–[28], [30]. Especially, the latest works are targeting this way of the design. However, such solutions are not welcomed by some designers because of possible additional issues with overall impedance regarding small-signal parasitic influences of active parts. Nevertheless, as it will be shown, disadvantages occurring in such cases, where a floating capacitor is used, are not always significant. The parasitic behavior (parasitic zero of frequency response) can be easily removed when suitable circuitry is utilized. We can summarize most important benefits of the newly presented approach to the following points:

1) Electronic adjustment of the MF influencing the value of the equivalent capacity,
2) Low current gain control (attenuation actually) used for electronic adjustment (causing negligible increase of the power consumption),
3) A wide range of adjustability and tunability for low gain ranges,
4) Eliminated parasitic effects of structures using a floating capacitor,
5) A simple electronic elimination of the lossy part (zero frequency) of the frequency response in the impedance plot by adjustment of another electronically controllable parameter,
6) Possible implementation of the floating capacitance multiplier, when additional terminals of AEs are added,
7) A simple option to extend the topology by additional elements of the same type in order to obtain even more extended range of electronic tuning of the equivalent capacity.

Compared to our work, the most similar results were obtained in [13] (similar ratios of adjustment efficiency and varied capacity). The circuit in [13] uses even a smaller number of AEs than our proposal (basic concept) and combines driving of two parameters (transconductance and current gain) in order to adjust the capacity. However, the applied range of the current gain is enormous (0.7-19) and the problem of serial parasitic resistances is not solved. The solution in [13] cannot be used in a differential mode and the value of MF is not lower than 1.

This paper has the following organization: Section 1 deals with recent solutions of capacitance multipliers, their features and gives suggestions to achieve the objectives of the presented research. The proposed concept is also compared with previous works in detail. Section 2 introduces the basic core of the presented capacitance multiplier. Sections 3 to 6 focus

TABLE 1. Comparison of relevant works introducing adjustable capacitance multipliers.

Reference	Number of passive; Active devices; Testing**	Based on topology with floating C	Serial connection of C to low-impedance terminal / input terminal (influence of serial resistance in CC for example)	Electronic adjustment / Reconfiguration between lossy and lossless mode	Type of adjustment (controlled value of)	Provided replacement of R by MOS for tuning	Compensation of serial parasitic resistance of current input terminal	Possibility of differential-mode operation	Multiplication factor adjustable electronically / Extended adjustability	Multiplication factor adjusted by attenuation (no amplification)	The largest reported range of C adjustment (range of the driving force)	Capacity ratio C_{max}/C_{min}	Ratio of adjustment efficiency (C_{max}/C_{min}):(driving$_{max}$/driving$_{min}$)
[3]	1; 3; m	Yes	Yes/No	Yes/No	A1 (g_m)	N/A	No	No	Yes/No	No	20 pF → 100 nF (1μA → 1000 μA)	5000	5
[4]	0-2; 4; s	No	No/No	Yes/No	A1 (R_X)	N/A	N/A	Yes	Yes/No	No	60 pF → 20 nF (1 μA → 1000 μA)	333	0.3
[5]	3; (1-2); m	Yes	Yes/No	No/No	A3 (R)	Yes	No	No	No/No	No	100 pF → 400 pF (gain factor R_2/R_1 0.1 → 1)	4	0.1
[6]	1; 4; s	No	No/No	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes*	No	103 pF → 9.55 μF (gain 1 → 1000)	$93{\cdot}10^3$	0.93
[7]	3; 3; s	No	No/No	No/No	A3 (R)	Yes	N/A	Yes	Yes/No	No	N/A	N/A	N/A
[8]	1; 4; s	No	Yes/Yes	Yes/No	A1 (R_X)	N/A	No	Yes	Yes/Yes	No	N/A	N/A	N/A
[9]	(5-7); (2-3); s	No	No/No	No/No	A3 (R)	No	N/A	Yes	No/No	No	10 nF → 4 μF (250 Ω → 100 kΩ)	400	1
[10]	1; 3; s	No	Yes/Yes	Yes/No	A1 (R_X)	N/A	No	Yes	Yes/Yes	No	N/A	N/A	N/A
[11]	1;2; s	No	No/No	Yes/No	A1 (R_X, g_m)	N/A	N/A	No	Yes/Yes	No	950 pF → 96 μF 10 nF → 1.03 mF (gain 1 → 100 000)	$101{\cdot}10^3$ $103{\cdot}10^3$	1.03
[12]	(1-2); (2-3); s	Yes	No/No	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes	No	N/A	N/A	N/A
[13]	2; 1; s	Yes	Yes/Yes	Yes/No	A2 (g_m, C gain)	N/A	No	No	Yes/Yes	No	190 pF → 31 nF (C gain 0.7 → 19)	163	6
[14]	3; 2; s	Yes	Yes/Yes	No/No	N/A	N/A	No	Yes	Yes/No	No	N/A	N/A	N/A
[15], [16]	1; 3; s	No	No/No	Yes/No	A1 (R_X)	N/A	N/A	Yes	Yes/Yes	No	N/A	N/A	N/A
[17]	3; 2; s	No	No/No	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes	No	N/A	N/A	N/A
[18]	1; 4; s	No	No/No	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes	No	N/A	N/A	N/A
[19]	1; 1; s	Yes	No/No	Yes/No	3 (R)	Yes	N/A	No	Yes/Yes	No	200 pF → 4.7 nF (gain factor R_2/R_1 1 → 50)	24	0.5
[20]	2; 1; s	No	No/No	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes	No	43 pF → 430 pF (0.2 mS → 1 mS)	10	2
[21]	3; 2; s	No	No/ possible	Yes/No	A1 (g_m)	N/A	N/A	Yes	Yes/Yes	No	N/A	N/A	N/A
[22]	2; 1; s	Yes	Yes/No	Yes/No	A1 (g_m)	N/A	No	No	Yes/Yes	No	0.5 nF → 10 nF (0.4 mS → 10 mS	20	0.8
[23]	2; 1; s	Yes	Yes/No	Yes/No	A1 (g_m)	Yes	No	No	Yes/Yes	No	0.22 nF → 0.72 nF (0.14 mS → 0.5 mS; 0.84 k → 5.24 k)	3.3	2
[24]	3; 1; s	No	No/No	Yes/No	A3 (R)	Yes	N/A	No	Yes/Yes	No	20 pF → 160 pF (gain factor R_2/R_1 1 → 16)	8	0.5
[25]	3; 2; s	No	Yes/Yes	No/No	A3 (R)	Yes	No	Yes	Yes/No	No	100 pF → 2 nF (gain factor 2 → 40)	20	1
[26]	2; 1; s	Yes	Yes/No	Yes/No	A1 (g_m)	N/A	No	Yes	Yes/Yes	No	0.3 nF → 1.6 nF (0.4 mS → 3 mS)	5.3	0.7
[27]	1; 5; s	Yes	Yes/Yes	Yes/No	A1 (g_m)	N/A	No	Yes	Yes/Yes	No	0.18 nF → 9.9 nF (gain factor 1 → 60)	55	0.92
[28]	2; 2; s	Yes	Yes/Yes	Yes/No	A1 (g_m)	N/A	No	Yes	Yes/Yes	No	N/A	N/A	N/A
[29]	2; 2; b	No	Yes/Yes	Yes/ Yes	A1 (g_m)	No	N/A	No	Yes/Yes	No	100 F → 4 mF (50 μA → 2000 μA)	40	1
[30]	(2-3); 1;m	Yes	Yes/Yes	No/No	A3 (R)	No	N/A	Yes	Yes/No	No	N/A	N/A	N/A
The proposed topologies													
Figs. 2-4	1; (2-3); b	Yes	Yes/Yes	Yes/ Yes	A2 (C and V gain)	N/A	Yes	Yes	Yes/No	Yes	1.0 nF → 9.3 nF (0.1 → 1)	9.3	0.93
Fig. 5	1; 4; b	Yes	Yes/Yes	Yes/No	A2 (C gain)	N/A	Yes	Yes	Yes/Yes	Yes	0.03 nF → 5.8 nF (0.1 → 1)	193	19.3

Notes: * four bias sources – multiplied gains; **test: s – simulated; m – measured; b – both; A1 – bias currents (driving of transconductance g_m or input resistance R_X); A2 – driving voltage (voltage or current gain); A3 – passive adjustment (resistor value); C – Current; V – Voltage; N/A – not available

on the specific modifications showing how the core circuit can be improved and extended for various use cases including effects of small-signal parasitic influences. Section 7 provides a detailed analysis of the selected designed topologies in the PSpice simulation tool and also more importantly by real laboratory experiments in the bandwidth from 10 kHz up to 10 MHz. Section 8 concludes this work.

II. THE BASIC CORE OF THE PROPOSED CIRCUIT

The idea presented in [30] gives the initial motivation for this work, mainly from the viewpoint of parasitic elements connected in series with the serial capacitor used between the output of the differential input voltage amplifier and the differential output current amplifier (see Fig. 4 in [30]). The current conveyor (CC)-based capacitance multiplier can be synthesized by a connection of the frequency dependent impedance (capacitance or inductance) to the current input terminal [2], [30]. This input terminal has small-signal finite resistance (R_X) that influences the input impedance of the multiplier. Compared to the recent structures using CC of the second generation (CCII) [1] and an operational transconductance amplifier (OTA) [1], the proposed concept reduces the complexity of the design due to the implementation of a differential voltage buffer (DVB) known also as differential unity gain amplifier [1] performing simple voltage subtraction: $V_O = V_+ - V_-$. The basic structure of the proposed circuitry is shown in Fig. 1. Thanks to the advanced type of the CC (the so-called electronically controllable CCII with negative output, abbreviated as ECCII- [31]–[33]), we have the following inter-terminal relations: $V_X = V_Y$, $I_Y = 0$, $I_Z = -B \cdot I_X$, where the parameter B can be used to control the current gain. From the viewpoint of the connection of the terminal Y (ECCII-), there are two options (see Fig. 1). The circuit in Fig. 1a) has the following input impedance in ideal case:

$$Z_{in1}(s) = \frac{1}{sC_m} = \frac{1}{2} \cdot \frac{1}{sC_1B}. \tag{1}$$

The controllable gain (B) of the ECCII- element ($2B$ respectively) in the denominator is also referred to as capacitance MF [30] forming the new adjustable capacity C_m. When the real input resistance of the terminal X (R_X) is assumed, then the input impedance changes into a not so beneficial form (including parasitic zero):

$$Z'_{in1}(s) = \frac{1}{2} \cdot \left[\frac{1 + sC_1R_X}{sC_1B} \right]. \tag{2}$$

When the output resistance of DVB (R_o) is also considered, then the serial connection of both resistances slightly modifies the previous expression to:

$$Z''_{in1}(s) = \frac{1}{2} \cdot \left[\frac{1 + sC_1 (R_o + R_X)}{sC_1B} \right]. \tag{3}$$

Fortunately, the output resistance of the DVB is very low in operational frequency bands (tens-hundreds of mΩ below 1 MHz) [34] and its impact on (1) is not so significant in comparison to R_X. The input impedance of the topology in

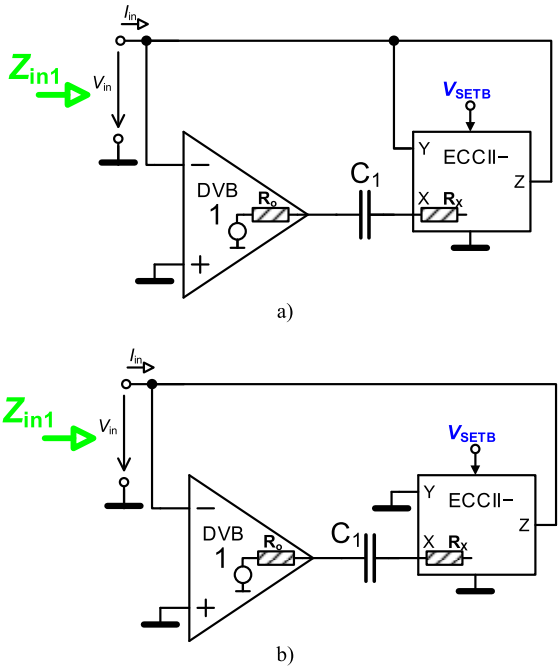

FIGURE 1. Initial (basic) core of the proposed circuit, i.e. capacitance multiplier using single DVB and ECCII elements: a) the Y terminal is used as a feedback, b) the Y terminal is grounded.

Fig. 1b), with the grounded Y terminal, is similar to (1), (2) and (3), only the constant 1/2 is replaced by 1. Therefore, the multiplication constant is given by the current gain B only. However, both topologies, shown in Fig. 1, have a lossy impedance character and the resistance R_X must be considered.

III. IMPROVED TOPOLOGY HAVING LOSSLESS CHARACTER

To achieve a significant improvement in the features of the previously presented topology, a feedback from the terminal X (ECCII-) to the positive input of the element DVB is applied. Thanks to this improvement, a lossless behavior is obtained. Two versions (used or unused/grounded Y terminal, similarly as in Fig. 1) of this concept are shown in Fig. 2. Both solutions have the same form for the input impedance, even in the non-ideal case including discussed parasitic influences (R_X, R_o). The expression for the ideal input impedance has the same form as in the case of the solution shown in Fig. 1b). However, the input resistance R_X has no influence on the non-ideal impedance (the impedance Z'_{in2} is identical to the ideal Z_{in2}). The resistance R_o (see Fig. 2 a) and b)) remains in impedance expression for both cases:

$$Z''_{in2}(s) = \frac{1 + sC_1R_o}{sC_1B}, \tag{4}$$

but for some active devices (with $R_o \ll 1\Omega$) its influence on the Z''_{in2} is negligible. Unfortunately, it is not valid in general (some opamps have the value of R_o in tens of Ω or even more). Therefore, it cannot be ignored in general case.

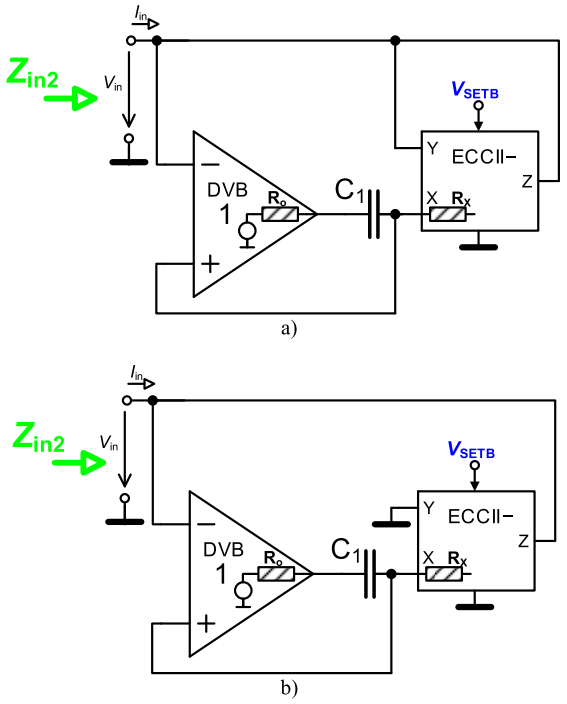

FIGURE 2. Improved topology of the capacitance multiplier using single DVB, ECCII and added feedback from X terminal of ECCII to positive terminal of DVB element in two variants: a) the Y terminal is used as a feedback, b) the Y terminal is grounded.

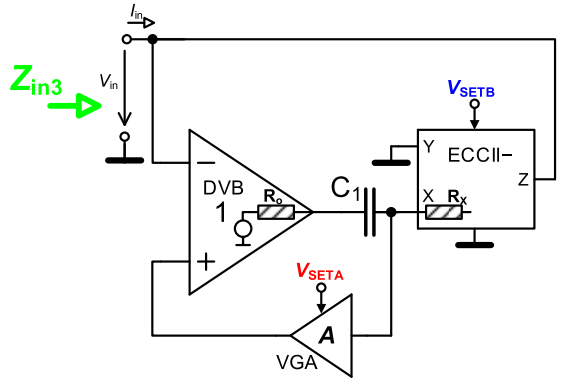

FIGURE 3. The capacitance multiplier using single DVB, ECCII and additional variable voltage gain amplifier (VGA) in feedback from X terminal of ECCII to positive terminal of DVB in order to eliminate possible impact of R_0.

IV. ELIMINATION OF THE IMPACT OF OUTPUT RESISTANCE (R_0)

Minimization or even elimination of the influence of the output resistance R_o is possible by adding of a VGA element to the feedback loop from the terminal X of the ECCII- to the positive (input) terminal of the DVB. Such a solution, shown in Fig. 3, is a modification of the structure presented in Fig. 2b) and has the following non-ideal input impedance:

$$Z''_{in3}(s) = \frac{1 + sC_1\,(R_o + R_X - A \cdot R_X)}{sC_1 B}. \tag{5}$$

The adjustable parameter A can be used for cancellation of the lossy part when $A = (R_o + R_X)/R_X$. Supposing $R_o = R_X$, just

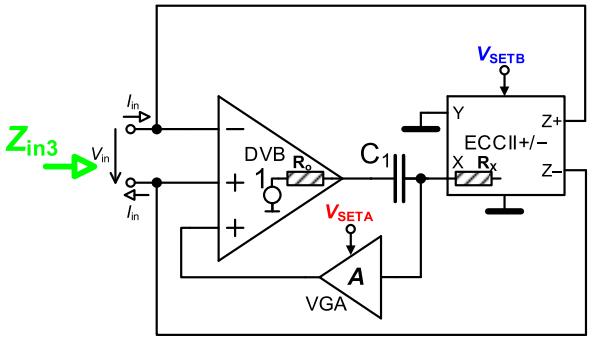

FIGURE 4. Capacitance multiplier from Fig. 3 extended to the differential-mode operation.

$A = 2$ is required. If $R_o \to 0\Omega$, as common in many cases, then the value of A equal to 1 is sufficient.

V. MODIFICATION FOR THE DIFFERENTIAL-MODE OPERATION

The previous topology (see Fig. 3) can be easily modified for differential or pseudo-differential operation [35], [36]. Additional output terminal of the ECCII device (both polarities of current output terminals) is required. In previous cases the DVB device had only two inputs. Fortunately, commercially available devices used for construction of DVB already include additional input terminals (see for example AD8130 [34] or AD830 [37]). These terminals are not frequently used in standard designs with DVB. Hence, the differential-mode operation is easily available without necessity of any additional active devices. The circuit in Fig. 3 was extended to the structure of a differential-mode capacitance multiplier as it is shown in Fig. 4. The input impedance has the form identical with (5).

VI. TUNABILITY EXTENSION OF THE PRESENTED STRUCTURES

Recent works [27], [28] introduced a boosted value of MF. This feature is also easily available in topologies presented above. The example of a tunability (minimal/maximal value of capacity) enhancement is shown in Fig. 5. In this particular case, the structure is analyzed without an additional VGA (added in section IV) because an insignificant effect of R_o is supposed. Note that only the last member of the chain, i.e. ECCII_n, should provide Z outputs of both polarities (Z±) in order to create a differential-mode capacitance multiplier as it was shown in the previous section. This configuration is not shown in this paper, however can also be easily obtained.

The non-ideal input impedance supposing $R_o \to 0\ \Omega$ has this form:

$$Z''_{in4}(s) = \frac{1}{sC_1 \prod_{i=1}^{n} B_i}. \tag{6}$$

Considering n ECCII devices, having identical (equal) gains B, in the loop, the MF theoretically achieves B^n. Resistances R_{X2} to R_{Xn} have no influence on the behavior of the

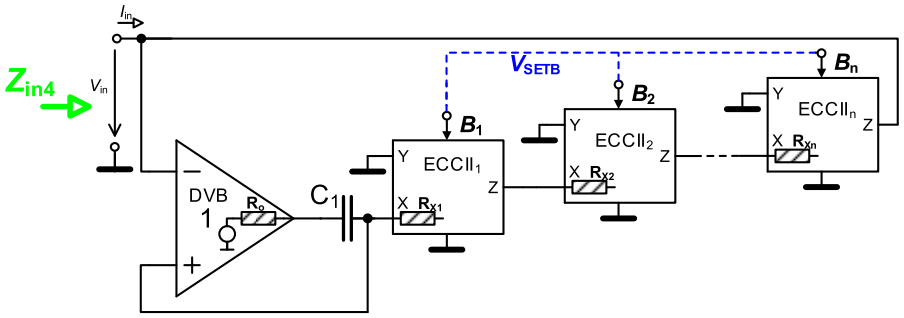

FIGURE 5. Extension of the topology of the presented capacitance multiplier (Fig. 2b) - enhanced multiplication constant (tunability).

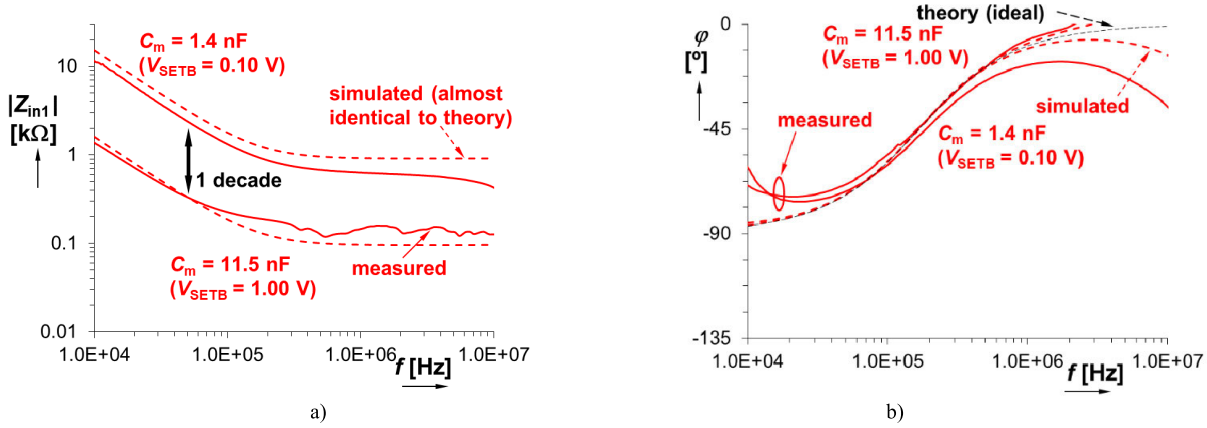

FIGURE 6. Comparison of measured and simulated impedance of capacitance multiplier using single DVB and ECCII from Fig. 1b: a) magnitude responses, b) phase responses.

circuit because the output of one device supplies the current sink of the following device (from the high-impedance current source to the low-impedance current input terminal). Note that the ECCII devices can be replaced by current amplifiers (the Y terminal is grounded in all cases in Fig. 5). A comprehensive comparison of impedances of the presented solutions from Fig. 1 to Fig. 5 is given in Table 2.

VII. EXPERIMENTAL VERIFICATION OF THE PRESENTED CONCEPTS

Features of several examples of solutions presented above (Fig. 1 to Fig. 5) were tested experimentally. Their design was provided for $C_1 = 10$ nF that equals also to C_m when $B = 1$ (obtained by $V_{SETB} = 1$ V because $B \cong V_{SETB}$ is in the case of the EL2082 device used as ECCII). All the tested topologies were tuned by V_{SETB} between 0.1 and 1.0 V ($B \cong 0.1 \rightarrow 1.0$ [−]). The PSpice simulation software as well as laboratory experiments were used to verify the features of the proposed circuits with AD8130 devices [34] (used as DVB) and EL2082 [38] (used as ECCII).

The E5071C vector network analyzer was used to measure the scattering parameter s_{11} (reflection factor) that allows to calculate the impedance. However, the measured impedance is limited between several tens of kΩ and hundreds of mΩ. The analyses of the presented concepts are targeted to the frequency band from 10 kHz (lower limit of E5071C) up to 10 MHz (the assumed validity of the experiments due to real features of the printed circuit board and active devices). The input power level used for the experiments was set to −20 dBm/50 Ω.

A. ANALYSIS OF THE LOSSY SOLUTION-FIG. 1B)

The results (magnitude and phase impedance plots) from the analysis of the lossy solution (shown in Fig. 1b)) are plotted in Fig. 6. It is important to note that all visible discrepancies and deviations in the measured traces at the lowest frequencies are caused by the used method and the analyzer (too high values of the impedance, where the accuracy of the equipment is limited). In case of the measurement, the obtained results prove a possible variability of C_m (total capacity) between 11.5 nF ($V_{SETB} = 1.0$ V) and 1.4 nF ($V_{SETB} = 0.1$ V). The simulated values of C_m for V_{SETB} equal to 1.0 V and 0.1 V were found between 10 nF and 1.1 nF, respectively. As it was expected, the value of C_m can be tuned in range of one decade by driving the DC voltage (V_{SETB}).

Note that there are several areas, where the lossy character of the impedance is useful. It can be used for adjustment of parameters in oscillators (condition of oscillations), filters (adjustment of the quality factor) or resonators (determined losses) [39].

B. ANALYSIS OF THE LOSSLESS SOLUTION - FIG. 2B)

The lossless solution (Fig. 2b) was tested under the same conditions as the lossy one and the obtained results are shown

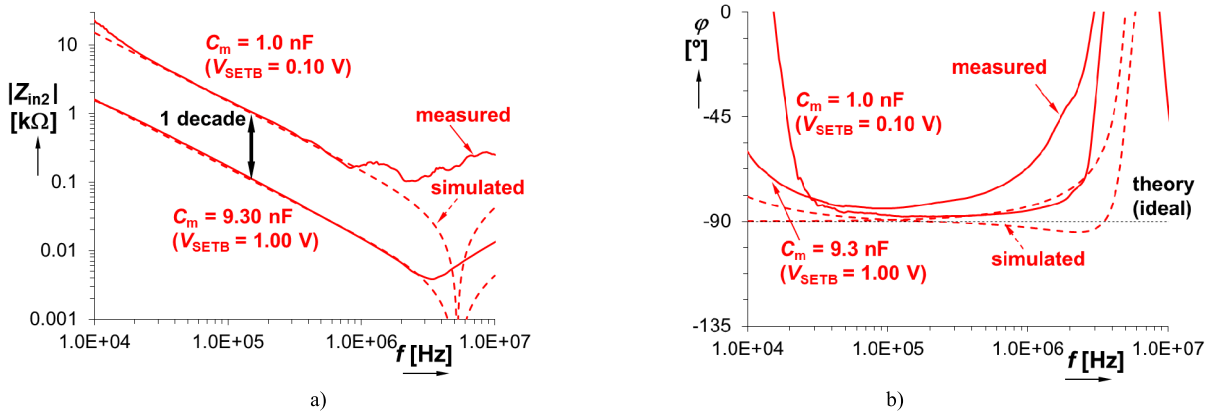

FIGURE 7. Comparison of measured and simulated impedance using single DVB, ECCII and additional feedback from X terminal to positive input of DVB (Fig. 2b): a) magnitude responses, b) phase responses.

TABLE 2. Comparison of the discussed features of the presented topologies.

Solution	Ideal input impedance	When R_X considered in input impedance	When both R_o and R_X considered in input impedance	Multiplication factor for lossless operation	Lossy operation	Lossless operation
Fig. 1a	$Z_{in1}(s)=\frac{1}{sC_1 2B}$	$Z_{in1}'(s)=\frac{1+sC_1R_X}{2\cdot sC_1B}$	$Z_{in1}''(s)=\frac{1+sC_1(R_o+R_X)}{2\cdot sC_1B}$	$2B$	Yes	No
Fig. 1b	$Z_{in1}(s)=\frac{1}{sC_1B}$	$Z_{in1}'(s)=\frac{1+sC_1R_X}{sC_1B}$	$Z_{in1}''(s)=\frac{1+sC_1(R_o+R_X)}{sC_1B}$	B	Yes	No
Fig. 2a,b	$Z_{in2}(s)=\frac{1}{sC_1B}$	$Z_{in2}'(s)=\frac{1}{sC_1B}$	$Z_{in2}''(s)=\frac{1+sC_1R_o}{sC_1B}$	B	Yes*	Yes**
Fig. 3,4	-	$Z_{in3}'(s)=\frac{1+sC_1R_X(1-A)}{sC_1B}$	$Z_{in3}''(s)=\frac{1+sC_1(R_o+R_X-A\cdot R_X)}{sC_1B}$	B	Yes***	Yes***
Fig. 5	$Z_{in4}(s)=\frac{1}{sC_1\prod_{i=1}^{n}B_i}$	$Z_{in4}'(s)=\frac{1}{sC_1\prod_{i=1}^{n}B_i}$	$Z_{in4}''(s)=\frac{1+sC_1R_o}{sC_1\prod_{i=1}^{n}B_i}$	B^n	Yes*	Yes**

Notes: *for significant value of R_o – intentionally added serial resistance to the output of DVB; **for low R_o; *** intentionally adjustable by voltage gain A

in Fig. 7. During the measurement, the total capacitance C_m was found between 1 nF and 9.3 nF for V_{SETB} adjusted from 0.1 to 1.0 V. Simulation-based analyses show the range of C_m from 1.05 nF up to 10 nF. Similarly, to the previous case, the range allowed by a single current gain control offers re-adjustability of the value of C_m in the range of one decade.

C. TEST OF RECONFIGURATION BETWEEN LOSSY AND LOSSLESS MODE OF OPERATION

The topology introduced in Fig. 3 was used for the simple verification of the lossy/lossless modes of operation when voltage gain A was adjusted between 0 and 1. The VGA (see Fig. 3) was implemented by using of the AD835 multiplier [40] (see Fig. 8). In the ideal case, it reaches a gain $A = 1$ for $V_{SETA} = 0.09$ V. However, in practice (mismatches and gain inaccuracies) it was set to 0.14 V in order to obtain the unity gain. The resulting impedance magnitude responses are captured in Fig. 9.

D. VERIFICATION OF THE ENHANCEMENT OF CAPACITANCE MULTIPLICATION FACTOR (MF) VARIABILITY

Enhancement of the number of ECCII blocks in the structure presented in Fig. 2b) offers extension of the range of the multiplication constant. Two and three blocks ($n = 2$ and $n = 3$) were experimentally tested in the loop in accordance to the idea introduced in Fig. 5. The magnitude impedance responses for both cases are shown in Fig. 10. In case of $n = 2$ ($0.1 \leq V_{SETB} \leq 1.0$ V), the expected ideal range of C_m is

TABLE 3. Comparison of obtained ranges of adjustability for all 3 discussed cases (n = 1,2 and 3).

n	Ideal range of C_m [nF]	Ratio	Simulated range of C_m [nF]	Ratio	Measured range of C_m [nF]	Ratio of adjustment efficiency
1	10 → 1	1:1	10 → 1.05	0.95:1	9.3 → 1	0.93
2	10 → 0.1	10:1	10 → 0.12	8.3:1	5.7 → 0.19	3
3	10 → 0.01	100:1	10 → 0.03	33.3:1	5.8 → 0.03	19.3

Notes: ratio is defined as: $(C_{m\_max}/C_{m\_min})/(V_{SETB\_max}/V_{SETB\_min})$

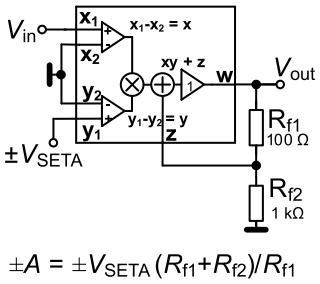

FIGURE 8. Solution of the VGA with analog multiplier AD835.

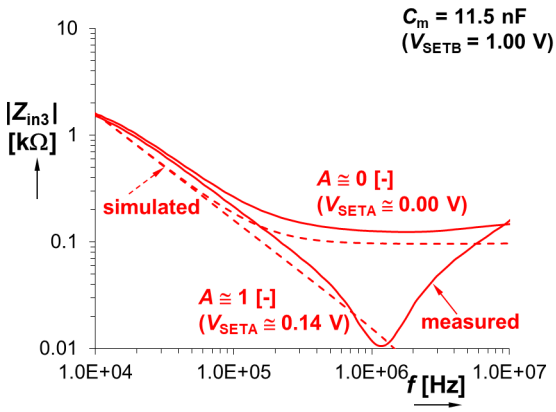

FIGURE 9. Comparison of the measured and simulated impedance magnitude plots for solution in Fig. 3 (re-adjustability test between lossy and lossless solutions).

from 0.1 nF up to 10 nF. Simulation and experimental results confirmed the adjustability from 0.12 nF up to 10 nF and from 0.19 nF up to 5.7 nF, respectively. When 3 blocks of ECCIIs are connected ($n = 3$) then the expected adjustability of C_m is between 0.01 nF and 10 nF. PSpice simulations indicate C_m between 0.03 nF and 10 nF while experimental measurements give values between 0.03 nF and 5.8 nF. Despite of some inaccuracies, these results bring significant improvement of re-adjustability (almost 2 decades for $n = 2$ and almost 3 decades for $n = 3$). The comparison of all discussed cases is shown in Table 3 and Fig. 11, respectively. As it is visible in Table 3, there are certain deviations from the theoretical expectations. They are caused by the nonlinearity of the gain dependence on the driving voltage and a mismatch of all driven gains in the chain. It is important to mention that V_{SETA} and V_{SETB} driving voltages do not have influence on the value of R_X.

Power consumption (±5 V supply) of the solutions in Figs. 1 and 2 reaches 360 mW, the circuit in Fig. 3 consumes 540 mW. Power consumption of the structure in Fig. 5 depends on the number of the used ECCII blocks (520 mW for $n = 2$ and 690 mW for $n = 3$). It is visible that the significant extension of the range of tunability only doubles the power consumption.

E. DEFINITION OF OPERATIONAL FREQUENCY BANDWIDTH

The operational bandwidth of the capacitance multiplier is limited by two factors: zero and pole frequencies of the impedance. Actually, these two parameters are caused by the small-signal parasitic features, which are indicated in Fig. 12 (as an example, lossless structure from Fig. 2 b) was selected), and by their combination with useful parameters of the structure. Note that only the most significant parasitic parameters are considered in the following text.

For simplicity, initially, it is supposed that $L_o \rightarrow 0$ H. Hence, the input impedance is:

$$Z_{in2}'''(s) = \frac{R_p\,(1 + sC_1R_o)}{1 + sC_1\left(R_pB + R_o\right)}. \tag{7}$$

It provides interesting information: the resistance R_p limits the maximal available impedance value at 0 Hz, the high-frequency zero is given by $\omega_z = 1/(C_1R_o)$ and the low-frequency pole is equal to $\omega_p = 1/(C_1 \cdot (R_o + R_pB)$. Zero frequency occurs between 1 and 10 MHz in each of the above presented results. The increasing value of R_o is not negligible [34] because the resistance R_o and the selected value for the working C_1 capacitor have a direct impact on ω_z.

However, the results indicate a "second-order" behavior of the resulting impedance function. The parameter L_o represents the inductive character of the output impedance of the used DVB (the value of the output resistance is increasing with the value of the frequency). This parameter also represents the total inductance of the wires (between the output of DVB and the input X of the block ECCII) used in the case of a real circuit. The consideration of R_p and L_o leads to a modification of the input impedance (7) into the following form:

$$Z_{in2}''''(s) \cong \frac{R_p \cdot \left(s^2 + \frac{R_o}{L_o}s + \frac{1}{L_oC_1}\right)}{s^2 + \frac{R_o + R_pB}{L_o}s + \frac{1}{L_oC_1}}, \tag{8}$$

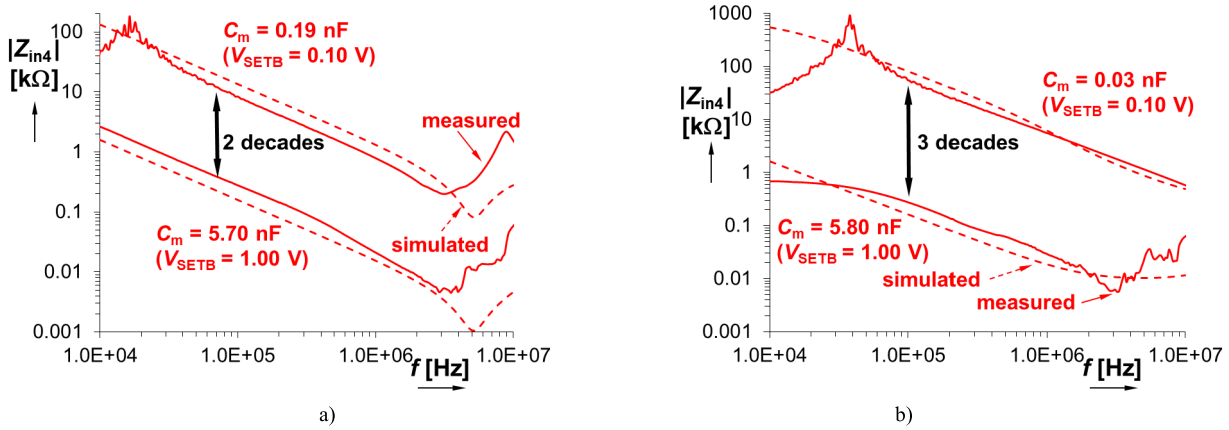

FIGURE 10. Comparison of measured and simulated impedance responses for capacitance multiplier using single DVB, ECCII and additional feedback from X terminal to positive input of DVB (Fig. 5) for: a) n = 2, b) n = 3.

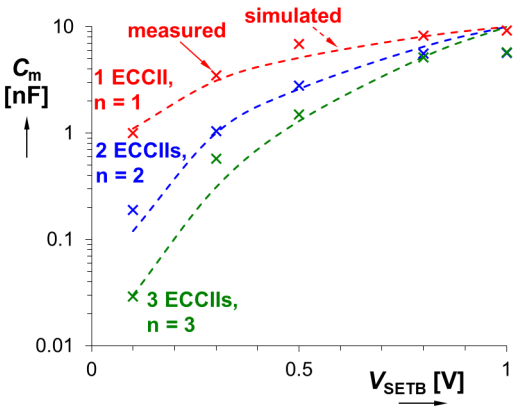

FIGURE 11. Dependence of C_m on current gain B (V_{SETB}) for variation of number of ECCIIs in the structure (n = 1, 2 and 3).

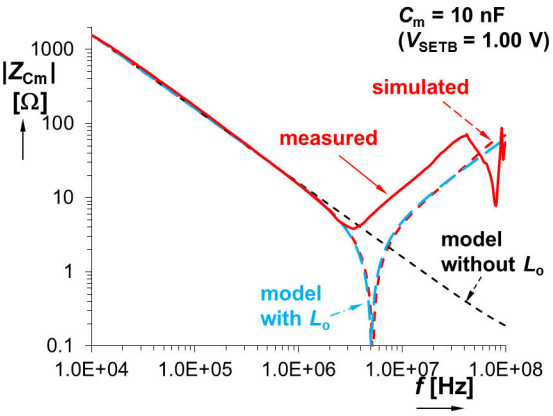

FIGURE 13. Detail on impedance plot of small-signal models with parasitic features discussed in this section and their comparison with simulation and experimental results.

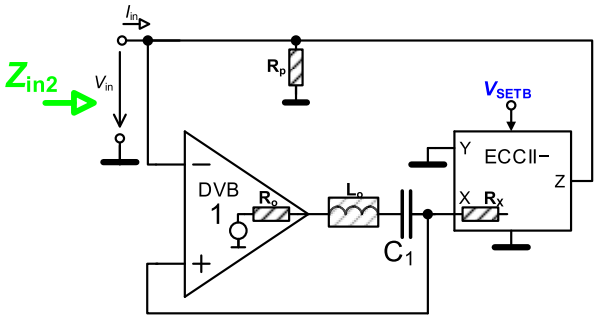

FIGURE 12. Main small-signal parasitic effects in the basic lossless circuit from Fig. 2 b).

where the complex conjugated zeros are given by:

$$z_{1,2} = 0.5 \cdot \left(-\frac{R_o}{L_o} \pm \sqrt{\left(\frac{R_o}{L_o}\right)^2 - \frac{4}{L_o C_1}} \right), \tag{9}$$

because, in our case, the discriminant

$$D = \left(\frac{R_o}{L_o}\right)^2 - \frac{4}{L_o C_1}, \tag{10}$$

is always negative (< 0) due to a low value of R_o. The poles of the impedance function are real (discriminant > 0) because R_p in the denominator of (8) has a significant role to overcome the value of $4/(L_o C_1)$:

$$p_{1,2} = 0.5 \cdot \left(-\frac{R_o + R_p B}{L_o} \pm \sqrt{\left(\frac{R_o + R_p B}{L_o}\right)^2 - \frac{4}{L_o C_1}} \right). \tag{11}$$

It must be noted that the value of B in (8) has an impact on the quality factor of the poles (intended for C_m adjustment) and therefore, also on the shape of the trace. However, the second pole is located too high (above frequency limitations of the used active devices) because $\omega_{p2} \approx BR_p/L_0$. This leads to very high theoretical values (unavailable in practice). The dominant pole frequency at low frequencies can be found at $\omega_{p1} \cong 1/(R_p C_1)$. A fast calculation using $C_1 = 10$ nF and $R_p \cong 0.5$ MΩ (the output resistance of EL2082 [38]) yields $f_{p1} \cong 32$ Hz. The complex conjugated zero frequency is given by $\omega_{z1} \cong 1/\sqrt{(L_o C_1)}$ and for $L_o = 100$ nH it results into the value $f_{p1} \cong 5$ MHz (see Fig. 13).

This is quite close to values measured in practice (visible between 1 and 4 MHz). The value of 100 nH was selected in order to fit simulation results (we do not know the exact value because the datasheet [34] does not contain this information). The difference between the experimentally measured trace and other traces is caused by other small-signal parasitic features (PCB). As a conclusion, it can be stated that the low frequency and high frequency limits of the useful band are given by ω_{p1} and ω_{z1}, respectively. Hence, the operational bandwidth will be: $1/(R_pC_1) < \omega_{max} - \omega_{min} < 1/\sqrt{(L_oC_1)}$.

VIII. CONCLUSION

In this paper, several new solutions of the capacitance multipliers (in general with the same internal core) were presented. Their features were proved by both simulation and experimental ways. The obtained results indicate that the floating capacitor can be easily used in the synthesis of these types of linear electronic circuits when some methods for elimination of the parasitic effects of low-impedance input terminals are applied. For these purposes, an additional feedback and its gain adjustment was used. Moreover, this feedback also serves for intentional adjustment between lossy and lossless modes of operation. The presented structures (basic core) can be used in the design of lossy, lossless and differential-mode capacitance multipliers. Moreover, enhanced adjustability of MF (exponential dependency) is also possible. Our experimental results confirmed simple tunability of all structures by current gain driven by DC voltage. The enhancement of the multiplication constant (and also its low values) leads to interesting tunability of the capacitance multiplier. The largest change of the capacitance value was tested for 3 ECCII blocks in the range of 5.8 → 0.03 nF (19:1).

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