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Monolithic Single PMUT-on-CMOS Ultrasound System With +17 dB SNR for Imaging Applications

IVÁN ZAMORA, EYGLIS LEDESMA, (Student Member, IEEE), ARANTXA URANGA, AND NÚRIA BARNIOL, (Member, IEEE)

Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain

Corresponding author: Núria Barniol (nuria.barniol@uab.cat)

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ABSTRACT This article presents a fully integrated ultrasound system based on a single piezoelectric micromachined ultrasonic transducer (PMUT) monolithically fabricated with a 0.13 μm complementary metal oxide semiconductor (CMOS) process analog front-end circuitry. The PMUT consists of an aluminum nitride, AlN, squared device with 80 μm side that resonates at 2.4 MHz in liquid environment. The monolithic integration of the PMUT with the CMOS circuitry allows a reduction of the parasitic capacitance, a reduction of the electronic noise contribution and a clear improvement in the Signal-to Noise ratio (SNR $\sim$ 27 dB better) compared to a non-integrated equivalent system. A pulse-echo experiment with the single PMUT-on-CMOS for transmitting and sensing simultaneously is demonstrated, ensuring a 17.3 dB SNR, higher than the minimal necessary for accurate fingerprint images, paving the way towards a pixel sized imaging system with no need of multiple simultaneous PMUTs transmitters. Consuming only 0.3 mW and getting an input-referred noise of 3.26 mPa/$\sqrt{}$Hz at 2.4 MHz, the proposed pulse-echo system achieves a competitive noise efficient factor in comparison with the state-of-the-art.

INDEX TERMS AlN, CMOS, CMOS-MEMS, piezoelectrical resonator, piezoelectric on CMOS, PMUT, PMUT-on-CMOS, ultrasound, ultrasound transducers.

I. INTRODUCTION

The ultrasound imaging technique has increased its population in the medical industry and authentication systems due to on the one hand its non-invasiveness, focusing capability and in-depth targeting, and on the other hand its robustness against unavoidable external contaminants like sweat or oil [1]–[3]. The development of wearable devices, the increasing use of authentication systems in mobile devices and the miniature probes for intra-vascular ultrasound systems (IVUS) demand a power-efficient and compact System-on-chip (SoC) to achieve high quality images. Micromachined ultrasonic transducers (MUT), capacitive (CMUTs) and piezoelectrical (PMUTs) have been evolved as clear alternative for their capability to be monolithically integrated in CMOS circuitry [4], [5]. Several examples of monolithic integration of CMUT with the CMOS analog front-end circuitry have been developed [6]–[8] achieving a good trade-off between performance and size, but requiring large polarization voltages [4]. Miniature piezoelectrical ultrasound transducers with less demanding power than CMUTs, have been also reported using different materials [5]. Two piezoelectrical thin-film materials have been basically reported: PZT [9]–[11] and AlN [2], [3], [12], [13]. The AlN, although exhibiting lower piezoelectric capabilities than PZT, has been widely reported as an alternative to compact systems due to its low temperature deposition and the possibility to be integrated over pre-processed CMOS wafers with the appropriate dimensions and using a parallel fabrication process [3], [14]. Currently only flip-chip technology with a dedicated eutectic bonding between AlN-PMUTs and CMOS has been reported in a full system configuration [2], [3], [15].

In this article we present, for the first time, a fully integrated AlN-PMUT with its analog front-end CMOS circuitry (PMUT-on-CMOS). With this implementation a single PMUT with two top-electrodes is used as acoustic

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transmitter and receiver, providing a single-pixel ultrasound echo system. The rest of the paper is organized in 4 sections: Section II explains the PMUT-on-CMOS design and fabrication towards optimization of the SNR; Section III details the experimental results including simulations with finite element modelization and comparison with the state-of-the-art; finally, Section IV concludes the paper.

II. DESIGN AND FABRICATION

Fig. 1a shows the cross-section profile of the PMUT built on a 0.13 μm CMOS wafer using the Silterra MEMS-on-CMOS fabrication process [16]–[18]. The Aluminum (Al) bottom and top electrodes with 0.4 μm and 0.35 μm thickness are settled on top and bottom of the piezoelectric layer, respectively. Metal vias contacts are used to directly connect the electrodes with the last metal of the CMOS Back-end-of-line (BEOL) layers avoiding any bonding technique and decreasing the parasitic capacitances. Aluminum Nitride (AlN) is chosen as piezoelectric material since it can be deposited allowing the integration with the standard CMOS process. A 1.3 μm thick AlN layer is deposited using Physical Vapor Deposition (PVD). An etching step allows the releasing of the membrane, defining a cavity with 600 nm height. Finally, a 1.5 μm Silicon Nitride (Si_3N_4) layer is deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD) process over all the PMUT structure. This last layer serves as passive elastic layer for the PMUT membrane movement, as well as sealing layer for the operation in liquid [14].

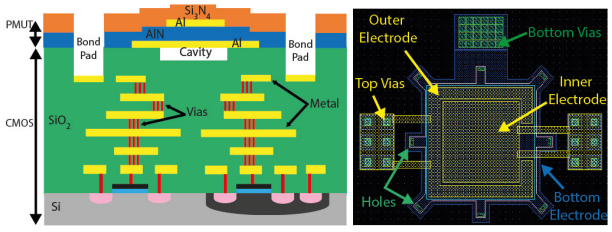

FIGURE 1. a) Cross-section of the PMUT-on-CMOS Silterra technology. (layers not to scale). b) layout of the squared PMUT with 80 μm side.

A. TRANSMISSION AND RECEPTION ULTRASOUND SYSTEM

The proposed PMUT is a square shaped device with 80 μm side and it has eight releasing holes out of the cavity, see Fig. 1b. The PMUT device used is operated in its first flexural resonant mode, as a two-port device with two top electrodes to demonstrate the capability to transmit and receive an acoustic pressure. The ultrasound system is composed of the PMUT along with a CMOS analog front-end circuitry to drive and sense the PMUT. Fig 2 shows a general diagram of the main blocks used in this system and Fig. 3 corresponds to the overall layout.

A High Voltage (HV) Transmitter (TX) is used to drive the PMUT, applying HV pulses at its resonance frequency in order to generate enough acoustic pressure to the surrounding

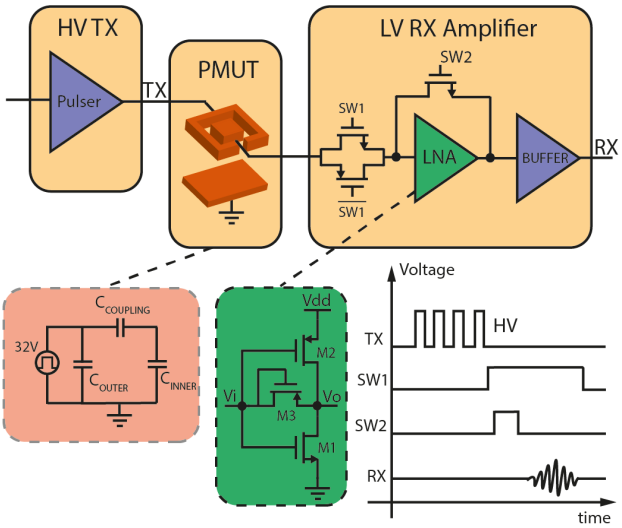

FIGURE 2. Block diagram of the proposed transmission and reception system. HV TX: High Voltage Transmitter; PMUT with two top electrodes and one bottom electrode (bottom box: electrical equivalent circuit, with COUTER and CINNER, capacitances between outer and inner PMUT electrodes and bottom PMUT electrode (grounded), respectively (CCOUPLING is the coupled capacitance between both). LV RX: Low Voltage Receiver (bottom box: electrical schematic of the receiver amplifier). Time diagram for one cycle of transmission and reception.

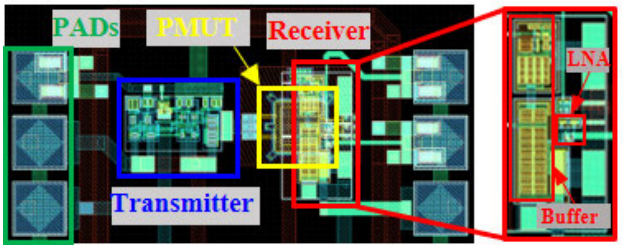

FIGURE 3. Full layout of the proposed Ultrasound System, with the PMUT (yellow box) monolithically integrated over the CMOS front-end circuitry TX/RX. Right: Enlarged layout of the RX showing LNA amplifier (25 μm × 23 μm) and the output buffer.

medium. To optimize area, power consumption and transmission efficiency we have chosen the HV Pulser designed in [19]. This circuit, based on level-shifters and inverters, is able to rise monophasic pulses from 3.3 V to 32 V. The detailed description and characterization of this circuit can be seen in [19].

In order to convert the electric charge generated by the PMUT when an acoustic wave is applied over its surface, we have designed a low noise amplifier (LNA). In the design of the LNA, a tradeoff between noise performance, gain and area needs to be considered. With this tradeoff in mind, and taking into account that the PMUT will be fully integrated with the LNA circuitry, we have chosen the Voltage Amplifier (VA) proposed in [19] as LNA topology, see Fig. 2. Noise cancellation technique [20] has not been considered to avoid an increase of complexity, area and power consumption. This amplifier is a single-ended input self-biased push-pull configuration where the output voltage depends on its open

loop gain and both the input parasitic and VA equivalent input capacitances. Low input noise, very low area and high gain are guaranteed with this topology. Its main drawback, the dependence of its transimpedance gain with the parasitic capacitances in the interface PMUT-LNA circuitry, is overcome with the monolithic integration where the parasitic capacitance may be negligible in front of the electrical PMUT capacitance (C_{INNER} = 262 fF, obtained from COMSOL simulation, between inner and bottom PMUT electrodes) and VA equivalent input capacitance (C_{inLNA} = 609 fF value computed from the cadence simulations and experimental results) (see Table 1). A deeper characterization of this amplifier can be found in [19].

TABLE 1. Summary of LNA and PMUT electrical parameters.

	Parameter	Value	Comments
PMUT	C_{INNER} (fF)	262	Extracted from COMSOL.
	C_{OUTER} (fF)	216	Extracted from COMSOL.
	$C_{COUPLING}$ (fF)	23	Extracted from Electrical Measurement in air.
LNA	C_M (fF)	19.8	Extracted from Cadence.
	C_{gs} (fF)	63	Extracted from Cadence.
	C_{OUT} (pF)	1	Extracted from Cadence.
	W1/L1 (µm/µm)	10/0.22	M1 aspect ratio.
	W2/L2 (µm/µm)	25/0.22	M2 aspect ratio.
	W3/L3 (µm/µm)	0.2/0.2	M3 aspect ratio.
	I_{BIAS} (µA)	200	LNA current bias.
	A_{ol} (dB)	28.5	Without buffer.
	C_{inLNA} (fF)	609	C_{gs}+C_M*(1+A_{ol}) Considering the Miller effect.
PMUT + LNA	$C_{parasitic}$ (pF)	0-7	Due to PCB, connectors (COMSOL) and bonding pads (Cadence).
	C_{inIS} (fF)	325	C_{gs}+C_{INNER}
	C_{inNIS} (pF)	0.33-7.33	C_{gs}+C_{INNER}+$C_{parasitic}$

One of the advantages of using one top electrode as an actuator and the other as a sensor is the possibility to avoid HV switches to isolate the HV used in the transmission from the Low Voltage (LV) circuitry used on the reception path. HV switches suffer from large parasitic capacitances and therefore the signal is greatly attenuated. However, since the outer top electrode is 2 μm spaced from the inner top electrode, this configuration exhibits large crosstalk. The equivalent coupling capacitance ($C_{COUPLING}$) between the two top electrodes is close to 23 fF (extracted from the electrical frequency response in air), which causes that ~1.6 V signal (0.82 V AC signal over 0.75 V DC operation point) to be coupled to the inner electrode during transmission when the PMUT is directly loaded with the LNA (C_{INNER} in parallel with $C_{in,LNA}$). Considering than the reception circuitry is powered with 1.5 V, it is necessary to reduce the crosstalk signal to avoid a damage of the circuitry. To overcome this issue, we have designed two LV switches. The first one (SW1 on Fig. 2) avoids the appearance of the crosstalk signal at the input node of the LNA during transmission, whereas the second one (SW2) allows the LNA to return to its adequate operation point (Vdd/2) thanks to the creation of a low impedance path between the input and output node of the LNA. Fig. 2 shows a time diagram for one cycle of transmission and reception. For measurement purposes, a source follower output buffer is designed, providing an overall reception gain of 21.5 dB.

B. SIGNAL-TO-NOISE RATIO (SNR) IMPROVEMENT WITH MONOLITHIC SOLUTION

The image quality is largely determined by the signal-to-noise ratio (SNR). For instance, in accurate fingerprints images, 12 dB are at least required [21]. We will demonstrate how the monolithic integration allows an improvement of the SNR, compared with the non-monolithic version. In order to evaluate it, we have analyzed the influence of the parasitic capacitances in two of the most key parameters of an ultrasound channel reception: the signal and noise level. The improvement on the SNR will be computed through the product of a signal and a noise improvement factors (F_s and F_n, respectively) between a non-integrated system (NIS) and an integrated system (IS). These factors were obtained considering the reception scheme without isolation switches, showed in Fig. 4, and considering that the individual performance of the PMUT and the LNA is the same in both systems. Table 1 summarizes the used LNA and PMUT electrical parameters.

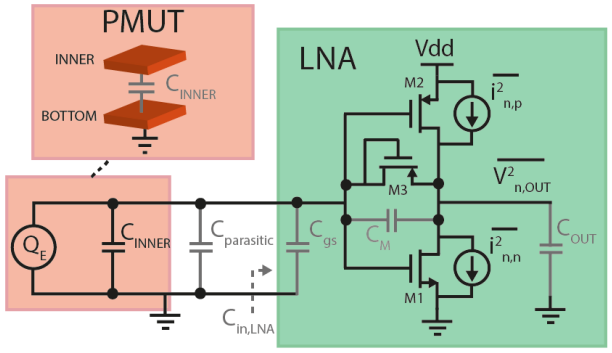

FIGURE 4. Reception scheme without isolation switches considering all electrical capacitance and noise current sources.

The signal improvement factor (Fs) can be defined by (1):

$$F_S = \frac{V_{IS}}{V_{NIS}} = 1 + \frac{C_{parasitic}}{C_{INNER} + C_{inLNA}} \quad (1)$$

where V_{IS} and V_{NIS} are the voltage amplitudes at the LNA output for the IS and NIS respectively, C_{INNER} is the PMUT capacitance (262 fF), C_{inLNA} is the LNA equivalent

TABLE 2. Parameters used in FEM simulation.

PMUT Layer	Side (μm)	Thick. (μm)	Mat.	Y (GPa)	ρ (kg/m^3)
Passive	100	1.5	Si_3N_4	250	3100
Piezo.	100	1.3	AlN	345	3300
Inner Elect.	56.6				
Outer Elect.	Ext. 77/ Int. 60.6	0.35	Al	70	2700
Bott. Elect	86	0.4	Al	70	2700
Substrate	100	2	SiO_2	70	2200
Cavity	80	0.6	-	-	-

Y: Young's Modulus ρ: Density

input capacitance (609 fF) considering the Miller effect and $C_{parasitic}$ is the parasitic capacitance at the PMUT-LNA interface ($C_{parasitic} = 0$ pF for IS).

To analyze the noise improvement factor (F_n) we have obtained the equivalent output-mean-square voltage noise ($\bar{V}^2_{n,out}$) for this LNA configuration. Assuming that all transistors work in the saturation region, the ($\bar{V}^2_{n,out}$) is defined by (2), as shown at the bottom of the page, where $Z_{out}(j\omega)$ is the output impedance, ω is the angular frequency, $\bar{i}^2_{n,n}$ and $\bar{i}^2_{n,p}$ are the mean-square current-noise sources for nMOS and pMOS transistors respectively, C_M is the Miller capacitance between the input and output of the LNA, C_{in} is the equivalent input capacitance without considering the Miller effect (gate-to-source capacitance, C_{gs}, in parallel with C_{INNER} in parallel with $C_{parasitic}$), C_{out} is the output capacitance of the LNA (dominated by the input capacitance of the output buffer), $g_{m,n}$ and $g_{ds,n}$ are the transconductances and output conductance of the nMOS transistor, and $g_{m,p}$, and $g_{ds,p}$ of the pMOS transistor.

The output noise improvement factor (F_n) can be defined by (3):

$$F_n = \sqrt{\frac{\overline{V^2_{n,out,NIS}}}{\overline{V^2_{n,out,IS}}}} = \frac{\frac{C_M}{C_{in,IS}} * A_{ol} + 1}{\frac{C_M}{C_{in,NIS}} * A_{ol} + 1} \quad (3)$$

where $C_{in,IS}$ is the integrated system equivalent input capacitance (C_{in} with $C_{parasitic} = 0$ pF), $C_{in,NIS}$ is non-integrated system equivalent input capacitance (C_{in}), and A_{ol} is the open loop gain of the LNA.

To validate F_s and F_n factors, some simulations were done changing the value of the parasitic capacitance ($C_{parasitic}$). To compute the signal improvement factor (F_s) the PMUT was modeled in COMSOL Multiphysics using 2D-Axisymmetric Model, see Fig. 5 (a), and it was loaded with the parasitic capacitance ($C_{parasitic}$) and the LNA equivalent input capacitance ($C_{in,LNA}$) (Fig. 6 inset lower). Table 2 summarizes the dimensions and properties of the materials used in the FEM model. Fig 5 (b) shows the acoustic pressure map along axial direction (left) and the acoustic pressure dependence in the AA' position (right) (corresponding with PMUT center) when the outer electrode is excited with 1 Vpp at the resonance frequency (2.3 MHz). Also, an acoustic simulation was done in order to obtain the generated voltage when a pressure (4 cycles with 200 Pa peak-to-peak) is applied over the PMUT surface.

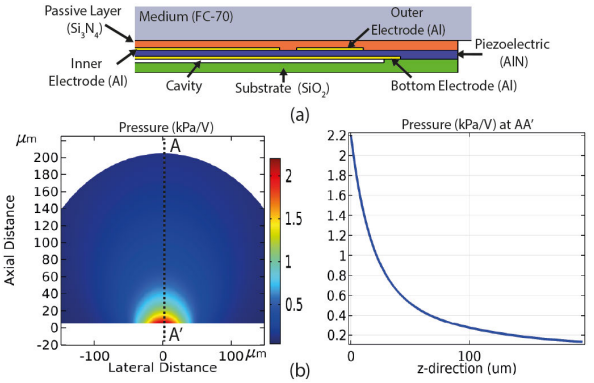

FIGURE 5. (a) Cross-section schematic of the PMUT used in 2D-Axisymmetric Model and, (b) Acoustic pressure map along axial direction (left) and the pressure dependence in the AA' position (right) when 1 Vpp is applied to the outer electrode.

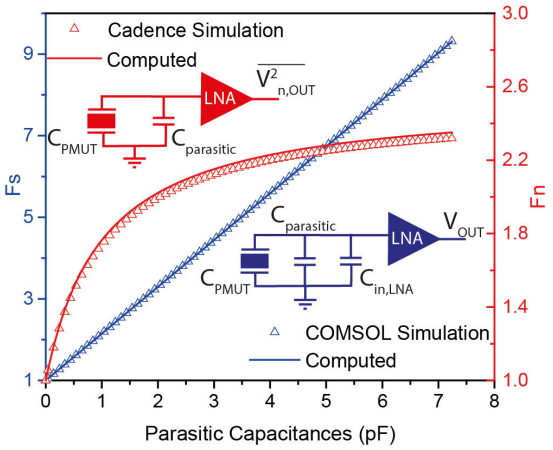

FIGURE 6. Computed and simulated results of: Signal Improvement Factor, Fs, (left axis, blue) and Noise Improvement Factor, Fn, (right axis, red).

In the same way, a noise analysis of the electronic circuits in Virtuoso Cadence was used to obtain the output noise and consequently the output noise improvement factor (F_n)

$$\overline{V^2_{n,out}} = |Z_{out}(j\omega)|^{2*}\left(\overline{i^2_{n,n}} + \overline{i^2_{n,p}}\right) = \frac{(C_M + C_{in})^{2*}\left(\overline{i^2_{n,n}} + \overline{i^2_{n,p}}\right)}{\left\{\left[C_M\left(g_{m,n} + g_{m,p}\right) + C_{in}\left(g_{ds,n} + g_{ds,p}\right)\right]\left[1 + \frac{j\omega(C_{in}C_M + C_{out}C_M + C_{out}C_{in})}{C_M\left(g_{m,n}+g_{m,p}\right)+C_{in}\left(g_{ds,n}+g_{ds,p}\right)}\right]\right\}^2} \quad (2)$$

(Fig. 6 inset upper). The results, computed (Eq. 1 and Eq. 3) and simulated, are shown in Fig. 6. Note that when the parasitic capacitance is 0 pF (monolithic solution), F_s and F_n are equal to 1, and when the parasitic capacitance gets bigger, the output signal is attenuated, and the output noise is increased. These results show than the SNR will be improved in 12 dB for a $C_{parasitic} = 1$ pF and up to 27 dB for a $C_{parasitic} = 7$ pF, clearly quantifying the benefits of the monolithic integration due to the reduction on the parasitic capacitances.

A complementary analysis was done in order to obtain the influence of the isolation switches in the noise performance. Fig. 7 shows the equivalent electrical circuit on the reception mode taking into account the generated thermal noise by switch 1 ($\bar{V}^2_{n,Rsw1}$) when is conducting, and the input-referred current and voltage noise sources of the LNA ($i^2_{n,LNA}$ and $\bar{V}^2_{n,LNA}$). Considering than $\bar{i}^2_{n,LNA}$ and $\bar{V}^2_{n,LNA}$ are correlated between them, but uncorrelated with $\bar{V}^2_{n,Rsw1}$, the input-referred noise ($\bar{V}^2_{n,IN}$) can be found Eq. (4):

$$\overline{V^2_{n,IN}} = \left(V_{n,LNA}\left|\frac{Z_{in,LNA}}{Z_{in,LNA}+Z_{eq}}\right| + i_{n,LNA}\left|\frac{Z_{in,LNA}Z_{eq}}{Z_{in,LNA}+Z_{eq}}\right|\right)^2 + \overline{V^2_{n,Rsw1}}\left|\frac{Z_{in,LNA}}{Z_{in,LNA}+Z_{eq}}\right|^2 \quad (4)$$

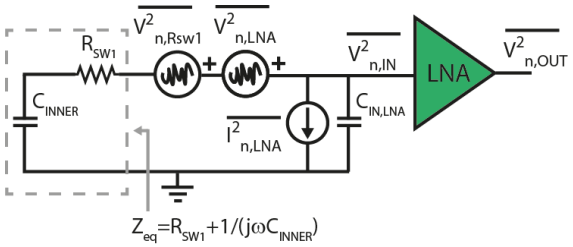

FIGURE 7. Simplified reception scheme considering the isolation switches and the input-referred noise sources.

where $Z_{in,LNA}$ is the equivalent input impedance of the LNA ($1/j\omega C_{in,LNA}$) and Z_{eq} is the equivalent impedance due to the serial connection of the ON resistor of the switch 1 (R_{SW1}) and the inner capacitance of the PMUT (C_{INNER}). Taking into account than the R_{SW1} is approximately 11 kΩ, at the resonance frequency of the PMUT $|1/j\omega C_{INNER}| \gg R_{SW1}$, and therefore the equation (4) can be rewritten in (5), as shown at the bottom of the page.

Note that the first term corresponds to the equivalent input-referred voltage noise when the PMUT is loaded with the LNA without isolation switches, and hence their contribution in the noise performance is given by the second term.

III. EXPERIMENTAL RESULTS

The PMUT-on-CMOS fabricated with the 0.13 μm HV CMOS process and MEMS-on-CMOS platform from Silterra is shown in Fig. 8. The interconnection vias between the PMUT and the circuitry are zoomed in. From this figure, the metal dummies of the CMOS BEOL metal layers (corresponding to M6 layer) are shown as well as the M6 metal layers and pads. To validate the previous results, acoustic characterizations in Fluorinert (FC-70) ($\rho_0 = 1940$ kg/m^3 and $c_0 = 685$ m/s) were done.

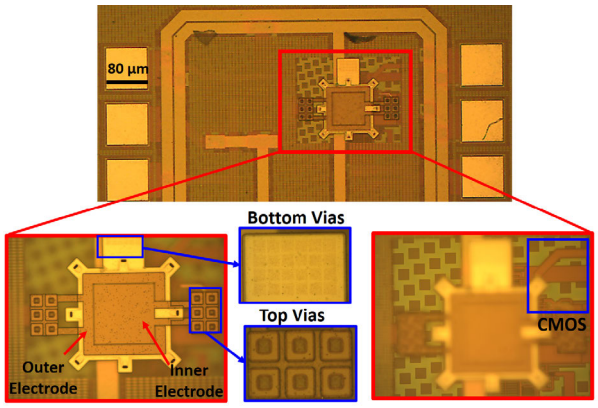

FIGURE 8. Optical image of the PMUT monolithically integrated on CMOS circuitry. The interconnection vias are zoomed. Right bottom figure is focalized on the M6 CMOS metal layer to clear visualize the different depth between PMUT and CMOS front end circuitry. The left bottom figure is focalized on the PMUT device.

Fig. 9 shows the experimental set-up used to characterize the monolithic PMUT-on-CMOS system and compare its results with a non-monolithically version. Fig 9a corresponds to non-integrated system where the PMUT and LNA circuitry were fabricated in two different chips and wire bonded to different printed-circuit-boards (PCBs). Whereas Fig 9b includes a single chip (integrated system), wire bonded to a PCB immersed in FC-70.

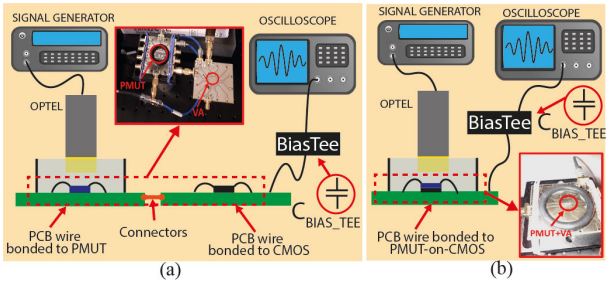

FIGURE 9. Set-up for the PMUT acoustic characterization as sensor in liquid environment: (a) non-integrated system and, (b) integrated system.

$$\overline{V^2_{n,IN}} = \left(V_{n,LNA}\frac{C_{INNER}}{C_{INNER}+C_{in,LNA}} + i_{n,LNA}\frac{1}{\omega(C_{INNER}+C_{in,LNA})}\right)^2 + \overline{V^2_{n,Rsw1}}\left(\frac{C_{INNER}}{C_{INNER}+C_{in,LNA}}\right)^2 \quad (5)$$

The non-Integrated system was tested first using a commercial transducer from OPTEL which was previously calibrated. The OPTEL was excited with 4 cycles at 2.4 MHz with 5 Vpp, generating an acoustic peak-to-peak pressure (P_A) of 3 kPa over PMUT surface. The peak-to-peak voltage at the LNA output (V_{OUT}) was acquired by the oscilloscope, giving 8 mVpp, that corresponds to a reception sensitivity ($SR = V_{OUT}/P_A$) of 2.67 V/MPa. Considering this value, the "End-of-cable Open Circuit Sensitivity" (SR_{EOC}) defined by Eq. (6) [22] gives ~6.4 V/MPa.

$$SR = SR^*_{EOC} G^* \frac{C_{INNER}}{C_{INNER} + C_{inLNA} + C_{parasitic}} \quad (6)$$

where G is LNA+Buffer Gain (21.5 dB), C_{INNER} is 262 fF, C_{inLNA} is 609 fF, and $C_{parasitic}$ is ~6.5 pF. The results show a degradation of the overall reception sensitivity of 42% due to the attenuation of the signal by the capacitive loading as expected.

The Integrated System was tested to validate the positive influence of the fully-monolithic-integration, see the set-up in Fig. 9b. An acoustic pressure of 300 Pa to 3 kPa peak-to-peak was applied over the PMUT surface using the same commercial transducer (OPTEL calibration at 2.4MHz, and amplitude voltages in a range of 0.5 V to 5 V).

Fig. 10 (black points) shows the maximum measured amplitude at the LNA output. A linear fit was done in order to obtain the slope that corresponds to the reception sensitivity (SR), giving 22.6 V/MPa. This result is higher than the non-integrated reception sensitivity (2.67 V/MPa) with an 8.5x factor since the PMUT is only loaded by the LNA equivalent input capacitance (in accordance with equation (6) and using the SR_{EOC} = 6.4V/MPa as was calibrated for the non-integrated PMUT). The measured sensitivity shows a good agreement with COMSOL simulation (blue line).

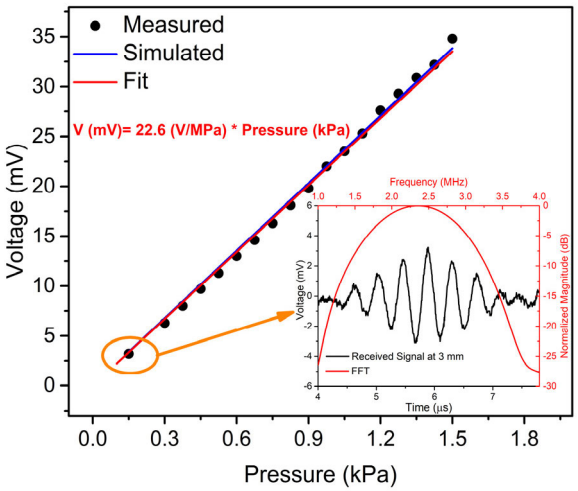

FIGURE 10. Output Voltage measurements at different applied pressures over PMUT surface. Inset: Time domain-response (bottom-left black axis) at 3 mm. In red the FFT from the ringdown (top-right red axis).

Fig. 10 inset shows the time-response when the maximum applied pressure is 150 Pa (black axis). Taking the ringdown and computing the Fast Fourier Transform, the quality factor and bandwidth at −3 dB was obtained, giving 2.2 and 1.06 MHz respectively. Besides, the fractional bandwidth at −6 dB was computed as BW_{-6dB}/f_0, being 63 %.

To obtain the output SNR, the output voltage signals were filtered using a pass-band Butterworth 6th order filter implemented in MATLAB, from 1.9 MHz to 2.9 MHz that correspond to the PMUT bandwidth. From the filtered time-response (Fig. 11 Inset), the rms output signal is approximated to Vmax/$\sqrt{2}$, and the rms output noise was computed from the interval time region in absence of echo. The output-referred integrated noise for the IS is 46 μVrms and 111 μVrms for NIS, that corresponds to an input-referred integrated noise of 3.87 μVrms and 9.34 μVrms respectively. With these values, the input-referred pressure noise spectral density, averaged inside the passband are 2.04 mPa/$\sqrt{}$Hz and 41.57 mPa/$\sqrt{}$Hz respectively, which demonstrates that the IS can detect signals 20.34x factor lower than NIS.

Fig. 11 shows the output SNR for both integrated (red dot) and non-integrated (blue square) PMUT systems. Taking the same applied pressure, the integrated system achieves an improvement of 27 dB, demonstrating a good agreement with the expected value (26 dB for 6.5 pF as $C_{parasitic}$, see Fig. 6). This difference can be minimized if the parasitic capacitances in the non-integrated system are decreased. As a consequence it can be stated that the monolithical integration of the PMUT on CMOS enhances the signal (due to the reduction of parasitic capacitance) as well as reduces the noise, improving the overall SNR, guarantying values in a range of 30 dB to 50 dB for applied pressures between 300 Pa to 3 kPa.

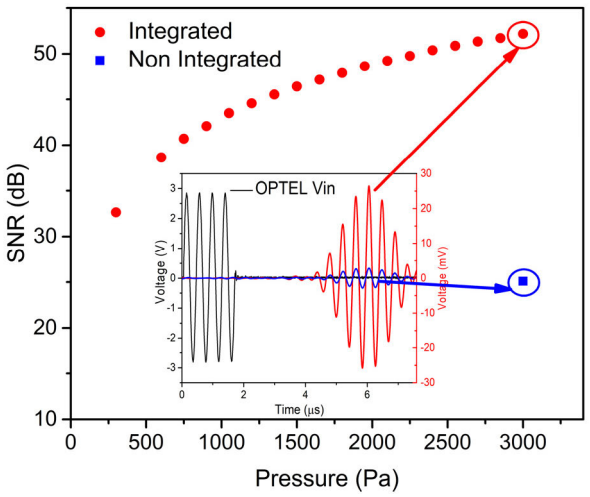

FIGURE 11. Measured signal-to-noise ratio as a function of applied pressure. Inset: Time domain response for integrated (red) and non-integrated (blue).

A. TRANSMISSION AND RECEPTION WITH A SINGLE PMUT-ON-CMOS

To validate this system a pulse-echo experiment with a single PMUT-on-CMOS was done using the air-liquid interface as

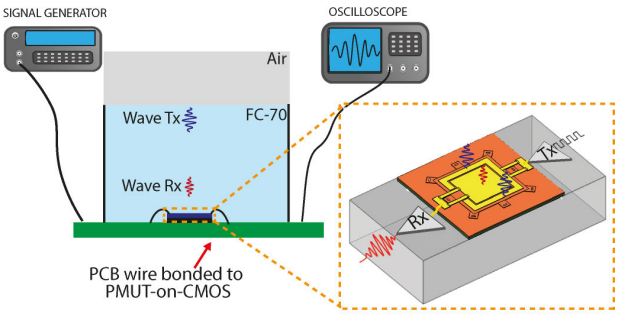

FIGURE 12. Set-up for single TX/RX PMUT in liquid environment.

reflective surface, see Fig 12. Four cycles of 3.3 V square signal at 2.4 MHz were applied to the transmitter input, which was powered by 32 V. In this case no decoupling capacitor was used between output buffer and oscilloscope in order to avoid slow charging and discharging of this capacitance when the switches change state. The removal of this decoupling capacitance results in a variation of the output buffer biasing point that changes its output resistance to 21 Ω. With these new conditions the overall gain of the receiver amplifier (LNA + Buffer) is 25.5 dB. With this new gain and considering that the system is the same than previously (i.e. the switches does not affect the parasitic capacitances) the reception sensitivity was obtained, giving 35.7 V/MPa.

Fig. 13 shows the received signal where the time-of-flight gives 5.84 μs that corresponds to 2 mm FC-70 thickness. Taking the peak-to-peak value (2.4 mVpp), and the computed reception sensitivity (35.7 V/MPa), a pressure of 67 Pa (23.7 Parms) over the PMUT surface is obtained. This value guarantees the acoustic measurements because it is about 7.3 times bigger than the acoustic medium noise (3.25 Parms), which is defined as $\sqrt{(4kTR_{med}\Delta f/S)}$ where k is the Boltzman's constant, T, the temperature (300K); $R_{med,}$ the medium acoustic impedance (1.35 MRayls); Δf, bandwidth (1 MHz); and S, the transducer effective area ($1/3^{*}80 \times 80\ \mu m^2$) [23].

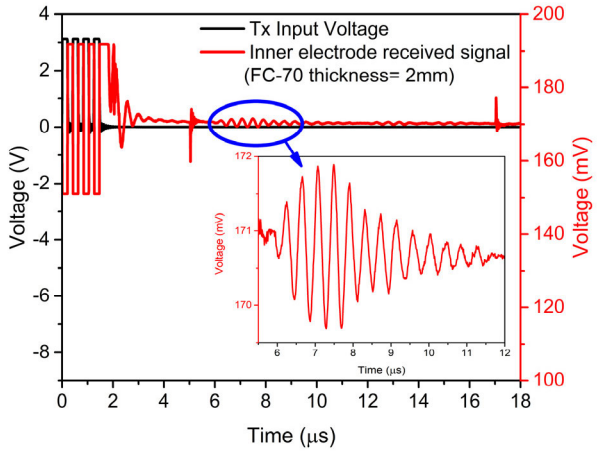

FIGURE 13. Time domain pulse-echo response using the single TX/RX PMUT system.

Fig. 13 also shows that the crosstalk effect is largely reduced from 820 mVpp (the crosstalk estimated in Section II) to 2 mVpp (41 mVpp/25.5 dB) at the LNA input, that correspond to a factor 410 times lower. The signal to noise ratio was computed filtering the measured signal with the previous implemented band-pass filter. The measured output-referred integrated noise of this system is 116 μVrms, that correspond to an input-referred integrated noise of 6.2 μVrms, which is 1.6 times greater than the measured without isolation switches. In order to validate how the presence of the isolation switches increase the equivalent input-referred voltage noise, the second term of the Eq. (5) was obtained through the difference between the equivalent input-referred power noise when the switches are used ($\bar{V}^2_{n,IN} = 6.2^2\ \mu V^2$) and the equivalent input-referred power noise without isolation switches (first term of the eq. (5) $= 3.87^2 \mu V^2$). The square-root of this result (~4.8 μVrms) shows a good agreement with its theorical value (~4.1 μVrms), using the thermal noise defined as $\bar{V}^2_{n,Rsw1} = 4kTR\Delta f$, where k is the Boltzman's constant, T = 300 K is the temperature, R = 11kΩ is the ON resistance of the switch and Δ f = 1MHz is the bandwidth.

In terms of acoustic pressure noise, the equivalent pressure noise spectral density, $P_{n,in}$, was obtained, through the output-referred integrated voltage noise and the reception sensitivity, giving 3.26 mPa/$\sqrt{}$Hz at 2.4 MHz. Finally, for a 2 mm of FC-70 thickness, a SNR of 17.3 dB is achieved, considering the measured rms output signal (2.4 mVpp/(2*$\sqrt{}$2) = 0.85 mVrms) and the output-referred integrated noise (116 μVrms). This value guarantees the minimal SNR (12 dB) for an accurate fingerprint image.

B. SYSTEM LEVEL COMPARISON WITH STATE-OF-ART

Table 3 summarizes the performance of the proposed full integrated systems (with and without switches), and compares them with the state-of-the-art. In order to compare with prior works, the noise-efficient factor (NEF' = $P^{*}_{n,in}\sqrt{}$Power), defined by [24], has been used as Figure-of-Merit. The presented PMUT-on-CMOS system without switches achieves a NEF' close to the lowest [7], and lower to the rest of the works (either based on CMUTs [8], [24], PMUTs [2] or based in PZT [10]) demonstrating the capabilities of the presented monolithically integrated PMUT-on-CMOS. In fact the reported system in [7] is able to detect 4.7 times smaller signals (assuming the same bandwidth, 1 MHz), but at the cost of consuming 16.3 times more power. From the table and comparing with PMUTs bonded to CMOS [2], our monolithical integrated PMUT-on-CMOS pulse-echo system presents competitive results in terms of better RX sensitivity, lower circuitry noise and lower power, which can be summarized in the much lower NEF' factor obtained with our system. The results show that if the system reported in [2] was able to obtain a fingerprint image, our proposal will be able to implement a fingerprint sensor with less fabrication complexity and cost (avoiding for instance the need of an

TABLE 3. System level comparison with the State-of-the-art.

	This Work		[7] (2020)	[10] (2018)	[24] (2016)	[2] (2016)	[8] (2011)
	w/o switch	With Switch					
Process	0.13 µm HV CMOS		0.18 µm BCDMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.18 µm HV CMOS	0.35 µm CMOS
Transducer	PMUT, AlN		CMUT	PZT	CMUT	PMUT, AlN	CMUT
Integration Method	Monolithic		Flip-chip	Direct Interconnection[2]	Flip-chip	Eutectic bonding	Monolithic
Acoustic medium	FC-70		Tissue phantom	Water	Vegetable oil	PDMS	Water
Transducer bandwidth [MHz]	1		N/A	6	N/A	4.67[4]	10
Max. TX Amplitude [V]	N/A	32	N/A	30	30	24	N/A
Overall RX Voltage-Voltage Gain [dB]	21.5	25.5	N/A	N/A	N/A	34 dB	N/A
Overall RX Transimpedance Gain [dBΩ]	119[9]	123[9]	106	108//119	104/116	N/A	130
Overall RX area [10^{-4} mm^2]	6		1200	N/A	600	N/A	98
RX Sensitivity IN (PMUT + LNA) [V/MPa]	1.9		N/A	4	N/A	0.344	N/A
RX Sensitivity OUT (PMUT + LNA) [V/MPa]	22.6	35.7	N/A	N/A	123	17.2[5]	130
Input referred voltage noise (LNA) [nV/√Hz]	3.87 @2.4 MHz	6.2 @2.4 MHz	N/A	N/A	N/A	21 @14 MHz	N/A
Input referred current noise (LNA) [fA/√Hz]	50.8 @2.4 MHz[10]	81.4 @2.4 MHz[10]	2000 @5 MHz	2000 @13 MHz	410 @5 MHz	N/A	90 @15 MHz
Input referred pressure noise ($P_{n,in}$) [mPa/√Hz]	2.04 @ 2.4 MHz	3.26 @ 2.4 MHz	0.43 @ 5 MHz[1]	1.9 @ 13 MHz[1]	2.3 @ 5 MHZ	61.88 @ 14 MHz[6]	3 @ 15 MHz
Power Consumption [mW]	0.3		4.9	0.42	1.4	1.86[7]	6.6
NEF' [mPa/√Hz *√mW]	1.12	1.79	0.96	1.23[3]	2.72	84.39[8]	7.71[8]

[1] Computed using the power consumption and NEF'.
[2] The bond pads on the ASIC provides electrical connections to the transducer elements [11].
[3] According with the reported value in [7].
[4] Computed using BW = f0/Q where Q is the Quality Factor in PDMS (Q ~ 3) and f0 is the resonance frequency (14 MHz).
[5] Considering the reception sensitivity at the LNA input (0.344 V/MPa) and the overall gain of the receiver chain (34 dB).
[6] Computed using the input voltage reference noise (46 µVrms), the estimated bandwidth (4.67 MHz) and the reception sensitivity at the LNA input (0.344 V/MPa).
[7] Including the overall receiver chain (computed using the consumed energy per column (2.4 µJ) and the full readout sequence per column (2.64 ms).
[8] Computed using NEF' = $P_{n,in}$*√Power where $P_{n,in}$ is the input referred noise (mPa/√Hz) and the LNA power consumption
[9] Computed using G_TIA[dBΩ] = G[dB]-20*log10(2*π*f0*(C_{INNER}+$C_{in,LNA}$)), where G[dB] is the Overall RX Voltage-Voltage Gain and f0 is the resonant frequency (2.4 MHz).
[10] Computed using $i_{n,IN}$ [A/√Hz] = $V_{n,IN}$*2*π*f0*(C_{INNER}+$C_{in,LNA}$), where $V_{n,IN}$ is the input referred voltage noise [V/√Hz].

eutectic bonding between piezoelectrical layer and CMOS integrated circuit, which increases complexity and decreases the achievable fill factor [2]). Comparing with the rest of the fabrication processes reported in Table 3, our system is based on the monolithic integration of the PMUT directly over the CMOS circuitry, only adding some post-processing

steps (including deposition of the AlN layer) similarly as is done for CMUT approaches [8]. This monolithical integration of the piezoelectric AlN material, does not require complex fabrication processes with the alignment of two different chips like needed in the flip-chip approach [7], [24] or special alignment and use of an interlayer conductive glue between PZT and the CMOS integrated circuit (as it is done in the direct interconnection process reported in [10], [11]). In consequence our monolithical PMUT-on-CMOS approach will result in more reliable and lower fabrication cost than the others.

IV. CONCLUSION

This article presents the characteristics and capabilities of fully monolithic PMUT transducers integrated on CMOS and fabricated with the MEMS-on-CMOS process from Silterra. The integration eliminates the signal degradation with the minimization of the parasitic capacitance in the interface PMUT-CMOS. In addition, the noise level of the implemented CMOS circuitry is minimized, achieving higher SNR levels with compactness and efficient power consumption. The ultrasound echo operation with a single PMUT-on-CMOS as a two-port device demonstrates the possibility to obtain the required SNR levels for imaging (17.3 dB) using low voltage switches on the reception side with very low power consumption (0.3 mW) allowing a power efficient echo ultrasound system. The monolithical integration and the optimal performance of the presented PMUT-on-CMOS system will allow to implement arrays with a wide range of PMUTs distribution for imaging application guaranteeing high fill factors, good SNR, small size and low power consumption for future all-integrated ultrasound imaging systems.

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IVÁN ZAMORA received the B.Sc. degree in telecommunication and electronic engineering from the Havana University of Technology José Antonio Echeverria, in 2014. He is currently pursuing the Ph.D. degree in electronics engineering with the Universitat Autònoma de Barcelona (UAB), Spain. His research interests include high-voltage electronics and low-power sensor interface CMOS circuits. He was a recipient of the PIF Scholarship, in 2017.

EYGLIS LEDESMA (Student Member, IEEE) received the B.Sc. degree in telecommunication and electronic engineering from the Havana University of Technology José Antonio Echeverria, in 2014. She is currently pursuing the Ph.D. degree in electronics engineering with the Universitat Autònoma de Barcelona (UAB), Spain. Her research interest includes piezoelectric MEMS devices for ultrasonic sensor applications.

ARANTXA URANGA was born in Burgos, Spain. She received the degrees in physics and electronics engineering from Valladolid University, Spain, in 1994 and 1996, respectively, and the Ph.D. degree in electronics engineering from the Universitat Autònoma de Barcelona, Spain, in 2001. Since 1996, she has been with the Department of Electronics Engineering, Universitat Autònoma de Barcelona, where she is currently an Associate Professor. Her research interests include the design and implementation of CMOS integrated circuitry intended to sense the movement of MEMS-NEMS resonators; the implementation of self-sustained oscillators based on MEMS, along with the study of the nonlinear behavior of MEMS NEMS and their application in the reduction of the oscillator phase noise; and the implementation of CMOS circuitry to excite and sense piezoelectric micromachined ultrasound transducers (PMUTs).

NÚRIA BARNIOL (Member, IEEE) received the Ph.D. degree in physics from the Universitat Autònoma de Barcelona (UAB), Spain, in 1992. She is currently a Full Professor with the Department of Electronics Engineering, UAB. She has been working for the last 20 years in the field of MEMS resonators and their integration within CMOS technologies focused on the reduction of dimensions towards nanoelectromechanical devices with optimized CMOS conditioning circuitry. She has coauthored more than 100 research articles and 200 peer-reviewed conferences. Her research interests include the study of novel piezoelectrical micro/nanometric ultrasonic transducers, their integration with CMOS toward efficient biometrics systems and exploitation of non-linear NEMS resonators. She has been on Program Committee of several conferences, including IEEE-IEDM, IEEE-MEMS, MNE, Transducers, and Eurosensors. She was a recipient of the Award of the Universitat Autónoma de Barcelona, for Research Excellence in the area of Technology, in 2009.