IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 8, 2020, accepted July 24, 2020, date of publication July 29, 2020, date of current version August 10, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3012699

A 5 GS/s 29 mW Interleaved SAR ADC With 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications

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This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFB1310000; in part by The Science and Technology Development Fund, Macau, under Grant SKL-AMSV(UM)-2020-2022(DP); and in part by the University of Macau under Grant MYRG2017-00192-FST and Grant MYRG2018-00204-AMSV.

ABSTRACT This article presents a 16-channel 5 GS/s time-interleaved (TI) SAR ADC for a direct-sampling receiver that employs a digital-mixing background timing mismatch calibration to compensate for timing-skew errors. It uses a first-order approximation to obtain the derivative of the autocorrelation of the input signal, subsequently used to evaluate the explicit amount of the timing-skew. Therefore, this allows a digital background calibration of the timing-skew, avoiding extra analog circuits. The proposed 16-channel TI ADC uses a splitting-combined monotonic DAC switching method for the individual SAR channel to achieve a trade-off of simple switching and small common-mode voltage variation of the comparator. The prototype, implemented in 28 nm CMOS, reaches a 48.5/47.8 dB SNDR with an input signal of 2.38/4.0 GHz after the proposed background timing mismatch calibration, respectively. Furthermore, the ADC core's power consumption is 29 mW sampling at 5 GS/s, with a Walden FoM of 26.7 fJ/conv.-step and a Schreier FoM of 157.9 dB.

INDEX TERMS Analog-to-digital converter (ADC), time-interleaved (TI) ADC, timing mismatch, digital background calibration, digital-mixing.

I. INTRODUCTION

The direct RF sampling receiver architecture is much simpler than the traditional IF sampling one. As shown in Fig. 1, it only consists of a low-noise amplifier (LNA), the appropriate filters, and the RF ADC. Unlike its IF version, the direct RF sampling receiver does not use the analog mixers and local oscillators (LOs). The ADC digitizes the RF signal directly and sends it to a DSP. However, direct sampling architecture cannot be practically implemented in the past ten years. The main limitation is the ultra-high requirements of the converter sample rates [1]. In nowadays broadband cable and satellite communications, the input spectrum ranges from tens of MHz to multi-GHz [2]. Therefore, a Nyquist rate converter in the GS/s range is required to sample the input signal in full bandwidth.

A time-interleaved (TI) ADC architecture is a power-efficient candidate for these wideband applications because it can increase the overall converter's effective sampling rate by multiplexing several ADC channels in parallel. The effective conversion rate (f_s) of an N-channel TI ADC becomes N times the rate of each sub-converter, as shown in Fig. 2. Nevertheless, the architecture suffers from inter-channel mismatches among the sub-ADC channels, which includes

The associate editor coordinating the review of this manuscript and approving it for publication was Venkata Rajesh Pamula.

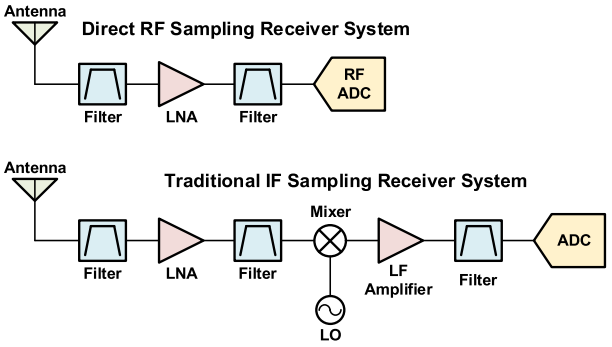

FIGURE 1. Direct RF sampling vs. traditional IF sampling.

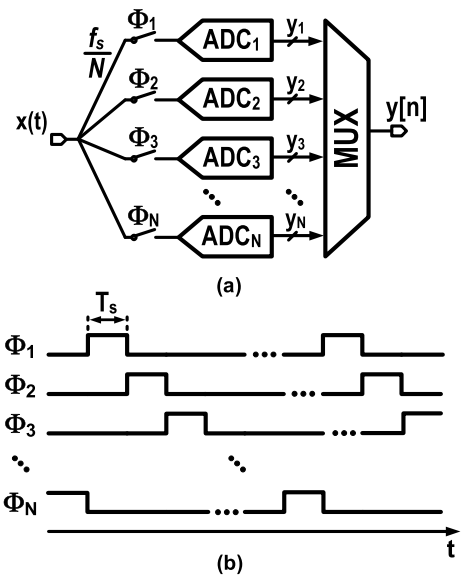

FIGURE 2. a) N-channel TI ADC, and (b) its clock phases.

offset, gain and timing mismatches [3]. Compared to the offset and gain mismatches, timing mismatch induces a dynamic error proportional to both input frequency and amplitude.

Compared to foreground calibration, the background calibration can actively track the supply and temperature changes without interrupting the normal operation although it has higher complexity. Adding a reference converter is an effective way to perform background calibration for timing mismatch [4]–[9]. However, the addition of this reference converter will bring additional area and power consumption.

Some recent works [3], [10]–[16] develop timing-skew mismatch calibration without the use of an additional reference channel. Some of them use digital-mixing based on the difference of the autocorrelation function between channels. [3], [11], and [13] estimate the polarity of the timing skew with fewer samples. [3] and [11] need a feedback loop from digital to analog for calibrating the timing-skew by tuning the delay line of individual sub-channel. In [13] they correct the timing mismatch error in the digital domain without a tunable delay line, but an auxiliary delta-sampling ADC is necessary to estimate the skew error.

This article presents a fully digital background timing-skew calibration without any additional analog circuits. Different from the previous works [3], [11] which only use digital-mixing to detect the polarity of the timing-skew, this method divides the derivative of the autocorrelation function of the input signal by the difference between channels' digital mixing [16]. Moreover, the article improves the accuracy over [16] with a more accurate bilateral estimation of the derivative of the autocorrelation function. We implement a 5 GS/s 16-channel TI-SAR ADC in 28 nm CMOS with a splitting-combined monotonic DAC switching method for a single-channel SAR ADC. After the proposed timing-skew calibration, the ADC obtains an SNDR of 48.5/47.8 dB with an input frequency of 2.38 /4.0 GHz, respectively. The ADC core consumes 29.0 mW (inter-channel mismatch calibration off-chip), while leading to a Walden FOM of 26.7 fJ/conv.-step and a Schreier FOM of 157.9 dB.

In addition to this introductory section, Section II describes the review for the timing-skew detection techniques in TI-ADCs with digital-mixing. Section III describes the proposed digital-mixing timing-skew calibration technique. Section IV demonstrates the circuit details of the 16-channel 5 GS/s TI-SAR ADC. Section V summarizes the measured performance, and Section VI concludes the article.

II. REVIEW OF TIMING-SKEW CALIBRATION WITH DIGITAL-MIXING

The following discussion of modeling of the TI ADC neglects the effect of quantization noise, as this permits us to fully investigate the effect of mismatches on the system. From Fig. 2, the input and output of the TI ADC are $x(t)$ and $y[n]$, respectively, and ideally $y[n] = x(nT_s)$, with T_s representing the sampling period. From [17], we can generally assume the input signal $x(t)$ is a wide-sense stationary (WSS) signal. For example, for a bandlimited signal with a white spectrum in the 1st Nyquist band, the autocorrelation follows a *sinc* function, as depicted in Fig. 3. Therefore, the autocorrelation function of the input signal $R(\tau) = E[x_k(t)x_k(t+\tau)]$ is independent of the time t.

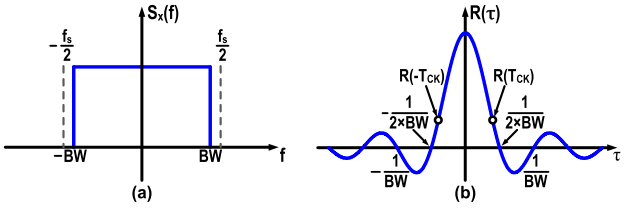

FIGURE 3. The waveform of (a) a low-pass wide-band random signal and (b) the autocorrelation function of this signal.

We first describe the timing mismatch analysis for a two-channel TI ADC. From Fig. 4, ADC_1 samples the input $x(t)$ at Φ_1 with the digital output of y_1(odd sample) and ADC_2 samples at Φ_2 with y_2 (even sample), with Φ_2 skewed from the ideal value by ΔT. This indicates a time difference between samples $y_1[k-1]$ and $y_2[k-1]$ of $2\Delta T$ seconds

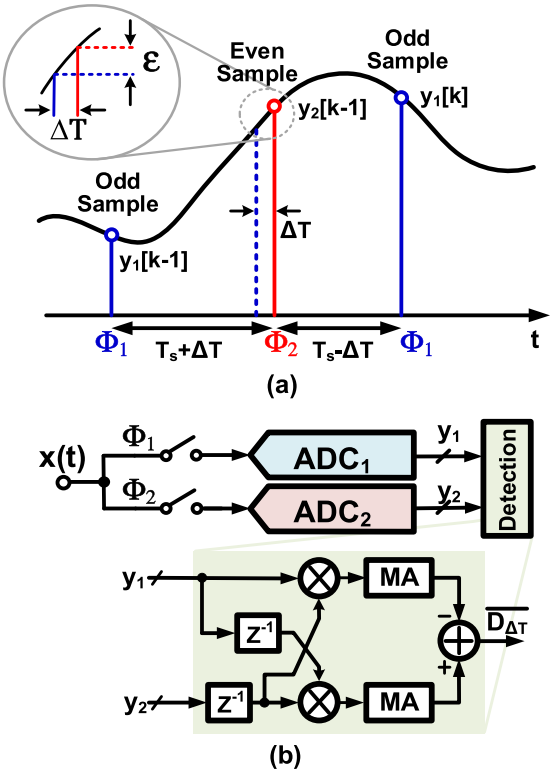

FIGURE 4. (a) TI-ADC sampling to illustrate the effect of the timing mismatch for two-channel TI ADC, and (b) the timing-skew detection topology based on digital-mixing.

larger than that between $y_2[k-1]$ and $y_1[k]$, as illustrated in Fig. 4(a).

The digital mixing technique evaluates both of the autocorrelation functions [3], one from the moving average (MA) of the product of $y_1[k-1]$ and $y_2[k-1]$ and the other from $y_2[k-1]$ and $y_1[k]$, as shown in Fig. 4(b), and expressed by:

$$R(T_s+\Delta T) = \frac{1}{n}\sum_{k=1}^{n} y_1[k-1]\,y_2[k-1] \quad (1)$$

$$R(T_s-\Delta T) = \frac{1}{n}\sum_{k=1}^{n} y_1[k]\,y_2[k-1] \quad (2)$$

Therefore, for a small value of timing-skew ΔT, we derive the difference between (1) and (2) as follows [3], [11]:

$$\begin{aligned}\overline{D_{\Delta T}} &= R(T_s+\Delta T) - R(T_s-\Delta T)\\ &\approx 2\Delta T\cdot\frac{dR(\tau)}{d\tau}|_{\tau=T_s}\end{aligned} \quad (3)$$

Thus, the evaluated timing-skew information $\overline{D_{\Delta T}}$ is proportional to the timing-skew ΔT and to the derivative of its autocorrelation function $R(\tau)$ at $\tau = T_s$.

With the information of the polarity for timing-skew ΔT in (3), [3] and [11] use a tunable delay line in the sampling clock generator to adjust earlier or later the sampling clocks until the value of $\overline{D_{\Delta T}}$ is negligible. The tunable delay line will increase the jitter noise of the sampling clock. In [13] the circuit presents a digital correction to eliminate the timing-skew error by adding extra auxiliary channels, also based on the above detection topology. Both approaches need modification/addition of analog circuits. In this article, we demonstrate a digital calibration method that avoids extra analog circuits.

III. DIGITAL TIMING-SKEW CALIBRATION USING DIGITAL-MIXING

The timing-skew in each sub-converter can induce a dynamic error, depending on both the amplitude and frequency of the input signal. As shown in Fig. 4(a), when we choose ADC_1 as the reference, the timing-skew ΔT of ADC_2 produces a skew-induced sampling error ε. Without the loss of generality, we assume the timing-skew ΔT to be much smaller than the sampling period T_s. Thus, for the input signal $x(t)$, the ideal (or calibrated) samples $y_{2,cal}$ can be approximated by a 1st-order Taylor series as:

$$y_{2,cal}[k] \approx y_2[k] - y_2'[k]\cdot\Delta T \quad (4)$$

where $y_2'[k]$ is the first-order derivative of even samples, which can be obtained by a derivative filter.

As expressed in (4), the skew-induced error correction assumes only first-order sampling errors, and we do not take into consideration the higher-order Taylor series terms. Moreover, the accuracy of the correction will decrease when the timing-skew becomes large. Fig. 5 plots the behavior study of a 16-channel TI ADC before and after the ideal linear approximation correction. The plot depicts the trends of SNDR with the input frequency of $f_{in} = 0.95 \times 0.5f_s$ versus the timing mismatch ratio (RMS value). From these curves, the accuracy of the digital correction degrades with the increase of the timing mismatch level. To guarantee excellent performance at high frequency, we use a retiming technique in the multi-phase clock generator to reduce both initial values of timing-skew and clock jitter (discussed in detail in the next section).

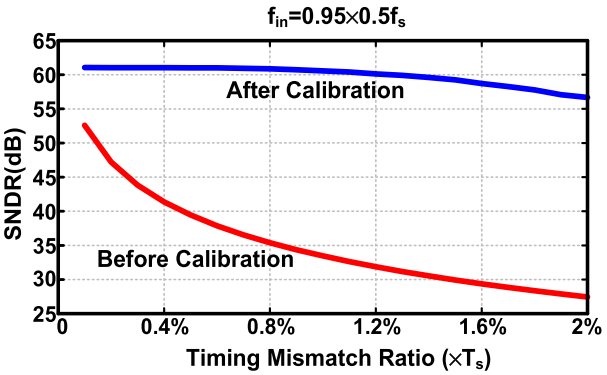

FIGURE 5. The SNDR of a 16 channel 10 bit ADC before and after an ideal linear approximation correction versus the timing-mismatch ratio.

This section presents the proposed fully digital timing mismatch calibration method. First, we use a two-channel TI ADC as an example to explain the basic principle and calibration algorithm. Furthermore, different from [16], here

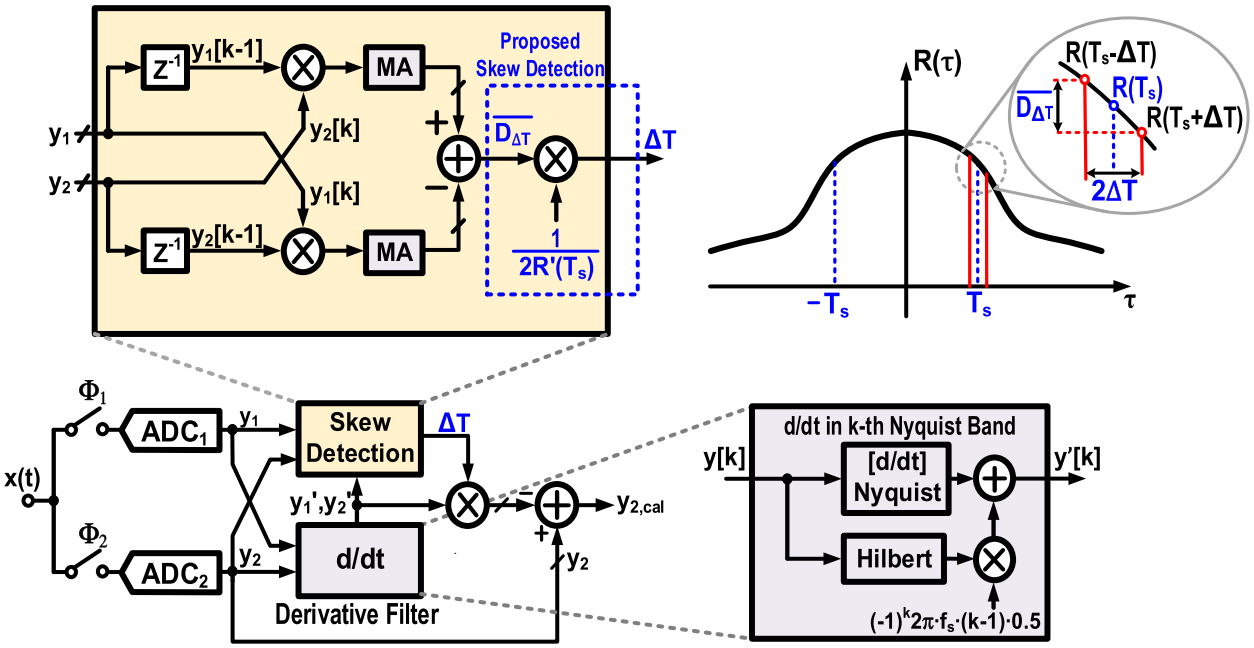

FIGURE 6. Proposed fully digital timing mismatch topology based on digital-mixing.

we use a bilateral linear approximation to obtain a more accurate derivative of the autocorrelation to improve the mismatch correction.

A. FORMULATION OF THE PROPOSED FULLY DIGITAL TIMING-SKEW CALIBRATION

Fig. 6 exhibits the principle of the proposed background calibration technique for timing mismatch. We use a digital differentiator to obtain $y_2'[k]$, and with a Hilbert transform filter, the derivative of the input at around 90% frequency range (0.05–0.95) can be obtained within any Nyquist band [15]. Then, from (3), the amount of the timing-skew ΔT can be calculated by

$$\Delta T \approx \frac{\overline{D_{\Delta T}}}{2 \cdot \frac{dR(\tau)}{d\tau}|_{\tau=T_s}} \tag{5}$$

The derivative of the autocorrelation function should be [11]:

$$\begin{aligned} \frac{dR(\tau)}{d\tau}|_{\tau=T_s} &= \frac{dE[y(t) \cdot y(t+\tau)]}{d\tau}|_{\tau=T_s} \\ &= E\left[y(t) \cdot \frac{dy(t+\tau)}{d\tau}|_{\tau=T_s}\right] \end{aligned} \tag{6}$$

In previous work [16], we use the moving average of the product of $y_1[k-1]$ and $y_2'[k-1]$ to approximate $\frac{dR(\tau)}{d\tau}|_{\tau=T_s}$:

$$\frac{dR(\tau)}{d\tau}|_{\tau=T_s} \approx \frac{1}{n}\sum_{k=1}^{n} y_1[k-1]\, y_2'[k-1] = \frac{dR(\tau)}{d\tau}|_{\tau=T_s+\Delta T} \tag{7}$$

However, due to the existence of timing-skew ΔT, the terms on the right-hand side of (7) are not an accurate value of $\frac{dR(\tau)}{d\tau}|_{\tau=T_s}$, but instead it is $\frac{dR(\tau)}{d\tau}|_{\tau=T_s+\Delta T}$. This induces an approximation error in our previous estimation of $\frac{dR(\tau)}{d\tau}|_{\tau=T_s}$ presented in [16].

Alternatively, for the small value of ΔT, the first-order derivative of the autocorrelation function at $\tau = T_s$ can be a bilateral approximation:

$$\frac{dR(\tau)}{d\tau}|_{\tau=T_s} = \frac{1}{2}\left[\frac{dR(\tau)}{d\tau}|_{\tau=T_s+\Delta T} + \frac{dR(\tau)}{d\tau}|_{\tau=T_s-\Delta T}\right] \tag{8}$$

By taking the moving averages for the product of $y_1[k-1]$ to $y_2'[k-1]$ and the other from $y_2[k-1]$ to $y_1'[k]$, as shown in Fig. 7, $\frac{dR(\tau)}{d\tau}|_{\tau=T_s+\Delta T}$ and $\frac{dR(\tau)}{d\tau}|_{\tau=T_s-\Delta T}$ can be obtained:

$$\begin{aligned} \frac{dR(\tau)}{d\tau}|_{\tau=T_s+\Delta T} &= R'(T_s+\Delta T) \\ &= \frac{1}{n}\sum_{k=1}^{n}\left(y_1[k-1]\, y_2'[k-1]\right) \end{aligned} \tag{9}$$

$$\begin{aligned} \frac{dR(\tau)}{d\tau}|_{\tau=T_s-\Delta T} &= R'(T_s-\Delta T) \\ &= \frac{1}{n}\sum_{k=1}^{n}\left(y_2[k-1]\, y_1'[k]\right) \end{aligned} \tag{10}$$

Then, by averaging (9) and (10), we determine the $dR/d\tau$ at $\tau = T_S$ as presented in Fig. 7, with the estimated amount of the timing-skew ΔT evaluated by (5) (as in Fig. 6).

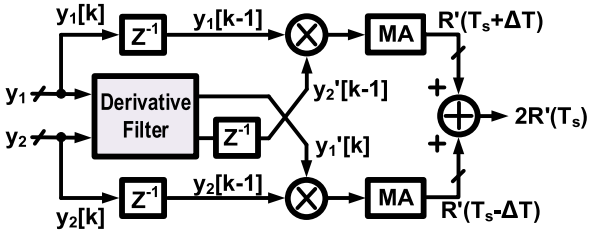

FIGURE 7. Proposed block diagram to obtain the first-order derivative of the autocorrelation function based on digital-mixing.

B. SIMULATION RESULTS

Fig. 8 illustrates the comparison of the SNDR vs. the input frequency after timing mismatch digital correction by two different detection methods ((a) used in [16] and (b) proposed here). We use the same 25 tap differentiation filter for a two-channel TI ADC during the comparison with an injected timing-skew of $0.5\% \times T_s$. When compared with the previous method [16], the new approximation for $\frac{dR(\tau)}{d\tau}|_{\tau=T_s}$ has an obvious advantage when the input is near Nyquist frequencies. It demonstrates that the decrease of SNDR after calibration with the detection method in [16] happens at the frequencies near $m \times 0.5f_s$. This happens because we implement the differentiation filter using a finite number of taps (Fig. 6) which limits the accuracy of the filter's frequency response near $m \times 0.5f_s$ [15]. Moreover, the inaccuracy of the predicted derivative of the input will also affect the required number of convergence samples during the detection of the timing-skew [15].

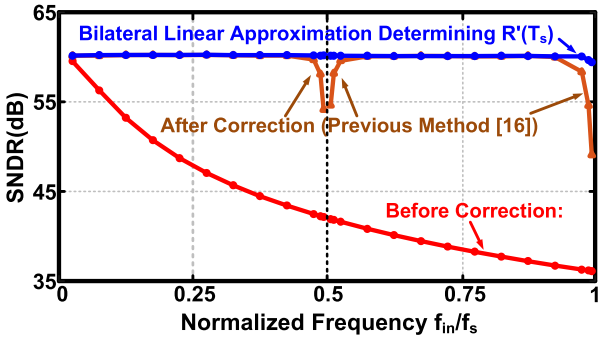

FIGURE 8. The SNDR of two channel TI ADC before and after correction (with two different method) as a function of input frequency.

Fig. 9 (a) and (b) shows the simulated ADC spectrum of a wide-band random signal before and after performing the proposed timing mismatch calibration. We did not observe any image pattern of the skew after the proposed calibration.

C. EXTENSION TO MULTIPLE CHANNELS

We now extend the above concepts to additional channels (16 channels chosen as an example). To this end, we define the sampling times of the first channel as the reference [13] (highlighted in Fig. 10). We then compute the timing of channels 2, 3, …, 13, 14 and 15 with respect to channel 1, which can be divided into four steps. First, we can detect and correct the mismatch between channels 9 and 1 by evaluating $\overline{D_{\Delta T9}}$ and $R'(8T_s)$. Second, we can correct the timing skews in channels 5 and 13 by $\overline{D_{\Delta T5,13}}$ and $R'(4T_s)$, relying on the corrected channel 9 as reference. The 3rd and 4th steps continue in a similar way until all the channels are calibrated.

IV. ADC IMPLEMENTATION

A. ADC ARCHITECTURE

Fig. 11 presents the 5 GS/s TI ADC prototype consisting of 16-channel time-interleaved 312.5 MS/s SAR sub-ADCs. The inter-channel mismatch, including offset, gain, and timing-skew, are all calibrated in the digital domain in the background off-chip. Besides, we use a bilateral digital-mixing background timing-skew calibration, as discussed previously. With this method, extra analog circuits

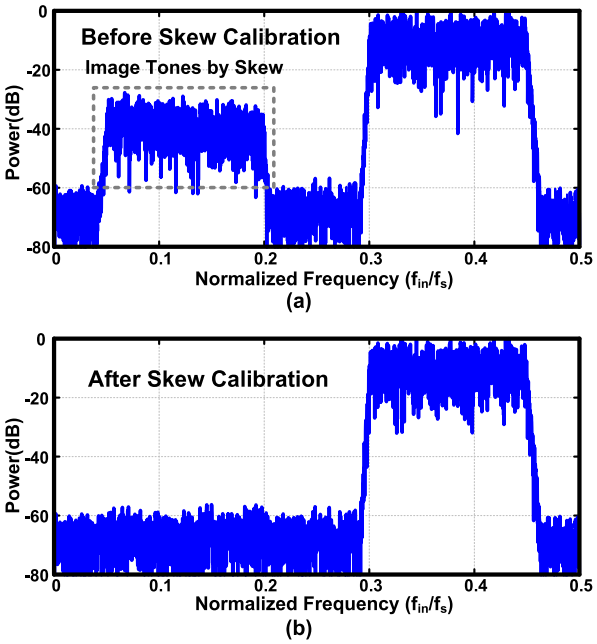

FIGURE 9. The simulated two channel TI ADC output spectrum (a) before and (b) after timing-skew calibration for a randomized input.

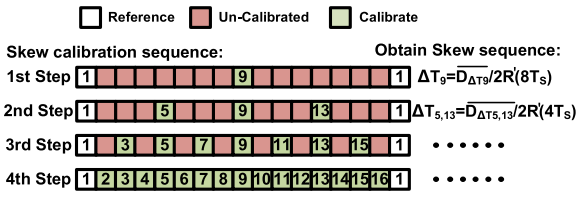

FIGURE 10. The sequence of calibration in a 16-channel TI ADC.

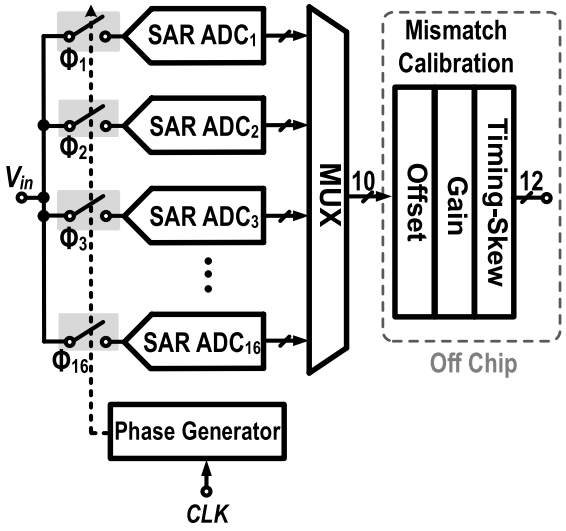

FIGURE 11. ADC Architecture.

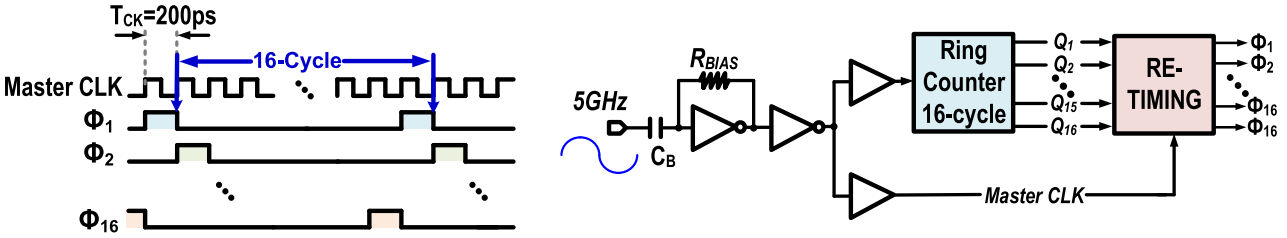

FIGURE 12. The timing diagram of the sampling for each sub-converter and block diagram of the clock generator.

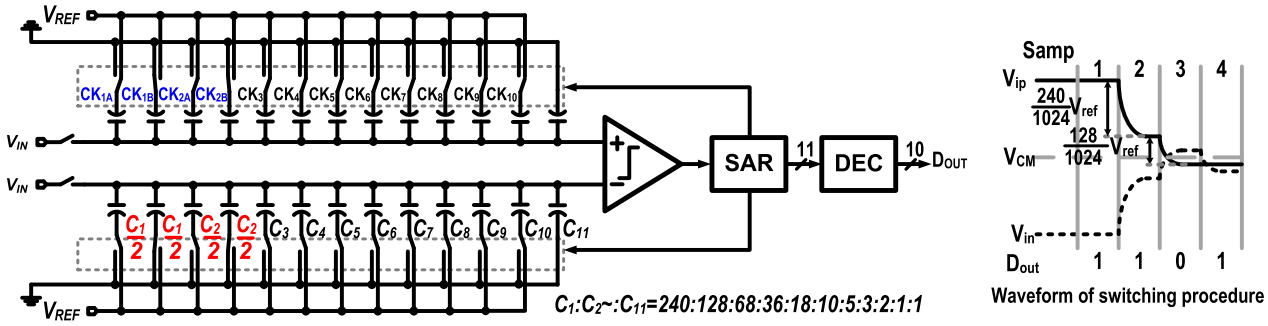

FIGURE 13. The block diagram of the single-channel ADC.

are not necessary (Fig. 11). From the measurements, 16 k samples are enough to achieve a good SNDR for the timing-skew calibration.

The 16-channel interleaved ADC needs sixteen clock phases with 6.25% duty cycle. Fig. 12 displays the clock generator with a master clock of 5 GHz, divided by the 16-cycle ring counter, produces the outputs Q_1-Q_{16}. The ring counter is constructed with D-type Flip-Flops (DFFs) forming a shift register. This can be considered as a cascade of logic gates, which accumulate a substantial amount of jitter. We reuse the master clock to retime Q_1-Q_{16} from the ring counter to impose that the falling edges of the final sample clock Φ_1-Φ_{16} depend only on the rising edges of the master clock [15]. Besides, to ensure an equal distance to each channel, we also use an H-tree routing paths for input signals and clocks in the layout. Benefitting from the combination of the retiming technique and the H-tree routing, we not only reduce the jitter produced by clock-division but also guarantee that the initial un-calibrated timing-skew of each channel is small enough.

B. SINGLE-CHANNEL SAR ADC

For the sub-channel implementation, the V_{CM}-based switching procedure [18] has an excellent power efficiency. However, the low power supply of the advanced process turns this structure not attractive in high-speed applications. The multi-bit per cycle SAR ADC [19], [20] is suitable for such applications, but this topology needs complex DAC and control logic. The capacitor DAC splitting structure is a popular choice for the high-speed SAR ADC [2], [13]. Still, this architecture imposes that both switches and the SAR decision logic have higher complexity than the solely monotonic switching structure [21]. In this work, we use the single-channel ADC with a splitting-combined monotonic switching method [22]. Fig. 13 shows the circuit diagram of the single-channel converter. Each SAR channel includes a two-stage dynamic comparator, bootstrap switches, custom DAC capacitor arrays, SAR decision logic, and digital error correction (DEC) to convert non-binary data to binary [23]. The ADC samples the input signal on the top plates of the capacitor arrays, determining the first MSB by the signal polarity on the top plates before the DAC conversion. As a result, the 10 bit ADC requires 2^9 capacitor DAC only. One extra redundant bit cycle is added to address the DAC settling issue in high-speed conversion [23]. Therefore, the 2^9 capacitor cells arrange into ten capacitor groups C_1-C_{10} with binary-scaled recombination as shown in Fig. 13.

Unlike [22], there are only two MSB DAC capacitors split into two halves, as Fig. 14 displays, thus the variation of the comparator input common-mode voltage (V_{CM}) is reduced from 0.5 V to 0.14 V (∼72% reduction), compared with the solely monotonic switching. The nine remaining LSBs are still in the traditional monotonic switching method. As a result, the splitting-combined monotonic switching method not only preserves the benefit of relatively-simple switches and SAR decision logic, like solely monotonic method, but also largely alleviates the variation of common-mode voltage that may lead to the dynamic offset of the comparator. Fig. 14 demonstrates a plot of the common-mode voltage (V_{CM}) vs. the RMS value of the offset (σ_{Offset}) for the comparator from 200 times Monte Carlo simulations. The V_{CM}-dependent variation of σ_{Offset} reduces from a solely

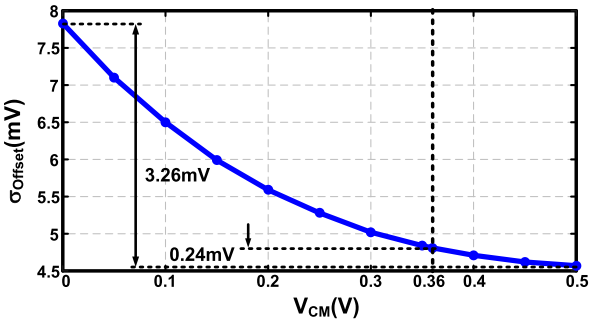

FIGURE 14. The simulated comparator offset versus common mode voltage.

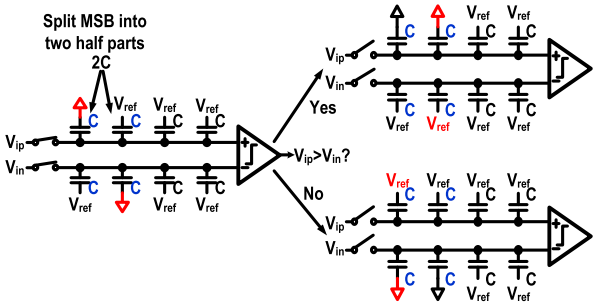

FIGURE 15. Conversion of splitting combined monotonic switching procedure for an example 3-bit ADC.

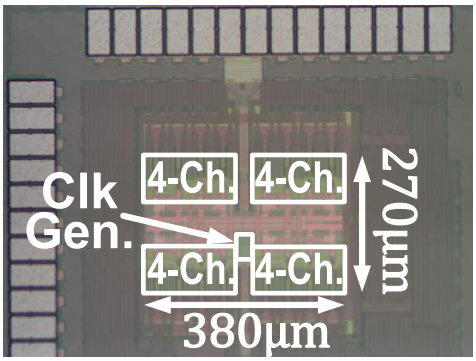

FIGURE 16. Chip micrograph.

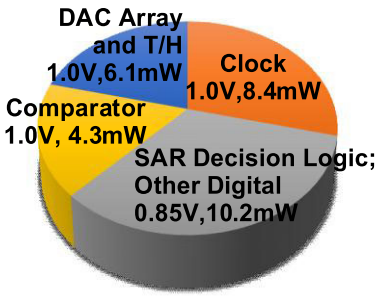

FIGURE 17. Power breakdown.

monotonic switching of around 3.26 mV (0.5V V_{CM} variation) to the splitting-combined monotonic values of 0.24 mV (0.14V V_{CM} variation) now. Fig. 15 illustrates an example of the conversion of a split-combined monotonic switching procedure for a 3 bit ADC, with only MSB divided into two halves.

V. EXPERIMENTAL RESULTS

The proposed 16-channel TI ADC is fabricated in a 28 nm CMOS with a core area of 380 × 270 μm^2 (Fig. 16). The DVDD digital supply, including the SAR logic and other control digital circuits, is 0.85 V. On the other hand, the AVDD analog supply, like comparators, track and hold (T&H) circuits, capacitor DAC switches, and the clock division circuit are 1.0 V for high sampling linearity and low-jitter noise. The total power consumption of the ADC core is 29mW (T&H and DAC array 21%, comparator 15%, SAR decision logic and other digital 35%, and clock generator 29%), as summarized in Fig. 17. The reference of the ADC are driven from AVDD, as no reference buffer is required. The inter-channel mismatch calibration algorithm is off-chip. The estimated number of gates for the proposed calibration algorithm are around 170 k. The estimated power consumption for the algorithm is 12.8 mW (DVDD = 0.85 V) and an estimated area of 0.11 mm^2. The measurement test-branch for the proposed TI ADC prototype is shown in Fig. 18.

Fig. 19 plots the measured output spectrum over the Nyquist rate with an input of 2.86 GHz before and after timing mismatch calibration. The 2.86 GHz input is over

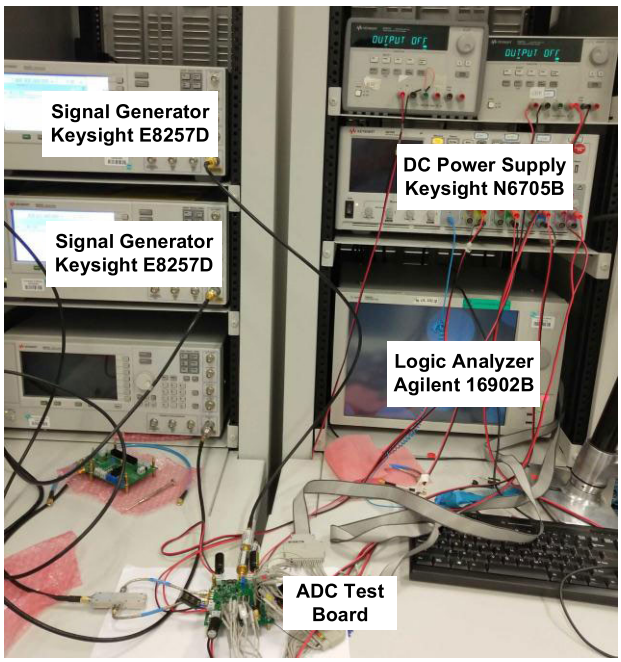

FIGURE 18. The measurement test-branch for the proposed TI ADC prototype.

the Nyquist rate, thus the measurement includes the effectiveness of the Hilbert Transform Filter of the differentiator [15]. From Fig. 19(b), the highest image tone generated by timing-mismatch improves from −69.7 dB with our previous

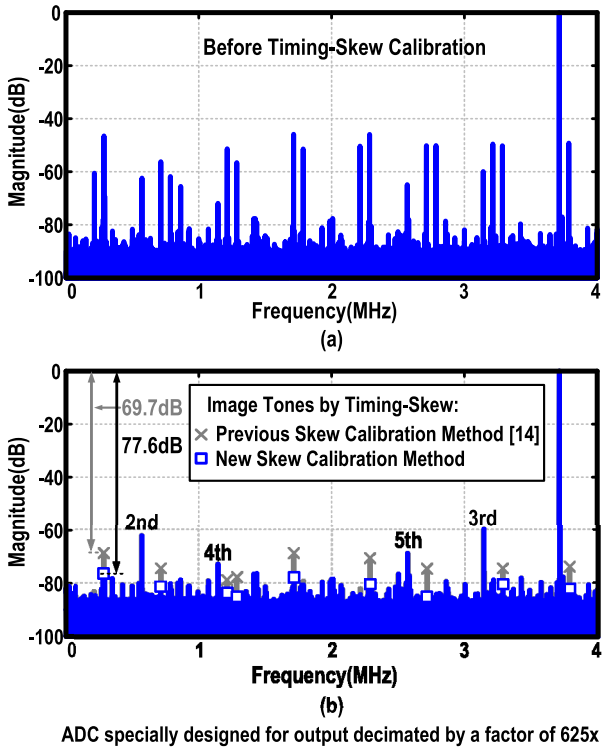

FIGURE 19. Measured output spectrum with an input frequency of 2.86 GHz (a) before and (b) after timing-skew calibration.

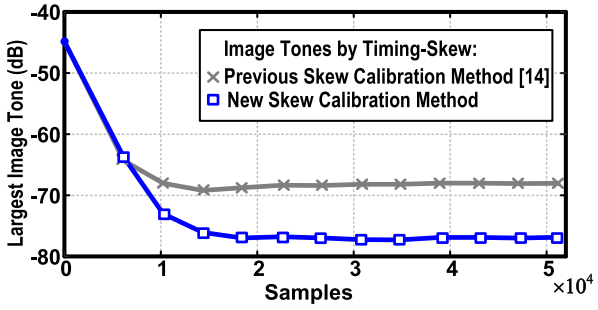

FIGURE 20. The measured largest image tone after timing-skew calibration with an input of 2.86 GHz versus the number of samples.

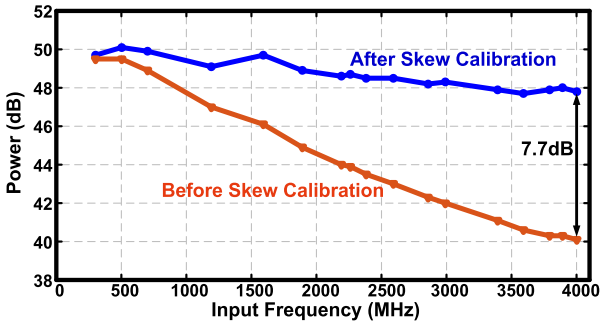

FIGURE 21. The measured SNDR versus input frequency before and after timing-skew calibration.

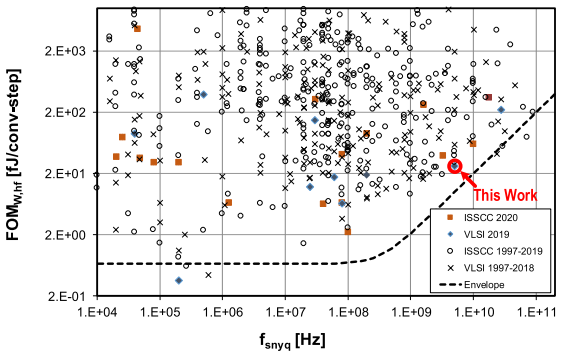

FIGURE 22. Compared to state-of-the-art for the Walden FOM [27].

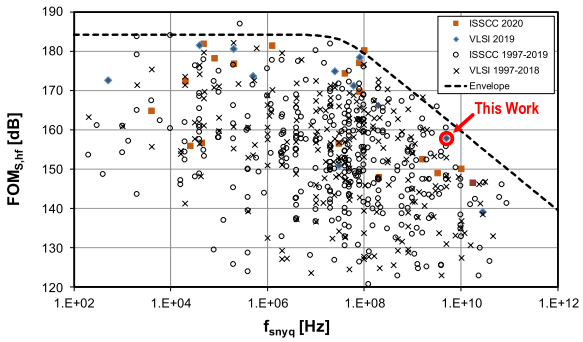

FIGURE 23. Compared to state-of-the-art for the Schreier FOM [27].

method [16] to −77.6 dB with the new, as discussed in Section V.

Fig. 20 shows the measured largest image tone by timing-skew with a 2.86 GHz input at 5 GS/s versus the number of timing-skew detection samples. Both the new method and the previous one [16] only need about 16 k samples convergence to achieve satisfactory dynamic performance. Compared to the method in [16], the new skew calibration method has a significant improvement in the largest image tone when the samples over 10 k.

Fig. 21 displays the SNDR vs. the input frequency at 5 GS/s. The SNDR peaks at 50.3 dB at the low input frequency. Benefiting from the proposed timing-skew calibration and retiming techniques, the SNDR only drop 1.8 dB and 2.5 dB at the frequency near the Nyquist rate and the frequency of 4 GHz, respectively. Therefore, thermal noise and distortion of the sampling switch are the main limiting factors for dynamic performance.

Table 1 illustrates the performance summary and a comparison with several state-of-the-art TI ADCs. These works include the recently published 10 bit TI ADC with similar sampling rates. The total power consumption of the ADC presented in this article achieves 48.5 dB SNDR near the Nyquist rate at 5 GS/s and only consumes 29 mW, with a Walden FOM of 26.7 fJ/conv.-step and a Schreier FOM of 157.9 dB. It makes this ADC having competitive power efficiency in the comparison.

Fig. 22, and Fig. 23 compares this ADC with all works published at ISSCC 1997-2020 and VLSI 1997-2019 [27]

TABLE 1. Table of comparison with state-of-the-arts.

	This Work		JSSC-15[2] M. Brandolini	TCASI-17[24] J. Fang	ISSCC-17[25] J. P. Keane	JSSC-18[13] C. Lin		JSSC-20[26] M. Baert
Architecture	TI-SAR		TI-Pipe-SAR	TI-SAR	TI-SAR	TI-SAR		TI-VCO
Technology	28nm		28nm	28nm	28nm FDSOI	40nm		28nm
Supply(V)	1.0/0.85		1.8/1.0	1.0	1.9/1.1/0.9	1.1		1.0/0.85
Resolution(bit)	10		10	10	10	10		10
Speed(GS/s)	5.0		5.0	5.0	8.0	2.6		5.0
Skew Correction	Digital		Analog	Analog	Analog	Digital		Analog
SFDR@Nyq.(dB)	59.6		58	54.4	60.3	57.8		57.1
SNDR@Nyq.(dB)	48.5		46.1	41.7	49.0	50.6		45.2
SNDR>Nyq.(dB)	47.8@4GHz		N/A	N/A	N/A	N/A		N/A
Power(mw)	29.0	41.8(1)	150	76	300	18.4	39.2(1)	22.7
Area(mm^2)	0.103	0.21(1)	0.45	0.57	0.184	0.825	0.92(1)	0.023
FOM_W@Nyq.(fJ/c.-Step)	26.7	38.5(1)	192.5	165	162.9	25.6	54.5(1)	30.5
FOM_W@Nyq.(dB)	157.9	156.3(1)	148.1	147.2	150.2	159.1	155.8(1)	155.6

(1) With estimated mismatch calibration power and area.

with the Nyquist sampling rate (equal to the sampling rate (f_s) divided by the oversampling ratio (OSR)), vs. the Walden FoM and Schreier FoM at high frequency, respectively. Both two figures demonstrating this work have competitive positions in the state-of-the-art high-speed ADC.

VI. CONCLUSION

This article presented a digital background timing-skew calibration for a TI ADC based on digital-mixing. With such method we can correct the timing mismatch of the TI ADC without additional analog circuits. Besides, there is no clock jitter noise from the supplementary tuning circuits. Moreover, we use the bilateral linear approximation to obtain the accurate derivative of the autocorrelation to enhance further the timing-skew mismatch detection. A prototype 16-channel 5 GS/s time-interleaved SAR ADC with a splitting-combined monotonic switching method, implemented in 28 nm CMOS, obtained a SNDR of 48.5 dB/ 47.8dB at 2.38 GHz/ 4.00 GHz, respectively.

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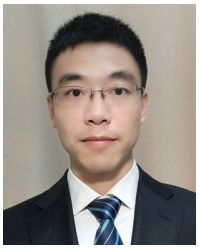

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