IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 18, 2020, accepted July 22, 2020, date of publication July 28, 2020, date of current version August 7, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3012467

Architectural Advancement of Digital Low-Dropout Regulators

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This work was supported in part by the NRF grant through the Korea government (MSIP and MSIT) under Grant NRF-2020R1I1A3073683 and in part by the Ministry of Science and ICT (MSIT), Korea, under the Information Technology Research Centre (ITRC) support program supervised by the IITPM under Grant IITP-2020-2018-0-01433.

ABSTRACT Digital Low-dropout (DLDO) regulators have been widely utilised for highly-efficient fine-grained power delivery and management in system-on-chips (SoCs) due to their process scalability, ease of integration, and low-voltage operation. However, conventional DLDOs suffer gravely from the power-speed tradeoff, which arises from the use of sampling clocks. To obtain reasonable performance in the undershoot and recovery during load transient states, a large output capacitor is inevitably required in these DLDOs. Moreover, they inherently involve large steady-state voltage ripples and poor power-supply rejection (PSR). These limitations of synchronous DLDOs and their counter measures are thoroughly discussed in this paper. Various design strategies of major building blocks, *i.e.* comparators and power transistor arrays, are explained in detail with examples. Architectural advances are also expounded including state-of-the-art DLDO architectures such as clock-boosted synchronous, analog-assisted synchronous, asynchornous, event-driven, and hybrid DLDOs. These state-of-the-art DLDOs do not only address the power-speed tradeoff and achieve fast load transient responses, but also can eliminate the use of an output capacitor in some cases. Moreover, some hybrid DLDOs successfully removed the steady state ripples and achieve high PSR. All of these DLDO are compared on basis of their performance metrics and figure-of-merits (FOMs).

INDEX TERMS Low-dropout regulator, digital LDO, event-driven LDO, hybrid LDO, asynchronous LDO, output capacitor-less, voltage ripples, power-supply rejection.

I. INTRODUCTION

Low-Dropout (LDO) Regulators have been extensively used to achieve fine-grained power delivery and power management in system-on-chip (SoC) platforms having multiple voltage domains and various load circuits [1]–[5]. Their power delivery networks commonly have hierarchical structures as shown in Fig. 1, where power-efficient switching-mode (DC-DC) regulators serve as pre-regulator and multiple LDOs integrated at point-of-load locations serve as post-regulators to provide dynamic scaling of voltages and currents to various load circuits [6], [7]. In SoCs, LDOs are easier to integrate in large numbers than switching-mode DC-DC regulators because of their small size and less number of required off-chip components.

The associate editor coordinating the review of this manuscript and approving it for publication was Yong Chen.

Conventionally, the predominant choice of post-regulators were analog LDOs due to their fast transient response, low quiescent current (I_Q), large unity-gain bandwidth (UGF) and high power-supply rejection (PSR). In addition, analog LDOs require only one integrated output capacitor (C_{OUT}) in most cases. As CMOS technologies and their supply voltage levels (V_{DD}) are downscaled, however, the performance of analog LDOs has degraded severely due to their insufficient gain of error-amplifiers under low-voltage levels.

To address this major challenge, digital designs of LDOs have been investigated extensively because digital LDOs (DLDOs) typically can achieve better performances under low voltage conditions like near-threshold voltage (NTV) levels. In addition, DLDOs do not involve stringent requirements of stability and compensation like analog LDOs, and they are much more process-scalable because most parts of DLDOs can be designed using standard

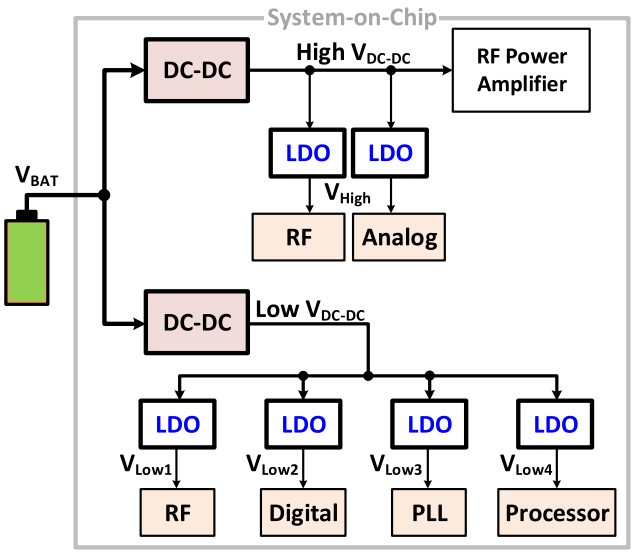

FIGURE 1. Fine-grained power delivery network of a system-on-chip.

cells. Due to these advantages, DLDOs have been commercially adopted in various SoCs already. For example, IBM in their 22-nm POWER8 processor [1] and AMD in their 14-nm RYZEN processor [5] integrated distributed DLDOs to achieve highly efficient fine-grained power management low supply voltages.

Even with substantial research and development so far, however, DLDOs have been hitherto considered as an inferior alternative of analog LDOs. One of the main reasons is that synchronous DLDOs require power-hungry clocking to obtain comparable performance. Moreover, DLDOs are typically inferior in steady-state voltage ripples (V_{RIPP}) and power-supply rejection (PSR).

To address these challenges, various DLDO architectures and techniques have been proposed to date. These architectures and techniques are discussed comprehensively in this review. To the author's best knowledge, this is the only report so far that thoroughly reviews design challenges and advancements in the field of DLDOs. The remainder of this paper is organized as follows. In the next section, operation principles and limitations of analog LDOs are reviewed along with general performance indicators of LDOs. Section III describes structure and operation principles of the first-proposed synchronous DLDO, and their four major limitations are discussed in Section IV. In Section V, design strategies of two major building blocks of DLDOs, *i.e.*, comparator and power transistor, are discussed. Section VI presents state-of-the-art DLDO architectures with comparisons of their advantages and disadvantages in Section VII, followed by conclusions and future research directions of DLDOs in Section VIII.

II. ANALOG LDOs

Analog LDOs have been widely used as supply voltage regulators in various SoCs and electronic devices [8], [9]. Work on a general-purpose LDO can be traced back to the generation using sub-5V voltage levels in early 1990s [10]. Later on, fully-integrated analog LDO designs were proposed to achieve on-chip power management [8], [11], [12]. Many of the fully integrated analog LDOs can offer fast load-transient response, high PSR, large bandwidth [13]–[15] with low I_Q [16], [17] and/or small-sized integrated output capacitor (C_{OUT}) [18]–[20].

A. LDO PERFORMANCE INDICATORS

LDOs always down-convert the supply voltage (V_{DD}) to a regulated output voltage (V_{REG}) using active devices. PMOS is typically used as this active device to attain a minimum dropout voltage (V_{DO}), which is the voltage difference between V_{DD} and V_{REG}. Fig. 2 shows a schematic of the classic analog LDO. It typically consists of an error amplifier, a power transistor, and a resistive divider. The reference voltage (V_{REF}) is usually supplied from a bandgap reference circuit, which is integrated on chip. The error amplifier controls the gate voltage (V_G) of the power transistor through the negative feedback that is created by connecting the output of resistive divider to the other input of the error amplifier. The PMOS is typically in the saturation region while controlling the PMOS current (I_{PMOS}), which is delivered to the load current (I_{LOAD}). The LDO tries to match the I_{PMOS} with I_{LOAD}, thus performing voltage regulation in V_{REG}. When $V_{REG} < V_{REF}$, the LDO decreases V_G to increase V_{REG}. Similarly, V_G is increased when $V_{REG} > V_{REF}$. The accuracy and bandwidth of this regulation is dictated by the open-loop gain and the dominant pole in the feedback loop [8], [21]–[23].

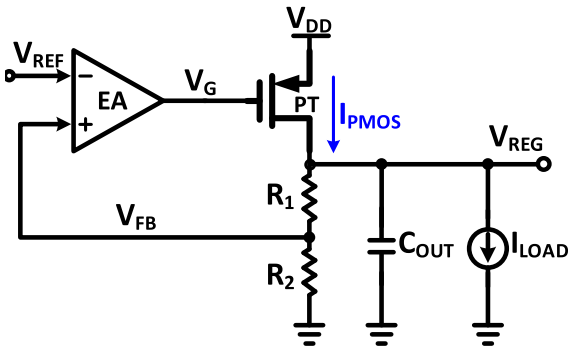

FIGURE 2. A classic analog LDO.

To evaluate the performance of LDOs, several performance indicators are widely used [24]. First, the dropout voltage (V_{DO}) is the voltage difference between the input V_{DD} and output V_{REG} at which the LDO ceases to regulate further against V_{DD}. A smaller V_{DO} is highly desirable because of its strong relationship to the overall power efficiency of LDO. Its power efficiency is given as follows:

$$\text{Power Efficiency} = \frac{I_{LOAD}}{I_{LOAD} + I_Q} \times \frac{V_{REG}}{V_{DD}} = \frac{I_{LOAD}}{I_{LOAD} + I_Q} \times \left(1 - \frac{V_{DO}}{V_{DD}}\right) \quad (1)$$

where I_Q is the total current consumption in the control circuitry of the LDO itself. I_Q can be taken as the difference between sum of all the input currents from V_{DD} and the output current I_{LOAD}. If the quiescent current (I_Q) of LDO is negligible,

$$\text{Power Efficiency} \cong \frac{V_{REG}}{V_{DD}} = 1 - \frac{V_{DO}}{V_{DD}}. \tag{2}$$

The current efficiency of LDO also depends on the I_Q and it is given as follows:

$$\text{Current Efficiency} = \frac{I_{LOAD}}{I_{LOAD} + I_Q}. \tag{3}$$

The *load* regulation of a LDO is the ability to maintain the accuracy of V_{REG} over its entire I_{LOAD} driving range. The *line* regulation is defined as the ratio between the changes in V_{REG} and V_{DD} at DC. The power-supply rejection (PSR) is the supply noise rejection capacity of LDO to prevent any changes on V_{REG} under AC perturbations on V_{DD}. The load transient response of LDO demonstrates how much and how quickly the LDO can limit the spike of voltage undershoot/overshoots on V_{REG} and recovers V_{REG} to the target level under abrupt changes in I_{LOAD}. To benchmark overall performance of a LDO, the following figure-of-merit (FOM) has been widely used [25]:

$$\text{FOM} = \frac{C_{OUT} \times \Delta V_{REG}}{\Delta I_{LOAD}} \times \frac{I_Q}{\Delta I_{LOAD}} \tag{4}$$

where ΔV_{REG} is the voltage under/overshoot which happens in LDO on the occurrence of step load current ΔI_{LOAD}.

B. LIMITATIONS IN DEEP SUBMICRON CMOS TECHNOLOGIES

As CMOS processes are downscaled to deep submicron, analog LDOs suffer severely from low supply voltages, which are often at near-threshold voltage (NTV) levels. Because analog LDOs cannot maintain enough error-amplifier gain under NTV conditions, many of the major performance metrics such as load transient response and line and load regulations are degraded drastically [26].

To resolve the error-amplifier gain issue at NTV and achieve low-voltage operations, an inverter-based LDO [27] and a ring-amplifier-based LDO [28] were recently proposed. These LDOs function well at NTV and even at sub-threshold levels. Unlike typical analog LDOs, the LDOs achieve the minimum dropout voltages of 50 mV in [27] and 20 mV in [28], respectively, and sufficient PSR performances at the same time. In addition, a transient-compensation path that is placed in parallel with the main regulation path is proposed in the ring-amplifier-based LDO to achieve fast transient response [28]. It recovers an undershoot of 45 mV within 25 ns for a step load current of 200 mA with peak current efficiency of 99.96%.

The trade-off between PSR and power efficiency is severer in typical analog LDOs. High PSR in analog LDOs can be achieved by maintaining a large V_{DO} to operate the power PMOS in the saturation region with an enough source-drain voltage V_{SD}. However, a large V_{DO} adversely affects the power efficiency as given in Eqs. (1) and (2). On the contrary, the power efficiency can be improved by reducing V_{DO}. As V_{DO} is decreased, the PMOS is pushed more into the triode region. In the triode region, the PMOS has much more resistive characteristics, which results in easier penetration of the supply noise from V_{DD} to V_{REG}, thus degrading PSR [29]. Moreover, from frequency compensation aspect, analog LDOs typically involve complex stability issues, thus requiring complicated compensation schemes [30]–[32].

In addition to these drawbacks, analog LDOs are considered inadequate to drive the digital load circuits. Digital load circuits typically have fast I_{LOAD} switching at sub-A/ns and a wide operating voltage range, which can come down to *NTV* levels. Under such load conditions, analog LDOs typically fail to provide acceptable performance metrics [33]. Therefore, the applications of analog LDOs are limited to analog load circuits in many cases.

III. SYNCHRONOUS DIGITAL LDO

To address the aforementioned issues of analog LDOs, the predominant design trends of LDOs have been shifted from analog to digital in current state-of-the-art SoC devices in deep submicron CMOS processes. The first work proposed in this domain was a digital-assisted analog LDO that employed a parallel topology of an analog and digitally controlled pass transistors for powering a DRAM [34]. Another digital-assisted analog LDO was proposed for biasing a DC-DC converter [35]. Its error amplifier was digitally controlled based on a push-pull network of digital-to-analog converter. As a result, this work achieved a fast load transient response time (T_R) of 288 ps while driving an I_{LOAD} of 1 A. However, this structure is still categorized as analog LDO because its core part is based on analog feedback control using an analog amplifier. A digital feedback-loop controller was used in the voltage regulator in [36]. But, it used a voltage-supply-hopping scheme for regulation unlike typical digital LDOs, in which PMOS transistors are used for voltage regulation. This scheme switches fast between two fixed-voltage power modes according to its digital feedback loop control to provide a target regulated voltage. This voltage-supply-hoping regulator is not considered a digital LDO because of its limited regulated voltage range, yet the controller design preceded a similar digital LDO in [37], which is considered the first DLDO.

The synchronous DLDO in [37] uses an external sampling clock F_{CLK} for the feedback controller and comparator. Its circuit diagram is shown in Fig. 3. It consists of three basic building blocks, (i.e.), a comparator, a digital controller based on bi-directional shift registers (BiSHRs), and a unary-weighted array of PMOS power transistors. The comparator quantizes the voltage error between V_{REF} and V_{REG} and generates its output *COMP*, which is fed to the digital controller. According to *COMP*, BiSHRs perform digital shifting operations at every rising edge of F_{CLK} to

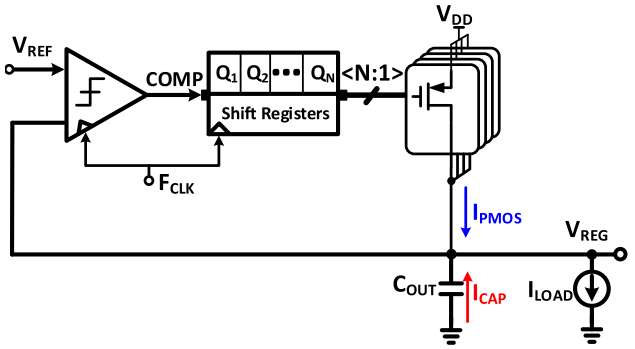

FIGURE 3. Circuit diagram of synchronous DLDO [37].

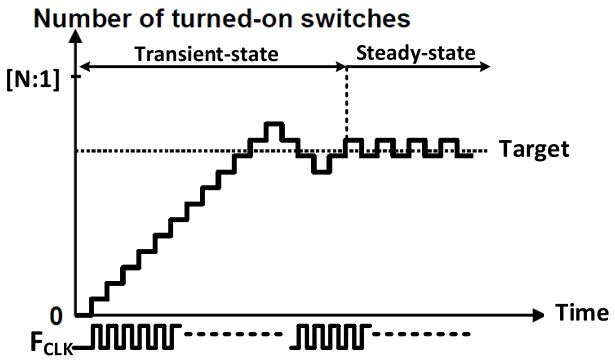

FIGURE 4. Number of turned-on power transistors during transient and steady states in synchronous DLDO.

control the number of turned-on power transistors. By doing so, the DLDO adjusts I_{PMOS} to regulate V_{REG} while providing a required I_{LOAD}, as shown in Fig. 4. During transient states of the DLDO, V_{REG} approach V_{REF} as fast as possible. When $V_{REG} \cong V_{REF}$, the DLDO is in steady state. During the steady state, an LSB code of BiSHRs toggles by *COMP* and F_{CLK} to switch on/off a corresponding power transistor continuously. As shown in Fig. 4, this continuous switching creates voltage ripples on V_{REG} even during the steady state. The prototype implemented in 65 nm CMOS process successfully achieved an NTV operation while supplying V_{REG} of 0.45 V from V_{DD} of 0.5 V. At this NTV operation, the synchronous DLDO achieved a very small V_{DO} of 50 mV with a minimum I_Q of 2.7 μA [37].

In a following-up work [38], a fully-integrated DLDO was demonstrated with a new parity-based error prediction and detection unit to achieve better adaptive voltage scaling. This work served as a seminal work in the co-design of a DLDO with digital load circuits. It showed 13% power saving by its adaptive voltage scaling.

Table. 1 compares overall characteristics between typical analog and digital LDOs. In general, analog LDOs are better at PSR and transient characteristics than digital LDOs. In contrast, digital LDOs are better at power efficiency due to their low dropout voltage, and they are easy to operate under low supply voltages. In addition, digital LDOs involve much less complicated stability issues.

TABLE 1. Structural comparison between analog and digital LDOs.

Design	Analog	Digital
Input range	> 1.0 V	> 0.4 V
Dropout Voltage	100 – 200 mV	> 40 mV
Compensation	External Cap (µF) On-chip Cap (pF-nF)	No
PSR	☺	☹
I_Q	☹	☺
Clock Signal	No	Yes
Switching Noise	No	Yes
Line/Load Transient	☺	☹
Low-V Operation	☹	☺

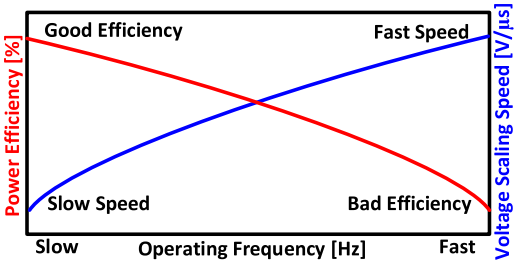

FIGURE 5. Power-speed tradeoff in typical synchronous DLDO.

IV. LIMITATIONS OF SYNCHRONOUS DLDOs

Although the first synchronous successfully achieved NTV operation with high current efficiency [37], this one and many other synchronous DLDOs inherently suffer from several fundamental limitations. Four major limitations are discussed in the following subsections.

A. POWER-SPEED TRADEOFF

There is a tradeoff between the power consumption and voltage-scaling speed in most synchronous DLDOs. This power-speed tradeoff mainly comes from the synchronous operation in the BiSHRs. The shift operations occurs only at the rising edges of F_{CLK} as shown in Fig. 4. Hence, the voltage-scaling speed of DLDO is dominated by F_{CLK}. The voltage scaling is the time taken for the DLDO output V_{REG} to track a certain voltage step of V_{REF} in the unit of V/μs. Therefore, when F_{CLK} increases, the DLDOs can achieve faster voltage scaling, but at the cost of power consumption, which is increased proportionally to F_{CLK} [39]–[41]. Such general trend of the power-speed tradeoff is illustrated in Fig. 5 and further explained elsewhere [42]. The power-speed tradeoff drastically affects the load transient performance of DLDO. It is thoroughly discussed in next subsection.

B. POOR LOAD TRANSIENT RESPONSE

The load transient performance of synchronous DLDOs is inevitably affected by power-speed tradeoff. During a load

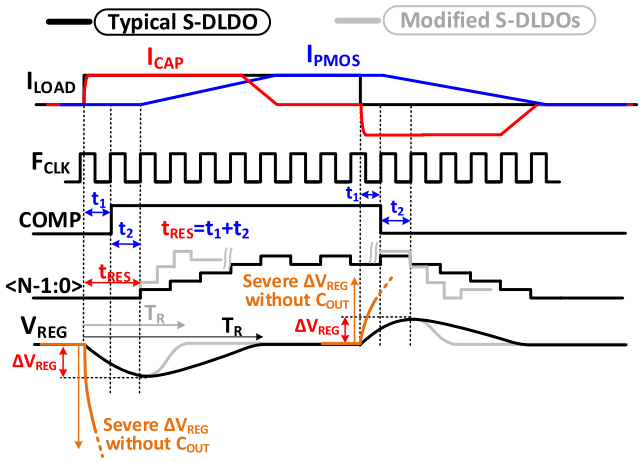

FIGURE 6. Load transient response of typical and modified synchronous DLDOs [43].

current transient, in which the load current is instantly changed, the DLDO is subject to induce a large voltage under- or over-shoot (ΔV_{REG}) and require a long recovery time (T_R).

To elaborate, Fig. 6 illustrates load transient responses of a typical synchronous DLDO [43], [44]. At the moment when I_{LOAD} steps up, the conventional DLDO cannot provide a correspondent I_{PMOS} to the I_{LOAD} instantly because of F_{CLK}-dependent delays in the comparator and BiSHRs. In the mean time, I_{CAP} the dynamic current from the output capacitor C_{OUT} starts discharging to the I_{LOAD} to compensate the voltage undershoot ΔV_{REG}. At the next rising edge of F_{CLK}, the comparator output *COMP* is toggled and fed to the BiSHRs. After one more clock period, the BiSHRs start shifting at the rising edge of F_{CLK}. Hence, it takes at least two or more cycles for the DLDO to start to react to the change. The maximum ΔV_{REG} caused by the total delay t_{RES} can be estimated as follows:

$$\Delta V_{REG} \cong \frac{\Delta I_{LOAD} \times t_{RES}}{C_{OUT}} \tag{5}$$

where t_{RES} is the response time of DLDO feedback loop.

The total recovery time T_R is the time taken until the under/overshoot is fully recovered to the target regulated voltage. T_R can be shortened by using large power transistors and fast F_{CLK} [39], [41], [45], [46] as shown by the gray waveform in Fig. 6. However, it still requires a similar t_{RES} until they start to respond to the step change of I_{LOAD}, thus it still suffers from a large ΔV_{REG}.

For the case with no C_{OUT}, ΔV_{REG} drops in a dramatic free-fall due to the absence of I_{CAP}. To reduce ΔV_{REG}, a large C_{OUT} is inevitably implemented in synchronous DLDOs [46]–[51]. However, C_{OUT} consumes either a pad pin and footprint area on board [46], [47], [49]–[51] or a large chip area [48]. Due to the use of C_{OUT}, the integration of multiple DLDOs in SoCs require multiple pad pins and board area, which adversely affect the cost of product. Alternatively, C_{OUT} can be integrated on chip, but it should be downscaled as much as possible to minimize the occupied silicon area. Since a downscaled C_{OUT} typically deteriorates the load transient response of DLDO as shown in Eq. (5), the feedback loop response time t_{RES} should be shortened together to achieve better ΔV_{REG}.

Various design techniques are proposed to shorten t_{RES} of synchronous DLDOs to achieve a better load transient response with a downscaled C_{OUT} or even without it. These design techniques include: 1) dynamic and adaptive frequency scaling [45], [52], 2) analog-assisted loop [44], [53], and 3) self-clocking [43]. Thanks to these techniques in DLDOs, the load transient performance can be significantly improved. The DLDO architectures using these design techniques and other state-of-the-art techniques resolving the power-speed trade off and poor load transient response issues are thoroughly discussed in Sec. VI.

C. STEADY-STATE VOLTAGE RIPPLES

Another intrinsic drawback of typical synchronous DLDOs is large voltage ripples V_{RIPP} on V_{REG} during the steady state. Because synchronous DLDOs operate discretely at F_{CLK} unlike continuous-time analog LDOs, they intrinsically induce voltage ripples at the clock frequency F_{CLK}. Such V_{RIPP} are typically resulted from the current mismatch between I_{PMOS}, which is discrete in both time and level, and I_{LOAD}, which is continuous in time and level. V_{RIPP} can be estimated with the following equation [55]:

$$V_{RIPP} \cong \frac{V_{DD} \times R_L}{R_{ds,on} \times N} \tag{6}$$

where R_L is the load resistance and $R_{ds,on}$ the on-resistance of PMOS switches. It is assumed that N number of the power transistors are turned on and all of them operate in the deep triode region.

The voltage ripple can be even more aggravated by limit cycle oscillation (LCO). In a typical DLDO with an ADC, loop controller and DAC (power transistors), LCO can be caused by insufficient resolution of the DAC in comparison to resolution of the ADC. At lighter load-current conditions, voltage change on the DLDO output caused by LSB change of the power transistors gets larger, the DAC resolution becomes coarser effectively. Because of such discrepancy of resolution between the ADC and DAC, the DAC may fail to tune the DLDO output accurately enough with sufficiently fine resolution as to the sensed value from the ADC. Then, output value of the controller and the DLDO output oscillates around the target value while average of the oscillating controller output value is the same as the target value. Fig. 7 shows waveforms of the controller output <N:1> for the LCO mode M of 1, 2 and 3. The V_{RIPP} corresponding to the mode of LCO has a frequency of $F_{CLK}/2M$, where F_{CLK} is the sampling frequency of the DLDO and M is the mode of LCO [54]–[57]. Note that the DLDO loop is stable under the case with LCO. LCO is not related to loop instability. As explained above, LCO is not caused by loop instability and does not make the loop unstable typically. To resolve the LCO issue, the DAC should have a higher resolution than that of the ADC.

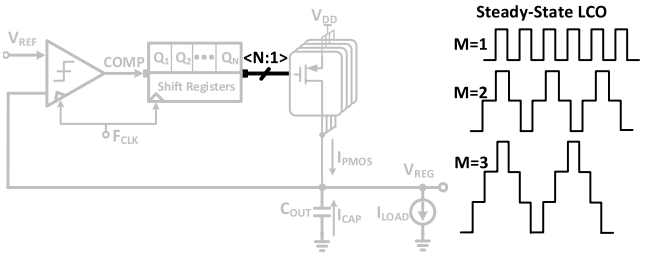

FIGURE 7. Limit-cycle oscillation (LCO) in synchronous DLDO: waveforms of code <N:1> with mode 1, 2, and 3 LCOs [54].

Various design techniques have been proposed to reduce V_{RIPP} in DLDOs. A freeze mode can successfully eliminate V_{RIPP} [58]. When V_{REG} reaches V_{REF} most closely, the controller goes into a freeze mode by fixing the number of power transistors. Depending on the frozen level of V_{REG} compared to V_{REF}, this method is prone to an offset between the two voltages which may happen due to the current error between I_{PMOS} and I_{LOAD}.

Alternatively, to suppress V_{RIPP}, a technique to control auxiliary power transistors based on the comparator output was proposed [54]. By using just 2 auxiliary power transistors in parallel besides main ones, this technique significantly reduced V_{RIPP} from 140 to 30 mV at minimum current driving conditions. However, it may still cause some offset voltage even with an optimized sizing of the auxiliary PMOS switches, yet its resulting ripple was not significantly low, $V_{RIPP} = 30$ mV @ $I_{LOAD} = 500\ \mu$A.

V_{REG} can be noise-shaped using a 1^{st} order $\Delta\Sigma$ modulator in a fine loop to suppress V_{RIPP} [59]. This architecture with 1-bit oversampled modulation significantly reduced V_{RIPP} to less than 1 mV. To filter out the high-frequency modulated ripples created by the $\Delta\Sigma$ modulator, however, it required a large external C_{OUT} of 100 nF, which is not desirable in SoCs due to an additional pad pin and extra board area.

A ripple-cancellation amplifier (RCA) was proposed to supply a sub-LSB current during the steady state to mitigate V_{RIPP} [60]. By resolving the current error between the actual load current I_{LOAD} and the digitized regulation current of the DLDO I_{PMOS}, it reduced V_{RIPP} down to 2 mV from 46 mV. However, it involves complex stability issues from the use of analog circuits (RCA). In addition, by using the RCA, the dropout voltage V_{DO} is increased, degrading the overall power efficiency.

D. POOR POWER-SUPPLY REJECTION

DLDOs suffer from poorer power-supply rejection (PSR) than analog LDOs. This is not only for synchronous DLDOs, but also for almost all other types of DLDOs, which are described in Sec. VI. While the power transistors in analog LDOs operate in the saturation region, those in DLDOs are fully turned on in the deep triode region. In the deep triode region, the transistors behave like a voltage-controlled resistor, so noises in V_{DD} can easily pass to the output voltage V_{REG} through the transistors. The characteristic transfer function from V_{DD} to V_{REG} can be expressed with the impedance ratio as:

$$\frac{V_{REG}}{V_{DD}} = \frac{Z_L}{R_{ds,on} + Z_L} \tag{7}$$

where Z_L is the total load impedance. $R_{ds,on}$ is the on-resistance of the power transistors and can be given as:

$$R_{ds,on} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{DD} - |V_{tp}|)} \tag{8}$$

where V_{tp} is the threshold voltage of the PMOS power transistors. This direct noise penetration is inevitable in DLDOs, resulting in poor PSR. Hence, DLDOs are typically unsuitable for driving noise-sensitive analog and RF circuits [29].

PSR of DLDOs may only be improved by incorporating an analog circuit in parallel to the digital. In this regard, analog-digital hybrid LDOs were proposed to aim to drive supply-noise-sensitive analog load circuits in SoCs [29], [60]. The hybrid architecture is discussed in Sec. VI.

V. DESIGN CONSIDERATIONS FOR BUILDING BLOCKS IN DLDOs

In general, DLDOs consist of three main building blocks as discussed in Sec. III, *i.e.*, a comparator, digital controller, and power switch array consisting of PMOS transistors. Comparators and switch arrays for DLDOs are discussed in the following subsections. Various architectures of digital controllers are discussed separately in Sec. VI.

A. COMPARATOR AND ANALOG-TO-DIGITAL CONVERTER (ADC)

In DLDOs, the comparator is considered the first stage of operation because it quantizes the voltage error between V_{REF} and V_{REG} and its output is used as input for the next stage: digital controller. Conventionally, there are two types of voltage comparators: comparators based on 1) open-loop high-gain amplifier, and 2) dynamic latches. Amplifier-based comparators offer high precision and high speed in general, but at the cost of large and continuous current consumption. In Contrast, dynamic-latch-based comparators consume power only at each comparison, thus typically resulting in much less power consumption. A circuit diagram of typical dynamic-latch-based comparator is shown in Fig. 8 [37], [46]–[48], [54], [61]–[70]. Because dynamic-latch-based comparators utilize a sampling clock F_{CLK} for their comparison operation, they can avoid continuous current consumption. However, they have several challenges. Firstly, the speed of comparator is limited by the clock speed. By using a fast clock, the speed can be enhanced, but at the cost of power consumption. Secondly, a fast F_{CLK} may exacerbate the problem of meta-stability, which inherently exists in latch-based comparators. The DLDO loop forces the difference between V_{REF} and V_{REG} to be as small as possible, and a smaller difference at the input of comparator increases the chance of meta-stable behaviors, leading to higher switching noises. In contrast, a slow F_{CLK} limits the comparator speed, degrading the overall transient performance. Lastly, dynamic-latch-based comparators suffer from input-referred latch offsets, which is the

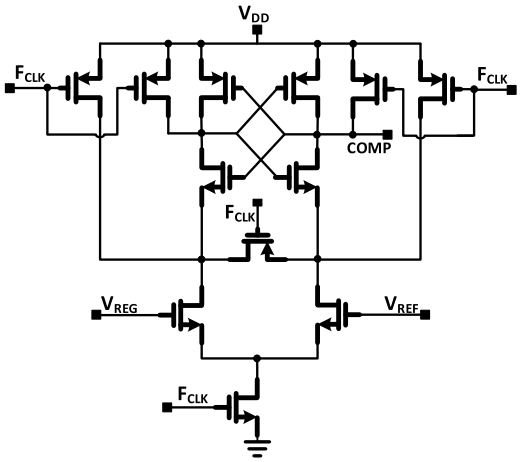

FIGURE 8. Circuit diagram of a typical latch-based comparator [37].

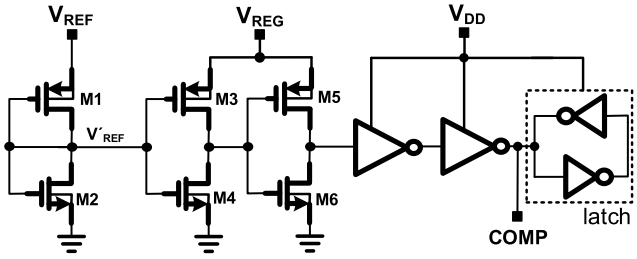

FIGURE 9. Circuit diagram of a continuous time comparator [49].

mismatches resulted from unbalanced parasitic capacitances and kick-back noises [49], [71]–[73].

As a promising alternative of two conventional comparator types, asynchronous comparators were proposed in DLDOs [42], [58], [74]–[76]. Asynchronous comparators are not clock-dependent, so the speed is not limited by the clock. Instead, they resolve their output with a minimum latency by using internal trigger signals. As a result, they are typically faster in the response, compared to clock-based comparators.

As another alternative, level-triggered event-driven comparators have been attractively applied in DLDOs [43], [49], [77]. These comparators provide a shortest latency and an enhanced power efficiency as compared to conventional comparators. They resolve their output at level-crossing events only, and remain idle otherwise, leading to significant current saving. In addition, they require fewer transistors, and thus occupy a smaller area.

Instead of comparators, analog-to-digital converters (ADCs) have also been adopted as voltage quantizer in DLDOs along with digital proportional-and-integral (PI) controllers to obtain a faster speed by directly quantizing the output voltage error in multiple levels. ADCs based on time-domain quantization are commonly applied in DLDOs because time-domain quantizers typically can consume less power and achieve higher accuracy than voltage-domain quantizers [45], [51], [52], [60], [78], [79]. For time-domain quantization, quantizers based on voltage-controlled oscillator (VCO) or voltage-to-time converter (VTC) are used instead of voltage comparator. For high resolution, however, a long delay-chains are required, increasing the chip area and slowing down the speed of DLDO. Alternatively, level-triggered event-driven ADCs have been increasingly adopted in DLDOs because of their shortest latency and clock-less operation [80]–[85]. Unlike time-domain ADCs, of which operation is strongly dependent on the clock, event-driven ADCs can immediately respond to new events.

The choice between a comparator and ADC should be made based on their advantages and characteristics. When a comparator, which acts as a 1-bit quantizer, and BiSHRs-based controller are used, it typically involves simpler design complexity and a lower I_Q. However, such bang–bang control requires many clock cycles to reach a steady state because the loop is updated by a fixed step in every cycle as discussed in Sec. III. Using a higher F_{CLK} is one of solution to improve the transient response, but this comes with a cost of a large power consumption. In addition, for DLDOs with comparator-based bang-bang control, the LCO problem is worse. The comparator operates like an ideal relay with zero dead time when any offset of the comparator is neglected [56]. Hence, a dead zone is normally added around V_{REG} to suppress LCOs [54], [56]. In contrast, ADCs inherently involve a dead zone, which is normally equivalent to the LSB voltage, so the LCO is mitigated significantly. For ADCs with higher resolution, the LCO can be further reduced because the ADC resolution is tightly related to the V_{REG} accuracy at steady state. Therefore, multi-bit voltage quantizers or ADCs have been more attractively used in DLDOs recently [83]–[85].

B. POWER SWITCH ARRAY: SIZING OF POWER TRANSISTORS

How power transistors are sized in the power switch array directly affects the transient responses and stead-state ripples of the DLDO. Unary-weighted sizing of power transistors was initially used, and later other strategies were proposed, such as binary-weighted and exponentially weighed schemes.

1) UNARY-WEIGHTED SIZING

In many synchronous DLDOs, the output code of BiSHRs can be changed by one bit per F_{CLK} only, so I_{PMOS}, the current through the power transistors, can be changed by the current amount of one transistor unit per F_{CLK} only. Consequently, the synchronous DLDOs with such scheme show slow load transient responses. A probable solution to speed up the load transient response is to increase size (W/L ratio) of the power transistors. The DLDO with larger-sized power transistors can change I_{PMOS} faster with a bigger current step per F_{CLK}, resulting in faster voltage recovery during load transients as shown in Fig. 10. During the steady state, however, the DLDO with larger power transistors induce larger V_{RIPP} as shown in the inset of Fig. 10. As shown, synchronous DLDOs with unary-weighted power switch array suffer from a tradeoff between the speed and V_{RIPP}. In addition, the DLDO with a faster clock will consume more power.

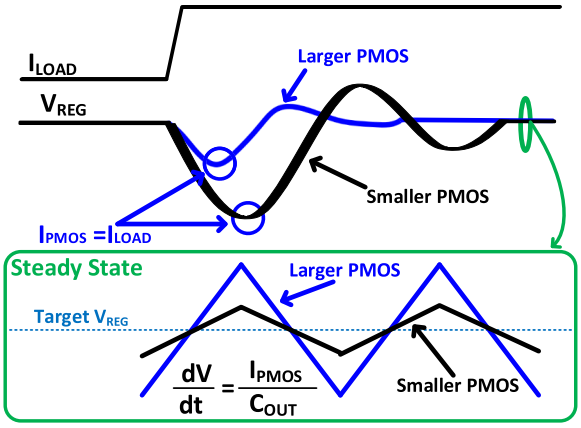

FIGURE 10. Effect of power transistors sizing on load transient state and steady state (inset) [51].

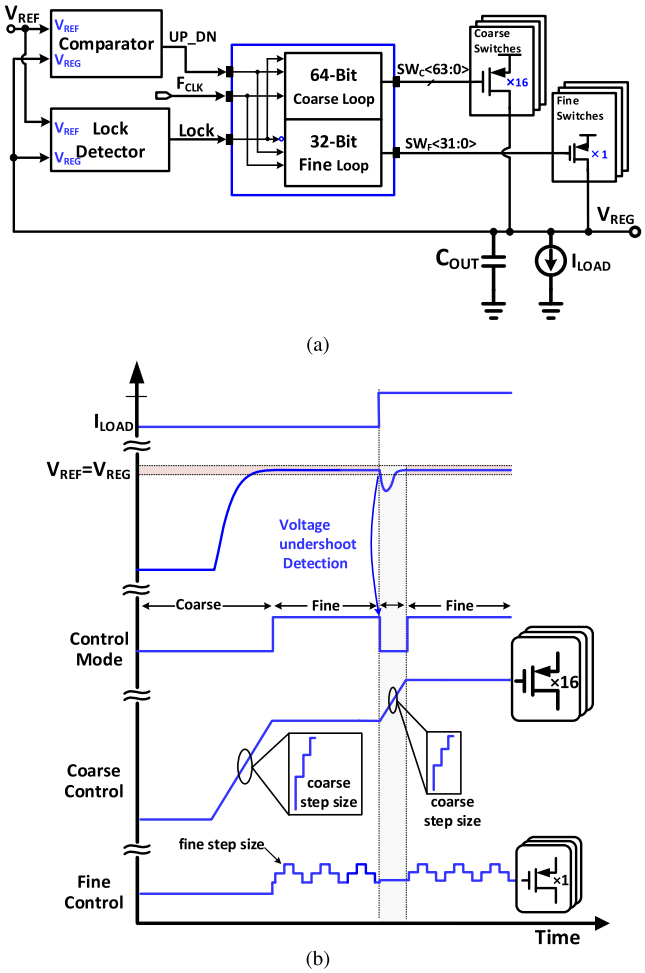

FIGURE 11. (a) Simplified block diagram of typical dual-loop DLDO. (b) Operational waveforms of the dual-loop DLDO using unary-weighted power transistors sizing.

To resolve this tradeoff, a structure with two control loops, *i.e.*, coarse and fine loops, was proposed [48]. Its simplified block diagram is shown in Fig. 11 (a). Here the DLDO has two arrays of power transistors, one array with larger power transistors and the other with smaller ones. During the start-up and load transient states, the coarse loop is activated and controls the array with larger power transistors to speed up the transient response time as shown in Fig. 11 (b). During the steady state, the fine loop now takes over and controls the small power transistors to minimize the ripple. Although the power-speed and the V_{RIPP}-speed tradeoffs can be resolved to some extent by using this dual-loop approach, the unary-weighted sizing still suffers from speed limitations.

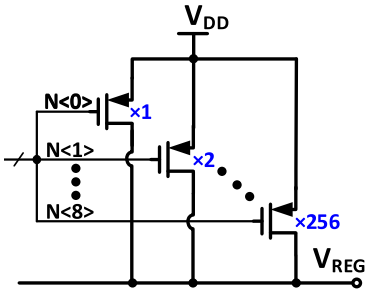

FIGURE 12. Binary-weighted sizing of power transistors.

2) BINARY-WEIGHTED SIZING

To improve the transient speed further, binary-weighted sizing of the power transistor array was proposed and implemented in DLDOs [51], [62], [86]–[88]. An example of binary-weighted transistor sizing is shown in Fig. 12. In general, DLDOs with binary-weighted power transistors have a faster transient response than those with unary-weighted ones during transient states when the load current changes largely. Starting from MSB to LSB, the DLDO quickly determines the desired on/off combinations of the power transistors. When the DLDO with binary-weighted sizing of power transistors is implemented with an N-bit binary-search controller such as a controller based on successive approximation, only N cycles are required for V_{REG} to approach the target V_{REF} [62], [88]. Such DLDO can have a much faster transient speed than the LDO with unary-weighted power switches as shown Fig. 13. However, the binary-weighted sizing may cause a longer settling time as shown in Fig. 13. In addition, large voltage ripples may be induced in the case when non-LSB bits are toggling during the steady state.

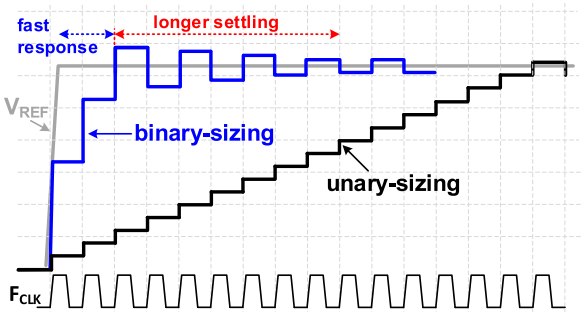

FIGURE 13. Comparison of the voltage tracking speed between unary- and binary-weighted power transistors sizing.

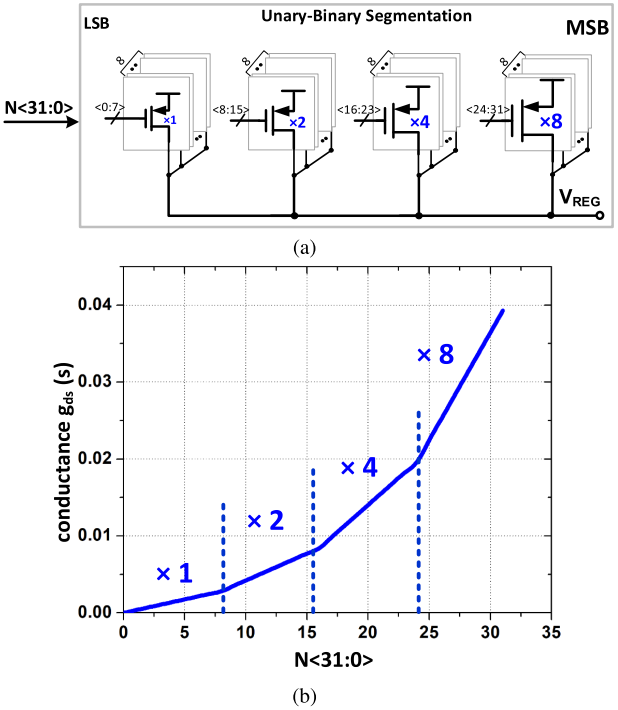

FIGURE 14. (a) Circuit diagram of unary-binary segmentation (UBS) scheme. (b) Its equivalent conductance of power transistors showing pseudo-exponential characteristics [43].

3) PSEUDO-EXPONENTIAL- AND EXPONENTIAL-WEIGHTED SIZING

To avoid the issues of long settling time and large voltage ripples in binary-search scheme and to achieve a balance between the speed and accuracy, a hybrid scheme based on unary-binary segmentation (UBS) was proposed [43]. The UBS scheme consists of binary-weighted groups, each of which consists of unary-weighted power transistors as shown in Fig. 14. As a result, the equivalent conductance of the UBS scheme has pseudo-exponential characteristics as shown in Fig. 14. While ensuring a wide dynamic current range, the UBS scheme can achieve much faster transient speed and smaller peaking at load transients than the unary scheme. In addition, its settling time is short than the binary-weighted cases.

Recently, exponentially weighted sizing of power transistors was proposed [89], [90]. As shown in Fig. 15, sizes of the power transistors increase exponentially. Here the increase ratio of W/L was chosen to be 1.02 so that all the transistors in the array are integer multiples of the unit size for good layout matching. The DLDO with this scheme achieved fast voltage scaling and a maximum-to-minimum output current ratio of 4000× with a 255-bit control word [89].

VI. STATE-OF-THE-ART DLDOs

Various DLDO architectures have been proposed over the last decade to resolve the aforementioned design tradeoffs and limitations. These state-of-the-art DLDO architectures are discussed below.

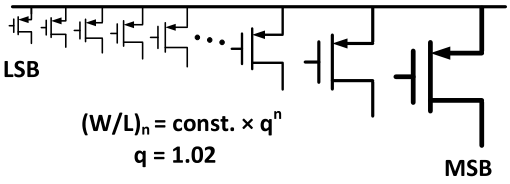

FIGURE 15. Exponentially sized power transistor array [89].

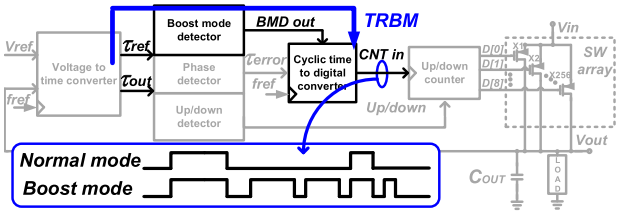

FIGURE 16. Clock-boosting scheme for synchronous DLDO [51].

A. ADVANCED SYNCHRONOUS DLDOs

To resolve the power-speed tradeoff that typical synchronous DLDOs inherently have, various techniques were demonstrated such as techniques using: coarse-fine dual-loop controllers [46], [48], [61], conditional clock-boosting [4], [47], [51], [68], PID controllers [60], [91], and adaptive sampling [52], [70], [92]. They are based on different types of digital controllers and techniques, but share a similar architectural topology, in which the clock speed is boosted to achieve a faster response during load transient states. During the steady state, they keep using a slow clock to minimize the switching power consumption. As an example, Fig. 16 shows a block diagram of a clock-boosting DLDO [51], which implemented a transient-response boost mode (TRBM). The TRBM is only activated during load transient state. During the TRBM, the DLDO monitors magnitude of the under/overshoot and boosts or reduces the clock speed accordingly.

In spite of such clock boosting techniques, synchronous DLDOs still exhibit slow load transient responses due to their slow feedback loop response (T_{RES}) to (ΔI_{LOAD}) as discussed in Section IV and shown in Eq. (5). Due to this slow response time, these synchronous DLDOs are unable to downscale much or eliminate C_{OUT}. In addition, the design margins of these DLDOs to ensure the stability across worst-case PVT variations further degrade their transient response performances.

To maintain fast transient responses across PVT variations, computational regulation techniques using autonomous and dynamic gain tracking schemes were recently proposed [85], [93]. In the computationally regulated DLDO in [85], the quantization error in V_{REG} is detected by its autonomous gain tracker and suppressed by its solver block within the same cycle. As a result, the computationally regulated DLDO [85] can drive a cortex microprocessor with a fast transient response time of < 20 ns for a fast switching load current of 5.6 mA/0.1 ns. The DLDO using a dynamic-gain control scheme and all-digital auto-tuning engine [93] also achieves sub-cycle transient responses and demonstrates

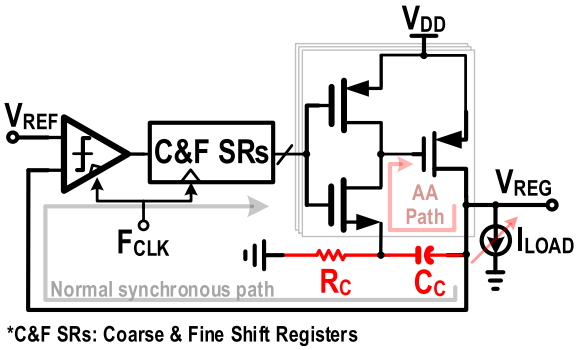

FIGURE 17. Analog-assisted synchronous DLDO [44].

55 ns of transient response time for a load current step of 40 mA/0.1 ns over process variations and aging.

B. ANALOG-ASSISTED SYNCHRONOUS DLDOs

To downscale or eliminate C_{OUT} in synchronous DLDOs, several analog-assisted techniques were proposed [44], [53], [94]–[98]. These analog-assisted techniques can instantly supply a dynamic current in response to load current transients by shortening T_{RES}. Thus, these techniques can successfully reduce the voltage undershoot ΔV_{REG} with a downscaled C_{OUT}.

Block diagram of an analog-assisted DLDO is shown in Fig. 17 [44]. It includes one additional feedback path besides a typical synchronous feedback path. The analog-assisted (AA) path is made with a high-pass network consisting of a compensation capacitor ($C_C = 100$ pF) and a resistor (R_C). During load transient states, the voltage change in V_{REG} is instantly conveyed to the power switch through C_C, supplying a corresponding dynamic current. As a result, ΔV_{REG} can be significantly suppressed by C_C instead of C_{OUT}. This analog-assisted DLDO successfully eliminated C_{OUT} and achieved an undershoot of ($\Delta V_{REG} = 105$ mV) for $\Delta I_{LOAD} = 10$ mA while supplying a regulated output voltage of 0.5 V [44]. However, ΔV_{REG} of more than 100 mV is still large at the given supply voltage level of 0.5 V, making this DLDO undesirable to drive digital load circuits.

Another analog-assisted DLDO using NMOS switch arrays and C_C was proposed [53]. Without C_{OUT}, it can also supply an instant current during load transient states using its AA path with C_C. Compared to [44], it reduced C_C from 100 pF to 24 pF. However, its NMOS-based switch array severely limits its regulation voltage range. Moreover, two different levels of voltage supplies are required along with multiple level–shifters, increasing the area consumption and design complexity. A large current driving, analog-assisted DLDO [97] proposes a direct ac-coupled high-impedance (ACHZ) feedback loop to dynamically enhance its load transient performance.In addition, its regulation accuracy is improved by using a small-current charge pump. The proposed AA-DLDO using ACHZ, recovers a $\Delta V_{REG} = 88$ mV within 65 ns for a $\Delta I_{LOAD} = 100$ mA, and achieves a minimum FOM of 1.8 fs. Although these analog assisted DLDOs successfully eliminated C_{OUT} [44], [53], [97], they instead require C_C, which still consumes large silicon area.

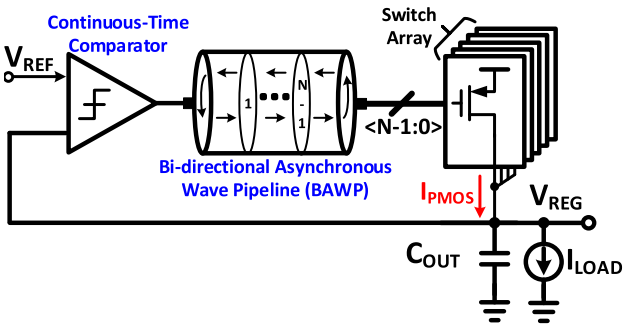

FIGURE 18. Asynchronous DLDO [58].

C. ASYNCHRONOUS DLDOs

To overcome the aforementioned clock-dependent limitations of synchronous DLDOs, a new class of DLDOs, *asynchronous* DLDO, was introduced [58], and several improved designs in this class were demonstrated [26], [29], [40], [42], [74]–[76]. This type of DLDO does not need an external clock F_{CLK} to operate, so it is categorized as an *asynchronous* DLDO. Fig. 18 shows a simplified block diagram of an asynchronous DLDO [58]. It employs a continuous-time clockless comparator instead of a clocked one like in Fig. 8. The controller is based on a bidirectional asynchronous wave pipeline (BAWP), which operates like shift registers, but without a clock. It shifts the control bits to the right for $V_{REG} < V_{REF}$ and shifts to the left for $V_{REG} > V_{REF}$, turning on and off the power transistors. In addition, a freeze mode was also firstly introduced to eliminate the steady-state ripples [58], and was also adopted in other asynchronous and synchronous DLDOs [26], [29], [44]. Thanks to its clock-less operation, asynchronous DLDOs excel synchronous DLDOs in I_Q, current efficiency, response time, and dynamic range of load current. In addition, some asynchronous DLDOs do not require C_{OUT} thanks to their parallel implementation with a switching-mode DC-DC converter [29], [42], [58]. However, the other asynchronous DLDOs [74]–[76] need a large C_{OUT} ($\geq$ 1.5 nF) to achieve better load transient response while driving a large load current ($\geq$ 500 mA).

To be able to drive a large load current without C_{OUT}, a novel self-shifting scheme was proposed [43]. This DLDO significantly shortened T_{RES} and successfully eliminated C_{OUT} by implementing an asynchronous kick-start scheme during load transients. Simplified block diagram of the self-shifting DLDO along with its operational waveforms during a load transient are shown in Fig. 19. Thanks to its asynchronous kick-start technique, which is implemented using logic-threshold-triggered comparator (LTTC), voltage-range detector (VRD), and self-shifting registers, the total feedback response time T_{RES} during load current transients is shortened to just summation of the logic delays of LTTC and VRD. Thus, I_{PMOS} can be immediately supplied just after a load transient happens, achieving a small ΔV_{REG} without using C_{OUT}.

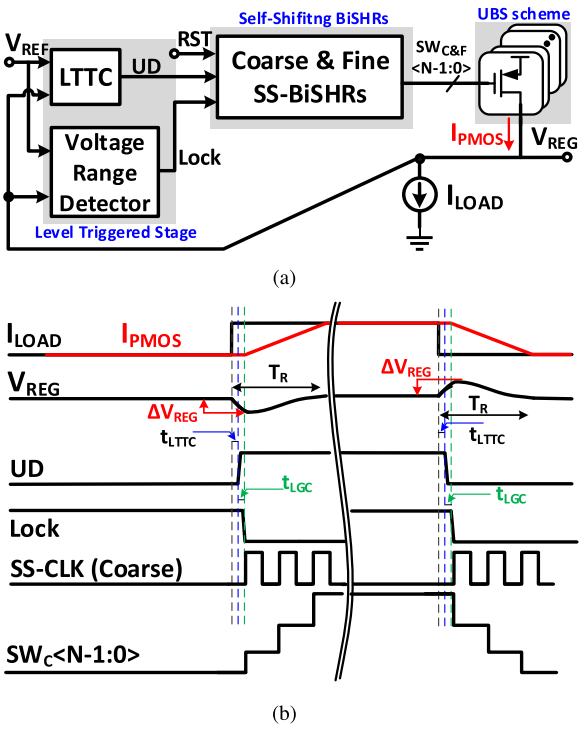

FIGURE 19. (a) Self-clocked DLDO and (b) its waveforms during a load transient [43].

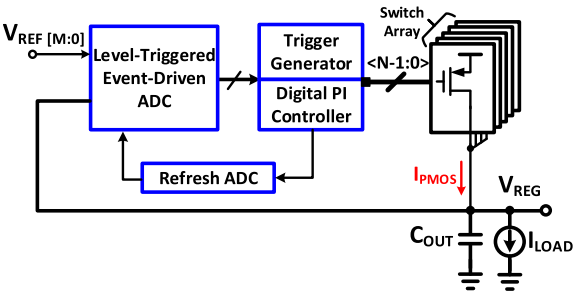

FIGURE 20. Event-driven DLDO [80].

However, operations of the asynchronous controller (BAWP) in [26], [29], [40], [42], [74]–[76] and the self-shifting controller in [43] are strongly based on the inherent delays of the internal circuits. These delays are greatly sensitive to PVT variations, and the operation gets even vulnerable in near- and sub-threshold voltage regions. Therefore, it becomes difficult for these asynchronous DLDOs to maintain the same performance over the entire regulation range although they can offer the best performance metrics at some specific conditions.

D. EVENT-DRIVEN ASYNCHRONOUS DLDOs

Event-driven DLDOs were proposed to overcome the clock-dependent limitations of conventional synchronous DLDOs and the PVT sensitivity issue of asynchronous DLDOs [80]–[83], [99]. A simplified block diagram of the first implemented event-driven DLDO is shown in Fig 20 [80]. It has a level-triggered ADC to detect any changes in V_{REG}, *i.e.*, *events*. The ADC output is fed to a digital proportional-integral (PI) controller, which generates control signals of the power transistors. Thanks to these blocks, any changes in V_{REG} can be detected and responded instantly without the use of sampling clock. Thus, the event-driven control can significantly reduce the latency of the control loop as compared to synchronous DLDOs. Due to this minimum loop latency, C_{OUT} can be significantly reduced to tens of pF in event-driven DLDOs [81], [83], [99]. In addition, the steady-state ripples are also absent in this type of DLDOs because there are no events (no change in V_{REG}) during the state state. However, the event-driven architecture may suffer from an issue called the sticking problem, in which the output voltage sticks or moves slowly near an undesired value [83]. The sticking problem can be resolved by using a watchdog counter, which generates self-triggered pulses to update V_{REG} constantly as long as $V_{REG} \neq V_{REF}$ [83]. In addition, the challenges of ensuring stable mode transitions under random load current conditions, switching losses, are also considerable in event-driven DLDOs. The typical event-DLDOs [80], [81], [83] my also prone to PVT variations because their trigger logics to control the MOS devices are based on the threshold crossing made by V_{REG}. To resolve these issues, a variation-adaptive computational DLDO is proposed in [100] featuring an event-driven computational controller. The voltage regulation based on the variation tolerant adaptive coefficients makes the DLDO [100] resilient to PVT variations. In addition, it exhibits the fastest settling time of < 20 ns for a step load current of 500 mA/0.25 ns and achieves a peak current efficiency of 99.9 %.

E. ANALOG-DIGITAL HYBRID LDOs

DLDOs are well suited for driving digital load circuits, which have relaxed requirements in supply noise sensitivity and steady-state voltage ripples. For driving RF and analog load circuits, however, DLDOs are not considered adequate due to their low PSR performance and high supply-noise sensitivity as compared to analog LDOs. To harness advantages of both analog and digital LDOs, hybrid architectures were developed [60], [77], [89], [101]–[103]. A representative hybrid topology with parallel analog and digital LDOs is shown in Fig. 21. The hybrid topology is fundamentally different from the dual-loop DLDOs, which employ two digital loops.

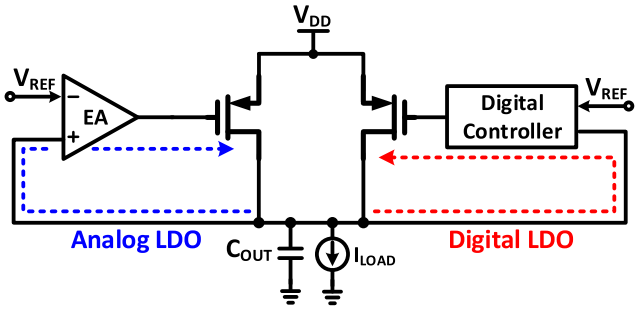

FIGURE 21. Parallel combination of analog and digital LDOs.

TABLE 2. Structural and performance comparison of state-of-the-art DLDO architectures.

DLDOs	Synchronous	Analog-Assisted	Asynchronous	Event-Driven	Hybrid
F_{CLK} requirements	Yes	Yes	No	No	Yes (digital)
Power-Speed tradeoff	Yes	No	No	No	Yes
Dropout voltage	Small	Small	Small	Small	Large
C_{OUT}	Large	C_{OUT} removed C_C used	C_{OUT} removed or small	Small	Large
Steady-state ripples	Large	Large	Ripple-less with freeze	Ripple-less	Ripple-less
PSR	Poor	Poor	Poor	Poor	Good
PVT Sensitivity	Good	Good	Poor	Good	Good
Loop Stability	Easy	Complex	Easy	Easy	Complex
Design Complexity	Low	High	Low	Medium	High

It adaptively switches its closed-loop control between digital to analog according to the voltage difference between V_{REF} and V_{REG}. When the voltage error is large during load transient states, the digital control loop is activated. When the voltage error is small, the analog controller takes over to acquire higher PSR and ripple-less voltage. Consequently, the hybrid LDOs can supply ripple-less V_{REG} with significantly high PSR and have good load transient performance at the same time [60], [77], [89]. However, these hybrid LDOs have similar drawbacks of analog LDOs. They typically have a large V_{DO} like analog LDOs, degrading the power efficiency and limiting the regulation range.

Recently, a universal modular-hybrid LDO in 14-nm CMOS was proposed by Intel [104]. The LDO can be efficiently configured to provide any desired combination of PSR, output ripple, load transient response while minimizing power losses and output capacitor usage. With this modular approach, it can resolve the limited-operating-range issue that typical hybrid LDOs inherently cannot avoid, while generating V_{REG} down to 0.7 V from V_{DD} of 1.0 V. However, 300 mV of dropout voltage is still considered too large to achieve a good power efficiency.

VII. COMPARISON OF DLDO ARCHITECTURES

General advantages and disadvantages of all the aforementioned DLDO architectures are summarised in Table. 2. As shown in the table, synchronous DLDOs are easy to design and robust to PVT variations, but they require a large C_{OUT}. Moreover, they also suffer from the power-speed tradeoff, large steady state ripples and poor PSR. With analog-assistance, synchronous DLDOs can improve these performance metrics and eliminate the use of C_{OUT} by using a smaller-sized compensation capacitor (C_C) instead. But, analog-assisted DLDOs still involve the use of C_C which consumes silicon area Asynchronous and event-driven DLDOs can avoid the clock-dependent limitations of synchronous DLDOs and also remove C_{OUT} completely in some cases. Lastly, the hybrid architectures are the most suitable for driving analog load circuits due to their high PSR and ripple-less nature. However, their range of voltage regulation is limited due to their large dropout voltage. Moreover, they are unsuitable for driving digital load circuits when operating in the hybrid mode.

Depending on structural attributes of each DLDO type, their target applications are different. As discussed in Sec. I, DLDOs are typically used in fine-grained power delivery networks of SoCs to power up various types of load circuits. For digital load circuits with low voltage and low current consumption, synchronous DLDOs are typically used [41], [46], [49], [68]. For multi-core processor platforms where fast switching load currents at sub-A/ns levels happen irregularly, analog-assisted DLDOs [97], [98], and asynchronous DLDOs [42], [43], [50], [76] are most suitable because of their fast transient response and large current driving capabilities. Output-capacitor-free DLDOs are the best choice for micro-regulators distributed across a process core [98], because they involve small silicon area and no output pad pins. In addition, they do not have the requirement of minimum C_{OUT} for stability unlike many other LDOs. Any load-induced parasitic capacitance at the output contributes to their load transient performance (voltage undershoot). Hybrid LDOs specifically targets for mixed-signal (analog and digital) load circuits where high PSR and fast load transient response are required simultaneously [102], [104].

Measured performance metrics of best performing LDOs from each architecture are summarised in Table 3. The synchronous DLDO with self-clocking burst logic in [68] downscaled C_{OUT} to 100 pF and achieved a minimum FOM of 75 fs, while consuming minimum I_Q of 0.69 μA. The analog-assisted DLDO in [44] eliminated C_{OUT}, but still used a 100 pF compensation capacitor. The analog-assisted DLDOs [44], [97] achieved very low FOMs at 3.8 and 5.7 fs, respectively. The asynchronous DLDOs in [43], [74] demonstrated a fast transient response time for a large load current step as compared to synchronous and analog-assisted counterparts. The self-shifting asynchronous DLDO in [43] successfully eliminated the C_{OUT} and outperforms synchronous and analog-assisted DLDOs by achieving the minimum FOM of 1.3 fs. The DLDO in [99] downscaled C_{OUT} to 100 pF while driving even larger load current than asynchronous

TABLE 3. Performance comparison of state-of-the-art best performing DLDOs.

	[68]	[52]	[44]	[97]	[76]	[43]	[83]	[99]	[102]	[104]
Architecture	Synchronous		Analog-Assisted		Asynchronous		Event-Driven		Hybrid	
Process [nm]	14	65	65	65	65	65	65	65	130	14
V_{DD} [V]	0.5 – 0.85	0.6 – 1.2	0.5 – 1	0.5 – 1	0.6 – 1	0.7 – 1.2	0.5 – 1	1.2	0.6[1], 1.1–1.2[2]	1 – 1.2
V_{REG} [V]	0.45 – 0.8	0.4 – 1.1	0.45 – 0.95	0.45–0.95	0.55–0.95	0.66–1.16	0.45–0.95	0.5 – 1	0.5–0.55[1], 0.8–1.1[2]	0.7 – 0.85
Max. I_{LOAD} [mA]	11	100	10	105	500	235	5.6	700	12	530
C_{OUT} [nF] ext./int.	0.1 int.	0.04 int.	0.1 int.[3]	0.042 int.	2 int.	Cap-free	0.1 int.	0.1 int.	0.5 int.	4 int.
ΔV_{REG} [mV] @ ΔI_{LOAD} [mA]	122 @ 10	108 @ 50	105 @ 10	185@100	250@500	96 @ 89	49.8@2.3	130@700	240@10	133@508
SR ΔI_{LOAD} [mA/ns]	10 / 4	50 / 2500	10 / 1	100 / 1	500 / 2	89 / 77	2.3 / 0.1	700 / 100	10 / 0.2	1000 / 1
T_R [ns]	110	1240	4000	62	50	77	26	12000	18	300
Load Regulation [mV/mA]	2.2	0.638	2.3	N. R	0.2	0.2	N. R	0.1	N. R	N. R
I_Q [µA]	0.69	100–1070	3.2	4.9	350	116–874	18.1	254	163.2	31.1–53.5
Steady-State V_{RIPP} [mV]	N. R	N. R	3	< 15	5	7.34	Ripple-free	< 20	Ripple-free	Ripple-free
PSR [dB] @ 1 MHz	N. R	-38	N. R	N. R	-9.6	-10	N. R	N. R	-12	-36
Current Efficiency [%]	99.99	97.9	99.97	99.99	99.93	99.86	99.22	99.95	98.5	99.98
Power Efficiency [%]	89.99	78.32	89.97	89.99	91.6	94.16	89.29	83.29	82.08	69.99
FOM [ps]	0.075	1.38	0.23	0.0038	0.7	0.0013	17	0.0067	195.8	0.067
FOM_2 [ps]	0.216	445	0.464	0.019	1.4	0.526	5.18	0.699	35.76	0.108
Normalized FOM_2 [ps]	0.216	0.958	0.099	0.004	0.302	0.113	1.115	0.150	3.851	0.108
Area [mm^2]	0.0035	0.0374	0.034	0.04	0.291	0.069	0.034	0.113	0.082	0.262

[1]Voltage range when LDO operates in only digital mode. [2]Voltage range when LDO operates in hybrid mode.
[3]Compensation capacitor (C_C) is used instead of C_{OUT}.

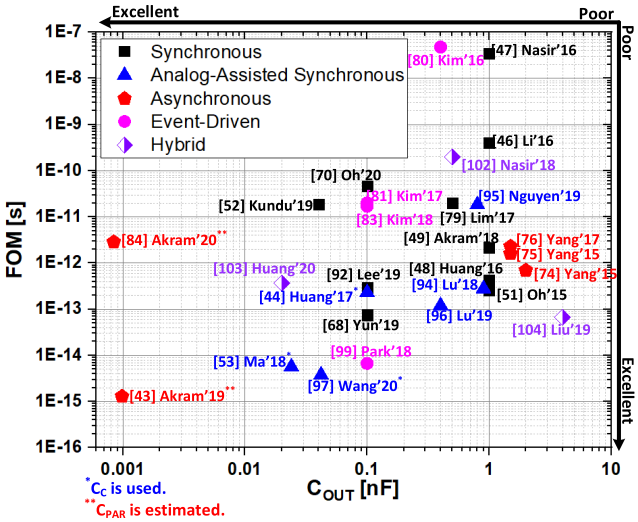

FIGURE 22. FOMs of state-of-the-art DLDOs over C_{OUT}.

DLDOs by utilizing event-driven techniques while achieving a minimum FOM of 6.7 fs. This is the best reported FOM with such large current driving capacity, *i.e.*, 700 mA. As compared to all the other DLDO architectures, the hybrid LDOs have limited operating range and low power efficiencies because of their large dropout voltage.

The best reported FOMs are plotted over the value of C_{OUT} in Fig. 22. When the DLDO does not include C_{OUT}, but C_C, then the value of C_C is used [44], [53]. When the DLDO has neither C_{OUT} nor C_C, parasitic capacitance at V_{REG} is estimated and used [43]. The smaller FOM, and the minimum required C_{OUT} being small are considered good. As it is shown in Fig. 22, synchronous DLDOs do not stand

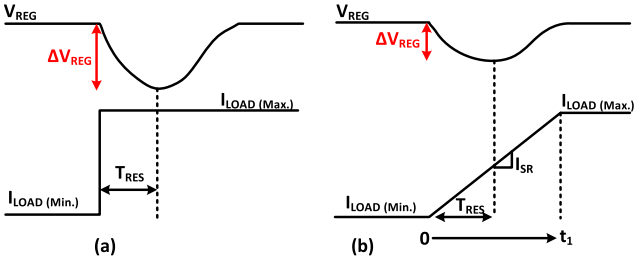

FIGURE 23. Effect of the I_{LOAD} slew rate on the voltage undershoot [79].

out in FOM. The analog-assisted synchronous DLDOs in [97] and [53] achieved the minimum FOMs of 3.8 and 5.7 fs at 24 pF and 40 pF of C_{OUT}, respectively. The self-shifting asynchornous DLDO in [43] showed the minimum FOM of 1.3 fs with no C_{OUT}. In this self-shifting DLDO, C_{OUT} was completely eliminated, so the parasitic capacitances of its switch arrays were estimated to be 0.98 pF, which is used in Fig. 22.

Although this FOM (Eq. (4) and Fig. 22) has been used most widely, it has some limitations [79], [104]. The FOM assumes the load current change ($\Delta I_{LOAD} = I_{LOAD,Max} - I_{LOAD,Min}$) to be instantaneous as shown in Fig. 23 (a). Then, the response time (T_{RES}) of LDO is given as follows:

$$T_{RES} = \frac{C_{OUT} \times \Delta V_{REG}}{\Delta I_{LOAD}} \tag{9}$$

However, the load current does not change instantly, but it changes rather with a finite slew rate I_{SR} as shown in Fig. 23 (b) [79], [104]. I_{SR} for the case in Fig. 23 (b) can be given as follows:

$$I_{SR} = \frac{I_{LOAD,Max)} - I_{LOAD,Min)}}{t_1 - 0}. \tag{10}$$

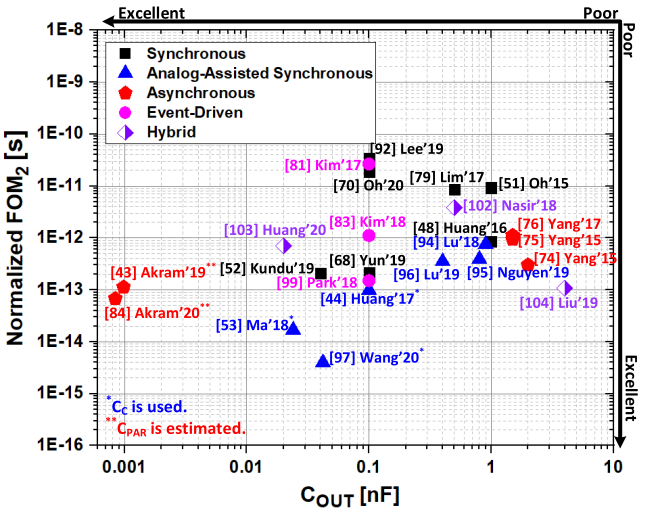

FIGURE 24. Normalized FOM_2 with respect to their CMOS process technology nodes.

As shown in Fig. 23, I_{SR} exerts a great impact on the voltage undershoot (ΔV_{REG}) and also on the overall load-transient response performance. To address this issue, a second FOM including the slew rate was proposed as follows [79]:

$$FOM_2 = \sqrt{\frac{2C_{OUT}\Delta V_{REG}}{I_{SR}}} \times \frac{I_Q}{\Delta I_{LOAD}} \tag{11}$$

In addition to I_{SR}, the CMOS process node should be considered in the benchmarking because the DLDOs compared in Fig. 22 were designed in various CMOS process technologies. For fairer comparison, each FOM should be normalized by their technology node as follows:

$$FOM_2^{\text{normalized}} = \frac{FOM_2}{\alpha} \tag{12}$$

where α is a scaling factor shown below [68]:

$$\alpha = \frac{\text{technology}}{\text{smallest technology}}. \tag{13}$$

$FOM_2^{normalized}$ for the same state-of-the-art DLDOs are shown in Fig. 24. Here the smallest process technology used to calculate α is 14 nm.

VIII. CONCLUSION

LDOs are key enablers to achieve highly efficient fine-grained on-chip power management in SoCs. With the CMOS process downscaling, the design trends of LDOs have been shifted from analog to digital due to severe design challenges of analog circuits in low-voltage environments. DLDOs perform better at low voltage levels. In addition, their digital designs can be synthesized and transported easily to other technologies. The design limitations of typical synchronous DLDOs, such as the power-speed tradeoff, slow load-transient response, large steady-state voltage ripples, and power-supply rejection (PSR) have been well addressed over the years by developing various design techniques and state-of-the-art DLDO architectures. These include clock-boosted synchronous, analog-assisted synchronous, asynchronous, event-driven, and analog-digital hybrid architectures. As discussed in Sec. VI, each of these DLDO architectures achieved best performance metrics at specific conditions. The analog-assisted synchronous DLDOs have faster load transient response as compared to typical and even clock-boosted synchronous DLDOs. The asynchronous and event-driven DLDOs can successfully overcome the clock-dependent limitations of synchronous DLDOs and eliminate C_{OUT} in some cases. The hybrid LDOs combine the strengths of both analog and digital LDOs and successfully achieved better PSR, steady state ripples, and faster load transient response performance, simultaneously.

These best performing DLDOs will be more adopted to be embedded deep inside a large-scale SoC in multiple numbers to realize highly efficient fine-grained power management. Since capacitor-free DLDOs can significantly contribute to cost efficiency by reducing the number of pin counts and board area, capacitor-free structures would be one of main research aims. In addition, synthesizable DLDOs will be further developed as some were recently proposed with promising performance metrics and ease of design and process scalability [105], [106]. To meet two disparate requirements from analog/RF and digital load circuits, hybrid LDOs are also worth pursuing further. Finally, a capacitor-free all-digital DLDO that can meet the stringent requirements of all kind of load circuits would be an ultimate goal of research.

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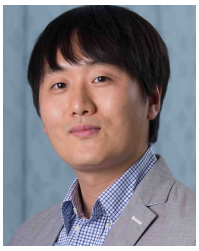

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