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Sub-10 nm Scalability of Junctionless FETs Using a Ground Plane in High-K BOX: A Simulation Study

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ABSTRACT The leakage mechanisms of inefficient volume depletion and lateral band to band tunneling (L-BTBT) restrict the scaling of SOI-junctionless (JL) FETs. Therefore, in this article, we investigate the scalability of the SOI-JLFETs by incorporating a ground plane (GP) inside a high-K buried oxide (BOX). Using calibrated 2-D simulations, it is demonstrated that a SOI-JLFET with the ground plane placed at a shallow depth within the high-K dielectric BOX not only assists in the efficient volume depletion of the channel but also results in a drastically reduced L-BTBT action. The efficient volume depletion, therefore, relaxes the constraints of ultra-thin silicon body for SOI-JLFET and circumvents the need of complex device architectures for achieving the same. Also, the depletion of the drain and source regions jointly results in a drastically reduced L-BTBT induced parasitic BJT action in the OFF-state and in the negative bias regime. The simultaneous suppression of both the leakage mechanisms results in an overall leakage current reduction leading to a significant ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of 10^6 and 10^5 even at the scaled gate length of 10 nm and 7 nm, respectively. Additionally, a significant reduction in the drain-induced barrier lowering and threshold voltage roll-off is observed in a GP-JLFET. The GP-JLFET also exhibits an appreciable I_{ON}/I_{OFF} ratio under the influence of process variations of doping and film thickness without any considerable degradation in the performance. Thus, the suppressed leakage mechanisms and short channel effects in the proposed device provide an incentive for realizing the SOI-JLFETs in the sub-10 nm regime for low power and low-leakage applications.

INDEX TERMS Band-to-band tunneling (BTBT), gate induced drain leakage (GIDL), Junctionless FET (JLFET), parasitic bipolar junction transistor (BJT), drain induced barrier lowering (DIBL).

I. INTRODUCTION

Junctionless FETs (JLFETs) have been explored in recent years as a substitute to the traditional MOSFETs due to their ease of fabrication owing to the absence of junctions discarding the need of complex thermal budgets [1]–[3]. However, the JLFETs exhibit a higher leakage current in the OFF-state ($V_{DS} = 1.0$ V, $V_{GS} = 0.0$ V) owing to an inefficient volume depletion of the heavily doped channel [3] which leads to a conduction path through the center of the body. Therefore, realizing the efficient volume depletion requires either a uniform ultrathin silicon layer or a gate metal work function in an excess of 5.5 eV for depleting the heavily doped silicon film [3]–[7]. Such a nanostructured uniform film is more prone to inevitable process variations. Moreover, realizing the efficient volume depletion leads to the band overlap of the channel region valence band with the drain region conduction band resulting in another leakage mechanism namely lateral band-to-band tunneling (L-BTBT). The lateral tunneling of the electrons from the channel to the drain region in the OFF-state results in the BTBT generated holes in the channel which actuates a parasitic N-P-N bipolar junction transistor (BJT) in the lateral direction [3]–[6]. The parasitic BJT action significantly increases the OFF-state current and is, therefore, the dominant leakage mechanism in SOI-JLFETs in OFF-state and for negative gate voltages. In the sub-10 nm regime, it is quite difficult to realize volume depletion of the channel resulting in a high leakage current even at a reduced drain bias ($V_{DS} = 0.5$ V) [6]. The highlighted leakage mechanisms hinder the scalability of JLFETs, leading to an unacceptable I_{ON}/I_{OFF} ratio in the sub-10 nm regime.

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Therefore, in this work, we investigate the application of ground plane (GP) within the high-K HfO_2 BOX for the scalability of the SOI-JLFETs for low leakage and low power applications. The technique of ground plane has been used in past to improve the performance of the nanoscale SOI-MOSFETs [8]–[14]. The ground plane in SOI-MOSFETs prevents the encroachment of the electric field lines originated from the drain into the channel region. This helps in minimizing the short-channel effects such as DIBL as the GP acts like a sink to the drain electric field in a SOI-MOSFET [8]. Furthermore, the ground plane technique has also been explored for tunnel FETs (TFETs) to reduce their ambipolar current [15]. However, the performance of JLFETs in the sub-10 nm regime using the application of GP has not been investigated. Our study shows that the deployment of a ground plane within high-K BOX in a JLFET facilitates the depletion of the drain-extension region which consequently reduces the peak electric field and leads to the electric field redistribution. This significantly enhances the tunneling width at the drain-channel interface which consequently suppresses L-BTBT. Furthermore, the simultaneous depletion of the extension regions and channel by the ground plane also facilitates the efficient volume depletion of the active silicon film. This relaxes the need of ultra-thin silicon films which is, otherwise, required for realizing the efficient volume depletion in SOI-JLFETs [16]. The previously reported work on SOI- JLFET with a high-k BOX [7] was only analyzed for a gate length of 20 nm and not for the ultra-short channel in the sub-10 nm regime where the device is highly susceptible to short-channel effects. Furthermore, the impact of L-BTBT has not been analyzed in [7] which is the dominant leakage mechanism in JLFETs [4], [5] and therefore, cannot be overlooked. Therefore, this work investigates an efficient way of simultaneously improving both the leakage mechanisms of volume depletion and L-BTBT for the ultra-short channel SOI-JLFETs and therefore overcome the major bottlenecks in the scaling of JLFETs. Our study explains the physics governing the improved performance of the JLFETs due to the ground plane even in the sub-10 nm regime which helps in the amelioration of the short-channel effects of drain-induced barrier lowering and threshold voltage roll-off. Furthermore, our analysis also shows that the drain-bias sensitivity of the L-BTBT induced leakage is also reduced in the proposed GP-JLFET. From calibrated 2-D simulations, our results show that the incorporation of GP at a shallow depth from the active silicon film leads to more efficient volume depletion of the silicon film. Moreover, it also presents a sustainable immunity against the process variations of film thickness and doping along with the reduced short channel effects. The depletion of the film at the drain-extension side due to GP leads to a reduction of the peak electric field at the drain-channel interface. This consequently increases the tunneling width and therefore, addresses the leakage issue of L-BTBT at the scaled gate lengths. Additionally, the depletion of the source extension region due to GP increases the source-channel barrier height which further prohibits the activation of the parasitic BJT. The proposed GP-JLFET exhibits an OFF-state reduction by 5 orders of magnitude leading to an enhanced I_{ON}/I_{OFF} ratio of 10^8 for a gate length of 20 nm. Moreover, the OFF-state current reduces by more than 4 orders of magnitude even when the gate length is scaled to sub-10 nm regime resulting in a significant I_{ON}/I_{OFF} ratio of 10^6 and 10^5, for a gate length of 10 nm and 7 nm, respectively.

We also demonstrate that the GP-JLFET exhibits a reduced threshold voltage roll-off and DIBL at the scaled gate lengths owing to the reduced coupling of the electric field lines of the drain with the source/channel region. Thus, the employment of a GP at a shallow depth inside the high-K BOX efficiently reduces the aforementioned leakage mechanisms and short channel effects and improves the scalability of the SOI-JLFET to the sub-10 nm regime. This makes the proposed device quite lucrative for the low-power and low-leakage applications, specifically for internet of things (IoT) and automotive applications where the ultra-low power consumption is highly desirable to support a long battery life essential for their wireless sensor nodes [17], [18].

II. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The schematic illustration of a GP-JLFET with a high-K BOX is shown in Fig. 1. The GP-JLFET architecture is essentially a SOI JLFET with a ground plane (GP) at a shallow depth d_{GP} inside the high-k HfO_2 BOX. While a majority of publications and in particular, ref. [19] have highlighted various methods to obtain SiO_2 BOX wafers, there are also reported works which have explored the potential benefits of high-k dielectric as the BOX [20], [21]. The use of Al_2O_3 as a BOX has been experimentally demonstrated for III-V on insulator resulting in an improved performance [22]. Since the SiO_2 BOX wafer process is well established, realizing HfO_2 BOX wafers with a ground plane using the smart-cut method should not encounter any unexpected difficulty. Using the detailed process flow as described in [19] for the fabrication of SiO_2 BOX wafers, we have proposed a process flow using the smart-cut process as shown in Fig. 3. The suggested process begins with a bare silicon substrate on which the high-K HfO_2 film is deposited using atomic layer deposition (ALD) or plasma enhanced chemical vapor deposition (PECVD) (Fig. 2(a) and 2(b)). This is followed by the deposition of

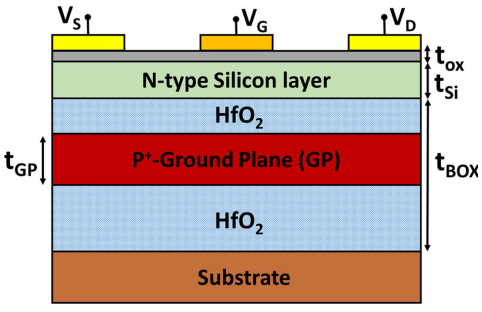

FIGURE 1. Schematic illustration of a GP-JLFET with high-K BOX.

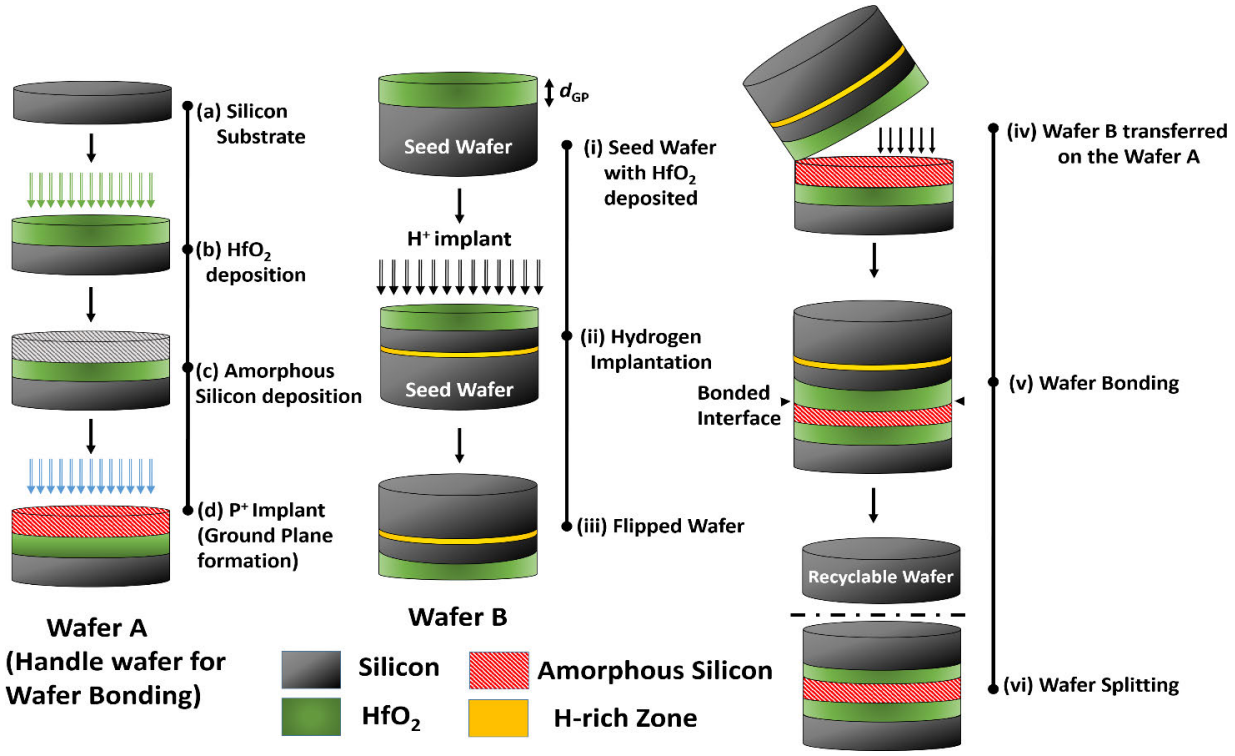

FIGURE 2. Suggested fabrication process flow based on the Smart Cut process to realize the high-K BOX SOI substrate with a ground plane.

amorphous silicon using thermal CVD (Fig. 2(c)). The amorphous silicon is then implanted with boron to form a P^+ ground plane. We refer the prepared wafer as wafer A which will serve as a handle wafer for the smart cut process. On the other hand, the wafer to be transferred on the handle wafer is referred as wafer B with the required process steps depicted from (i) to (iii) in Fig. 2. Firstly, the crystalline seed wafer is taken and deposited with the HfO_2 of the required thickness (d_{GP}). This is followed by the implantation of the hydrogen ions through the oxide typically at a dose of around 10^{16}-10^{17} cm^{-2}. Hydrogen ion implantation plays a role of an atomic scalpel in the smart cut process that enables thin slices of monocrystalline film to be cut from a seed wafer and transferred on top of a handle wafer. The wafer B formed after hydrogen implantation is then flipped and bonded to wafer A using a fusion process (2(iv)) where the two wafers are held together due to atomic attraction forces (Vander Waals' forces). Bonding between the high-K dielectric and silicon can be achieved using the technique of surface activated bonding (SAB) by irradiation of Ar beam which is well suited for the wafer bonding of high-k materials to Si wafer [10]. The wafer bonding is followed by the two-phase heat treatment. During first heat treatment at $\sim$ 400-600°C, the implanted wafer A splits along the H-rich zone giving rise to an SOI wafer with an incorporated ground plane (Fig. 2(v) and Fig. 2(vi)). The remainder of the seed wafer can be recycled through a chemical mechanical step as a new handle wafer. The second-high temperature treatment phase (around 1100°C) strengthen the chemical bonds between the two substrates. Finally, a CMP process smoothens the wafer surface.

The 2-D simulations are performed using the Sentaurus device simulator (release I-2013.12) [23]. Various models invoked in the simulation set up are Lombardi mobility model and Philips unified mobility model. Bandgap narrowing effects are included using Slotboom model. Fermi-Dirac statistics, Auger recombination, and Shockley—Reed–Hall recombination are also enabled. For considering L-BTBT, a nonlocal band-to-band tunneling is used [23], which is a well-established TCAD model and has been extensively used to investigate the ambipolar tunneling leakage mechanisms in TFETs [15], and lateral band-to-band-tunneling in SOI-JLFETs [5], nanowire JLFETs [24] and nanotube JLFETs [25]. Furthermore, we have not invoked any direct tunneling model to account for gate leakage through the gate dielectric in our simulations as also done in the previously reported works on SOI-JLFETs [5], [16]. The simulation set-up was well calibrated from the results reported in [5], as shown in Fig. 3(b). The simulation setup was first calibrated with the experimental results of a long-channel (1 μm) JLFET [1] as shown in Fig. 3(a), in which the BTBT-induced parasitic BJT action is not dominant Then, a nonlocal tunneling model is invoked and calibrated to account for lateral band to band tunneling in JLFETs as done in [3]–[5]. The parameters used for the device simulations are listed in Table 1.

TABLE 1. Device parameters used for the simulations.

Parameter	SOI- JLFET	GP- JLFET
Channel doping (N_{Ch})	$1x10^{19}$ cm^{-3}	$1x10^{19}$ cm^{-3}
Gate oxide (SiO_2) thickness (t_{ox})	1 nm	1 nm
Silicon film thickness (t_{Si})	10 nm	10 nm
Gate length (L_g)	7 nm - 20 nm	7 nm - 20 nm
Gate Work function	5.1 eV	5.1 eV
Thickness of GP (t_{GP})	10 nm	10 nm
BOX dielectric	SiO_2	HfO_2
BOX thickness (t_{BOX})	60 nm	60 nm
GP Doping (N_A)	10^{20} cm^{-3}	10^{20} cm^{-3}
Depth of GP (d_{GP})	4 nm-10 nm	4 nm- 10 nm

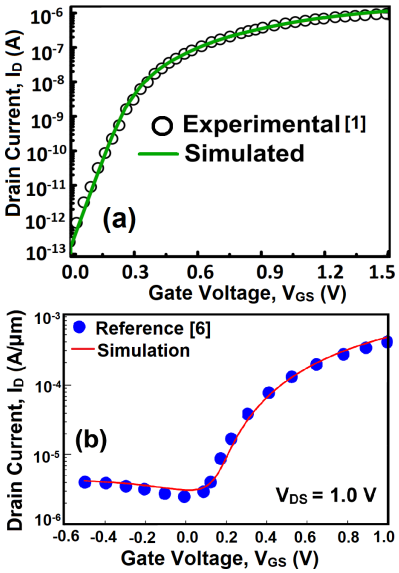

FIGURE 3. (a) Simulation models calibrated by reproducing the experimental results of a long channel JLFET reported in [1]. (b) Using the calibrated models of (a), the non-local BTBT model is next calibrated by reproducing the results of [5].

III. RESULTS AND DISCUSSIONS

The transfer characteristics of a conventional SOI-JLFET with a ground plane inside the SiO_2 BOX for a silicon thickness of 6 nm and 10 nm are shown in Fig. 4. We can observe from Fig. 4 that the SOI-JLFET with a GP inside the SiO_2 BOX exhibits a higher leakage for a t_{Si} of 10 nm which is attributed to L-BTBT and inefficient volume depletion. However, the OFF-state leakage current even for a silicon film thickness of 6 nm is still of the order of 10^{-6} A/μm leading to a poor I_{ON}/I_{OFF} ratio of $\sim 10^2$ for a gate length of 20 nm. This is attributed to the L-BTBT induced parasitic BJT action which enhances the OFF-state current even after volume depletion. On the other hand, the GP- JLFET with a high-K BOX exhibits a drastic reduction in the OFF-state leakage by 6 orders of magnitude leading to a significant I_{ON}/I_{OFF}

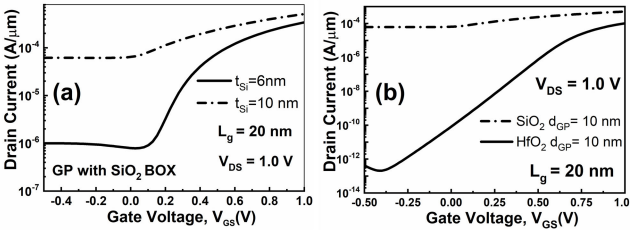

FIGURE 4. Transfer characteristics of (a) SOI-JLFET with SiO_2 BOX and (b) GP-JLFET with a GP in HfO_2 BOX. (c) Output characteristics of GP-JLFET.

ratio of 10^7 for a gate length of 20 nm with a t_{Si} of 10 nm as shown in Fig. 5(a). The drain current in GP-JLFET reduces with negative gate voltages whereas the drain current of SiO_2 BOX based SOI JLFET is independent of the gate voltage for $V_{GS} \leq 0.0$ V. The underlying physics for the improved performance is attributed to the reduced L-BTBT induced parasitic BJT action and can be understood with the help of OFF-state energy band profiles as shown in Fig. 5(b). The P^+ ground plane that spans from the source to drain inside the high-K dielectric not only depletes the channel but also leads to the depletion of the source and drain extension regions. The depletion of the drain extension region increases the tunneling width at the drain-channel interface. Unlike the conventional SOI JLFETs where the peak electric field in OFF-state is concentrated near the drain-channel interface, the depletion of the drain extension region in a GP-JLFET results in the redistribution of the electric field leading to a reduced field near the drain-channel interface as evident from Fig. 6. This is reflected as a gradual band bending at the drain-channel interface in the energy band profiles which consequently increases the tunneling width for the electrons at the channel-drain extension interface as evident from Fig. 5(b). This leads to a reduced L-BTBT which in turn suppresses the hole generation rate (Fig. 9) in the channel region of GP-JLFET. The hole concentration contour plot shown in Fig. 7 and Fig. 8 is suggestive of this. The hole concentration in the channel region of SOI-JLFET with the SiO_2 BOX (Fig. 7(a) and Fig. 8(a)) is higher than GP-JLFET with the high-K BOX (Fig. 7(b) and Fig. 8(b)). This diminished hole concentration prevents the internal biasing of the source-channel junction (emitter-base junction of the lateral parasitic BJT) leading to a significantly reduced parasitic BJT action. Moreover, the depletion of the source extension region by the GP leads to an increased barrier at the source-channel interface which further hinders the activation of the parasitic BJT. All these factors jointly lead to a diminished parasitic BJT action in GP-JLFET with a high-k BOX. The GP-JLFET with GP placed at the shallow depth inside the high-K BOX shows a further improvement in the OFF-state performance. As shown in Fig. 5(a), the GP with a reduced d_{GP} exhibits: (i) a reduced leakage for the same gate length due to improved coupling of the GP with active silicon resulting in an enhanced depletion of the silicon film and (ii) a reduced L-BTBT in OFF-state as well as in negative gate bias regime due to an increased tunneling

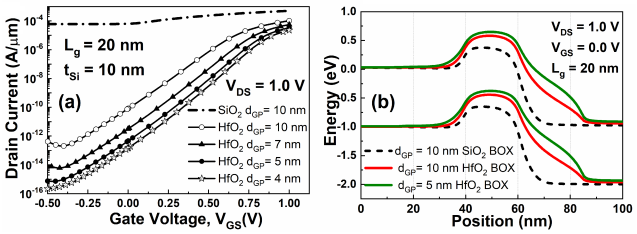

FIGURE 5. (a) Transfer characteristics of GP-JLFET with a high-K BOX (b) Energy band profiles in the OFF-state for a gate length of 20 nm.

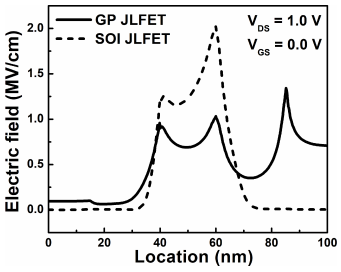

FIGURE 6. Electric field profile of the SOI JLFET and GP-JLFET in the OFF-state (V_{DS} = 1.0 V and V_{GS} = 0.0 V) for a gate length of 20 nm.

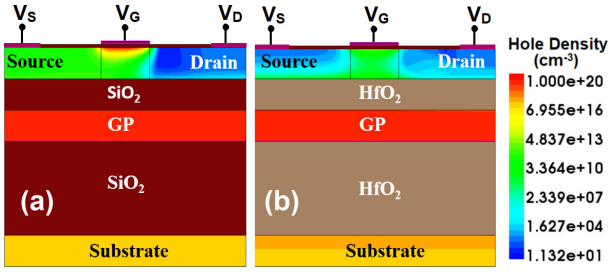

FIGURE 7. Hole concentration contour plot for (a) SOI- JLFET (b) GP-JLFET in the OFF-state (V_{GS} = 0.0 V and V_{DS} = 1.0 V).

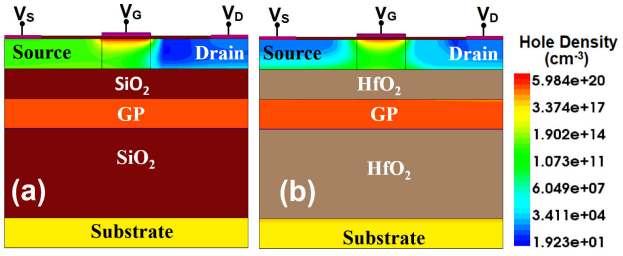

FIGURE 8. Hole concentration contour plot for (a) SOI- JLFET with SiO_2 BOX (b) GP-JLFET in the OFF-state (V_{GS} = −0.5 V and V_{DS} = 1.0 V).

width at the drain-channel interface. Moreover, the presence of an enhanced barrier at the source-channel interface further prevents the electrons from the source to surmount the barrier and therefore, sustains the efficient volume depletion of the channel. Thus, the GP-JLFET with high-k BOX considerably relaxes the constraint of ultra-thin silicon film and shows superior performance even at the silicon thickness of 10 nm.

We have also analyzed the output characteristics of GP-JLFET as shown in in Fig. 10. A higher source-channel

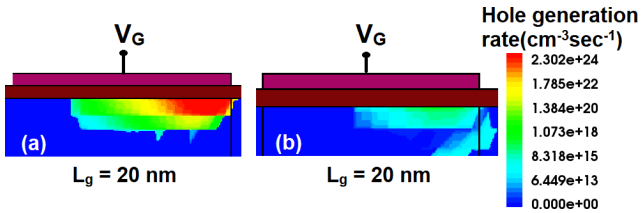

FIGURE 9. L-BTBT-induced hole generation rate in (a) SOI- JLFET (b) GP-JLFET in the OFF-state (V_{GS} = 0.0 V and V_{DS} = 1.0 V) for L_g = 20 nm.

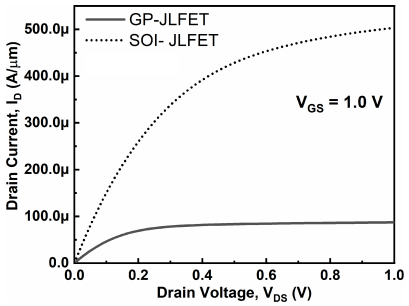

FIGURE 10. Output characteristics of SOI-JLFET and GP-JLFET.

barrier in GP-JLFET leads to a higher threshold voltage resulting in a lower saturation current (I_{DSAT}) as evident from Fig. 10. However, the extension of the ground plane below the drain-extension region in the GP-JLFET with high-K spacer helps in achieving an effective pinch-off of the electron conduction path which is desirable as shown in Fig. 11. This results in a better saturation of the drain current in GP-JLFET compared to SOI-JLFET.

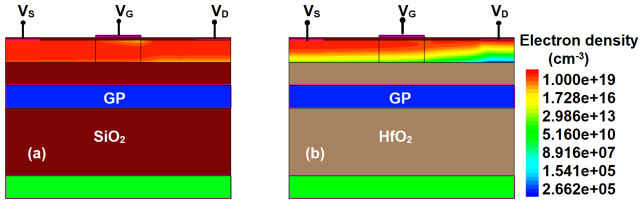

FIGURE 11. Electron concentration contour plot of (a) SOI-JLFET and (b) GP-JLFET in the ON-state (V_{GS} = 1.0 V and V_{DS} = 1.0 V).

We have also analyzed the performance of GP-JLFETs with different ground plane doping as shown in Fig. 12.

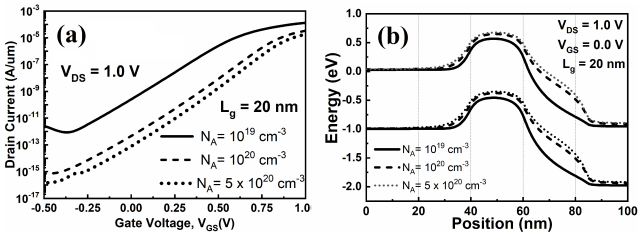

FIGURE 12. (a) Transfer characteristics and (b)) Energy band profiles in the OFF- state of GP-JLFET for various dopings of the ground plane.

As can be observed from Fig. 12(a), the ground plane with a higher doping is relatively more effective leading to a reduced OFF-state current. This is reflected in the OFF-state energy band profiles (Fig. 12(b)) where the tunneling width at the channel-drain interface is higher for a GP-JLFET with a heavily doped ground plane compared to a lightly doped ground plane. The ON-state current also reduces slightly with the increase in ground plane doping but the reduction in the OFF-state current is remarkable leading to an overall enhanced I_{ON}/I_{OFF} ratio. Thus, the OFF-state current is quite sensitive to the ground plane doping and therefore, the ground plane should be heavily doped to maintain a significantly low OFF-state current. Moreover, we have also compared the performance of the GP-JLFET when ground plane is at the bottom of the high-K BOX. The improvement in the electrostatics is not observed when the GP is placed at the bottom of high-K BOX as shown in Fig. 13. Thus, the ground plane is only effective when placed at a shallow depth (d_{GP}) from the active silicon layer.

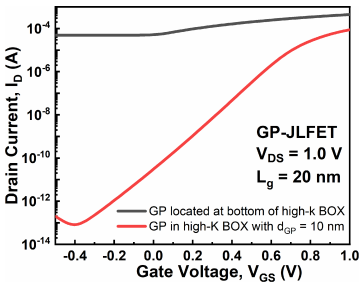

FIGURE 13. Transfer characteristics of a GP-JLFET with ground plane at the bottom of high-k BOX and with a d_{GP} of 10 nm in BOX.

The JLFETs are quite sensitive to process variations and, therefore, exhibits a significantly degraded performance if the silicon film doping and thickness are more than the intended values [26]–[28]. The poor I_{ON}/I_{OFF} ratio of the SOI-JLFET due to an increase in the film thickness is evident from Fig. 4. However, as shown in Fig. 14, the GP-JLFET with high-K BOX exhibits (a) an appreciable I_{ON}/I_{OFF} of 10^6 when the film thickness increases by 20 % (i.e. $t_{Si} = 12$ nm) and (b) an appreciable I_{ON}/I_{OFF} of 10^7 when the film doping increases by 20 % (i.e. $N_D = 1.2 \times 10^{19}$ cm^{-3}). Thus, the GP-JLFET exhibits a sustainable performance even when there is an unintentional increase in either film thickness or doping, making it immune to process induced variations.

The electrostatic potential contours of the two configurations in the OFF- state are shown in Fig. 15. It can be observed that for the SOI-JLFET, there is a direct and strong coupling of the electric field lines from the drain side to the source as can be seen from Fig. 15(b) and (d). However, in the case of the GP JLFET, the direct coupling of the electric field lines is minimized. The GP in a high-K BOX reduces the direct encroachment of electric field lines from the drain to the source, as shown in Fig. 15(a). The coupling reduces with the reduction in d_{GP} as decreasing the d_{GP} further screens the channel against penetration of the drain field into the source

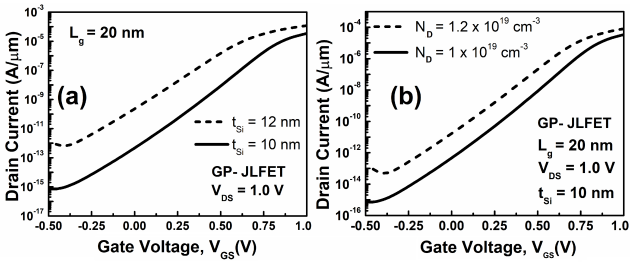

FIGURE 14. Transfer characteristics of the GP-JLFET for 20 % increase in (a) silicon film thickness and (b) silicon film doping.

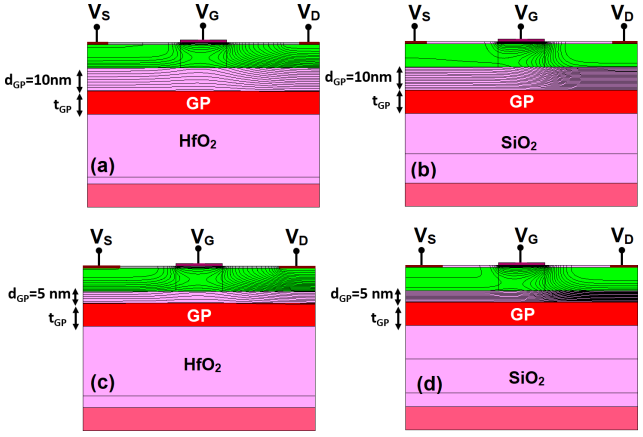

FIGURE 15. Electrostatic potential contour of GP-JLFET and SOI- JLFET for the d_{GP} of 10 nm and 5 nm.

due to stronger influence of the GP from the bottom via high-K BOX as shown in Fig. 15(c). The reduced direct coupling consequently diminishes the drain induced barrier lowering (DIBL) as shown in Fig. 16 and, hence, improves in the SCE suppression in the GP JLFETs.

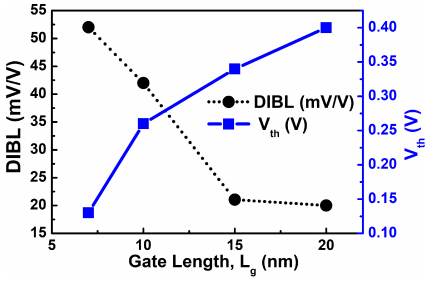

FIGURE 16. DIBL and V_{th}-roll-off of GP-JLFET at the scaled gate lengths.

IV. SCALABILITY ANALYSIS OF GP-JLFET

We have also analyzed the performance of the GP-JLFET with high-K BOX to check their efficacy at the scaled gate lengths. The GP-JLFET exhibits a reduced hole generation rate even at the scaled gate lengths owing to reduced L-BTBT as shown in Fig. 17. This shows that the GP-JLFET with high-K BOX is effective in suppressing the L-BTBT when the gate lengths are scaled to even sub-10 nm regime. The transfer characteristics of the proposed device at the scaled gate lengths are shown in Fig. 18(a). As shown in Fig. 18(a), the proposed device exhibits a reduced I_{OFF} of $\sim 10^{-11}$ A/μm

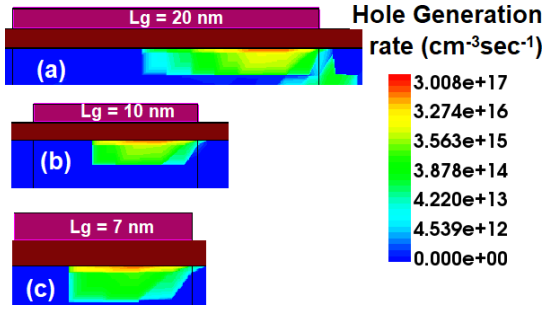

FIGURE 17. L-BTBT induced hole generation rate in GP-JLFET at the scaled gate lengths.

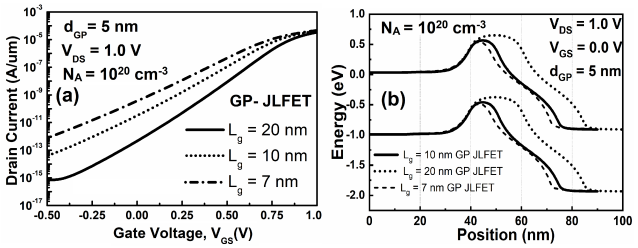

FIGURE 18. (a) Transfer characteristics of GP-JLFET with high-K BOX at scaled gate lengths. (b) Energy band profiles in the OFF- state for various gate lengths taken at a cutline 1 nm below the Si/SiO_2 interface.

and 10^{-10} A/μm for a gate length of 10 nm and 7 nm, respectively with a t_{Si} of 10 nm which is at par with a conventional SOI-JLFET. This leads to an appreciable I_{ON}/I_{OFF} ratio of 10^6 and 10^5 for a gate length of 10 nm and 7 nm, respectively. The remarkable performance at scaled gate lengths are attributed to increased tunneling width and higher source to channel height as can be observed from the OFF-state energy band profiles in Fig. 18(b). Thus, the GP-JLFET exhibits a superior performance even at the scaled gate lengths and therefore, circumvents the need of scaling the channel thickness.

We have also analyzed the short channel effects in GP-JLFETs such as DIBL and V_{th} roll-off. The DIBL is computed at the constant drain current of 1nA/μm [15] using the equation:

$$DIBL = \frac{V_{GS}\ (V_{DS} = 0.05V) - V_{GS}\ (V_{DS} = 1.0V)}{1 - 0.05} \quad (1)$$

The DIBL is approximately 21.05 mV/V, 42.1 mV/V and 52 mV/V for the gate lengths of 15 nm, 10 nm, and 7 nm, respectively, as shown in Fig. 16. The threshold voltage at scaled gate lengths is also shown in Fig. 16. The V_{th} roll-off is calculated as

$$\Delta V_{th} = V_{th}\left(L_{g1}\right) - V_{th}(L_{g2}) \quad (2)$$

where $L_{g1} = 20$ nm and L_{g2} is the scaled gate length. The Vth roll-off comes out to be 0.14 V for $L_{g2} = 10$ nm. However, the gain in the OFF-state performance and improved short channel effects for our proposed device comes at the expense of the degraded subthreshold swing. This is attributed to the higher capacitance between the channel and the ground plane owing to the high-K dielectric constant of HfO_2. The subthreshold swing for the SOI FET is given by:

$$S = (1 + \alpha).kT/Q.\ln(10) \quad (3)$$

where kT/q is the thermal voltage, and α is the ratio of the capacitance between the active channel and the ground substrate to the gate capacitance [8], [26]. For a GP-JLFET, the capacitance between the active channel and ground plane (C_{GP-Ch}) is high owing to the high-K dielectric of the BOX above the ground plane. For a steeper subthreshold swing, a smaller C_{GP-Ch} is required which can only be obtained by either increasing the BOX thickness or replacing the BOX material with a low-K dielectric. However, either way, it will adversely increase the leakage mechanisms of volume depletion and L-BTBT which deteriorates the functionality and scaling of JLFETs. Thus, there exhibits a trade-off between the subthreshold swing and OFF-state performance of the GP-JLFET but the reduced short-channel effects and the superior OFF-state performance even for the sub-10 nm regime with a significant I_{ON}/I_{OFF} ratio makes the proposed device quite lucrative for the low-power and low-leakage applications where the ultra-low power consumption is highly desirable to support a long battery life essential for their wireless sensor nodes [17], [18].

The transfer characteristics of GP-JLFET and SOI-JLFET for various drain biases at a gate length of 7 nm are shown in Fig. 19. The drain current in SOI-JLFETs is quite sensitive to the drain-bias in the OFF-state and negative gate voltages. The drain-bias sensitivity of the OFF-state current at the gate length of 7 nm is shown in Fig. 20. The OFF-state current increases about an order of magnitude for SOI-JLFET with an increase in drain bias. However, the sensitivity of the OFF-state current to drain bias is quite reduced in the proposed. GP-JLFET. While the L-BTBT is not initiated at a low drain bias of 0.5 V, a higher V_{DS} (> 0.7 V) leads to an increased L-BTBT. However, in the GP-JLFET, the L-BTBT is significantly suppressed leading to a reduced sensitivity of the OFF-state current to the drain bias. The I_{ON}/I_{OFF} ratio of GP-JLFET as a function of drain bias is shown in Fig. 21 which clearly shows that the GP-JLFET exhibits a marginal reduction in I_{ON}/I_{OFF} with the rise in drain bias.

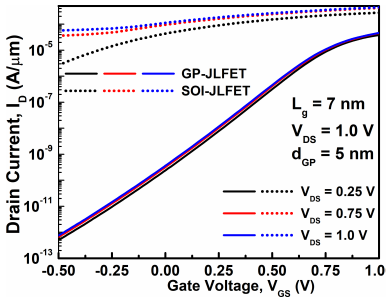

FIGURE 19. Transfer characteristics of GP-JLFET and SOI-JLFET for a gate length of 7 nm for different drain biases.

We have also analyzed the performance of GP-JLFET for a scaled silicon thickness of 6 nm as shown in Fig. 22.

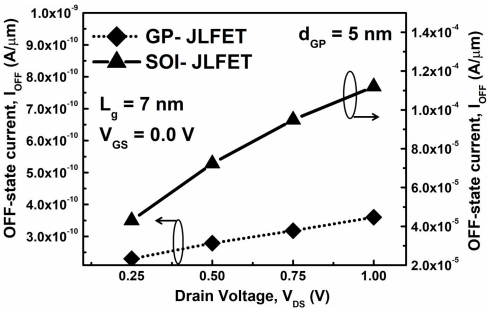

FIGURE 20. Drain-bias sensitivity of OFF-state current in GP-JLFET and SOI-JLFET.

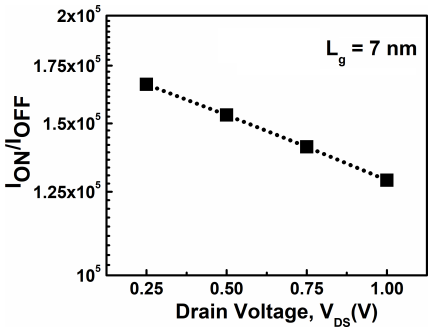

FIGURE 21. I_{ON} /I_{OFF} of GP-JLFET as a function of drain bias.

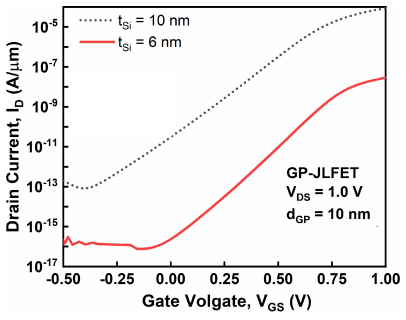

FIGURE 22. Transfer characteristics of GP-JLFET for silicon thickness of 6 nm and 10 nm for a gate length of 20 nm.

The GP-JLFET with a reduced silicon thickness exhibits a slightly better subthreshold swing due to better electrostatic gate control over the thin silicon film. However, the ground plane strongly depletes the thin silicon film due to which the device remains in the depleted state even on the application of the positive gate bias. This leads to a much-degraded ON-state current which is lower by 3 orders of magnitude compared to GP-JLFET of 10 nm silicon thickness even for a V_{GS} of 1.0 V. Therefore, at scaled silicon film thickness, the GP-JLFET exhibits a very poor ON-state current without any remarkable improvement in the subthreshold swing.

We have also compared the performance of the proposed GP-JLFET with the emerging 3D-FET architectures as shown in Table 2. The comparison shows that the normalized OFF-state current of the GP-JLFET and I_{ON}/I_{OFF} ratio is relatively better compared to the emerging complex 3-D device architectures such as conventional gate all around nanowire (NW) JLFETs [24] as well as core -shell

TABLE 2. Performance comparison of the proposed architecture with the emerging 3-D JLFET architectures.

Device architecture	OFF-state Current		I_{ON}/I_{OFF}	
	L_g = 20 nm	L_g = 10 nm	L_g = 20 nm	L_g = 10 nm
Conventional GAA NW JLFET [24]	~10^{-11} A/μm	~10^{-10} A/ μm	~10^{6}	~10^{5}
Conventional NT JLFET [25]	4.2 x 10^{-10} A/μm	35 x 10^{-9} A/μm	~10^{6}	~10^{4}
GP-JLFET (This work)	4x10^{-13} A/ μm	10^{-11} A/ μm	10^{8}	10^{6}

TABLE 3. Performance comparison of the proposed architecture with the other reported junctionless architectures in literature.

Device architecture	Gate Length (L_g)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}
SOI JLFET	20 nm	10^{-4}	~10
Gaussian doped SOI JLT (GDP SOI JLT) [29]	20 nm	1.4 x 10^{-8}	2.2 x 10^{6}
JLFET with spacers [30]	20 nm	~ 10^{-10}	~10^{7}
This Work	20 nm	4 x 10^{-13}	10^{8}
Bulk Planar JLFET [16]	10 nm	~ 10^{-7}	~10^{3}
This Work	10 nm	~ 10^{-11}	10^{6}

nanotube (NT) JLFETs [25] for an active silicon device layer thickness (t_{Si}) of 10 nm. Thus, our proposed device shows a comparatively improved OFF-state performance and I_{ON}/I_{OFF} ratio compared to the conventional 3-D JLFET architectures.

We have also compared the performance of the GP-JLFET with respect to the other reported planar JLFET architectures in the literature as shown in Table 3. The proposed GP-JLFET shows significant performance improvement in OFF-state current and I_{ON}/I_{OFF} ratio compared to the previously reported device architectures even at a scaled gate length of 10 nm which is mainly attributed to the suppression of parasitic BJT action in the OFF-state.

V. CONCLUSION

In this article, a JLFET with a ground plane is proposed to facilitate the scaling of the SOI-JLFETs to sub-10 nm regime. Our well-calibrated 2-D simulation results demonstrate that the GP-JLFET with high-K dielectric BOX exhibits a drastically reduced OFF-state current leading to an extremely high I_{ON}/I_{OFF} ratio of ~ 10^{6} and 10^{5} for a gate length of 10 nm and 7 nm, respectively. The GP-JLFET exhibits a drastically reduced parasitic BJT action even when the gate length is scaled to 7 nm. The proposed GP-JLFET architecture also

exhibits suppressed short channel effects such as V_{th} roll-off and DIBL and a reduced drain bias sensitivity of the leakage current proving the efficacy of the device for scaled technology nodes. The mitigated parasitic BJT action is attributed to the suppressed L-BTBT and efficient volume depletion, thereby relaxing the need for thickness scaling and use of complex architectures. The proposed device also shows better performance even with the process variations of silicon film thickness and doping. Thus, the superior OFF- state characteristics of GP-JLFET even for sub-10 nm channel lengths make it very lucrative as a future device for low-power and low-leakage applications, specifically for internet of things (IoT) and automotive applications where the ultra-low power consumption is desirable. The interesting attributes explored through the employment of a ground plane inside the high-K BOX for realizing the nanoscale SOI-JLFETs are, therefore, worth experimenting.

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