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An Improved Dimensional Measurement Method of Staircase Patterns With Higher Precision in 3D NAND

PEIZHEN HONG[1,2], (Member, IEEE), ZHIGUO ZHAO[1,3], JUN LUO[1,2,4], ZHILIANG XIA[1,2,3], XIAOJING SU[2,4], LIBIN ZHANG[4], CHUNLONG LI[1], AND ZONGLIANG HUO[1,2,3], (Member, IEEE)

[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
[2]College of Microelectronics, University of Chinese Academy of Sciences, Beijing 100049, China
[3]Yangtze Memory Technologies Company Ltd., Wuhan 430205, China
[4]Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Corresponding authors: Chunlong Li (lichunlong@ime.ac.cn) and Zongliang Huo (huozongliang@ime.ac.cn)

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ABSTRACT 3D NAND is a great architectural innovation in the field of flash memory. The staircase for control gate is a unique and important process in the manufacturing of 3D NAND. The staircase is employed to form the electrical connection between the control gate and contact. The current method used to measure the dimension of staircase patterns is, however, not precise enough for the development of state-of-the-art 3D NAND. In this circumstance, an accurate measurement of dimension for as-formed staircase patterns is of great importance and technical interest. In this paper, an improved measurement method is proposed to meet the requirement for higher precision. By taking the overlay into account, a calculation formula for measuring the dimensional error of as-formed staircase is derived for the first time. Two kinds of anchor design (convex SS0 and concave SS0) are put forward to perform dedicated experiments. Achieved results show that the measurement error of as-formed staircase using this improved method is improved from 31.6 nm for normal measurement method to 14.1 nm. The dimensional uniformity of as-formed staircase is therefore improved significantly which in turn leads to well controlled word line leakage. Furthermore, in advanced staircase structure of stair divided scheme (SDS), the convex SS0 shows an advantage in cost compared to the concave SS0.

INDEX TERMS 3D NAND, staircase, large dimension measurement, high precision.

I. INTRODUCTION

The 3D NAND has become a mainstream technology in flash memory [1]–[6]. However, with the increase of the stack numbers, more and more challenges have been arising in the manufacturing of 3D NAND, such as the control of multi-layer thickness [7], precision and cost for forming staircase patterns [8]–[11], etch of channel hole with ultra-high aspect ratio [12]–[15], stress engineering [16]–[18], and defect detection [19] *etc*. Among them, the formation and measurement of staircase patterns precisely is a more and more challenging task as the evolution of 3D NAND technology. As a result, this paper mainly focuses on this issue.

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As well known, the thick photoresist (PR) plays an important role in forming the staircase patterns of control gate in 3D NAND [20]–[22]. To be specific, the coating of thick PR is followed by the depositions of SiO_2 and Si_3N_4 (ON) multilayers on Si wafers. After the thick PR is exposed, trimming and etching are repeated to make stairs. These multiple trim-etch repetitions improve the efficiency and reduce the cost greatly for fabricating the staircase [1].

In this fabrication process of staircase, a lot of challenges and issues need to be solved. Huang *et al.* [8] investigated the uniformity control of CD (critical dimension) of the thick PR in a staircase and concluded that the optimized profile of PR could significantly improve the uniformity of both ADI CD (after development inspection critical dimension) and AEI CD (after etch inspection critical dimension).

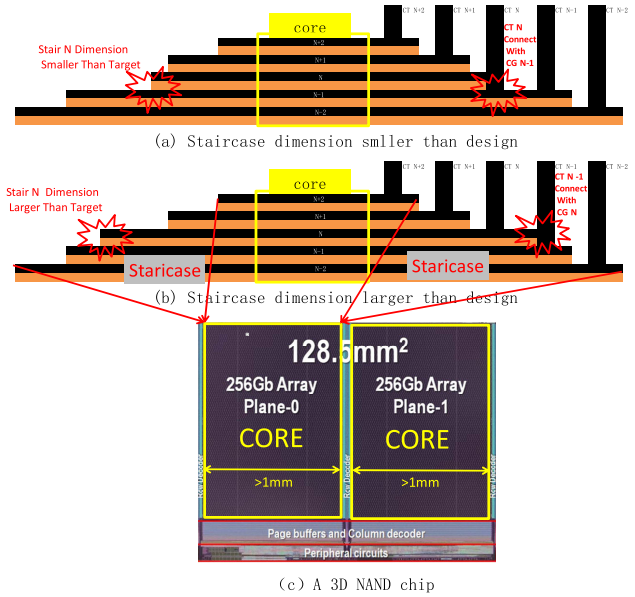

FIGURE 1. Illustrations of dimension error issues of Staircase in a 3D NAND chip.

Iwamoto [21] studied the issues of film transparency as well as film cracking and delamination of thick PR. By using a multi-focus exposure within a single scan, Canon company has introduced a Scan Flex method to improve the sidewall profile of thick PR [22]. In our previous study, we proposed both a PR consume model and a staircase scheme to improve the process efficiency and to reduce the cost [10].

Since the staircase is used to form the electrical connection between the control gate and contact, the dimension of staircase should be accurately defined to ensure the correct landing of contact holes on the right stair level [9]. As shown in Fig. 1(a), when the dimension of staircase N is smaller than design, the contact N will be connected to control gate N-1, leading to word line leakage. As shown in Fig. 1(b), when the dimension of staircase N is larger than design, the contact N-1 will be connected to control gate N, also leading to word line leakage. In such a circumstance, the accurate measurement of dimension of as-formed staircase is crucial. Note that the core array area needs to be protected during the multiple trim-etch process for fabricating staircase. Consequently, the staircase pattern should consist of both the core array area and the stairs. The illustration of the staircase in a 3D NAND chip is presented in Fig. 1(c). As seen, the dimension of the core area in a 3D NAND chip is very large and generally larger than 1 mm [2] [3], where the length of each stair is about 500 nm [21]. Therefore, the dimension of protection patterns for staircase is in millimeter level. It is easy to measure each stair while it is challenging to measure the dimension of protection patterns for staircase in nanometer size precisely. In current lithography technology, the precision for the patterns in micrometer or nanometer size can be nanometer-level or atomic-level [23]–[26]. However, relevant work on the precision of nanometer for patterns in millimeter size was rarely reported and very limited. There are two main reasons that render the precision of nanometer for patterns in millimeter size challenging. First, the measurement accuracy for protection patterns in millimeter size is restricted by magnification and can only reach the micrometer level. Second, it is not feasible to use the traditional CD bar patterns to measure the dimension of as-formed stairs in the protection area directly. When the CD bar of ∼micrometer reaches the target value with nanometer accuracy, the protection area of ∼millimeter does not reach the target value with the same accuracy.

With the aim to solve this problem, Huang *et al.* [8] proposed a measurement method of the dimension of staircase pattern. Namely, the authors put reference marks around the large pattern, and indirectly determined the dimension of the large patterns by measuring the distance between the edges of large patterns and those of the reference marks. However, the dimension of the staircase pattern obtained in this way is greatly affected by the width of reference mark.

In order to meet the requirement for higher precision as the stack number of 3D NAND increases, an improved measurement method for the dimension of the staircase pattern is proposed. By involving the overlay, a calculation formula for the measurement error of staircase dimension is derived for the first time.

Two kinds of SS0 anchors—convex SS0 and concave SS0 are introduced, and the experiments with two SS0 are conducted in 39 layers of staircase and 71 layers of staircase. From the experimental results, the measurement error for proposed method is calculated to be 14.1 nm, while the measurement error of Huang's method is 31.6 nm. By improving the dimensional uniformity of staircase, the word line leakage is well controlled. Besides, the convex SS0 has cost advantages over concave SS0 in advanced SDS (stair divided scheme) staircase structure.

The rest of this work is organized as follows. In Section II, the proposed method and algorithm for measuring the dimension of staircase patterns is introduced. In Section III, the experiments are described. Achieved results are presented and discussed in Section IV. Lastly, the conclusions are drawn in Section V.

II. THE PROPOSED METHOD AND ALGORITHM FOR MEASURING THE DIMENSION OF STAIRCASE PATTERNS

A. THE PROPOSED METHOD FOR MEASURING THE DIMENSION OF STAIRCASE PATTERNS

The protection patterns of staircase is too large to be measured directly using the CD SEM (critical dimension scanning electron microscopy). In this work, the dimension of staircase patterns is determined by setting fixed anchors close to the edges of the protection patterns of staircase. During the lithography process, when a wafer is placed on a stage, it is first aligned and then exposed. The size of the exposure area and the location of the alignment mark are pre- designed. So, when the SS0 anchors are set on both the left and right corners of the large staircase patterns, it can be assumed that the distance of two anchors is also fixed. Therefore, the

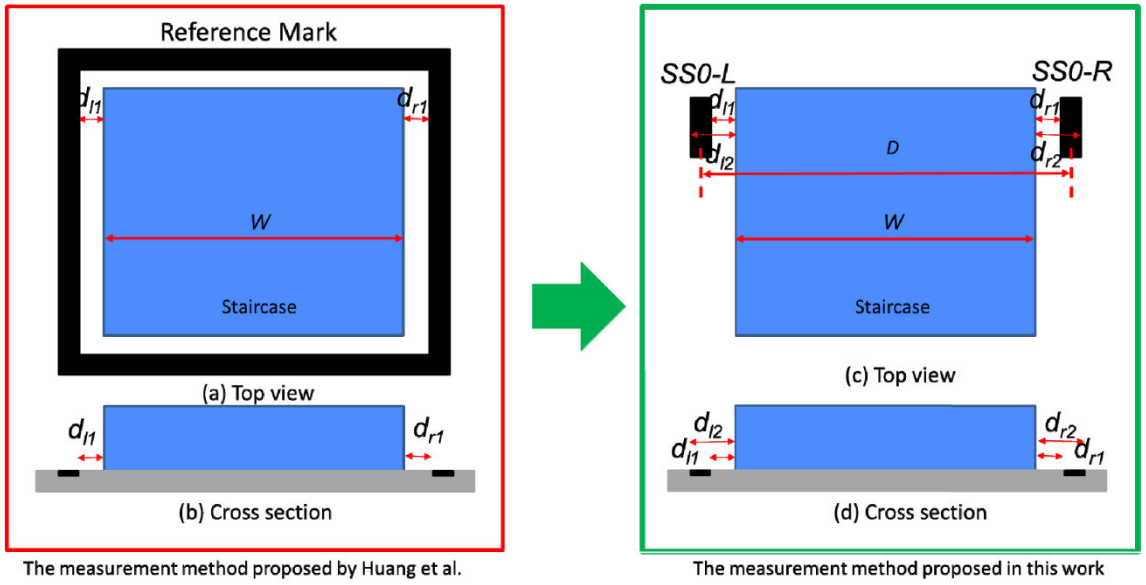

FIGURE 2. Two methods to define the dimension of the staircase pattern.

dimension of the staircase protection patterns can be derived indirectly by measuring the distance from the edges of the staircase protection patterns to the anchors on both sides.

Figs. 2(a) and 2(b) display the dimension measurement method of large patterns proposed by Huang *et al*. As shown in Fig. 2 (a), a reference mark is set around the periphery of the staircase protection pattern, and the distance from the edges of staircase patterns to the reference mark edges is measured. As a result, the boundaries of the staircase patterns are defined. In this scheme, the error in width of the reference mark can cause the measurement error, which further leads to the error in the dimension of staircase.

The proposed measurement method is shown in Figs. 2(c) and 2(d). The SS0 anchors are placed closed to the left and right corners of the staircase protection patterns. By measuring the distance from the edges of staircase protection patterns to the left and right edges of two anchors, the distance from the edges of staircase protection patterns to the centers of two anchors is obtained. Consequently, the dimension of staircase protection patterns is obtained using the distances from the left and right edges of the staircase protection patterns to the center of two anchors on each side.

B. THE ALGORITHM FOR DIMENSION MEASUREMENT ERROR OF STAIRCASE PATTERNS

Assume that the staircase width is denoted as W, the distances from the two sides of the staircase protection patterns to the left and right sides of two anchors are denoted as $d_{l1}, d_{l2}, d_{r1}, d_{r2}$ respectively. The sum of distances between the two edges of the staircase and the centers of two anchors on both sides is denoted as d, and calculated by:

$$d = \frac{d_{l1} + d_{l2}}{2} + \frac{d_{r1} + d_{r2}}{2}. \tag{1}$$

Assume that the coordinate sets of the SS0 anchor on the left and right sides are (x_1, y_1) and (x_2, y_2) respectively. Then the width of the staircase W is given by:

$$W = |x_1 - x_2| - d \tag{2}$$

Therefore, the measurement error of W in the proposed method can be expressed as:

$$\delta_W = \sqrt{\delta^2_{(x_1\text{-}x_2)} + \delta^2_d} \tag{3}$$

$$\delta_d = \frac{\sqrt{\delta^2_{d_{l1}} + \delta^2_{d_{l2}} + \delta^2_{d_{r1}} + \delta^2_{d_{r2}}}}{2} \tag{4}$$

where $\delta_{(x_1 - x_2)}$ denotes the bias between the real distance of the two anchors to the design value. δ_d denotes the measurement error of d. $\delta_{d_{l1}}, \delta_{d_{l2}}, \delta_{d_{r1}}, \delta_{d_{r2}}$ denote the measurement errors of $d_{l1}, d_{l2}, d_{r1}, d_{r2}$ respectively. Then, the overlay for the measurement value (δ_x, δ_y) between the staircase patterns to SS0 is introduced. The overlay is basically calculated by 10 parameters: translation along X and Y axis (T_X, T_Y), wafer expansions along X and Y axis (M_X, M_Y), the rotation $(R^{\backprime})$, non-orthogonality (NO), symmetric and asymmetric field magnification (M_S, M_A), symmetric and asymmetric field rotation (R_S, R_A). The overlay deviations along X and Y axis δ_X and δ_Y are expressed as below [27]:

$$\begin{aligned}\delta_X = {} & T_X + M_X{}^* X - (R^{\backprime} + NO)^* Y \\ & + (M_S + M_A)^* X^{\backprime} - (R_S + R_A)^* Y^{\backprime}\end{aligned} \tag{5}$$

$$\begin{aligned}\delta_Y = {} & T_Y + M_Y{}^* Y - R^{\backprime}{}^* X \\ & + (M_S - M_A)^* Y^{\backprime} - (R_S - R_A)^* X^{\backprime}\end{aligned} \tag{6}$$

where (X, Y) is the coordinate set of the wafer while $(X^{\backprime}, Y^{\backprime})$ is the coordinate set of the filed.

From equations (5) and (6), the overlay includes all errors of field width and position. As shown in Fig. 1, there are 2 planes in a 3D NAND chip, so the distance between the

left SS0 anchor and the right SS0 anchor is about half width of the field, it can be derived:

$$\delta_{(x_1-x_2)} \cong \frac{\delta_X}{2} \tag{7}$$

Then,

$$\delta_W = \sqrt{\frac{\delta_X^2}{4} + \delta_d^2} \tag{8}$$

In Huang *et al.*'s measurement method, the coordinate sets of the centers of the left and the right bars of the reference mark are $(x_1^{\backprime}, y_1^{\backprime})$ and $(x_2^{\backprime}, y_2^{\backprime})$, the width of the left and the right bars of the reference mark are $d_1^{\backprime}$ and $d_2^{\backprime}$. Then the width of the staircase W is calculated by:

$$W = \left|x_1^{\backprime} - x_2^{\backprime}\right| - \frac{d_1^{\backprime}}{2} - \frac{d_2^{\backprime}}{2} - d_{l1} - d_{l2} \tag{9}$$

Therefore, the measurement error of W in Huang *et al.*'s method can be expressed as:

$$\delta_W^{\backprime} = \sqrt{\delta^2_{(x_1^{\backprime}-x_2^{\backprime})} + \frac{\delta^2_{d_1^{\backprime}}}{4} + \frac{\delta^2_{d_2^{\backprime}}}{4} + \delta^2_{d_{l1}} + \delta^2_{d_{r1}}} \tag{10}$$

In a chip with 2 planes, the distance between the left and the right bars of the reference mark is about half width of the field. It can be derived:

$$\delta_{(x_1^{\backprime}-x_2^{\backprime})} \cong \frac{\delta_X}{2} \tag{11}$$

Then,

$$\delta_W^{\backprime} = \sqrt{\frac{\delta_X^2}{4} + \frac{\delta^2_{d_1^{\backprime}}}{4} + \frac{\delta^2_{d_2^{\backprime}}}{4} + \delta^2_{d_{l1}} + \delta^2_{d_{r1}}} \tag{12}$$

Since d_{l1}, d_{l2}, d_{r1}, d_{r2} are at the same level of micrometer, their measurement errors are the same with the measurement accuracy of tool. Therefore,

$$\delta_{\mathrm{d}}^2 = \frac{\delta^2_{d_{l1}} + \delta^2_{d_{l2}} + \delta^2_{d_{r1}} + \delta^2_{d_{r2}}}{2} \cong \delta^2_{d_{l1}} + \delta^2_{d_{r1}} \tag{13}$$

So,

$$\delta_W^{\backprime} = \sqrt{\frac{\delta_X^2}{4} + \frac{\delta^2_{d_1^{\backprime}}}{4} + \frac{\delta^2_{d_2^{\backprime}}}{4} + \delta_d^2} \tag{14}$$

It can be inferred from equations (8) and (14) that:

$$\delta_W < \delta_W^{\backprime} \tag{15}$$

III. EXPERIMENS

In this section, two kinds of SS0 are proposed *i.e.* concave SS0 and convex SS0, as shown in Fig. 3 (a) and 3(b). The concave SS0 is fabricated with 39 pairs of ON in normal staircase scheme while the convex SS0 is fabricated with 71 pairs of ON in stair divided scheme [10]. The difference between normal staircase and stair divided schemes is detailed in [10]. Besides, three silicon lots are manufactured with different lithography conditions in forming staircase to reduce the word line leakage.

The photolithography is carried out using a 248 nm KrF scanner. The etch process is implemented in a commercial conductor etching chamber. The tool of dimension measurement is Hitachi critical dimension scanning electron microscopy (CD SEM).

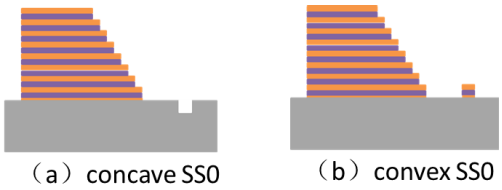

FIGURE 3. Two kinds of SS0 anchors.

A. PROCESS OF 39L STAIRCASE WITH CONCAVE SS0

Firstly, Si wafers are cleaned, and then 39 pairs ON are deposited by plasma enhanced chemical vaper deposition (PECVD). It is then followed by SS0 lithography and etching. Afterwards, SS1/SS2/SS3/SS4/SS5 (the first staircase process/the second staircase process/the third staircase process/the fourth staircase process/ the fifth staircase process) lithography with focus and energy matrix (FEM) and etching are carried out for 5 pilot wafers sequentially. The distances between SS1/SS2/SS3/SS4/SS5 and SS0 are measured separately. The best focus and energy condition of lithography is chosen which is employed in the lithography of prime wafers. For the etching of SS1/SS2/SS3/SS4, 7 trimming and 8 etching processes are performed, while for the etching of SS5, there are 6 trimming and 7 etching. One pair of ON is etched in an etching step. So, after the completion of SS1/SS2/SS3/SS4/SS5, 39 layers are etched and grooves of the SS0 structure are also formed on Si substrate as shown in Fig. 3(a). The process flow and the layout design are illustrated in Figs. 4(a) and 4(c). Different lithography condition and mask design is implemented to reduce the word line leakage of 3D NAND.

B. PROCESS OF 71L STAIRCASE WITH CONVEX SS0

The process of 71L staircase with convex SS0 is the same with our previous work [10]. In this work, the combination of SS0 Mask and SDS mask is expected to save processing cost. Firstly, all wafers are cleaned and 71 pairs of ON are deposited by PECVD. Then, a combination of SDS and SS0 lithography and etch are performed with 2 trimming and 3 etching to form four zones of staircase. Then, SS1/SS2/SS3/SS4 lithography with focus and energy matrix (FEM) and etching are carried out for 4 pilot wafers sequentially. The distances between SS1/SS2/SS3/SS4 and SS0 are measured separately. The best focus and energy condition of lithography is chosen which is employed in the lithography of prime wafers. For the etching of SS1, 4 trimming and 5 etching are performed, while for the etch of SS2/SS3/SS4, there are 3 trimming and 4 etching. In SS1/SS2/SS3/SS4, 4 pairs of ON are etched in an etching step. So, after the completion of SS1/SS2/SS3/SS4, 68 layers are etched and a convex ON stack of the SS0 structure is also formed on Si substrate as shown in Fig. 3(b). The process flow and the layout design are illustrated in Figs. 4(b) and (d).

IV. RESULTS AND DISCUSSION

A. BEST LITHOGRAPHY CONDITION FOR STAIRCASE

Fig. (5) shows that the distance between SS1 and SS0 increases with the exposure energy during lithography

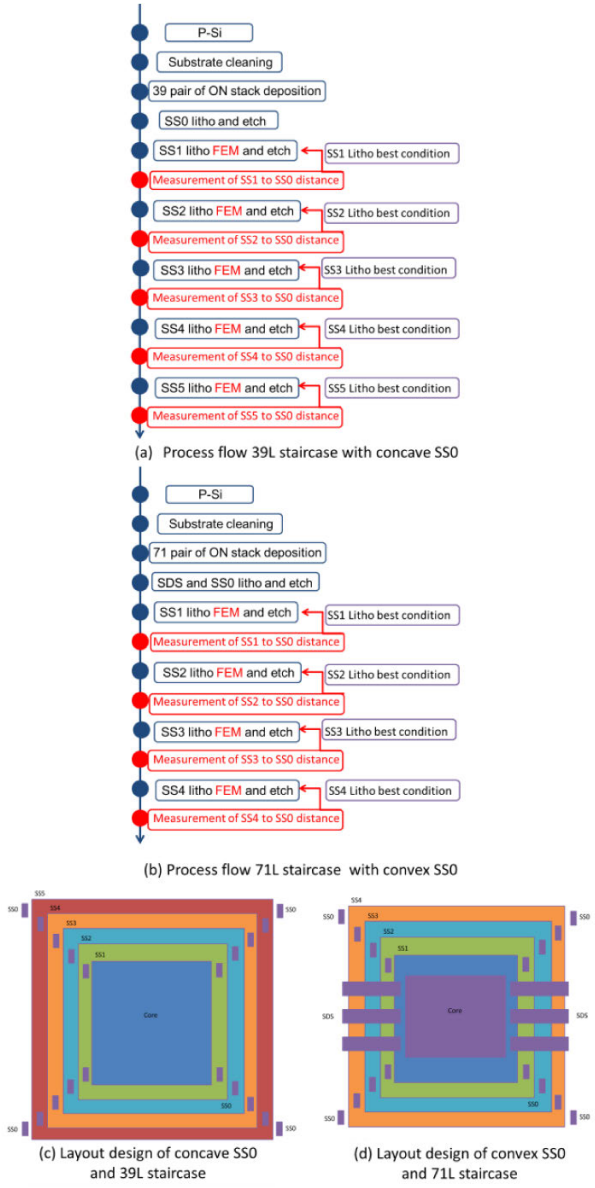

FIGURE 4. The process flows and layout designs of concave SS0 and convex SS0.

in 39 layers of staircase. The step of the energy matrix is 1.5 mJ/cm^2. At an energy of 18.5 mJ/cm^2, the distance bias (the measurement value and the design value) of SS1 to SS0 is ∼4 nm, which means that the SS1 dimension is almost the same as designed. Therefore, the energy condition of 18.5 mJ/cm^2 is the best lithography condition for SS1 in 39L staircase. The best lithography conditions of staircase in other layers are all obtained in this way as SS1. The trends of the distance bias of other staircases to SS0 are the same with SS1 (results not shown here).

B. SS0 CD SHIFT

As shown in Fig. 6, the dimension of the concave SS0 is enlarged by ∼200 nm after the etching of 39 layers of staircase. Besides, the dimension uniformity is also degraded

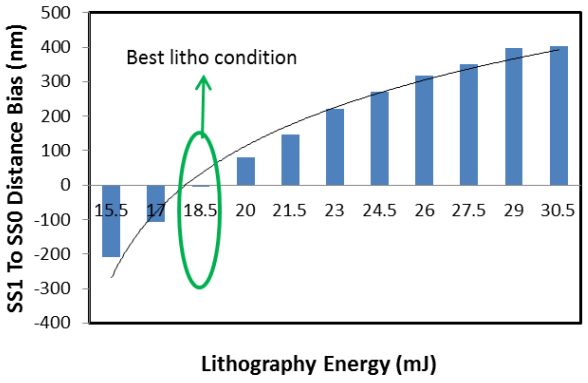

FIGURE 5. SS1 to concave SS0 distance bias VS lithography exposure energy in 39 layers of staircase.

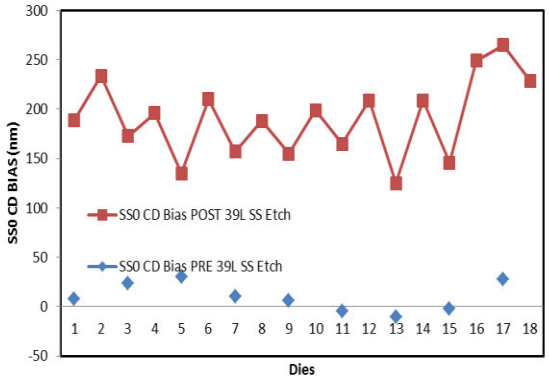

FIGURE 6. Concave SS0 dimension bias pre- and post- etching of 39 layers of staircase.

after etching. The standard deviation of concave SS0 pre- and post-etching of 39 pairs of ON is ∼14 nm and ∼40 nm respectively.

C. CALCULATION OF DIMENSION MEASUREMENT ERROR OF STAIRCASE

Since the dimension of SS5 is indirectly measured by SS0 after the etching of 39 pairs of ON, 40 nm of SS0 standard deviation is taken to calculate the measurement error of Huang *et al.*'s method. In this case, δ_{d_1} and δ_{d_2} are 40 nm. The overlay of SS5 to SS0 is measured to be ∼20 nm, that is, δ_X can be set as 20nm. From reference [27], the measurement precision is about 1% of dimension for etched isotropic line larger than 100 nm. The distance between the edges of staircase and SS0 anchors are not larger than 1 micron, so $\delta_{d_{l1}}$, $\delta_{d_{l2}}$, $\delta_{d_{r1}}$, $\delta_{d_{r2}}$ are set as 10 nm conservatively. Hence δ_d can be calculated as 10 nm from equation (4). Then δ_W can be calculated as ∼14.1 nm from equation (8) while $\delta_W^{\backslash}$ can be calculated as ∼31.6 nm from equation (14). When considering the SS0 CD shift, δ_{d_1} and δ_{d_2} would be ∼200 nm. $\delta_W^{\backslash}$ can be calculated to be larger than 140 nm from equation (14). Using the measurement method proposed by Huang *et al.*, the measurement error of staircase dimension is greatly influenced by the reference mark. Nevertheless, the SS0 CD

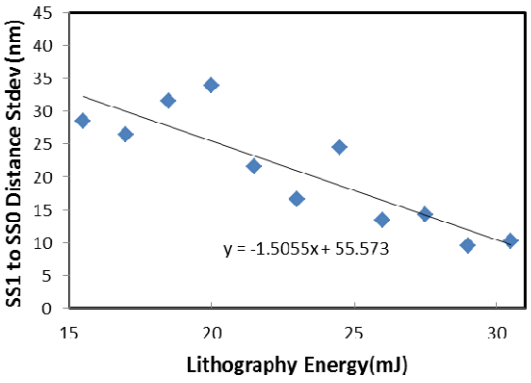

FIGURE 7. The uniformity of the distance between SS1 and SS0 improves with the increase of exposure energy.

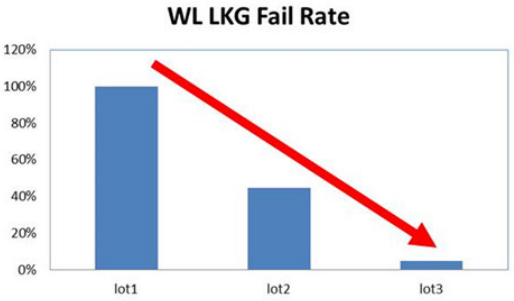

FIGURE 8. Fail rate of word line leakage improves with different lot conditions.

shift and SS0 CD uniformity do not lead to additional error in the dimension measurement of staircase using proposed method in this work for both concave SS0 and convex SS0. The measurement method proposed in this work can achieve high measurement precision with both concave SS0 and convex SS0.

D. REDUCTION OF WORD LINE LEAKAGE

Since the staircase forms the connection between the control gate and word line, the dimension error of staircase can lead to the word line leakage. As shown in Fig. 7, the uniformity of the distance between SS1 and SS0 improves with higher energy in lithography. To reduce the word line leakage, tests were done in three lots to improve the dimension uniformity of staircase so as to reduce word line leakage. For lot1, the adopted best lithography condition was obtained by measuring the distance of staircase edges to SS0 centers. The lithography exposure energy of lot2 is increased to improve the staircase dimension uniformity. The word line leakage in lot2 is improved compared to lot1 as shown in Fig. 8. However, the distance between the staircase and SS0 is larger than design value which means the staircase CD is smaller than designed value. The staircase layout of lot3 is therefore enlarged by using high exposure energy in order to meet the designed value. As shown in Fig. 8, the word line leakage of lot3 is further improved compared to lot2.

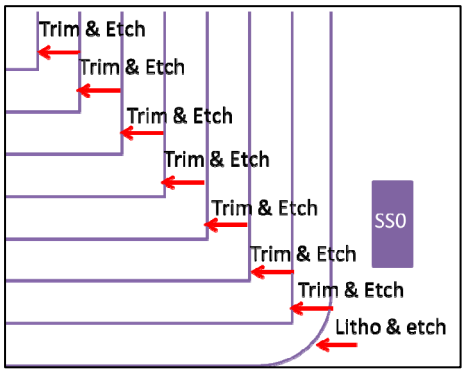

FIGURE 9. The illustration of lithography corner rounding effect.

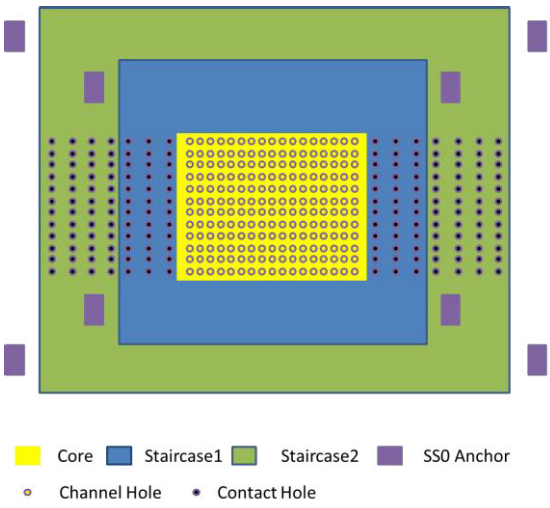

FIGURE 10. Layout of staircase, channel hole and contact holes.

E. SS0 LAYOUT DESIGN

After the lithography and etch, the corner of staircase patterns became rounding, and the corner rounding distance R_d was about 0.5 micron, as shown in Fig. (9). However, after each trimming and etching, the rounding corner turned squared. This should be attributed to the loading effect during the photoresist trimming process. Therefore, in order to reduce the measurement error, the SS0 patterns and the distance measurement points of SS to SS0 should be far away from the rounding edges. However, there are still rooms for SS0 to be placed at the redundant area in a chip where there are no contact holes as shown in Fig. (10), while the reference mark needs to cross places with contact holes.

F. COMPARISON OF TWO KINDS OF SS0

The process flows shown in Fig. 4 present that the convex SS0 in combination with SDS saves one mask compared to the concave SS0. Thus, the manufacturing cost of the convex SS0 is lower than that of the concave SS0. From the perspective of measurement accuracy of staircase dimension, high precisions can be achieved in both kinds of SS0 using proposed measurement method in this work. Hence, the convex SS0 has cost advantage over the concave SS0 for advanced staircase of SDS [10].

V. CONCLUSION

In this paper, an improved method to measure staircase pattern with nanometer precision is proposed. The accuracy of the proposed method is theoretically calculated for the first time by involving overlay. Two kinds of SS0 anchors *i.e.* concave SS0 and convex SS0 are introduced to perform the experiments in 39 layers and 71 layers of staircases separately. The measurement error of proposed method is calculated with experimental results to be 14.1 nm without impact of SS0 CD non uniformity or SS0 CD shift. And the measurement error of normal method would be larger than 30 nm and even more than 140 nm when taking SS0 CD shift into account. Besides, SS0 can be placed in redundant places in a 3D NAND chip. Therefore, the proposed method represents a more precise and flexible approach of measurement than employing reference marks. Furthermore, the convex SS0 has cost advantage over the concave SS0 for advanced staircase of SDS without additional mask. Achieved results in this work is ought to beneficial in advancing the state-of-the-art 3D NAND technology in the future.

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PEIZHEN HONG (Member, IEEE) received the master's degree from the School of Information Science and Technology, Peking University, China, in 2011. She is currently pursuing the Ph.D. degree with the Institute of Microelectronic, Chinese Academy of Sciences, and the University of Chinese Academy of Sciences, Beijing, China. Her research interests include 3D NAND device and process.

ZHIGUO ZHAO received the M.S. degree from Tianjin University, China, in 2006. His current research interest includes process development of 3D NAND flash.

JUN LUO received the B.S. degree from the Chinese University of Geosciences, in 2002, the M.S. degree from Xiamen University, in 2005, and the Ph.D. degree from the Royal Swedish Institute of Technology, in 2010. His current research interests include integrated circuit technology and MRAM.

ZHILIANG XIA received the Ph.D. degree from Peking University, China, in 2007. His current research interests include process, device characterization, and reliability of novel flash memory device.

XIAOJING SU received the B.S. degree in electronic engineering from the University of Electronic Science and Technology of China (UESTC), in 2012, and the M.S. degree in wireless and optical communications from University College London, in 2013. Her current research interests include design for manufacturing, design and technology co-optimization, yield improvement, and defect predictions of lithography.

LIBIN ZHANG received the Ph.D. degree from the State Key Laboratory of Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, China, in 2014. His current research interest includes integrated circuit advanced photolithography calculation and measurement.

CHUNLONG LI received the B.S. degree from Nanchang University, in 1999, the M.S. degree from Zhejiang University, in 2003, and the Ph.D. degree from the University of Chinese Academy of Sciences, in 2017. His current research interest includes process developing of semiconductor devices.

ZONGLIANG HUO (Member, IEEE) received the B.S. and Ph.D. degrees from Peking University, China, in 1998 and 2003, respectively. His current research interests include process, device characterization, and reliability of novel flash memory device.