IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 2, 2020, accepted July 17, 2020, date of publication July 27, 2020, date of current version August 5, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3012028

An Implantable Neural Stimulator IC With Anodic Current Pulse Modulation Based Active Charge Balancing

JIN-YOUNG SON, (Graduate Student Member, IEEE), AND HYOUK-KYU CHA, (Senior Member, IEEE)

Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul 01811, South Korea

Corresponding author: Hyouk-Kyu Cha (hkcha@seoultech.ac.kr)

This work was supported by the Advanced Research Project funded by Seoultech (Seoul National University of Science and Technology).

ABSTRACT Implantable electrical stimulators can be used to treat a variety of neurological disorders and restore paralyzed body functions. In electrical neural stimulation, the stimulator circuit with safe charge balancing is essential to minimize damage to electrodes and biological tissue. In this paper, an implantable current-mode neural stimulator for long-term safe electrical stimulation is presented. Anodic current pulse modulation active charge balancing technique is proposed to keep the residual voltage on the electrode within the safe window, which enables long-term safe stimulation. To ensure more complete charge balancing, the proposed active charge balancing technique can also be used with passive electrode shorting. Transistor stacking and dynamic gate biasing techniques can prevent the breakdown of standard MOSFET devices from high supply voltages, which enable the implementation of output current driver and charge balancing circuits without using HV process. The stimulator IC designed with 0.18-μm standard CMOS process can generate up to 1 mA of stimulation current and only consumes an area of 0.11 mm^2. Since all functions are implemented on-chip without using external components, the proposed stimulator IC is suitable for high-density implantable stimulation applications.

INDEX TERMS Neural stimulation, electrical stimulator, charge balancing.

I. INTRODUCTION

Implantable electrical stimulation can be used for various neural applications such as vagus nerve stimulation (VNS) for treat epilepsy [1], [2], deep brain stimulation (DBS) for treat Parkinson's disease [3], and functional electrical stimulation (FES), which can restore paralyzed body function [4]. In addition, it can be used to restore various sensory functions such as in cochlear and retinal implant devices [5]. Furthermore, closed-loop brain-computer interface (BCI) comprised of neural stimulation and recording signal processing blocks has been shown to restore functionality to people with severe motor deficits [6], [7].

Among several types of stimulators such as voltage-mode stimulator, current-mode stimulator, and charge-mode stimulator, current-mode stimulation is the most widely used of the three topologies because it has the advantage of being able to accurately transfer charges to tissues with relatively compact size implementation.

However, current-mode stimulation requires high voltage (HV) compliance to deliver sufficient charge to the tissues with high impedance, and therefore a high supply voltage is needed. Many conventional current-mode stimulator circuits use a special process with HV transistor device options [8]–[12] to avoid circuit reliability problems. But these HV processes are usually more expensive and have a relatively large on-resistance due to the high threshold voltage of the HV thick-oxide device, which limits the voltage compliance of the stimulator circuit. In order to reduce the on-resistance of the MOS-switch device, the size of the device can be increased, but there is a trade-off with the total circuit area and parasitic components.

Another important issue to consider in current-mode stimulation is implementing the long-term safe stimulation. Due to the stimulation current, residual charge accumulates at the electrode-electrolyte interface and generates DC current flow. This can cause irreversible damage to the

The associate editor coordinating the review of this manuscript and approving it for publication was Mitra Mirhassani.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

nerve tissue, corrode the electrodes, and produce toxic substances [13], [14]. Several charge balancing techniques have been used in many stimulator circuit designs for the long-term safe stimulation [15]–[18]. It is commonly known that the safe window range of electrode residual voltage that does not damage the tissue and electrode is ±50 mV [19], [20] or ±100 mV [21], and many stimulator design works aim to maintain the residual voltage within the safe window.

The basic idea of charge balancing is using biphasic pulses composed of cathodic and anodic pulses. In general electrical stimulation, the cathodic pulse generates a desired neural reaction (action potential), and the anodic pulse compensates the charge injected into the electrode-electrolyte interface during the cathodic pulse, thereby neutralizing the residual voltage of the electrode [22]. Therefore, it is important that the cathodic pulse accurately delivers the charge to the tissue, and the anodic pulse precisely compensates for the injected charge.

Many previous works have focused on perfect matching of cathodic and anodic pulses to reduce the residual charge during stimulation [23]. However, due to a number of factors such as device mismatch, supply noise, electrode-tissue impedance fluctuation, rising/falling edge of the stimulator control signal, logic delay of level shifter circuit, and PMOS/NMOS switch device skew, a difference inevitably occurs between the amount of injected and released charge during the cathodic phase and anodic phase, respectively. Even though this charge difference is very small through careful circuit design, residual charge can be accumulated in long-term stimulation. Therefore, in the electrical stimulation, some additional form of charge balancing must be used to compensate for the residual charges.

In addition to using biphasic pulse stimulation waveform, charge balancing can be classified into passive charge balancing and active charge balancing. The passive charge balancing is such that the stimulator circuit operates passively to discharge and/or prevent the accumulation of charge regardless of the value of the electrode residual voltage. On the other hand, in most active charge balancing techniques, the electrode voltage is measured and the charge is compensated according to the polarity and/or magnitude of the measured voltage to neutralize the residual voltage.

There are two passive charge balancing techniques used in many stimulator circuit designs: DC blocking capacitor [10], [16] and electrode shorting [11], [17].

The concept of each passive charge balancing technique is shown in Fig. 1. In the DC blocking capacitor technique, a capacitor is inserted between the electrode and the tissue. This capacitor blocks the DC current flowing between the electrode and the tissue to prevent damage to the nerve tissue and the electrode. However, the DC blocking capacitor technique has some critical drawbacks. Since the blocking capacitor consume a very large area, it is not suitable for on-chip implementation and microelectrode array (MEA) applications such as in retinal implants. In addition, blocking capacitor limits the voltage compliance of the entire stimulator

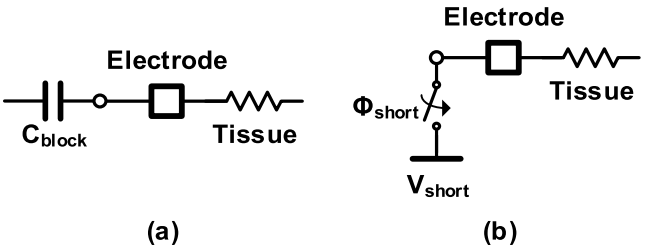


FIGURE 1. Concept of passive charge balancing techniques (a) DC blocking capacitor. (b) Electrode shorting.

circuit and reduces the maximum stimulation current [15]. Due to these drawbacks, the stimulator circuit requires a higher supply voltage, which can reduce the stimulator efficiency or cause reliability problems.

Electrode shorting technique is a method of literally discharging the residual voltage of the electrode by shorting the electrode between each stimulation phase. But this technique has imperfections according to the impedance variation of the electrode-electrolyte interface, stimulation current amplitude, and stimulation frequency [18]. If the impedance of the electrode-electrolyte interface is too high or the stimulation frequency is too fast, it is not possible to sufficiently discharge residual voltage before the next stimulation phase. On the other hand, if the impedance is too low, it can cause a large peak current that damages the nerve tissue. In the past few years, to overcome these drawbacks of the passive charge balancing techniques, many studies have proposed various active charge balancing techniques: pulse insertion [9], [15], [18], [19] and offset regulation [15]. The concept of each active charge balancing technique is shown in Fig. 2.

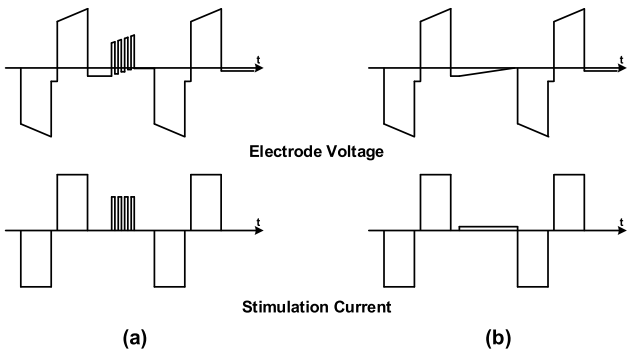


FIGURE 2. Concept of active charge balancing techniques (a) Pulse insertion. (b) Offset regulation.

Pulse insertion is a method of performing charge balancing by measuring the electrode residual voltage between each stimulation phase and injecting an additional short cathodic or anodic pulse according to the polarity of the residual voltage. However, this method has the potential that the injected short pulse can induce unwanted neural reactions [24]. And the concept of offset regulation technique is similar to pulse insertion technique, but charge balancing is performed by

injecting DC current instead of a short pulse. However, since this technique requires continuous offset current injection to the electrode and tissue, it cannot be combined with the passive charge balancing technique for more complete charge balancing. These two techniques can perform charge balancing quite accurately but there are common disadvantages that additional current consumption is needed between each stimulation phase, and that it can only be applied to monopolar-type output current driver.

Another notable active charge balancer circuit proposed in [25] performs charge balancing by measuring the residual voltage after each stimulation phase and adjusting the amplitude of the next anodic current pulse according to the value. This charge balancing technique does not suffer from the disadvantages of the other techniques mentioned above, and can perform accurate charge balancing with a simple principle. However, the implemented circuit is modularized with many off-chip components, and since a monopolar-type output current driver is used, twice the supply voltage is required to obtain the same voltage compliance compared to the bipolar method.

In this work, transistor stacking and dynamic gate biasing techniques [26] are used to implement a current-mode stimulator circuit with high voltage compliance and circuit reliability using a standard CMOS process without using HV transistors. By using the transistor stacking technique, the output current driver and charge balancing circuit can be protected from high voltage. In addition, an anodic current pulse modulation active charge balancing technique for safe electrical stimulation is proposed [27]. During stimulation, the proposed active charge balancing technique can maintain the electrode residual voltage in a safe window by automatically adjusting the anodic current pulse amplitude, and can be used simultaneously with the passive electrode shorting technique for a more complete charge balancing.

This paper is organized as follows. Section II describes the system design considerations and detailed circuit design, and Section III explains the concept and principle of the proposed active charge balancing. Section IV presents the experimental results of the implemented stimulator IC circuit, followed by the conclusions in Section V.

II. SYSTEM DESIGN CONSIDERATIONS

A. ELECTRODE-ELECTROLYTE INTERFACE

Between the electrodes and tissue, electrical stimulation is performed through two major charge transfer mechanisms. The first mechanism is chemical charge redistribution in the electrode-electrolyte interface that called as non-Faradaic reaction. And the second mechanism is an oxidation-reduction reaction that is called as Faradaic reaction [13].

In this work, the equivalent model of the electrode-electrolyte interface is a combination of C_{dl} representing a non-Faradaic reaction, R_F modeling a Faradaic reaction, and tissue impedance R_S. as shown in Fig. 3. Equivalent models

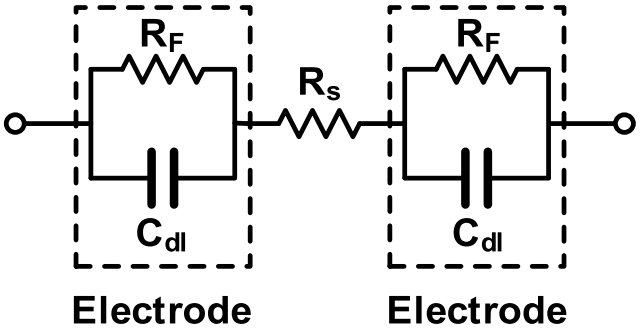


FIGURE 3. Equivalent model of electrode-electrolyte interface.

of $C_{dl} = 100$ nF, $R_F = 10$ MΩ, and $R_S = 10$ kΩ were used for simulation and measurement with reference to the platinum electrode model for retina implant [19], [28].

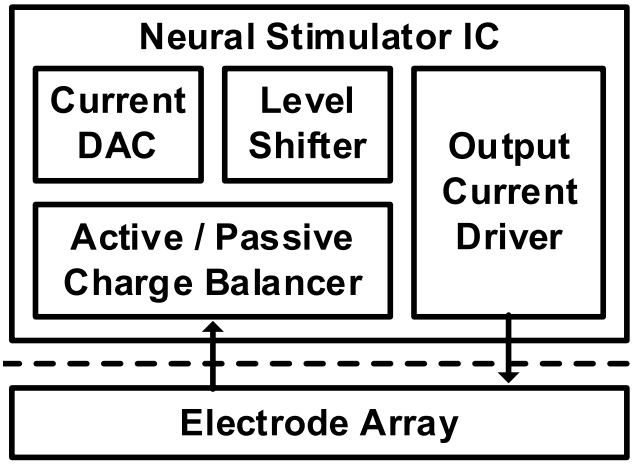


FIGURE 4. Block diagram of proposed stimulator IC.

B. SYSTEM ARCHITECTURE

Figure 4 shows the system block diagram of the proposed stimulator IC. The overall system consists of a 5-bit current digital-to-analog converter (DAC), digital control signal level shifter, output current driver, and charge balancer circuits. Current DAC can control the stimulation current up to 1 mA with 5-bit resolution. The level shifter changes the DC-level of digital control signal for output current driver. The output current driver receives the digital control signal and generates the stimulation current through the tissue to produce cathodic and anodic current pulses. Finally, the charge balancer circuit consists of the proposed active charge balancer and passive electrode shorting switch. The active charge balancing and passive shorting techniques can be used selectively, and charge balancing can be performed more completely by using both techniques simultaneously.

C. OUTPUT CURRENT DRIVER

Figure 5 shows the schematic of the output current driver used in the proposed stimulator. Bipolar-type output current driver

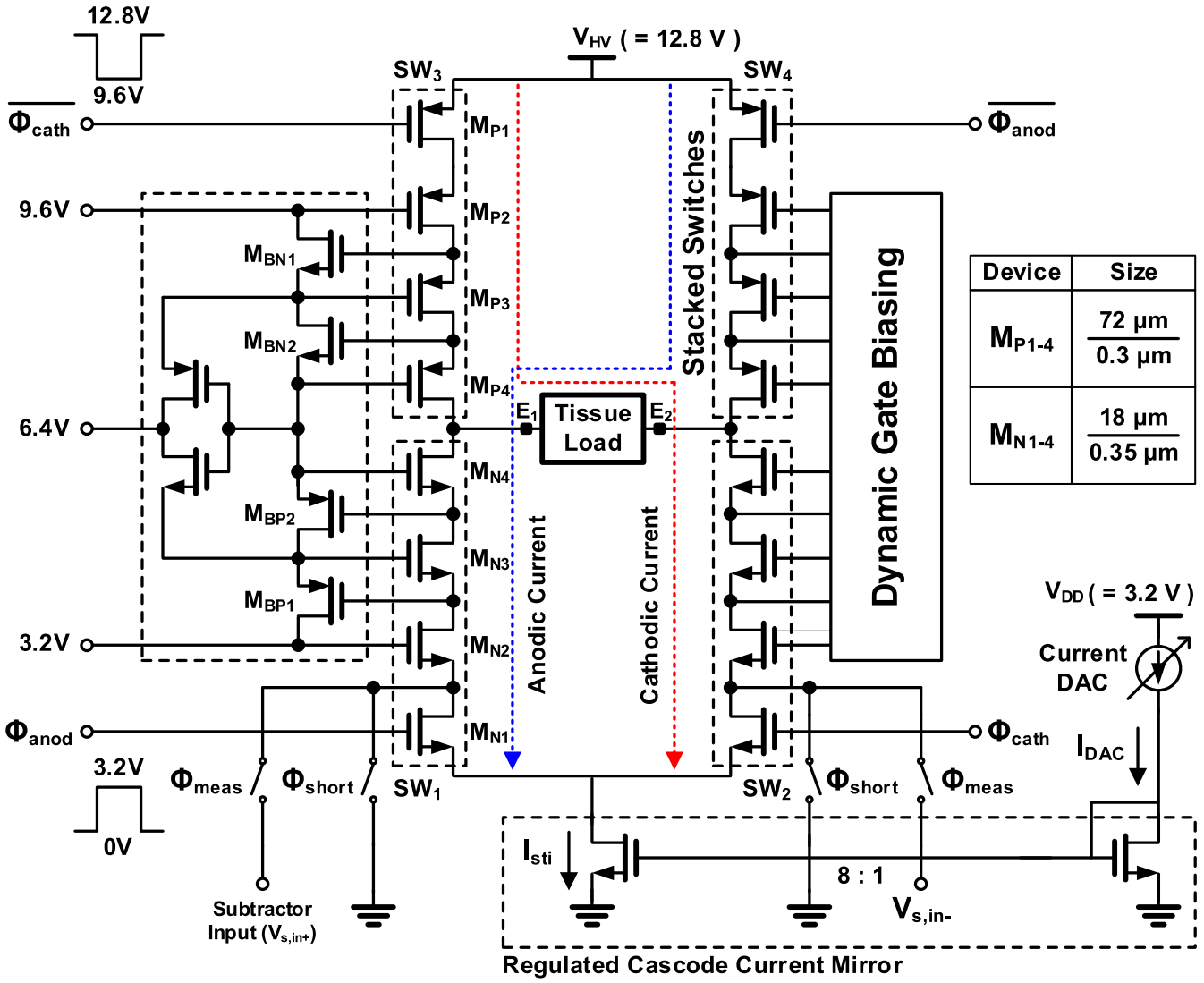


FIGURE 5. Transistor stacking output current driver.

is employed which achieves the desired voltage compliance with less supply voltage compare to a monopolar type. A high supply voltage (V_{HV}) of 12.8 V is selected to deliver up to 1 mA of current to a 10 kΩ of tissue load. This value is chosen considering the headroom voltages in the current sink transistor, voltage drops in the stack, and the n-well to substrate voltage limitation in the process. Transistor stacking and dynamic gate biasing techniques are used to implement the output driver using standard 3.3-V CMOS thick oxide transistors. Each switch (SW_{1-4}) is implemented by stacking four 3.3-V transistor devices. The stacked switches are biased through the dynamic gate biasing circuit to keep the voltage across each terminal within 3.2 V to prevent breakdown due to high supply voltage.

To explain the operation of the output driver circuit, the operation of SW_1 is explained first. When a control signal of 3.2 V is applied to the gate terminal of M_{N1}, the M_{N1} switch is turned on. And the source terminal of M_{N2} is shorted to the low voltage node. And since the 3.2 V voltage source is supplied to the gate terminal of M_{N2}, the M_{N2} switch is turned on. When the M_{N2} switch is turned on, the gate terminal of M_{BP1} is shorted to the low voltage node and M_{BP1} switch is also turned on. Therefore, the gate terminal of M_{N3} is shorted to the 3.2 V voltage source and that switch is also turned on. In the same operation, the M_{BP2} and M_{N4} switches are turned on so that entire switch SW_1 is turned on. Next, the operation of SW_3 is explained. When the 9.6 V control signal that generated by level shifter circuit is applied to gate terminal of M_{P1}, the M_{P1} switch is turned on. Therefore, since the source terminal of M_{P2} is shorted to high voltage node and the gate terminal the M_{BN1} switch is turned on. Similarly, M_{P3}, M_{BN2}, and M_{P4} switches are also turned on by same operation, so that entire switch SW_3 is turned on. The remaining switches SW_2 and SW_4 operate with the

same mechanism, thus achieving a HV compliance while preventing the transistor breakdown.

Furthermore, another advantage of the transistor stacking technique is that active charge balancing circuit and switch devices used for passive electrode shorting are not directly connected to the electrodes. These devices can be connected to the drain terminal of the lowermost NMOS switch device (M_{N1}) of the output driver instead of being directly connected to the electrode. Therefore, not only the output driver circuits, but charge balancer circuits also can be protected from the high supply voltage. Fig. 6 shows the simulated drain terminal voltage of the NMOS stacked transistors (M_{N1-4}). During the stimulation, the voltage difference between each terminal of all NMOS devices is kept within the safe value. Similarly, the voltage difference between each terminal of the PMOS stacked transistors (M_{P1-4}) is also kept within the safe value. The size of each device used as a switch in the output driver was optimized to allow maximum current of 1 mA flow while not consuming too much chip area.

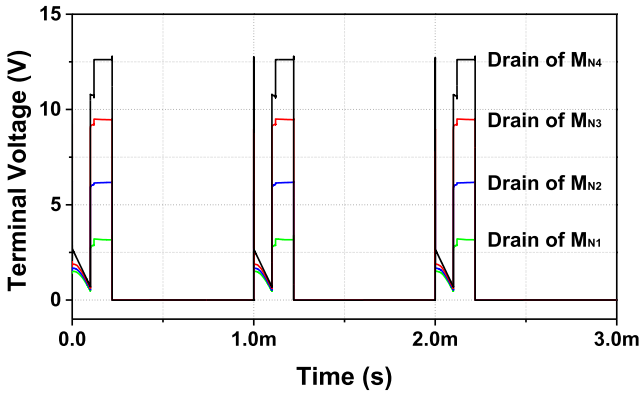


FIGURE 6. Drain terminal voltage of NMOS stacked transistors.

D. LEVEL SHIFTER

The level shifter circuit of Fig. 7 is used to shift the DC-level of the digital signal needed to control the output current driver. Similar to the output current driver, the transistor stacking technique was used for the design. The level shifter circuit converts the 0-3.2 V digital control signal into a 9.6-12.8 V signal for the PMOS stack input in the output driver and keeps the gate-source voltage variations of all devices of the output current driver within 3.2 V.

E. CURRENT DAC AND REGULATED CASCODE CURRENT MIRROR

The current DAC can adjust the stimulation current with a 5-bit resolution. In the current DAC, cascode structure was used to generate an accurate output current regardless of channel length modulation.

The current mirror circuit in Fig. 8 is used to copy the output current of the 5-bit current DAC to the output driver. The high output resistance of the current mirror is required to accurately transfer the copied DAC output current (I_{DAC})

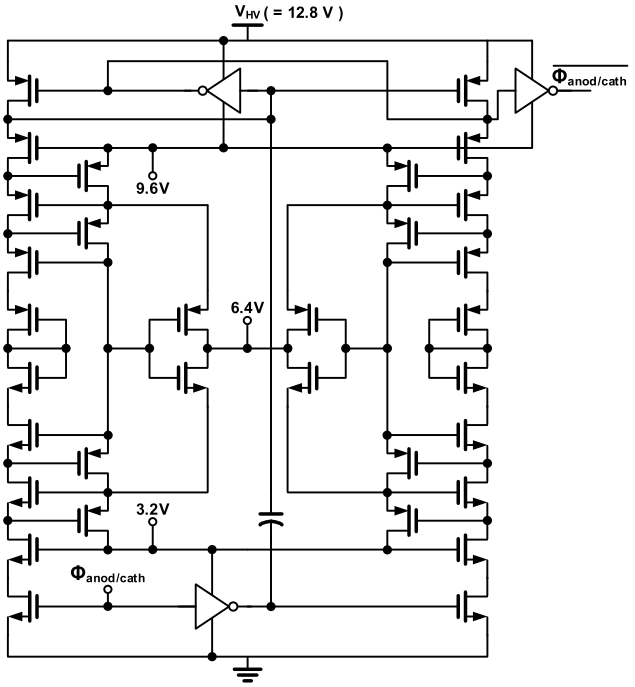
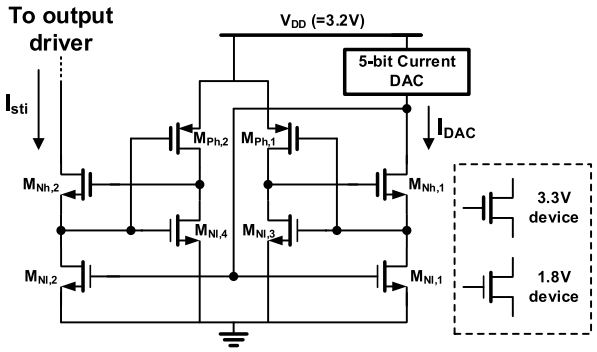


FIGURE 7. Schematic of level shifter circuit.



Device	Size
$M_{Nh,1}$	5 µm / 0.5 µm
$M_{Nh,2}$	8 * (5 µm / 0.5 µm)
$M_{Ph,1-2}$	0.22 µm / 10 µm

Device	Size
$M_{NI,1}$	5 µm / 0.5 µm
$M_{NI,2}$	8 * (5 µm / 0.5 µm)
$M_{NI,3-4}$	20 µm / 2 µm

FIGURE 8. Schematic of regulated cascode current mirror circuit.

to the nerve tissue and reduce mismatch of the stimulation current. When the telescopic cascode topology is used to obtain high output resistance, the output voltage compliance is sacrificed due to the high voltage headroom. In the proposed stimulator circuit, regulated cascode current mirror topology [29] was used to alleviate the trade-off between output impedance and voltage compliance. In the current mirror circuit, 1.8-V devices ($M_{Nl,1-4}$) and 3.3-V devices ($M_{Nh,1-2}, M_{Ph,1-2}$) are properly used to achieve both low voltage headroom and high output resistance. The size of each device and symbols of 1.8-V and 3.3-V devices are shown in Fig. 8.

In this stimulator IC, the layout is very carefully designed for accurate matching of cathodic and anodic current pulses, and accurate charge balancing. Including bipolar output

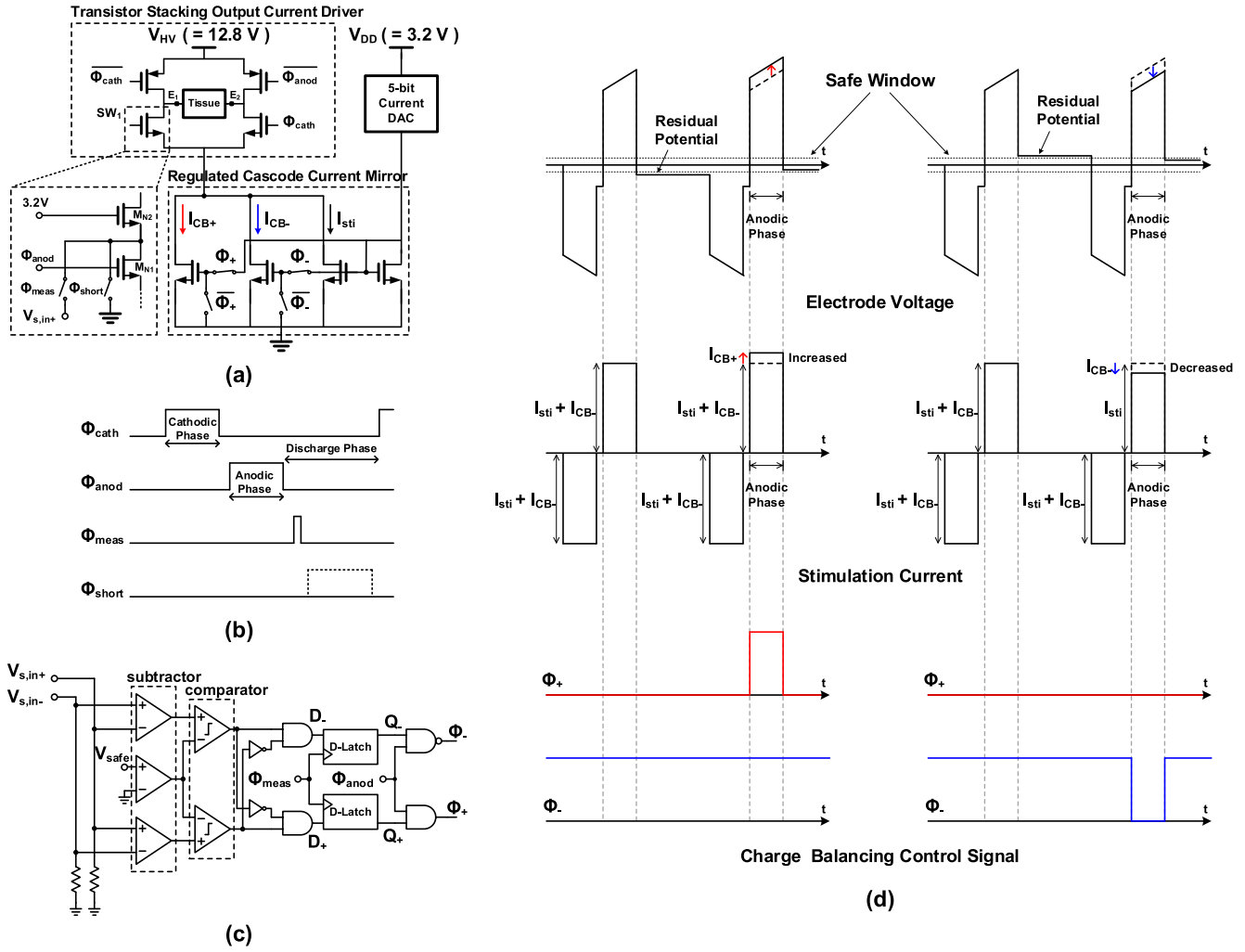


FIGURE 9. (a) Overall system schematic. (b) Timing diagram of control signals. (c) Proposed active charge balancing circuit. (d) Concept of proposed active charge balancing.

current driver and level shifting circuits, the entire circuit is designed symmetrically, and a common-centroid layout with dummy device is used for current DAC and current mirror circuits.

III. CHARGE BALANCING

Figure 9 shows the schematic of stimulator IC and proposed active charge balancing technique. In the overall stimulator circuit schematic of Fig. 9(a), the output current driver and current mirror circuits are briefly described for explanation. The current mirror circuit employs the regulated cascode structure as described in Section II, and ICB+ and ICB- branches are added for active charge balancing. Charge balancing current I_{CB+} and I_{CB-} are turned on and off according to $\emptyset_+$ and $\emptyset_-$ signals, respectively.

Figure 9(b) shows the timing diagram of the control signal for stimulator and charge balancing operations. The $\emptyset_{cath}$ and $\emptyset_{anod}$ signals generate cathodic pulse and anodic pulse, respectively. And the $\emptyset_{meas}$ and $\emptyset_{short}$ signals are activated between each stimulation phase for active charge balancing and passive shorting, respectively.

In this work, the total stimulation period was set to 1 ms, and the width of $\emptyset_{cath}$ and $\emptyset_{anod}$ signals was each set to 100 μs with 20 μs of interphasic delay. The $\emptyset_{meas}$ signal is activated for 10 μs after the anodic phase to measure the electrode residual voltage and perform active charge balancing in the next anodic stimulation phase. The $\emptyset_{short}$ signal can be activated as an option during the remaining discharge phase after the $\emptyset_{meas}$ s signal to electrode shorting operation to perform a more complete charge balancing operation.

Figure 9(c) shows the block diagram of the proposed active charge balancing circuit. The operation of the charge balancing circuit is described below. First, the upper and lower subtractor circuits sense the residual voltage of the electrode through the transistor stacking output current driver circuit. At this time, the subtractor circuit is protected from high voltage. Second, the middle subtractor circuit senses the voltage difference between V_{safe} and GND, and generates an

output error signal. This error signal sets the safe window range for the active charge balancing. Third, two comparator circuits compare the output voltage of each subtractor circuit and output the logic HIGH or logic LOW signal. Through the following NOT gate and AND gate, two logic signals (D_+, D_-) are generated. If the value of the electrode residual voltage is higher than the safe window, D_- signal is changed to the logic HIGH state, and if the residual voltage is smaller than the safe window, D_+ signal is changed to the logic HIGH state. When the electrode residual voltage value is within the safe window, the D_+, D_- signals all maintain the logic LOW state. Forth, D-Latch circuits store the state of the D_+, D_- signals only while the $\emptyset_{meas}$ signal is activated, and outputs the Q_+ and Q_- signals. Fifth, the following NAND gate and AND gate receive $\emptyset_{anod}$ signal and Q_+, Q_- signals, and control the logic state of $\emptyset_+$, $\emptyset_-$ signals only during anodic phase. Finally, the $\emptyset_+$, $\emptyset_-$ signals control the switches of the current mirror shown in Fig. 9(a) and perform active charge balancing operation.

Figure 9(d) briefly shows the concept of proposed active charge balancing. After the first stimulation phase, the state of the $\emptyset_+$, $\emptyset_-$ signals are controlled during the next anodic phase according to the value of electrode residual voltage. As the result of described charge balancing circuit operation, the anodic current is automatically increased or decreased. In the proposed stimulator circuit, the amplitude of the default stimulation current is set to ($I_{sti} + I_{CB-}$). And current amplitude is adjusted to 5-bits according to the current DAC control. In order to perform stable charge balancing regardless of the current amplitude, I_{CB+} and I_{CB-} values were set to be proportional to I_{sti} value. According to the post-layout simulation results, in order to minimize the residual voltage within the safe window and perform stable charge balancing for all process corners, ICB+ and ICB− values were set to 2% and 6% of I_{sti} in this design, respectively. To achieve optimal charge balancing conditions, V_{safe} voltage can be controlled reconfigurably. The proposed active charge balancing technique does not require additional current pulses or offset currents for charge balancing. Therefore, it can prevent the unwanted neural reactions and can be used simultaneously with passive electrode shorting technique to perform charge balancing more completely. Compared to other active charge balancing techniques that use monopolar output driver, since it can be applied to bipolar output current drivers, desired voltage compliance is achieved with less supply voltage.

Figure 10 shows the stimulation voltage waveform of the post-layout simulation of the proposed stimulator IC. In the post-layout simulation, the width of anodic and cathodic pulses was set to 100 μs with 20 μs of interphasic delay, and the total stimulation period was set to 1 ms. The amplitude of the stimulation current was set to 1 mA and the electrical equivalent model of the electrode-electrolyte interface described in Section II was used as the stimulation load. To verify the operation of the proposed active charge balancing technique, a mismatch of 1% was intentionally applied between cathodic and anodic pulses. In Fig. 10(a), due to the

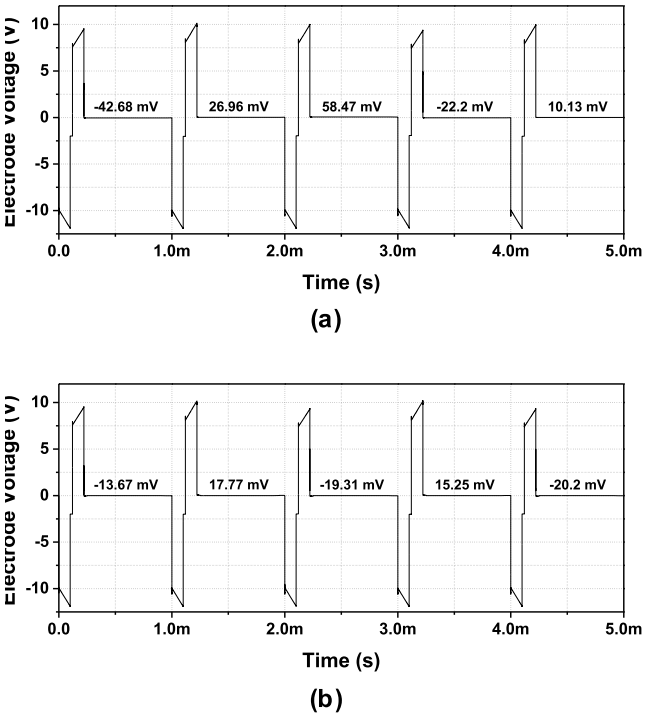


FIGURE 10. Post-layout simulated voltage across electrode-tissue equivalent model (a) with active charge balancing. (b) with active charge balancing and passive electrode shorting.

proposed active charge balancing operation, the amplitude of the anodic pulse is adjusted so that the residual voltage maintains within the safe window. And in Fig. 10(b), active charge balancing and passive electrode shorting techniques are used together for more complete charge balancing. The safe window was adjusted to an appropriate range. Because both charge balancing techniques were used simultaneously, the average absolute value of the residual voltage was reduced.

IV. EXPERIMENTAL RESULTS

The proposed electrical stimulator IC is fabricated in 0.18-μm standard CMOS process. The chip micrograph of the stimulator IC is shown in Fig. 11. The active area of core circuit including output current driver, level shifter, current DAC, and charge balancing circuits is 0.11 mm^2. The IC is packaged using chip-on-board (COB) method and is assembled on a FR4 PCB for testing. All the digital control signals and bias voltages for the stacked output driver and level shifter are applied externally using waveform generators and DC power supply, respectively. Electrical testing was done to demonstrate the stimulator IC and its charge balancing operation.

A. CHARGE BALANCING

The fabricated stimulator chip is measured using the electrode-electrolyte equivalent model on the PCB and control signal parameters described in Section II and III, respectively. Similar to the post-layout simulation results, the safe

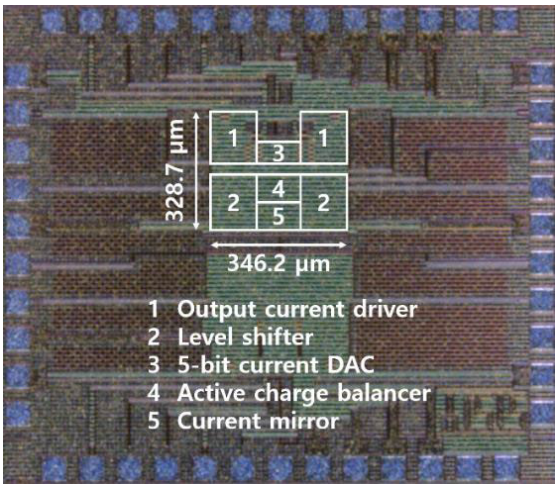


FIGURE 11. Chip micrograph of fabricated stimulator IC.

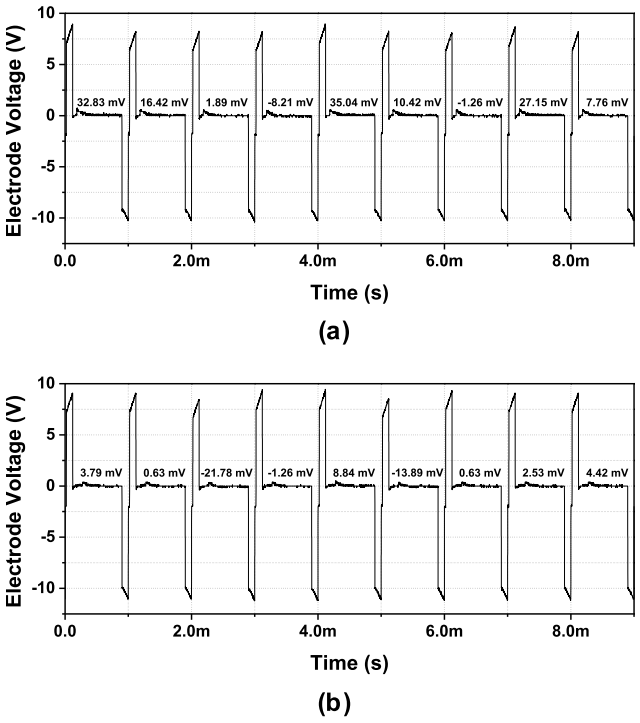


FIGURE 12. Measured voltage across electrode-tissue equivalent model (a) with active charge balancing. (b) with active charge balancing and passive electrode shorting.

window was adjusted in each case through the V_{safe} bias voltage for optimal charge balancing. Fig. 12(a) shows the measured output voltage of the stimulator IC using the proposed active charge balancing technique. In the measurement result, the amplitude of the cathodic current pulse is kept constant, and the amplitude of the anodic current pulse is increased or decreased according to the residual voltage after each stimulation phase so that the electrode residual voltage is maintained within the safe window. The measurement results of the stimulator IC with the proposed active charge balancing and passive electrode shorting technique simultaneously are shown in Fig. 12(b). After the active charge balancer circuit measures ($\emptyset_{meas}$) the electrode residual voltage, passive shorting is applied ($\emptyset_{short}$) until before the next stimulus phase. Because both charge balancing techniques are used at the same time, the residual voltage is discharged more completely and ensuring safe long-term stimulation. In the measurement results, when the both charge balancing techniques are used together, the average absolute value of residual voltage is decreased. The residual voltage exhibited similar behavior to the post-layout simulation results shown in Fig. 10.

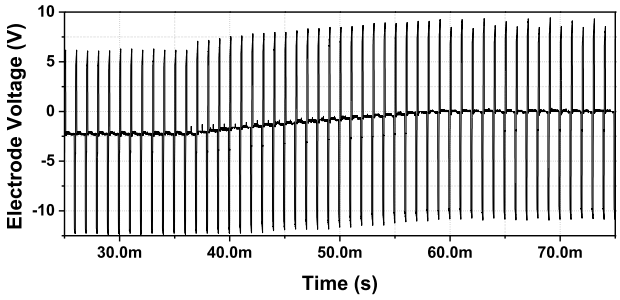


FIGURE 13. Measured residual voltage behavior with proposed active charge balancing technique.

Figure 13 shows the residual voltage behavior by proposed active charge balancing. Under the same measurement conditions that is previously mentioned without applying any charge balancing techniques, the electrode residual voltage was settled at −2.3 V. In this graph, the proposed active charge balancing is activated at 36 ms. Due to the anodic current pulse modulation operation, the residual voltage rapidly moves toward the safe window and settling is complete at 60 ms. After the settling, the residual voltage is maintained within the safe window.

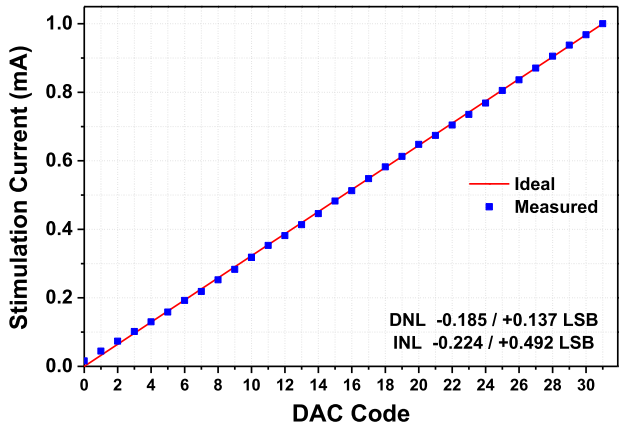


FIGURE 14. Measured DAC control stimulation current.

B. STIMULATOR CIRCUIT PERFORMANCES

The regulated cascode current mirror properly designed using 1.8-V and 3.3-V devices has very low voltage headroom and high output resistance, thus providing high voltage compliance and stimulation current linearity of the entire stimulator circuit. Fig. 14 shows the measured amplitude of the

stimulation current under the control of the current DAC. Up to 1 mA of stimulation current can be controlled with 5-bit resolution depending on the application. The amplitude of the stimulation current pulse is linearly controlled according to the DAC control, and the anodic current pulse is adjusted to +2% or −6% by active charge balancing operation. The measured differential nonlinearity (DNL) and integrated nonlinearity (INL) of the current DAC are −0.185/+0.137 LSB and −0.224/+0.492 LSB, respectively. Fig. 15 shows the voltage compliance of stimulator circuit. The measured voltage compliance of the designed stimulator circuit is 12.3 V under the 12.8 V supply voltage and maximum output current conditions. Therefore, 1 mA of maximum stimulation current can be sufficiently applied to tissue load of 10 kΩ impedance.

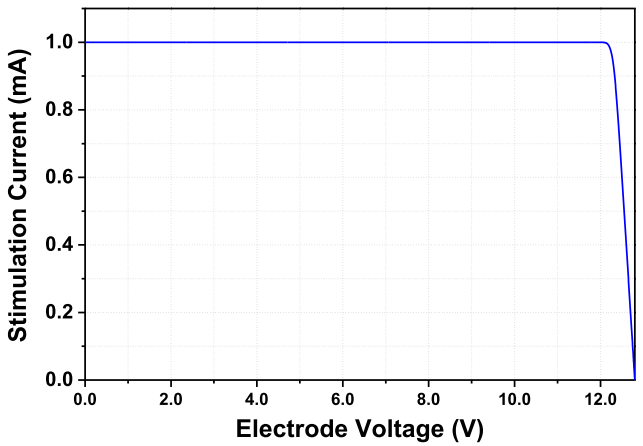


FIGURE 15. Measured voltage compliance of stimulator circuit.

The power efficiency of the proposed stimulator IC is calculated at 1 mA of maximum stimulation current, 10 kΩ of tissue load, and stimulation conditions mentioned above. The power efficiency is defined as P_{out}/P_{in}. P_{out} is the power delivered to the tissue load, and P_{in} is the total power dissipation of the stimulator circuit. To calculate P_{out} and P_{in}, power consumption at each voltage source is calculated. During the stimulation phase, the current consumption of 12.8 V supply voltage is 1 mA and it consumes 12.8 mW of power ($P_{in,HV}$), and the power transferred to the tissue (P_{out}) is 10 mW. During the discharge phase, 12.8 V supply voltage does not consume power. As the 9.6 V and 6.4 V supply voltages are only used to bias the output current driver and level shifter circuits, the power consumption of 9.6 V and 6.4 V supply voltages is very small and negligible. Finally, the power consumption of 3.2 V supply voltage ($P_{in,LV}$) by the current DAC, current mirror, and charge balancing circuit blocks is 0.59 mW. Since the 3.2 V supply voltage consumes the static power, power efficiency depends on the duty ratio of the stimulation phase. Therefore, the power efficiency of the proposed stimulator IC at the stimulation condition mentioned above is calculated to 44.8 %. The power efficiency can be improved as the duty ratio of the stimulation phase increases.

TABLE 1. Comparison with other similar works.

Parameter	This work	[8]	[9]	[10]	[11]
Voltage Compliance	12.3 V	< 12 V	< 20 V	12 V	13 V
Maximum Stimulation Current	1 mA	94.5 µA	10 mA	1.45 mA	15 mA
Current DAC Resolution	5-bit	8-bit	6-bit	9-bit	5-bit
Charge Balancing	Anodic Current Modulation & Electrode Shorting	Electrode Shorting	Pulse Insertion	DC-Blocking Capacitor	Electrode Shorting
Process	0.18-µm Standard CMOS	0.6-µm HV CMOS	0.18-µm HV CMOS	0.18-µm HV CMOS	0.18-µm HV CMOS
Area	0.11 mm²	10 mm²	3.36 mm² (including PAD)	9 mm²	N/A

Table 1 shows the comparison with other similar works. Compared to other works using HV CMOS process, high voltage compliance was achieved using a low-cost standard CMOS process. And the active charge balancing technique has been proposed that overcomes the drawbacks of other charge balancing techniques. The overall system was implemented on-chip with a small area of 0.11 mm^2.

V. CONCLUSION

In this paper, an implantable current mode stimulator IC with the safe active charge balancing technique is proposed and implemented. Transistor stacking and dynamic gate biasing techniques are used to protect the MOS device from high supply voltage without using the HV process. The active area of the stimulator IC using 0.18-μm standard CMOS process is 0.11 mm^2, and all functions are implemented on-chip without using external components. The proposed anodic current pulse modulation active charge balancing technique automatically adjusts the amplitude of the anodic current pulse through a simple digital logic circuit to keep the electrode residual voltage within a safe window and prevent tissue and electrode damage. The passive electrode shorting technique and proposed active charge balancing technique can be used simultaneously to ensure safer long-term stimulation.

REFERENCES

[1] P. E. Ben-Menachem, "Vagus-nerve stimulation for the treatment of epilepsy," *Lancet Neurol.*, vol. 1, no. 8, pp. 477–482, Dec. 2002, doi: 10.1016/s1474-4422(02)00220-x.

[2] H. A. Sackeim, A. J. Rush, M. S. George, L. B. Marangell, M. M. Husain, Z. Nahas, C. R. Johnson, S. Seidman, C. Giller, S. Haines, and R. K. Simpson, Jr., "Vagus nerve stimulation (VNS) for treatment-resistant depression: Efficacy, side effects, and predictors of outcome," *Neuropsychopharmacology*, vol. 25, no. 5, pp. 713–728. Nov. 2001, doi: 10.1016/S0893-133X(01)00271-8.

[3] A. L. Benabid, "Deep brain stimulation for Parkinson's disease," *Current Opinion Neurobiol.*, vol. 13, no. 6, pp. 696–706, Dec. 2003, doi: 10.1016/j.conb.2003.11.001.

[4] P. H. Peckham and J. S. Knutson, "Functional electrical stimulation for neuromuscular applications," *Annu. Rev. Biomed. Eng.*, vol. 7, no. 1, pp. 327–360, Aug. 2005, doi: 10.1146/annurev.bioeng.6.040803.140103.
[5] H. Chun, Y. Yang, and T. Lehmann, "Safety ensuring retinal prosthesis with precise charge balance and low power consumption," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 108–118, Feb. 2014, doi: 10.1109/TBCAS.2013.2257171.
[6] W. Wang, J. L. Collinger, A. D. Degenhart, E. C. Tyler-Kabara, A. B. Schwartz, D. W. Moran, D. J. Weber, B. Wodlinger, R. K. Vinjamuri, R. C. Ashmore, J. W. Kelly, and M. L. Boninger, "An electrocorticographic brain interface in an individual with tetraplegia," *PLoS ONE*, vol. 8, no. 2, Feb. 2013, Art. no. e55344, doi: 10.1371/journal.pone.0055344.
[7] M. J. Vansteensel, E. G. M. Pels, M. G. Bleichner, M. P. Branco, T. Denison, Z. V. Freudenburg, P. Gosselaar, S. Leinders, T. H. Ottens, M. A. Van Den Boom, P. C. Van Rijen, E. J. Aarnoutse, and N. F. Ramsey, "Fully implanted Brain–Computer interface in a locked-in patient with ALS," *New England J. Med.*, vol. 375, no. 21, pp. 2060–2066, Nov. 2016, doi: 10.1056/NEJMoa1608085.
[8] D. Jiang and A. Demosthenous, "A multichannel high-frequency power-isolated neural stimulator with crosstalk reduction," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 4, pp. 940–953, Aug. 2018, doi: 10.1109/TBCAS.2018.2832541.
[9] M. N. van Dongen and W. A. Serdijn, "A power-efficient multichannel neural stimulator using high-frequency pulsed excitation from an unfiltered dynamic supply," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 61–71, Feb. 2016, doi: 10.1109/TBCAS.2014.2363736.
[10] K. N. Hageman, Z. K. Kalayjian, F. Tejada, B. Chiang, M. A. Rahman, G. Y. Fridman, C. Dai, P. O. Pouliquen, J. Georgiou, C. C. Della Santina, and A. G. Andreou, "A CMOS neural interface for a multichannel vestibular prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 269–279, Apr. 2016, doi: 10.1109/TBCAS.2015.2409797.
[11] U. Bihr, T. Ungru, H. Xu, J. Anders, J. Becker, and M. Ortmanns, "A bidirectional neural interface with a HV stimulator and a LV neural amplifier," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Beijing, China, May 2013, pp. 401–404.
[12] N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl, "A 22 V compliant 56 μW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2298–2310, Aug. 2018, doi: 10.1109/JSSC.2018.2828823.
[13] D. R. Merrill, M. Bikson, and J. G. R. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, no. 2, pp. 171–198, Feb. 2005, doi: 10.1016/j.jneumeth.2004.10.020.
[14] J. Xu, R. K. Shepherd, R. E. Millard, and G. M. Clark, "Chronic electrical stimulation of the auditory nerve at high stimulus rates: A physiological and histopathological study," *Hear. Res.*, vol. 105, pp. 1–29, Mar. 1997, doi: 10.1016/s0378-5955(96)00193-1.
[15] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 162–170, Jun. 2010, doi: 10.1109/TBCAS.2010.2040277.
[16] X. Liu, A. Demosthenous, and N. Donaldson, "Five valuable functions of blocking capacitors in stimulators," *Biomed. Techn.*, vol. 53, no. 1, pp. 322–324, Sep. 2008.
[17] A. Rothermel, L. Liu, N. P. Aryan, M. Fischer, J. Wuenschmann, S. Kibbel, and A. Harscher, "A CMOS chip with active pixel array and specific test features for subretinal implantation," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 290–300, Jan. 2009, doi: 10.1109/JSSC.2008.2007436.
[18] R. Ranjandish and O. Shoaei, "Polarity detection base pulse insertion for active charge balancing in electrical stimulation," in *Proc. IEEE Conf. Biomed. Eng. Sci. (IECBES)*, Kuala Lumpur, Malaysia, Dec. 2014, pp. 38–41.
[19] M. Ortmanns, A. Rocke, M. Gehrke, and H.-J. Tiedtke, "A 232-channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007, doi: 10.1109/JSSC.2007.908693.
[20] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2216, Sep. 2013, doi: 10.1109/JSSC.2013.2266862.
[21] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns, "A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 244–256, Jan. 2012, doi: 10.1109/JSSC.2011.2164667.
[22] R. Ranjandish and A. Schmid, "An active charge balancing method based on chopped anodic phase," in *Proc. 14th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Prague, Czech Republic, Jul. 2018, pp. 261–264.
[23] E. K. F. Lee and A. Lam, "A matching technique for biphasic stimulation pulse," in *Proc. IEEE Int. Symp. Circuits Syst.*, New Orleans, LA, USA, May 2007, pp. 817–820.
[24] S. Moradi, E. Maghsoudloo, and R. Lotfi, "A new approach to design safe and reliable electrical stimulator," *Int. J. Biomed. Eng. Technol.*, vol. 15, no. 4, pp. 305–316, Sep. 2014, doi: 10.1504/IJBET.2014.064820.
[25] R. Ranjandish and A. Schmid, "An active charge balancing method based on anodic current variation monitoring," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Turin, Italy, Oct. 2017, pp. 1–4.
[26] A. Banuaji and H.-K. Cha, "A 15-V bidirectional ultrasound interface analog front-end IC for medical imaging using standard CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 8, pp. 604–608, Aug. 2014, doi: 10.1109/TCSII.2014.2327455.
[27] J.-Y. Son and H.-K. Cha, "An anodic current pulse modulation active charge balancer for implantable electrical stimulator," in *Proc. 34th Int. Tech. Conf. Circuits/Systems, Comput. Commun. (ITC-CSCC)*, Jeju-Si, South Korea, Jun. 2019, pp. 1–4.
[28] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An integrated 256-channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946–1956, Sep. 2010, doi: 10.1109/JSSC.2010.2055371.
[29] B. Razavi, *Design of Analog CMOS integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill, 2001, pp. 364–373.

JIN-YOUNG SON (Graduate Student Member, IEEE) received the B.S. degree in electrical and information engineering from the Seoul National University of Science and Technology, Seoul, South Korea, in 2019, where he is currently pursuing the M.S. degree in electrical and information engineering. His research interest includes the design of bidirectional analog front-end CMOS integrated circuits.

HYOUK-KYU CHA (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2009, respectively.

From 2009 to 2012, he was a Scientist with the Institute of Microelectronics, (IME), Agency for Science, Technology, and Research (A∗STAR), Singapore, where he was involved in the research and development of analog/RF ICs for biomedical applications. Since 2012, he has been with the Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul, South Korea, where he is currently an Associate Professor. His research interests include low-power CMOS analog/RF IC and system design for implantable and wearable biomedical devices.