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High Power and High Frequency CMOS Oscillator With Source-to-Drain Coupling and Capacitive Load Reduction Circuit

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ABSTRACT A design for a high-output-power, high-frequency CMOS oscillator is presented in this paper. The proposed oscillator can increase the output power by coupling the signal at the source of the core transistor to the drain of the buffer transistor. In addition, the source-to-drain coupling generates an optimum negative transconductance at the desired operating frequency. A capacitive load reduction circuit is also applied to increase the fundamental oscillation frequency. Using these techniques, the fundamental and push-push oscillators were implemented using 65 nm CMOS technology. The measurement results of the fundamental and push-push oscillators showed 2.7 and −25 dBm of peak differential output power at 194 and 394 GHz, respectively. In the 200 GHz frequency band, the proposed fundamental oscillator shows the highest output power among recently reported state-of-the-art CMOS oscillators.

INDEX TERMS CMOS, oscillator, output power, THz, transformer.

I. INTRODUCTION

Recently, circuits operating in the Terahertz (THz) frequency band, which is defined as 300 GHz to 3 THz [1]–[3], is an attractive research topic. Because THz signals have properties such as penetration, straightness, and harmlessness, they have been applied for various scientific applications [4]. In the field of communication, the THz frequency band allows high-speed communication with abundant available unlicensed bandwidth [5]–[7]. Furthermore, THz waves have good penetration and are biologically innocuous, so they have been implemented in security imaging systems to find objects hidden in the human body, and in healthcare imaging systems to detect unhealthy tissues or in other biomedical applications [8]–[10]. To implement these systems, a THz signal source should have high output power and high operating frequency.

However, with THz frequency signal sources, it is hard to generate high power when implemented optically or electrically because the frequency range is too high for electronics but too low for optical devices [11], [12]. High-power THz sources were implemented using a quantum cascade laser and backward wave oscillator with the output power of a THz signal source in the milliwatt range [13]–[15]. However, the disadvantage of this approach is its bulkiness. Traditionally, compound technologies such as InP HBT and III-V compound semiconductors, are employed for implementing THz signal sources [16]–[18]. Nonetheless, the problem with this approach is that it is expensive and of low yield. Recently, due to the continuous scaling down of CMOS processes, the maximum oscillation frequency (f_{max}) of active devices has been increased. However, the effective f_{max} is still below 300 GHz, and f_{max} could be decreased further because of parasitic capacitance generated by the buffer stage and layout [19], [20]. Recent oscillators operating under 100 GHz can adopt variety techniques such as multi-resonant resistor-inductor-capacitor-mutual-inductance [21] or multi LC tank [22] to improve their performances, but these techniques are usually not efficient at operating frequency near f_{max}.

To overcome the operating frequency limitation in CMOS technology, several techniques are proposed to increase the oscillation frequency. First, a frequency multiplier [23]–[27]

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is used to generate a harmonic frequency by employing the characteristic of nonlinear devices (such as varactor and diode p-n junction) to distort the input signal. In [24], the frequency multiplier chain, which employs symmetric capacitance voltage (CV) varactor and asymmetric-CV varactor, generates an output power of −22.7 dBm at 1.4 THz. However, because the frequency multiplier presents high loss at high frequency, a high-power input signal source (18 dBm) at 140 GHz is required. Therefore, the integration of such a high-power oscillator in CMOS technology is challenging. As a result, in most of the published work using frequency multipliers, the signal source is generated using an external signal generator that is bulky and expensive in real operations. Second, the harmonic oscillators extract the n^{th} harmonic signal from output port [28]–[30]. At several GHz frequency range, rotary traveling-wave oscillators (RTWOs) that could extract high order harmonic frequencies are widely adopted [31]–[33]. Nonetheless, the single-output power-values at the harmonic frequencies are lower than those at the fundamental frequency, and thus are not high enough for use in a sub-THz signal source. To improve the output power, in a recent paper, a reasonable output power level (< 2.6 mW) was demonstrated by power combining of multiple oscillators, but the trade-off was large area (> 0.36 mm^2) and high-power dissipation (> 227 mW) [34], [35]. In this work, a high-power, high-frequency CMOS oscillator is proposed. The output power is increased by coupling the signal at the source of the core transistor to the drain of the buffer transistor. To obtain higher fundamental oscillation frequency, the proposed topology includes a capacitive load reduction circuit (CLRC). Using these techniques, a 194 GHz fundamental oscillator with the output power of 2.67 dBm was designed and implemented. This work is the extension of our work from [36]. To compare with [36], the two techniques applied to the proposed oscillator were systematically analyzed. In addition, to verify the analysis of the source-to-drain coupling, a 236 GHz fundamental oscillator with output power of −9 dBm was also designed. Furthermore, to enter the THz frequency band, a push-push oscillator was designed that oscillates at 394 GHz with output power of -25 dBm by using the proposed fundamental oscillator as oscillator core.

In Section II, the limitation of the conventional cross-coupled oscillator (XCO) with source inductor at high frequency is explained. In Section III, the proposed high power and high fundamental CMOS oscillator with the source-to-drain coupling (STDC) and CLRC is systematically analyzed and its function verified using a simulation tool. The design and measurement results of the fundamental and push-push oscillators are shown in Section IV. Finally, in Section V, the key features of this paper are summarized.

II. CROSS-COUPLED OSCILLATOR WITH SOURCE INDUCTOR

Figure 1 (a) and (b) show the schematic of the conventional XCO and XCO with source inductor (LS), respectively. Ideally, the maximal oscillation amplitude of a conventional

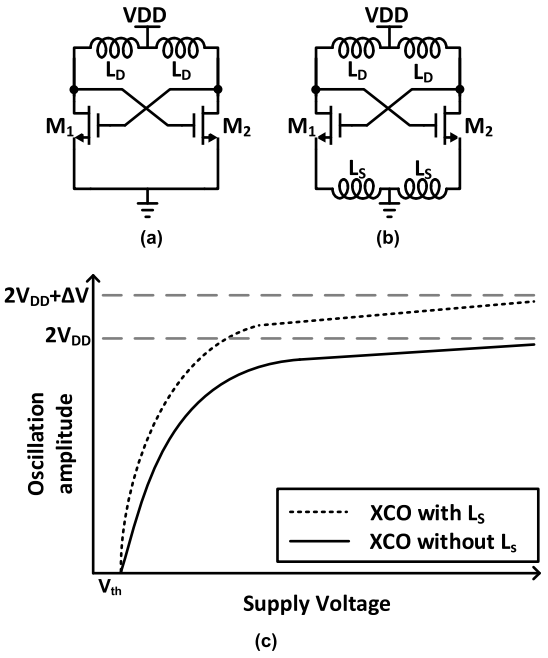


FIGURE 1. a) Conventional XCO, b) XCO with $_{LS}$, c) Oscillation amplitude of conventional XCO (solid line) and XCO with $_{LS}$ (dash line).

XCO can reach 2 VDD. On the contrary, the XCO with Ls enlarges the oscillation amplitude because the source inductor allows the voltage swing below ground. As a result, the XCO with L_S topology has been widely adopted to obtain high output power at low oscillation frequency. Different from the previous approach for only high-output power, the proposed oscillator uses the XCO with L_S to obtain not only high output power, but also high oscillation frequency.

To give insight into the effect of L_S on the oscillator performance, the small signal of the oscillator is analyzed. Figure 2 shows a simplified model of a transistor for analysis. To simplify the calculation and get tractable equations, the gate resistor (R_G), channel resistor (r_0), and gate-to-drain capacitor (C_{GD}) are ignored. The simplified model is applied in small-signal-equivalent circuits for a conventional XCO, and XCO with LS, as shown in Fig. 3 (a) and (b), respectively.

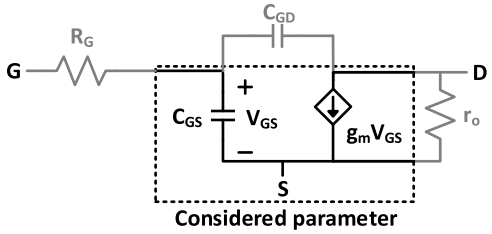


FIGURE 2. Simplified model of a transistor.

From Fig. 3(a), the input admittance of the conventional XCO is

$$Y_{in} = \frac{1}{2} \cdot (sC_{GS} - g_m) . \quad (1)$$

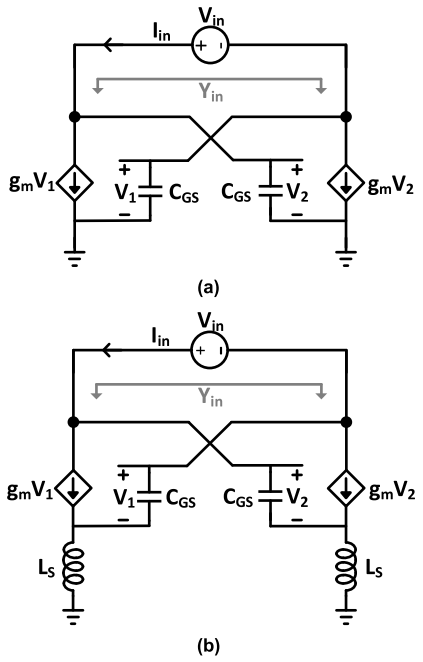


FIGURE 3. Equivalent small signal circuit of (a) conventional XCO, (b) XCO with LS.

where C_{GS} and g_m are the gate-to-source capacitance and transconductance of the transistor, respectively.

From (1), the real and imaginary parts of Y_{in} of the XCO are

$$\mathrm{Re}\{Y_{in}\} = -\frac{g_m}{2}. \tag{2}$$

$$\mathrm{Im}\{Y_{in}\} = \frac{\omega C_{GS}}{2}. \tag{3}$$

From Fig. 3 (b), the input admittance of the XCO with L_S is given by

$$Y_{in} = \frac{1}{2} \cdot \frac{sC_{GS} - g_m}{1 + g_m s L_S + s^2 L_S C_{GS}}. \tag{4}$$

From (4), the real and imaginary parts of Y_{in} of the XCO with L_S is

$$\mathrm{Re}\{Y_{in}\} = -\frac{g_m}{2} \cdot \frac{1 - 2\omega^2 L_S C_{GS}}{\left(1 - \omega^2 L_S C_{GS}\right)^2 + \omega^2 g_m^2 L_S^2}. \tag{5}$$

$$\mathrm{Im}\{Y_{in}\} = \frac{1}{2} \cdot \frac{\omega g_m^2 L_S + \omega C_{GS}\left(1 - \omega^2 L_S C_{GS}\right)}{\left(1 - \omega^2 L_S C_{GS}\right)^2 + \omega^2 g_m^2 L_S^2}. \tag{6}$$

Figure 4 shows the simulated transconductance and equivalent capacitance of the XCO with L_S from (5) and (6), at 200 GHz oscillation frequency. With a small value of the L_S (< 20 pH), the equivalent capacitance increases from 15 fF to 48 fF with increase in L_S, which leads to a decrease in the oscillation frequency. In contrast, with a large value of L_S (> 20 pH), the equivalent capacitance decreases with the increase of L_S, and becomes smaller than the equivalent capacitance of the conventional XCO with $L_S = 0$, so the effective oscillation frequency can be effectively increased.

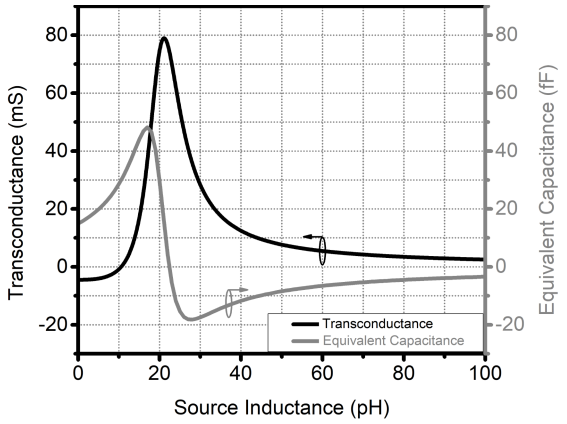


FIGURE 4. Transconductance and equivalent capacitance of XCO with LS calculated from equations at 200 GHz.

However, at that moment, the conventional XCO with L_S only generates positive transconductance, so the oscillation does not occur.

III. ANALYSIS OF PROPOSED FUNDAMENTAL OSCILLATOR

An XCO with a high L_S value could potentially improve the oscillation frequency by reducing the effective capacitance; however, it cannot satisfy the start-up condition to sustain the oscillation because of no negative transconductance generated at the high frequency. Therefore, a source-to-drain coupling (STDC) technique is proposed to solve this problem because it helps the XCO with L_S generate the negative transconductance at high frequency.

A. SOURCE-TO-DRAIN COUPLING

Figure 5 shows the schematic of the proposed oscillator with the source-to-drain coupling (STDC) technique. The coupling between the source inductor of the core transistor (M1 and M2) and the drain inductor of the buffer transistor (M3 and M4) forms a positive feedback. First, the effect of the STDC on the transconductance is analyzed. Figure 6 shows the small signal equivalent circuit for simplified calculation of the XCO with STDC. Here, it was assumed that all the transistors and inductance of the transformer are of the same size, so $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$, and $L_1 = L_2 = 2L$.

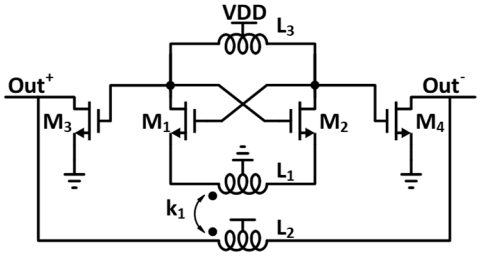


FIGURE 5. Proposed oscillator with source-to-drain coupling.

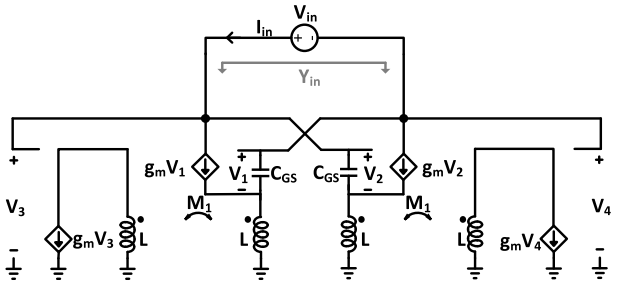


FIGURE 6. Equivalent circuit of proposed oscillator with STDC.

From Fig. 6, the input admittance of the XCO with STDC is

$$Y_{in} = \frac{1}{2}\frac{\frac{1}{sL} + \frac{M_1}{L}g_m}{g_m + sC_{GS} + \frac{1}{sL}}(sC_{GS} - g_m). \tag{7}$$

where M_1 is the mutual inductance of the STDC transformer. From (7), the real part of the oscillator is

$$\mathrm{Re}\{Y_{in}\} = \frac{2\omega^2 LC_{GS}g_m - g_m - \frac{M_1}{L}g_m + \frac{M_1}{C_{GS}}g_m^3 - \frac{M_1}{L}}{2\left[\left(1-\omega^2 LC_{GS}\right)^2 + \omega^2 L^2 g_m^2\right]}. \tag{8}$$

When $\omega = 1/\sqrt{LC_{GS}}$, it can be given by

$$\mathrm{Re}\{Y_{in}\} = \frac{g_m - \frac{M_1}{L}}{2g_m^2\frac{L}{C_{GS}}}. \tag{9}$$

From (9), because g_m is smaller than M_1/L, the proposed XCO with STDC can generate negative transconductance at the resonant frequency. Moreover, the negative transconductance can be tuned to a desired frequency by changing L or C_{GS}. To verify the theoretical equation and analysis, a circuit simulation with the value of L was carried out and the results are shown in Fig. 7. As can be seen in Fig. 7, the proposed XCO with STDC generates negative conductance range, and its frequency range is shifted up with decrease in L. The simulation results match well the prediction from (9).

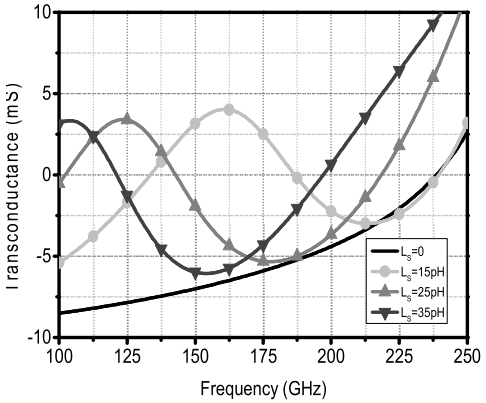


FIGURE 7. Transconductance of proposed oscillator with STDC versus Ls.

Next, the effect of the STDC on the voltage gain is analyzed. For calculation of the voltage gain, a half circuit of the XCO with STDC and its equivalent circuit are shown in Fig. 8. From Fig. 8 (b), the voltage gain from V_{in} (at the core transistor) to V_{out} (at the buffer transistor) is defined as follows:

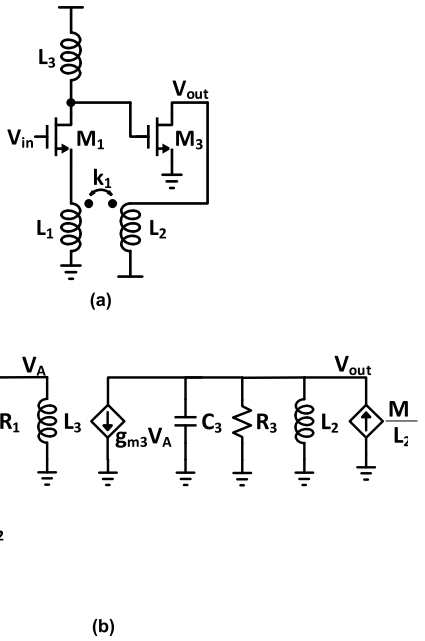


FIGURE 8. (a) Schematic and (b) Equivalent circuit of half circuit of XCO with STDC.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1}Z_{D1} \times g_{m3}Z_{D3}}{1 + g_{m1}Z_{S1}} + k_1\sqrt{\frac{L_2}{L_1}}\frac{g_{m1}Z_{D3}}{1 + g_{m1}Z_{S1}}. \tag{10}$$

where g_{m1} and g_{m3} are the transconductance of M_1 and M_3, respectively; Z_{D1}, Z_{D3}, and Z_{S1} are the respective impedances at the drain terminal of M_1, M_3, and the source M_1; and k_1 is the coupling factor between L_1 and L_2. On the other hand, the voltage gain of the XCO without coupling can be calculated from (10) by substituting $k_1 = 0$. The voltage gain of the proposed XCO with STDC has a larger voltage gain from the second term than that of the XCO with uncoupled source and drain inductors. Therefore, the proposed oscillator achieves higher output power.

Figure 9 shows the voltage magnitude of V_{in} and V_{out} with an increase in k1 at a supply voltage of 1.2 V in the proposed XCO with STDC. With increasing values of k1, the value of V_{out} also increases, because the larger second term of (9) results in an increase in the voltage gain. However, V_{out} is saturated above $k_1 = 0.6$, because of the steady decrease in V_{in}. Therefore, the optimum value of k_1 is 0.6, wherein both V_{in} and V_{out} are large, as seen in Fig. 9.

B. CAPACITIVE LOAD REDUCTION CIRCUIT

For further increase in the oscillation frequency, the CLRC is applied to the XCO with the SDTC structure. The inductor L in Fig. 5 is split into 2 inductors L_3 and L_4, so the inductance value $L = L_3 + L_4$ and the parasitic capacitance $C = C_3 + C_4$.

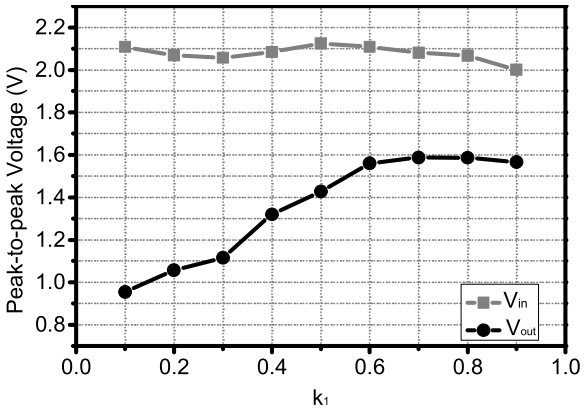


FIGURE 9. Simulated peak-to-peak voltage of V_{in} and V_{out}.

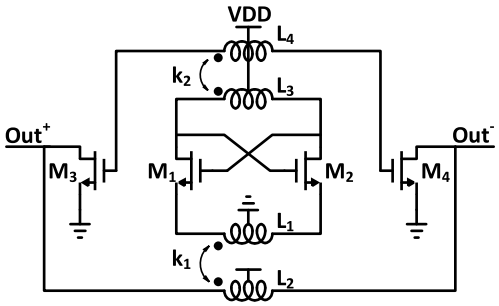


FIGURE 10. Proposed oscillator with CLRC.

Figure 10 shows a schematic representation of the proposed oscillator that combines CLRC and STDC with a conventional XCO. The CLRC significantly suppresses the effect of the parasitic load capacitance on oscillation frequency as it indirectly connects the buffer transistor to the LC-tank through the transformer with k_2 [32]. In Fig. 10, the primary port (L_3) of the transformer with a coupling factor k_2 is connected to the drain node of the core transistor (M_1 and M_2). The gate node of the buffer transistor (M_3 and M_4) is loaded to the secondary port (L_4).

Figure 11 shows the schematic and equivalent circuit of the CLRC. The load capacitor C_L represents the capacitor at the gate of transistor M_3 and M_4. Instead of directly connecting C_L to the oscillator tank as in a conventional XCO, C_L is indirectly connected to the oscillator tank through a transformer with coupling factor k_2. The equivalent capacitance C_{eq} (from the oscillator tank) is

$$C_{eq} = \frac{1}{\frac{1}{k_2^2}\left(\frac{L_3}{L_4}\cdot\frac{1}{C_L} - \omega^2 L_3\left(1-k_2^2\right)\right)}. \tag{11}$$

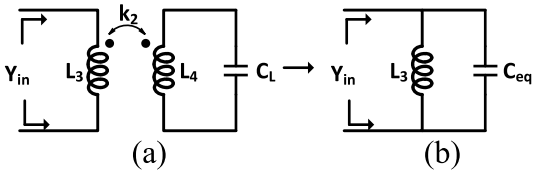


FIGURE 11. (a) Schematic and (b) Equivalent circuit of CLRC.

Based on (11), the normalized C_{eq} with the coupling factor k_2 from 0 to 1 was calculated and is shown in Fig. 12. As can be seen in Fig. 12, with the decrease of coupling factor k_2, C_{eq} of the XCO with CLRC is decreased, while C_{eq} of the XCO without CLRC keeps a constant value. To validate the effect of CLRC, the oscillation frequency and output power of the XCO with CLRC was simulated with coupling factor k_2 and plotted in Fig. 13. The oscillation frequency increases from 165 to 221 GHz with the decrease of coupling factor k_2 from 0.9 to 0.1, respectively. This shows a good match between equation theory and simulation result. However, the decrease of coupling factor k_2 from 0.9 to 0.1 results in reduction of the output power from 4.1 to −0.1 dBm, as can be seen in Fig. 13. Therefore, to achieve both high oscillation frequency and high output power, a coupling factor (k_2) of 0.4–0.5 was selected.

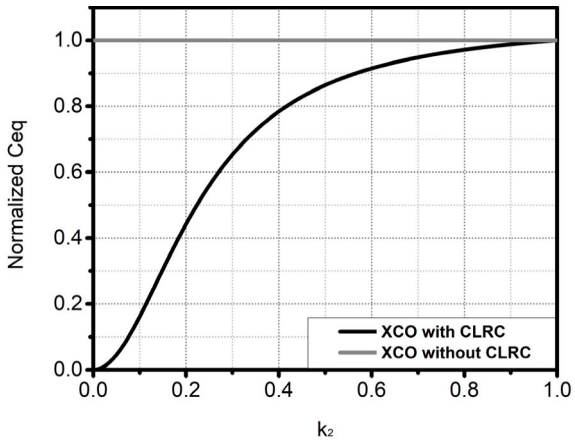


FIGURE 12. Equivalent capacitance versus coupling factor k_2.

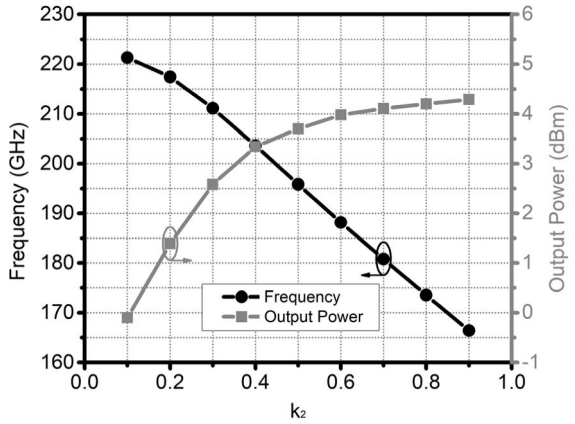


FIGURE 13. Simulation results of the oscillation frequency and output power versus coupling factor, k_2.

To verify the theoretical analysis, the voltage magnitude of the proposed oscillator with STDC and CLRC was simulated at 200 GHz (the fundamental oscillation frequency) and compared with those of the circuit simulation seen in Fig. 14. According to theoretical analysis, the proposed CLRC oscillator with the STDC has larger V_{out} (in the overall supply

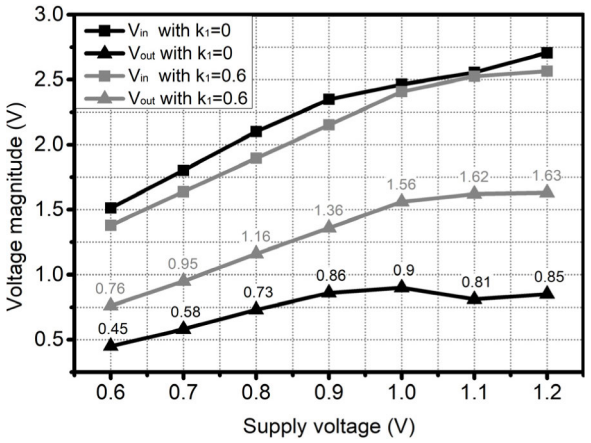


FIGURE 14. Simulated voltage of V_{in} and V_{out} with k2.

voltage range) than that of the conventional CLRC oscillator. Specifically, the V_{out} of the proposed oscillator (1.59V) is almost two-times greater than that with the conventional topology (0.81V) at a supply voltage of 1.1 V, while V_{in} of both oscillators is similar.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

A. DESIGN OF THE PROPOSED FUNDAMENTAL OSCILLATORS

To validate the theoretical analysis and performance of the proposed topology, the high fundamental CMOS oscillator shown in Fig. 15 was designed to operate at 194 and 236 GHz. Compared with the 194 GHz oscillator, only the size of the transistors was reduced in the 236 GHz oscillator; the other components are identical. For the 194 GHz oscillator, the sizes of the core transistors (M_1 and M_2) were 16μm and 0.06μm, the inter-stage transistors (M_3 and M_4) were 10μm and 0.06μm, and the buffer transistors (M_5 and M_6) were 16μm and 0.06μm. For the 236 GHz oscillator, the sizes of the core transistors (M_1 and M_2) were 9.6μm and 0.06μm, the inter-stage transistors (M_3 and M_4) were 4.8μm and 0.06μm, and the buffer transistors (M_5 and M_6) were 9.6μm and 0.06μm. The size of the inter-stage transistor is half of that of the core transistor to reduce the loading effect, which leads to improvement of the oscillation frequency.

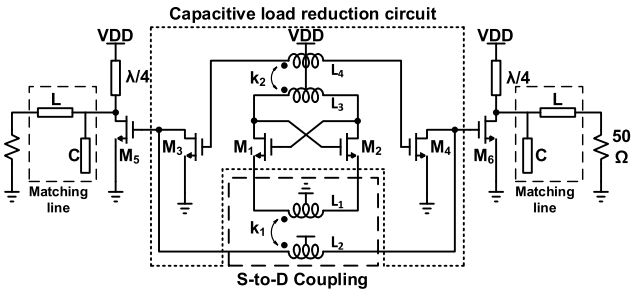
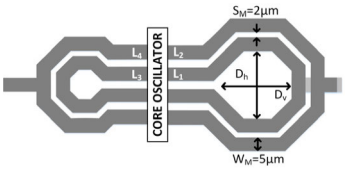


FIGURE 15. Schematic of the proposed fundamental oscillator.

Several losses degrade the quality factor of an on-chip transformer in the sub-THz frequency band. The resistive loss due to metal resistance and skin effect is critical at high frequency. The substrate loss due to the coupling power from the transformer to the lossy bulk is also noticeable. At frequency lower than 100 GHz, the patterned ground shield technique is proposed to minimize the coupled power to substrate loss by reducing the silicon substrate resistance, so it can effectively improve the Q-factor of the transformer. However, the shielding techniques are not effective at frequency higher than 100 GHz because the increase of parasitic capacitance becomes the dominant factor in determination of the quality factor, rather than the decrease of silicon substrate resistance [38]. Therefore, an unshielded transformer is used with the proposed oscillators.

The transformer was designed and optimized using an EM simulator. Figure 16 shows the layout pattern of the transformers for the STDC with k_1 and CLRC with k_2. Based on the transistor sizes above, the inductance value of the STDC transformer was $L_1 = 57$ pH, $L_2 = 85$ pH, with Q-factor of 31 and 23, respectively. The inductance value of the CLRC transformer was $L_3 = 21$ pH, $L_4 = 42$ pH, with Q-factor of 26 and 27, respectively. Both transformers were implemented using an ultra-thick metal layer with width of 5μm to minimize the skin effect. The turn space of the transformer was 2μm, which is equivalent to a coupling factor k_1 of 0.6 and k_2 of 0.45. These two values of the coupling factor satisfy the condition to optimize both high output power and high oscillation frequency for the proposed oscillator, as discussed for the transformer designs shown in Fig. 9 and Fig. 13. For the transformer design, the ratio (γ) between the length of horizontal direction (D_h) and vertical direction (D_v) is also a critical factor to determine the Q-factor. As discussed in [39], γ should equal 1 to achieve the optimum Q-factor, so D_h and D_v were selected to provide $\gamma = 1$ in our transformer design.



CLRC Transformer

L_3	21 pH
L_4	42 pH
k_2	0.45
Q_3	26
Q_4	27

STDC Transformer

L1	57 pH
L2	85 pH
k_1	0.6
Q_1	31
Q_2	23

FIGURE 16. Layout and parameters of transformers.

In Fig. 15, the $\lambda/4$ line and matching line are implemented as the transmission line. Because the transmission line transfers the output power of the oscillator to load, the insertion loss of the transmission line should be minimized. The $\lambda/4$ transmission line is implemented as a microstrip line and implemented on the ultra-thick metal (UTM) layer with

a metal ground at 2 bottom metal layers M1 and M2 to minimize loss. The λ/4 transmission line has a dimension W×H = 3.5 × 3.4um for a characteristic impedance of 50Ω to match with a 50Ω output load.

B. DESIGN OF THE PUSH-PUSH OSCILLATOR

A push-push oscillator was implemented using the proposed high fundamental frequency oscillator to extend the oscillation frequency into the THz frequency band. The 2nd harmonic frequency is extracted from the transmission line. Compared with standing wave push-push VCO which was presented in [34], the transmission line has more flexible choices of length since the transmission line is connected to buffer stage not to oscillator tank. Figure 17 shows the schematic of the push-push oscillator using the proposed XCO with the STDC and CLRC. The fundamental oscillator shown in Fig. 15 has differential outputs, and the λ/4 and matching transmission lines (L and C) were realized individually. In contrast, one transmission line in the proposed push-push oscillator in Fig. 17 plays the role of both the λ/4 line, and inter-stage matching between the core oscillator and output load. In addition, the transmission line has two functions. The first function is to supply DC power at one end, and the second is to extract the 2nd harmonic frequency at the other end.

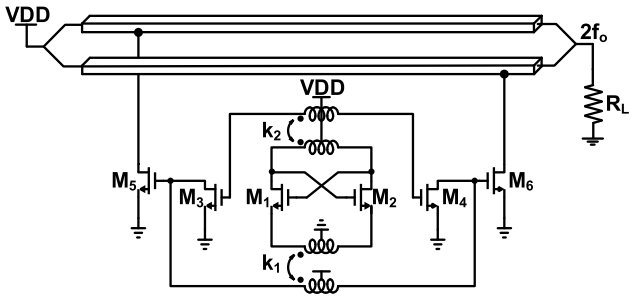


FIGURE 17. Schematic of proposed push-push oscillator.

Figure 18 shows the layout and dimension of the transformers and transmission line of the proposed push-push oscillator. In this design, for the maximum output power extraction

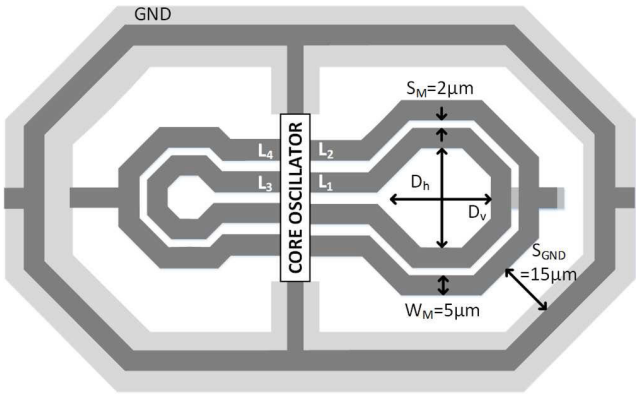


FIGURE 18. Layout and dimensions of transformers and transmission line.

the electrical length from the core oscillator to power supply equals 90° at the 2nd harmonic frequency, so most of the 2nd harmonic power goes to the output port. For the balance voltage swing between the two sides of the transmission line, the length of the transmission line from the core oscillator is the same as the length of the transmission line from the core oscillator to the power supply. To minimize the undesired coupling effect between transmission line and transformers, the minimum space between the two elements was set to 15 μm with coupling factor smaller than 0.1.

C. MEASUREMENT RESULTS OF THE FUNDAMENTAL OSCILATORS

The proposed fundamental oscillators were fabricated using 65 nm CMOS technology. Fig. 19 (a) and (b) show the chip micrograph of the 194 GHz and 236 GHz proposed fundamental oscillators with chip area of 468μm × 376μm and 450μm × 340μm, respectively.

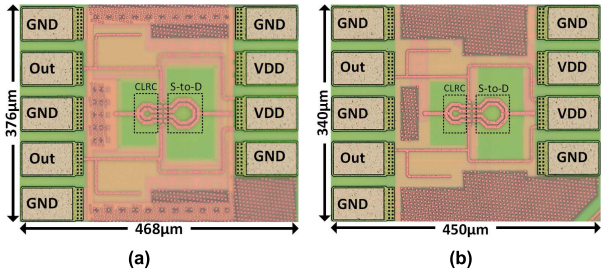


FIGURE 19. Chip micrograph of the (a) 194 GHz and (b) 236 GHz proposed fundamental oscillators.

Fig. 20 (a) shows the frequency measurement setup of the G band (140–220 GHz) for the 194 GHz fundamental oscillator. A GGB model 220 RF probe was used to probe the output signal. A waveguide WR-5 was connected to the probe, and then the output signal was down-converted using an OML WR-5 harmonic mixer. The down converted IF signal was sent to a spectrum analyzer. Figure 21 (a) shows the spectrum measurement result with the measured oscillation frequency of 194 GHz. Figure 21 (b) shows the tuning range from 200 GHz to 194.6 GHz with the voltage supply from 0.5 to 2 V. A power meter PM5 was used to measure the

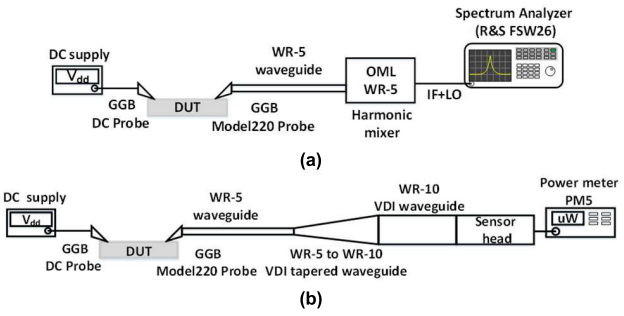


FIGURE 20. G band measurement setup (a) Spectrum frequency, (b) Output power.

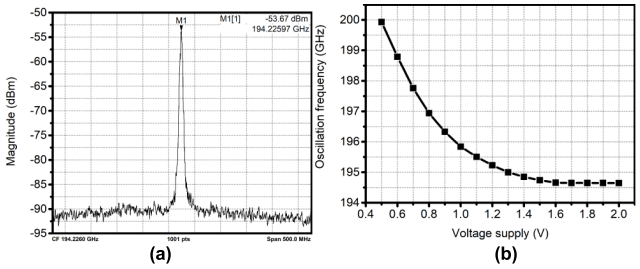


FIGURE 21. (a) Measured spectrum frequency and (b) measured tuning range of the 194 GHz proposed fundamental oscillator.

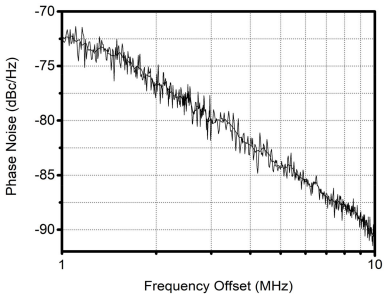


FIGURE 22. Measured phase noise of the 194 GHz proposed fundamental oscillator.

output power of the proposed oscillators. Figure 22 shows the measured phase noise of the 194 GHz fundamental oscillator is −92dBc/Hz at 10 MHz offset. The G-band power measurement setup is shown in Fig. 20 (b). A GGB model 220 probe was used to probe the output signal. After that, the output signal was transmitted through a WR-5 waveguide, a WR-5 to WR-10 VDI tapered waveguide, and a WR-10 VDI waveguide. Finally, the output signal entered the sensor head, and the output power level was read by the power meter PM5. The total insertion loss from the probe tip (4dB), WR-5 waveguide (1 dB), WR-5 to WR-10 VDI tapered waveguide (0.35 dB), and WR-10 VDI waveguide (0.2 dB) is 5.6 dB. Figure 23 (a) shows the highest measured calibrated output power of the 194 GHz fundamental oscillator was 1.85 mW (2.7 dBm). As shown in Fig. 23 (b), the output power of the 194 GHz oscillator was 0.05–1.85 mW with

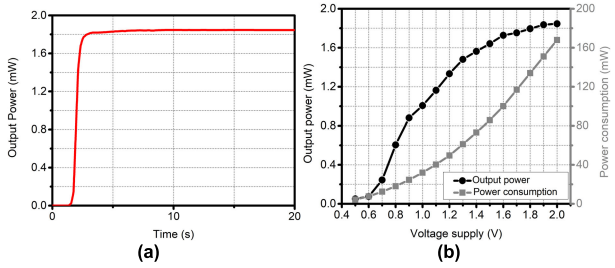


FIGURE 23. (a) Measured maximum output power and (b) measured output power vs. voltage supply of the 194 GHz proposed fundamental oscillator.

supply voltage from 0.5–2 V while dissipating from 4.35 to 168 mW of DC power.

To measure the frequency spectrum and output power of the 236 GHz oscillator, a J-band frequency (220–325 GHz) measurement setup was used. Compared with the measurement setup for G-band frequency, the difference in the measurement setup for J-band frequency was replacement of the WR-5 interface with a WR-3 interface. Figure 24 shows the measured spectrum output at the frequency of 236 GHz and its tuning range. The measured tuning range of the 236 GHz oscillator was from 238 to 234.2 GHz when the supply voltage changed from 0.6 to 1.4 V. Figure 25 shows the measured phase noise of the 236 GHz fundamental oscillator is −80dBc/Hz at 10 MHz offset. The insertion losses of the GGB 325B probe, WR-3 waveguide, WR3.4-WR10 VDI taper waveguide, and WR-10 VDI waveguide which are used in the power measurement setup at the J-band frequency are (3, 1, 0.37, and 0.22) dB, respectively, so the total insertion loss is 4.6 dB. Figure 26 (a) shows the highest measured power of 0.125 mW (−9 dBm) at the supply voltage of 1.1 V. Figure 26 (b) shows the output power from 0.022 to 0.125 mW with power supply voltage from 0.6 to 1.1V, while dissipating from 5.37 to 85 mW of DC power.

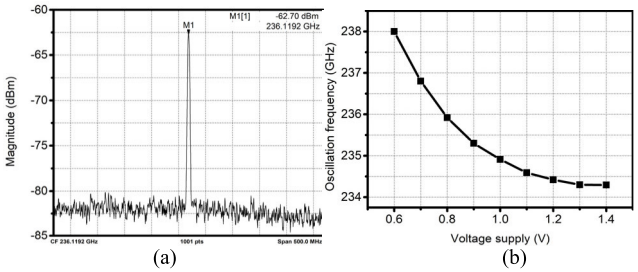


FIGURE 24. (a) Measured spectrum output and (b) measured tuning range of the 236 GHz proposed fundamental oscillator.

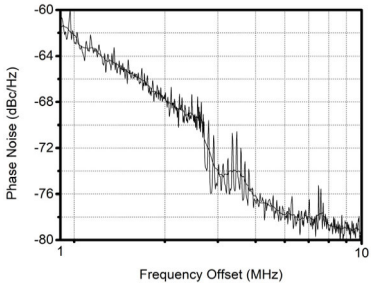


FIGURE 25. Measured phase noise of the 236 GHz proposed fundamental oscillator.

D. MEASUREMENT RESULTS OF THE PUSH-PUSH OSCILLATOR

The proposed push-push oscillator was fabricated using 65 nm CMOS technology. Figure 27 shows the chip micrograph of the proposed push-push oscillator with chip area of 410μm × 210μm. Figure 28 shows the frequency measurement setup of the 394 GHz push-push oscillator. A GGB

TABLE 1. Performance comparison with state-of-the-art sub-Thz signal generators.

	Frequency (GHz)	Type	P_{out} (dBm)	P_{DC} (mW)	Efficiency (%)	FoM (dBc/Hz)	Area (mm^2)	Technology
[37]	219	Fundamental	-3	24	2.08	-	0.105	65nm CMOS
[39]	239	2nd Harmonic	-4.8	18.5	1.79	173.3	0.18	65nm CMOS
[40]	190.5	2nd Harmonic	-2.1	294	0.2	163.5	0.64	130nm SiGe
[41]	210	2nd Harmonic	1.4	61	2.3	176	0.08	130nm SiGe
[42]	201.5	2nd Harmonic	-7.2	30	0.6	178	0.073	130nm SiGe
[43]	164.6	2nd Harmonic	1	88	1.4	143.9	0.1	65nm CMOS
[44]	228	3rd Harmonic	-6.2	86.4	0.3	178	0.172	90nm CMOS
[45]	210	Fundamental	-13.5	42	0.1	171.3	3.5	32nm SOI CMOS
This	**194**	**Fundamental**	**2.7**	**168**	**1.1**	**155.5***	**0.176**	**65nm CMOS**
This	**236**	**Fundamental**	**-9**	**29**	**0.4**	**152.8***	**0.153**	**65nm CMOS**
[46]	410	2nd Harmonic	-47	16.5	1.2E-4	-	0.25	45nm CMOS
[47]	482	3rd Harmonic	-7.9	61	0.3	171	0.022	65nm CMOS
[48]	553	4th Harmonic	-36.5	64.6	3.4E-4	-	0.29	45nm CMOS
This	**394**	**2nd Harmonic**	**-25**	**38**	**0.008**	**-**	**0.086**	**65nm CMOS**

* FoM calculated with DC power consumption of buffer stage
FoM=|PN{f_{offset}}-20log(f_{osc}/f_{offset})+P_{DCcore}(dBm)|

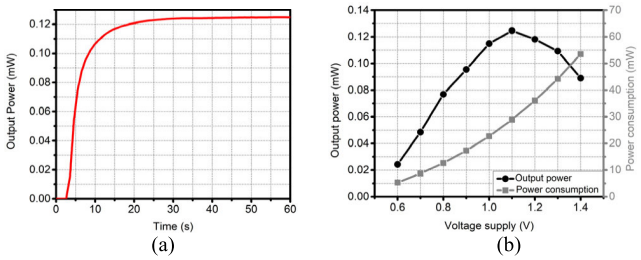


FIGURE 26. Measured maximum output power and measured output power vs. voltage supply of the 236 GHz proposed fundamental oscillator.

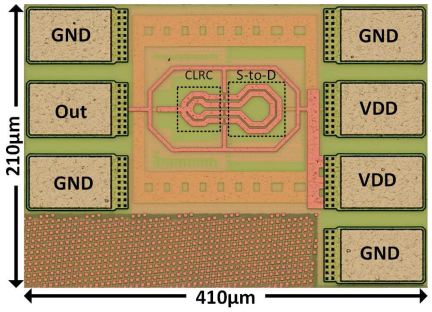


FIGURE 27. Chip micrograph of the 394 GHz proposed push-push oscillator.

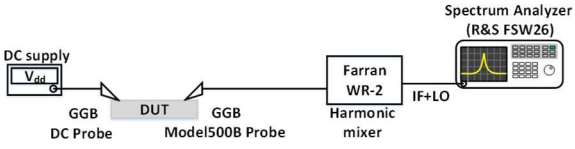


FIGURE 28. Y band spectrum frequency measurement setup.

model 500B RF probe was used to probe the output signal. A Farran WHMB-02 harmonic mixer was connected to the probe tips to down-convert the output signal with the LO signal generated from a spectrum analyzer (R&S FSW26). After that, the IF signal was sent to the spectrum analyzer.

Figure 29 shows the measured spectrum output at the frequency of 394 GHz. The insertion losses of the GGB 500B probe, WR-3 waveguide, WR3.4–WR10 VDI taper waveguide, and WR-10 VDI waveguide used in the power measurement of the Y-band frequency were 4dB, 2dB, 0.45dB, and 0.3dB, respectively, so the total insertion loss is 6.8 dB. Figure 30 illustrates the highest measured power of 3.15 μW (−25 dBm) at the supply voltage of 1 V while dissipating 38 mW of DC power.

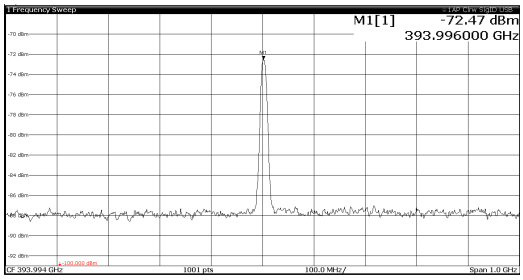


FIGURE 29. Spectrum measurement result of the proposed push-push oscillator.

Table 1 shows a comparison of the performance of the proposed CMOS oscillators with state-of-the-art high frequency oscillators that were operated in the frequency range of 160 to 240 GHz and 390 to 550 GHz. Even with the differential output signal and using the standard 65 nm CMOS process, the proposed fundamental oscillator at 194 GHz has the highest output power, as can be seen in Fig. 31. Furthermore, the proposed 236 GHz CMOS oscillator has the highest fundamental oscillation frequency among similar CMOS processes with competitive output power. At the highest output power, compared to the 236-GHz oscillator and the

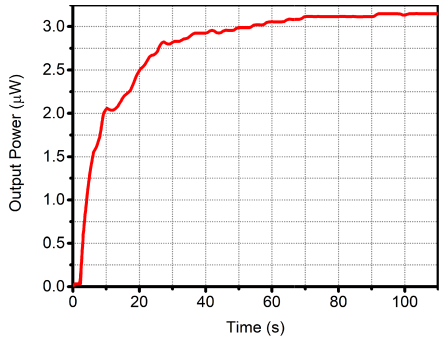


FIGURE 30. Measured maximum output power of the 394 GHz proposed push-push oscillator.

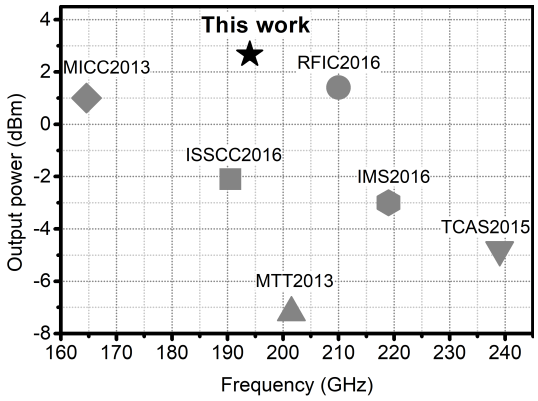


FIGURE 31. Comparison of output power of the 194 GHz proposed fundamental oscillator with other state-of-the-art oscillators.

394-GHz oscillator, the 194-GHz oscillator consumes a high DC power consumption; however, at the same output power, the 194-GHz oscillator has a lower DC power consumption compared with the 236-GHz oscillator and the 394-GHz oscillator. The proposed push-push CMOS oscillator also shows a high operating frequency at the second harmonic and good output power.

V. CONCLUSION

This work presents circuit techniques and theories to improve the output power and oscillation frequency using the CMOS process. The coupling technique between the source and the drain signals (STDC) in a conventional cross-coupled oscillator with source inductor can significantly increase both the oscillation frequency and amplitude. The capacitive load reduction circuit (CLRC) technique further increases the oscillation frequency. Applying both techniques, a cross-coupled fundamental oscillator and a push-push oscillator with STDC and CLRC are newly proposed in this paper. To verify the results of theoretical analysis, and projected performance, two prototypes were implemented using the 65 nm CMOS process. The proposed fundamental CMOS oscillators were operated at l94 GHz and 236 GHz with maximum output power of 1.85 mW and 0.125 mW, respectively. The fabricated push-push CMOS oscillator was measured at 394 GHz with output power of 3.15 μW. The proposed 194 GHz CMOS oscillator showed the highest output power among state-of-the-art oscillators that include the compound semiconductor and SOI process operating around 200 GHz. The proposed CMOS oscillator can be used as a low-cost, compact, high output power signal source for THz applications.

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