IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 2, 2020, accepted July 20, 2020, date of publication July 23, 2020, date of current version August 5, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3011453

An Investigation of Frequency Dependent Reliability and Failure Mechanism of pGaN Gated GaN HEMTs

ROSHAN L. KINI, (Member, IEEE), SHANKAR DHAKAL, (Member, IEEE), SADAB MAHMUD, (Member, IEEE), ANDREW J. SELLERS, (Member, IEEE), MICHAEL R. HONTZ, (Member, IEEE), CHEIKH A. TINE, (Member, IEEE), AND RAGHAV KHANNA, (Senior Member, IEEE)
The University of Toledo, Toledo, OH 43606, USA

Corresponding author: Raghav Khanna (raghav.khanna@utoledo.edu)

This work and related experiments were conducted in the Electrical Engineering and Computer Science Department at University of Toledo, Ohio, USA. The work was supported by the US Office of Naval Research under Grant N00014-18-2676 and was approved for public release under Document Control Number 43-6560-20.

ABSTRACT This paper presents a frequency dependent reliability study of commercially available GaN HEMTs. Both circuit and device-level experiments were performed to better understand the device-level cause of degradation. It was determined through step-frequency analysis performed in a boost converter that there is a frequency-dependent device degradation for positive gate stress. The point of degradation and its primary effect on the converter before the circuit ultimately failed have been analyzed with converter efficiency, gate current, and gate voltage overshoot. The findings of this experiment clearly show a decline in efficiency and voltage overshoot and increment in gate current, which are linked to device degradation. Furthermore, the recovery behavior of degraded devices has been investigated. However, after initial degradation, devices did not show any signs of recovery over twenty-four-hour recovery periods. The causal origin of these phenomena associated with the gate structure of the device was established by gate step-stress testing as well as an examination and analysis of the possible conduction mechanisms through the gate structure.

INDEX TERMS Frequency dependent, gate-stress, GaN, reliability, voltage overshoot.

I. INTRODUCTION

Wide bandgap (WBG) semiconductor devices, such as those based on gallium nitride (GaN) and silicon carbide (SiC), facilitate the development of high-power, switch-mode power electronics that can realize higher temperatures, voltages, and frequencies as compared to those utilizing traditional silicon (Si) devices. This allows power electronics based on WBG semiconductors to achieve higher power densities and efficiencies than previously possible. Of particular interest is GaN high electron mobility transistors (HEMTs). HEMTs combine the voltage blocking properties inherent in GaN's wide bandgap with high conductivity due to GaN's ability to spontaneously form a two-dimensional electron gas (2DEG) when interfaced with aluminum gallium nitride (AlGaN). These properties allow the use of GaN HEMTs in power electronic applications that are not realizable with other device technologies [1]–[4].

Nearly all commercially-available GaN devices are lateral HEMTs. In recent years, technological development has been devoted toward the AlGaN/GaN HEMT, which leads to increased breakdown voltage, reduced ON-resistance, suppressed current collapse, and reduced gate leakage current [5]. Although, from the terminal behavior, these HEMT devices exhibit similar current-voltage (I-V) characteristics to traditional MOSFETs, the unique construction and physics involved in GaN HEMTs give rise to properties that are not seen in MOSFETs [6].

One phenomenon unique to GaN HEMTs arises as a consequence of the AlGaN/GaN heterojunction. The spontaneous piezoelectric effect causes a 2DEG to form at the AlGaN/GaN interface, forming a channel in the device at zero bias unless designs are implemented to compensate for this [7]–[9]. Such a depletion-mode or normally-on device is not desirable for

The associate editor coordinating the review of this manuscript and approving it for publication was Yu Wang.

power electronics systems, so steps must be taken to create an enhancement mode device. There are several effective ways to accomplish this, each with their own benefit: the use of fluorinated gate dielectrics [10], the use of a recessed gate structure [11], a pGaN gate [12], a pAlGaN gate, and a cascode of an enhancement mode device with a low-voltage normally-off Si device [13].

Despite significant advances in GaN device capabilities, a major factor inhibiting the widespread adoption of GaN devices in deployed power electronic systems is a lack of knowledge concerning GaN devices' reliability, especially in particular converter circuits. Previous semiconductor physics research has focused on phenomena such as (but not limited to) current collapse, hot carrier injection, trap generation, gate edge degradation, and the inverse piezoelectric effect. In order to overcome these challenges and hasten the adoption of GaN devices, two concurrent research paths must be pursued. The first involves the design of devices that mitigate or solve these reliability problems. The second involves the study and quantification of these effects and their impacts on converter-level performance. This enables converters to be designed in such a way that reduces the likelihood of degradation. However, the variety in converter topologies as well as available GaN devices complicate the second research path. Additionally, the use of hard-switching in power electronics [14] also increases the stress on components regardless of material. Although GaN technology allows for the efficient implementation of higher switching frequencies in converters, these high edge rates, and large ringing exacerbate the failure of switching devices in hard switching conditions, which can lead to system failure [15]. Therefore, it is necessary to investigate the reliability study of switching devices at the circuit level in addition to the device level.

In application-relevant reliability testing, analysis is usually performed with double-pulse testing (DPT) due to its simplicity and isolation of temperature effects. The analysis in this paper is performed using a boost converter, thereby allowing investigation of device reliability in a more practical setting. The transistor in the converter operates in three fundamentally different bias conditions: the off-state, the semi-on state, and the on-state. These bias conditions are responsible for different degradation modes [16]. Forward bias gate breakdown, for example, is mainly associated with on-state and semi-on state biases, which can be analyzed in a hard-switched converter.

Although the converter is more complex, it accounts for two effects that are not present in the DPT. This enables the performance and reliability of the device in a commercial setting to be assessed. The first is the presence of parasitic inductances that are observed in converters and have a potentially significant effect on device performance [17]. The second is the effect of higher switching frequency on degradation mechanisms. In a commercial use case, the device is operated at a higher switching frequency in order to reduce the size of the converter and increase power density. It is, therefore, vital to investigate frequency-dependent degradation mechanisms at the converter level, as parasitic inductances are most influential in high-frequency operation.

The reliability study presented in [18] for MOS-gated devices, exhibits a frequency-dependent mean-time-to-failure (MTTF) for positive gate stress. The device failure is caused by the locally altered electric field due to trapping/de-trapping of charges in the dielectric or the interface. Time-to-breakdown depends on trapping and de-trapping rate and thus depends on the switching frequency [18]. However, reliability studies for commercially available Schottky type p-GaN gate HEMTs on the frequency-dependent gate degradation for positive gate stress are limited. The reliability study presented in [19] exhibits no noticeable difference by varying frequencies between 10kHz and 100kHz in the MTTF for positive gate voltage stress.

In this paper, the frequency-dependence of gate stress reliability of commercially available lateral 100-V Schottky type p-GaN gated devices [20] is assessed for frequencies ranging from 100kHz to 1.5MHz. The analysis was performed at both the circuit level as well as the device level. In circuit-level experimentation, the device was subjected to stress typical of a device in a commercial, hard-switched boost converter. Testing was performed at varying frequencies and a varying steady-state gate driving voltages. Device-level testing was focused on step-stress methods consistent with work presented in previous literature for GaN reliability [21]–[23]. The relation between observations of converter-level performance and degradation were then correlated with device-level phenomena and testing. In addition, degraded GaN devices have been re-tested in the frequency sweep test to analyze the recovery behavior of the device. The results have revealed a close relationship between V_{GS} overshoot, gate current, and efficiency pre, post, and during degradation, which can be very useful in understanding converter failure mechanisms. In this way, this paper provides a framework for assessing the effects of device reliability and degradation on circuit performance while also demonstrating where effort in device design can be directed to improve converter performance of GaN devices.

The motivation for the frequency-dependent investigations pursued here can be attributed to the emergence of spectral content in GaN and SiC-based power converters traditionally observed in the RF community. That is, the extended dynamics observed in GaN and SiC-based power converters can result in spectral content orders of magnitude above the switching frequency. As discussed in [24], the spectral content observed in GaN and SiC-based circuits can lead to capacitive dispersion, where the inter-electrode capacitances exhibit frequency-dependence. Such phenomena can be difficult to model, and by extension, predict. Indeed, in [25] a preliminary method for modeling dispersive behavior in wide bandgap semiconductors was presented. The model in [25] was only capable of predicting the device's empirical performance when the frequency dependence of the parasitics was taken into consideration. This was demonstrated by adopting a behavioral modeling approach, where frequency-dependent

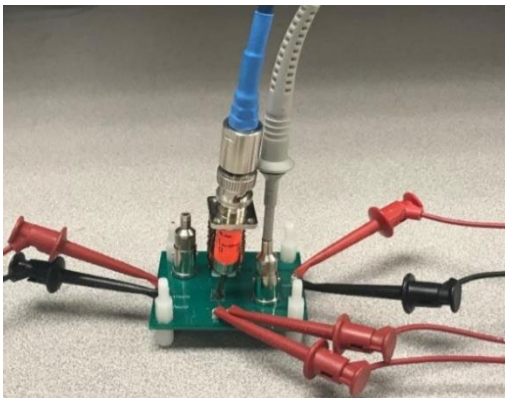

FIGURE 1. Experimental setup for device reliability testing in a converter.

curve-fitting parameters were used as coefficients to adjust the magnitude of the device capacitance. The behavioral modeling technique conclusively showed the necessity of taking into account capacitive dispersion for next generation wide bandgap semiconductor model-development. However, the power electronic community would also benefit from a more physically descriptive model of the anomalous high-frequency behavior seen in both GaN and SiC, as well as an assessment of the effects of this extended frequency content on the performance and failure of commercial devices. For these reasons, a converter-level frequency-dependent investigation was pursued here. The phenomena observed and reported in this paper, as well as the explanations provided, can thus be used to inform and expand the design of future physical models based on GaN and SiC.

This paper is organized as follows: Section II presents a converter-level experiment setup and its results. Section III presents a device-level reliability study and its results. Section IV investigates the device degradation phenomena. Section V concludes the presented work and discusses future scope.

II. CONVERTER LEVEL EXPERIMENTAL SETUP AND RESULTS

A. POSITIVE GATE STRESS TEST WITH VARYING SWITCHING FREQUENCY IN BOOST CONVERTER

The aim of the converter level forward-biased gate reliability study is to contribute to the understanding of the failure mechanisms of GaN-based transistors in real-life applications when encountering higher-than-recommended gate voltages. The device performance was assessed in a prototype boost converter shown in Fig. 1, with the schematic and parameters shown in Fig. 2 and Table 1. With the GaN device placed in a hard-switched boost converter, a step-frequency stress analysis was performed to analyze the devices' failure mechanisms at different forward biased gate voltages. The critical degradation point of the devices was closely monitored in terms of converter efficiency, gate current, and gate voltage overshoot. In this experiment, the frequency was varied from 100 kHz to 1.5 MHz in increments of 100kHz every three

TABLE 1. Boost converter parameter.

Parameter	Value
Output Voltage	60 V
Power	36W
Duty Cycle	0.5
Switching device (Q1)	100V GaN [20]
Gate resistor	6.2 Ω
Inductor (L1)	0.8 mH
Capacitor (C1)	0.47 µF
Current viewing resistor	SDN-414-10

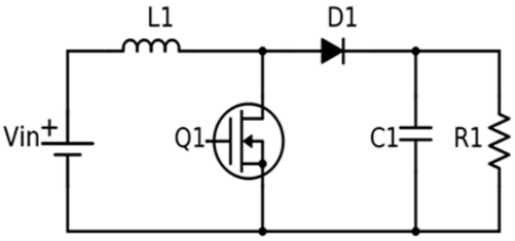

FIGURE 2. Boost converter topology.

minutes at a given steady-state Gate-to-Source voltage (V_{GS}). This process was then repeated for different steady-state V_{GS} values from 5.2V to 6V of 0.2V increment. The various results were analyzed to find the optimum operating conditions of the converter. By progressively stepping frequency and gate voltage, specific points at which the GaN device started to show signs of performance degradation could be identified. Various parameters were tracked for performance: input current, output voltage, gate voltage overshoot, and steady-state gate current. In order to scrutinize the performance of the device at out-of-specification gate voltages, forward-biased gate voltages were applied, which were in excess of the recommended 5V [20].

The step-frequency stress analysis allowed for several significant observations. While operating at the recommended gate voltage, the converter remained consistent in performance, and no unexpected significant drops in efficiency were recorded. The GaN devices showed no sign of degradation throughout the test. However, when the steady-state V_{GS} was increased to 5.8V or higher, a significant drop in efficiency was recorded after some time. The drop in efficiency occurred concurrently with an increase in gate current. The efficiency changes versus frequency and its comparison with gate current and gate voltage overshoot can be seen in Figs. 3 and 4.

GaN devices, here termed as ''Part Q'', and ''Part T'' were run from 100 kHz to 1.5 MHz with 100 kHz increment as shown in Fig. 3 and 4. After the entire spectrum of frequencies was swept, V_{GS} was incremented by 0.2V and the frequency sweep was repeated again. This process repeated from 5.2V to 6V gate source voltage. At each V_{GS} and frequency pair, the efficiency of the converter, gate current, and gate voltage overshoot was recorded.

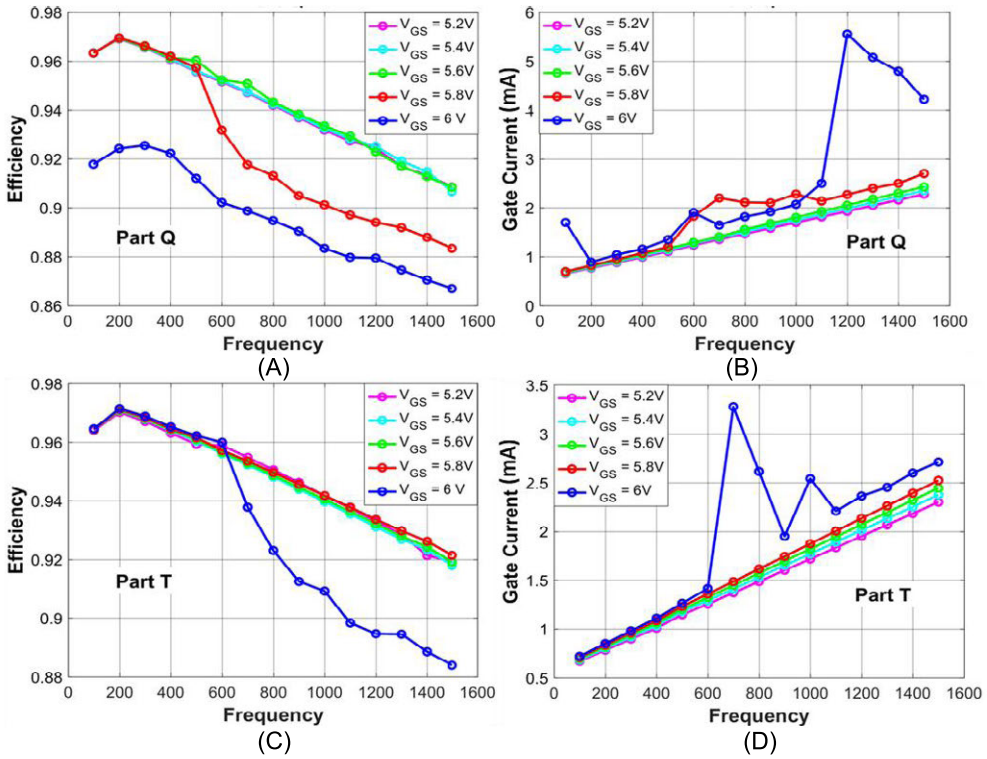

FIGURE 3. A and C) Efficiency vs. frequency for part Q and part T, respectively. B and D) Gate current vs. frequency for part Q and part T, respectively.

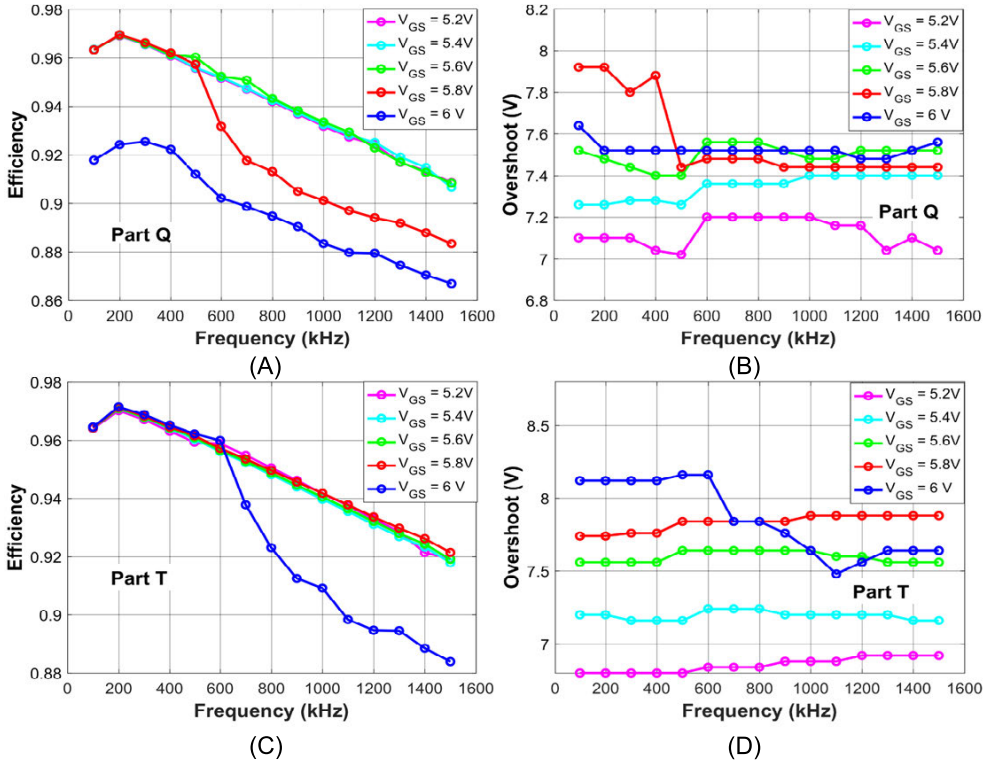

FIGURE 4. A and C) Efficiency vs. frequency for part Q and part T, respectively. B and D) Gate voltage overshoot vs. frequency for part Q and part T, respectively.

As shown in Fig. 3A for "Part Q" at a V_{GS} of 5.8 V and frequency of 500 kHz, the performance of the converter declines due to the degradation of the device. It was observed that the overall efficiency of the device decreases as frequency

increases, with a maximum recorded efficiency of 97% around 200 kHz when operating at V_{GS} values of 5.2V, 5.4V, 5.6V, and 5.8V. For the first three gate voltages, the overall efficiencies decrease by approximately 0.5% per 100 kHz rise with the lowest efficiency of 90.8% recorded at 1.5 MHz. However, for V_{GS} of 5.8V, a sharp drop in efficiency was observed from 95.7% at 500 kHz to 93.1% at 600 kHz. This drop-in efficiency corresponds to the moment when the gate current increases, as observed in Fig. 3B. Similarly, in Fig. 3C and 3D, a drop-in efficiency, and corresponding gate current increase are observed for Part T at 6V. These observations were noted for numerous different devices with degradation consistently occurring between 5.8V and 6.0V, at frequencies between 400 and 600 kHz.

Referring back to Fig. 3A, it is important to note that when the device was operated at a V_{GS} of 6V, the initial efficiency was 91.78% at 150 kHz. This is lower than the efficiency of the converter corresponding to 150 kHz when the device was operated at the other gate voltages. This behavior is believed to be due to the device degradation from the previous test at a V_{GS} of 5.8V. Indeed, the device never recovered back to its initial condition after degradation occurred. This phenomenon can be potentially explained by the creation of traps at the AlGaN/GaN heterostructure, which causes a decrease in mobility of the channel of the device resulting in increased on-resistance [26]–[28].

An important observation made during the test was a decrease in the observed overshoot of the gate voltage when degradation occurred as observed in Figs. 4A and 4B for part Q. When the "Part Q" is operated at V_{GS} values of 5.2V, 5.4V, and 5.6V, the overshoot value is nearly constant over the entire spectrum. Contrarily, when the GaN device degrades at V_{GS} of 5.8V, as seen in Fig. 4A (which is the same as Fig. 3A), the overshoot value experiences a clear change, noted in Fig 4B. This observation is likely attributed to the breakdown of the gate-dielectric over time, leading to poor device performance. Similarly, for Part T, the device degrades at 6 V gate stress voltage, as seen in Fig. 4C (same as Fig. 3C), and the overshoot experiences a rapid decline in its value, shown in Fig. 4D.

One of the reasons that GaN devices are attractive to device engineers is their ability to display high performance at higher frequencies of operation than most competing devices. This leads to an increase in converter power density. Therefore, it is important to study the effects of higher frequency on the degradation of GaN devices. This study shows that there is a direct correlation between frequency increase and device degradation when a device is stressed at higher gate voltages. Furthermore, a correlation between device degradation and converter failure and their influence on gate current and gate voltage overshoot has been demonstrated.

B. GATE TO SOURCE VOLTAGE STRESS TEST AT CONSTANT SWITCHING FREQUENCY

This section verifies the degradation point suggested in Fig. 3 and 4 by the forward gate stress test for the boost converter at constant switching frequency and constant gate voltage conditions. In such conditions, for non-degraded devices, the efficiency, gate current, and V_{GS} overshoot of the converter should be constant. Conversely, these parameters are not expected to be constant for a degraded device.

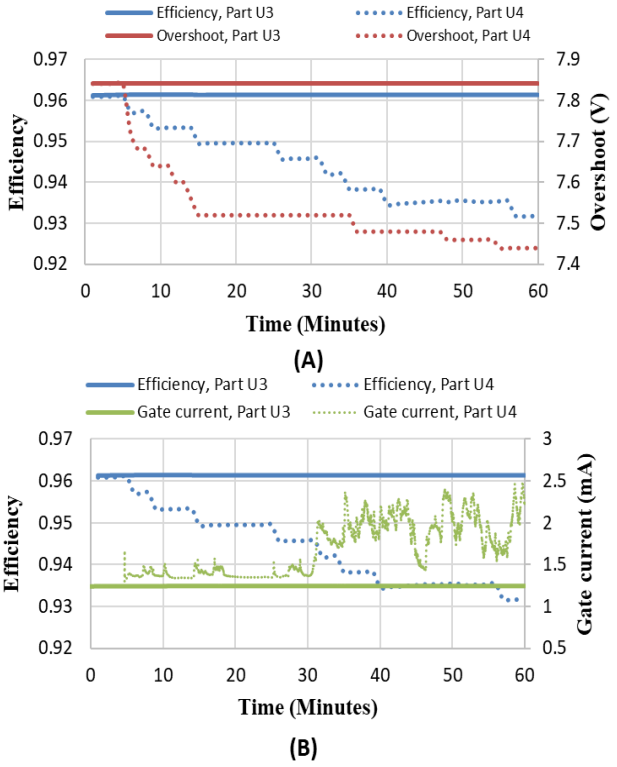

FIGURE 5. A) Efficiency and overshoot vs. time for part U3 and part U4. B) Efficiency and gate current vs. time for part U3 and part U4.

As from Fig. 3 and Fig. 4, it was observed that the device would show signs of degradation at for V_{GS} V_{GS} at 5.8V or higher and frequencies of 500 kHz or above. Therefore, the first V_{GS} stress experiment was performed on the boost converter at a V_{GS} of V_{GS} 5.6V, with a switching frequency of 500 kHz. This test investigated if degradation would occur below 5.8V, particularly under continuous operation for an extended period of time. However, no signs of degradation were present in any of the ten trials performed at a V_{GS} voltage of 5.6V. Under these conditions, the efficiency, V_{GS} overshoot, and gate current were all constant throughout the experiment.

This is shown in Figs. 5 A and B for Part U3. In response to this, Part U3 was operated at a gate voltage of 5.8V in the next experiment, where indications of degradation became visible after 5 minutes of continuous operation, also illustrated in Figs. 5A and B for Part U4. As the gate-voltage has been increased, the adopted naming convention for the test necessitates that Part U3 now be termed Part U4. It should be noted that Part U3 and Part U4 are the same device – the difference in name is attributed to the different operating conditions or test trial. The results in Figs. 5A and B for Part U4 show the degradation mechanism similar to that mentioned in previous experiments. The efficiency and overshoot of Part U4 began

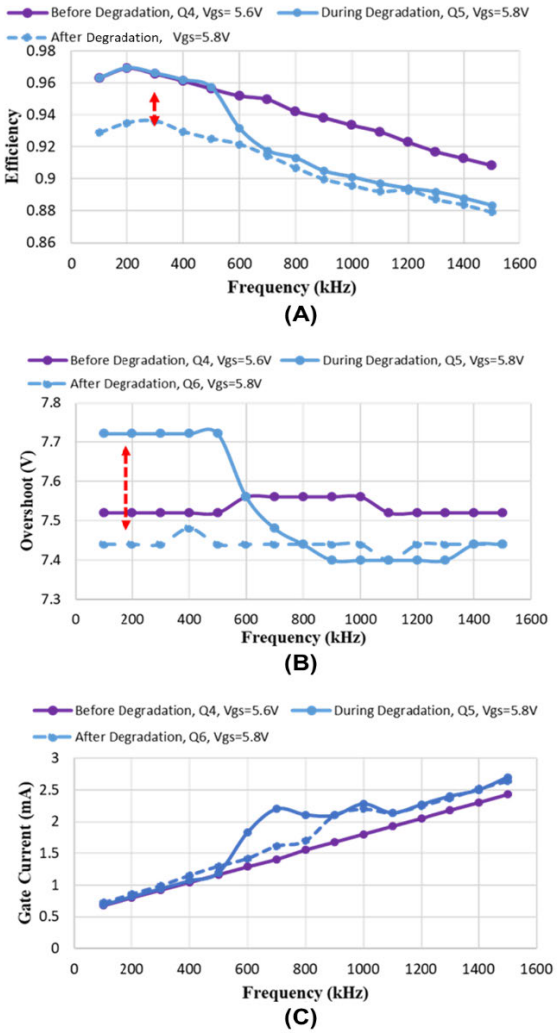

FIGURE 6. A) Efficiency vs. frequency-before, during, and after degradation. B) Overshoot vs. frequency–before, during, and after degradation. C) Gate current vs. frequency-before, during, and after degradation.

to drop after approximately 5 minutes of operation, as noted in Fig. 5A. Also, as observed in Fig. 5B, the gate current of Part U4 increased and fluctuated continuously, contrary to the performance of Part U3. These observations strongly support the findings illustrated in the previous section for Figs. 3 and 4.

C. RECOVERY BEHAVIOR

The objective of this study was to investigate if the degraded device recovers to its normal condition after an extended rest period. Figs. 6 A, B, and C demonstrate efficiency, overshoot, and gate current, respectively. In this case study, the recovery behavior of the degraded device is analyzed on the same boost converter testbed that yielded the results in Fig. 3, and Fig. 4. In Fig. 6 A-C, Part Q4, Part Q5, and Part Q6 represent the device status before, during, and after degradation with V_{GS} voltages of 5.6V, 5.8V, and 5.8V, respectively. Again, Part Q4, Part Q5, and Part Q6 are the same device, just subjected to different operating conditions or trial numbers. The reason that 5.8V was used a second time was to determine if the device would exhibit the same behavior as the previous 5.8V test, or if the behavior would be different after degradation.

As observed in Fig. 6, Part Q5 degraded at a gate drive voltage of 5.8V. The experiment was then repeated after a recovery period of twenty-four hours. At this time, the device still exhibited a reduced efficiency and overshoot, as shown in Fig. 6 A-C, for Part Q6. The profile of both efficiency and V_{GS} overshoot for Part Q6 against the entire frequency spectrum was similar to the pre-degraded device (Part Q4) but with a similar magnitude to the degraded device (Part Q5) at frequencies above 500 kHz.

Although an extended recovery period of twenty-four hours was allowed, the device did not show any signs of recovery, indicating that a further extended recovery period would likely yield similar results. Also, since every device has a unique degradation point based on associated trapping behavior, the recovery period varies accordingly. It is difficult to define the amount of time required by a GaN device to recover completely after the degradation process, and so far, there is no concrete information available in the literature to substantiate the recovery period.

III. DEVICE LEVEL RESULTS TO JUSTIFY RESULTS OBTAINED IN CONVERTER LEVEL EXPERIMENT

More detailed information on the physical origin of degradation presented in the above section can be obtained by step-stress analysis. It is, therefore important to evaluate the devices under positive gate stress to identify the related degradation modes and mechanisms. In this experiment, as shown in Fig. 7A, the device drain and source terminals are shorted to ground, thereby eliminating the possibility of current-collapse-related device degradation. Instead, degradation is attributed to the generation of hot spots in the AlGaN/GaN HEMT due to the high electric field in the AlGaN layer, resulting in the formation of leakage paths [7], [29]. In addition, increased gate current is attributed to an increase in the generation of hot electrons, and a high electric field accelerates the degradation by creating surface traps.

Fig. 7B and 7C report the results of a step-stress experiment carried out on a commercially-available GaN-HEMT subjected to a positive gate bias, using the configuration in Fig. 7A. The gate voltage was increased by 0.2V every 60s, and the corresponding gate current was continuously recorded. During the first two trials of the experiment, the device did not degrade when gate voltages increased step-wise (0 – 8V), and the gate currents are normal throughout trial 1 and 2 periods, as shown in Fig. 7B. However, from Fig. 7C, for voltages above 8V, the device gate current has increased abnormally during trial 3 of the experiment. The sudden rise in gate current at approximately 8V illustrates that device degradation occurred at a voltage greater than the absolute maximum V_{GS} of 6V. After the degradation, the I-V curve of the gate exhibits short circuit behavior. In trial 4, the device gate current is significantly higher compared to

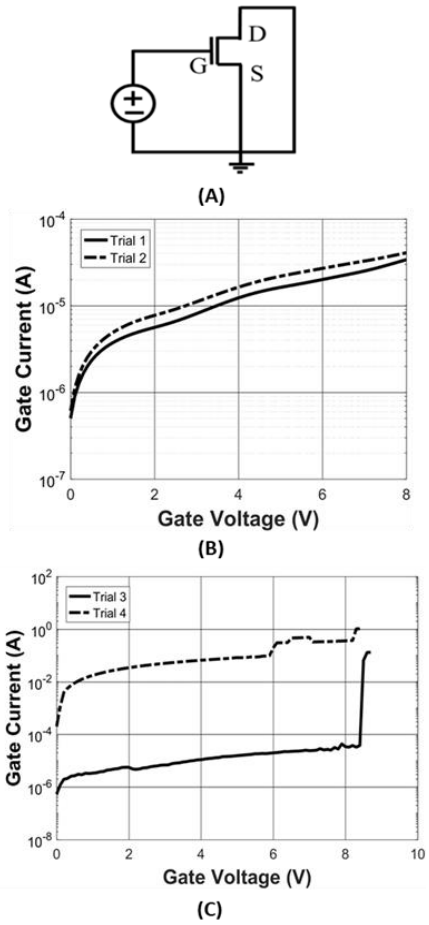

FIGURE 7. A) DC gate-bias circuit for device level testing, B) gate current vs gate voltage for trial 1 and 2 without degradation, and C) gate current vs gate voltage for trial 3 and 4 with degradation.

all other trials, as seen in Fig. 7C. This suggests that the device never recovered to its original state, similar to the phenomenon observed in the converter level experiment.

To further show that this phenomenon is the result of trapping, the step-stress experiment was conducted at 125 degree Celsius. An analysis of conduction behavior was performed against standard diode-like conduction (thermionic or diffusion) as should be expected from this gate structure [30], [31]. That is, the gate current should follow (1) with n values (ideality factors) between $\sim$1 and 3.

$$I_G = I_s \left(\exp\left(\frac{qV_{gs}}{nkT} \right) - 1 \right) \tag{1}$$

where q is the electron charge, k is Boltzmann's constant, T is temperature, and I_S is the reverse-saturation current. This analysis is shown in Fig. 8 in which, at both room and elevated temperature, n values were fit as 52.8 and 166, respectively. It should be noted that the experimental data shown in Fig. 8 was taken without loading the device, and as such, any observed current should be the result of only the gate structure and condition.

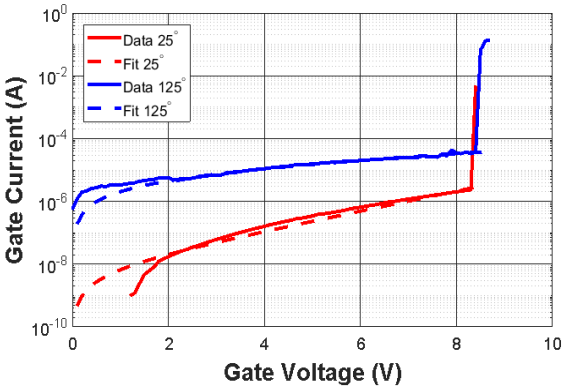

FIGURE 8. Fitted gate current and voltage characteristics of degraded part to expression (1) at 25 °C (red) and 125 °C (blue).

As previously stated, (1) is based on the main current mechanism in the junction being either thermionic or diffusion current with minimal junction recombination effects. Such unreasonable numbers for n indicate that there must be substantial tunneling and/or trapping effects (trap assisted tunneling (TAT), Shockley-Reed-Hall (SRH) emission etc.) contributing to the current, as an exceptionally high n value indicates significant junction imperfections and recombination effects. This is strong evidence that trapping and degradation effects are present at the gate of this device which gives rise to and acts as the mechanism of the device degradation shown previously in Section II.

IV. GATE DEGRADATION MECHANISM

As described in the literature, GaN power devices and specifically GaN HEMTs are vulnerable to high gate-to-source voltage stress and any gate bias stress beyond critical voltage could lead to gate current surge [33]. This can also be seen from the experiments performed in Section II and III. However, voltage overshoot drop due to device degradation has never been noted in literature before.

To describe these effects, the band structures of the devices under test can be examined for the possible tunneling and trap effects described in Section III. Fig. 9 shows typical gate current mechanisms with E_C being the conduction band energy, E_V being the valence band energy, F_n is the quasi-Fermi level for electrons, F_n is the quasi-Fermi level for holes, and E_{FM} is the Fermi level of the metal gate contact. Fig. 9 was formed based on available information from [30], [31]. Here four main current mechanisms are identified, consistent with the temperature dependence in Fig. 8: thermionic emission of electrons and holes, $J_{n,TE}$ and $J_{p,TE}$ respectively, and thermionic field emission of electrons and holes, $J_{n,TFE}$ and $J_{p,TFE}$ respectively. It is possible that significant diffusion current may replace some or all of the indicated thermionic current, but would still be insufficient for describing the results in Fig. 8. The mathematical and theoretical underpinnings of thermionic(-diffusion) current as well as thermionic field emission are given in [34].

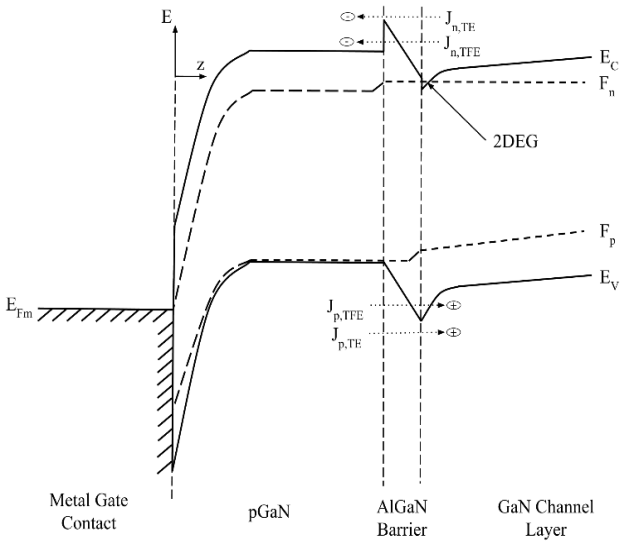

FIGURE 9. Typical gate current mechanisms expected to be present at the gate contact of the device at high positive bias.

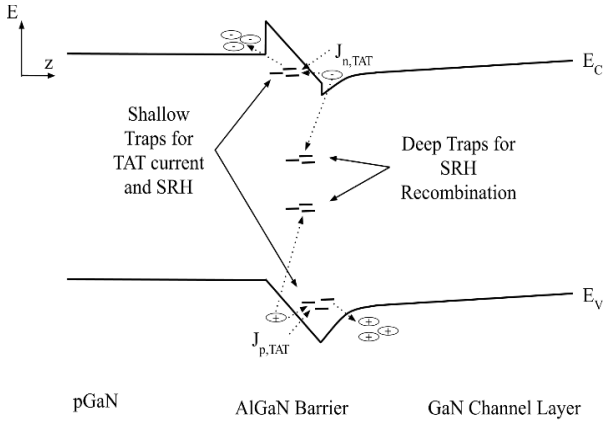

FIGURE 10. Trapping effects present at the gate interface of the device under test.

Fig. 10 then identifies the main theorized trapping effects at play in this device. These are namely trap-assisted tunneling through shallow interface traps, $J_{n,TAT}$ and $J_{p,TAT}$ for electrons and holes respectively, and Shockley-Reed-Hall recombination through shallow and deep traps. These highly non-linear effects then can be used to account for the non-idealities in Fig. 8, as well as providing information useful to explaining the experimental observations in Section II.

As described in [19], hole injection from the gate electrode to p-GaN can become significant under a large positive gate stress. Charge carriers (electrons and holes) then would be accelerated by the high electric field in the pGaN and AlGaN interface This high-energy carriers would mainly be transferred through the thermionic(-diffusion) and thermionic field emission mechanisms. These carriers then could have sufficient energy to generate defects and traps in the AlGaN barrier layer. In addition to this, existing shallow and deep trap levels at the interface can facilitate additional trap-assisted tunneling current that feeds into the previous high-energy carrier degradation. Shockley Reed-Hall recombination as well, will cause traps to become occupied/depleted altering the shape of the pGaN/AlGaN/GaN structure. This barrier alteration through trap occupation/depletion then can cause either positive or negative feedback to the above current and recombination mechanisms.

These mechanisms then are dependent on all bias conditions examined in Section II, but most notably in this work, switching frequency. Since trapping and de-trapping time constants may be on the order of the switching period of the device, the total number of traps generated and therefore the magnitude of the traps' effects on the device's performance and characteristics will be frequency dependent. Additionally, these effects can build up over time to cause both the soft degradation and hard degradation (failure) exhibited by the devices in Section II either through over-currents, threshold voltage instability, or thermal runaway.

In converter-level testing, it was additionally shown that the device exhibited frequency-dependent degradation. This likely emerged due to the interplay of device and package parasitics with surrounding circuit parasitics. This interplay can be directly related to the physical explanations given here based on the devices expected frequency-dependent characteristics. The rapid switching capability of GaN HEMTs emerges largely from their relatively small device footprints and reduced parasitic capacitances. While this enables enhanced edge rates, it also results in the injection of high frequency content at switching edges. This can result in the emergence of momentary dispersive effects causing apparent capacitance and inductance values to fluctuate. If these new apparent values introduce harmonics near the switching frequency, excessive oscillation can occur, causing reduced efficiency and increased gate stress. Soft gate breakdown from these mechanisms can then result in the introduction of new trap states in the gate structure induced by the feedback process described previously. Such states would result in increased device input capacitance, explaining both reduced efficiency and reduced overshoot following a frequency dependent breakdown as well as the observed hard device failures.

V. CONCLUSION

This paper demonstrates experiments conducted on commercially available GaN devices to ascertain their frequency-dependent and bias-dependent reliability and lifetime in converter applications. This testing demonstrated a clear dependence of device degradation on both switching frequency and gate voltage stress. Furthermore, a non-linear fall in overshoot was also observed with a surge in gate current. As a result, efficiency is reduced during and following degradation events. The gate current experiences surges during the degradation period, otherwise it is linear with respect to frequency. The experimental results yielded new findings

related to the behavior of V_{GS} overshoot, gate current and converter efficiency that have never been presented before in literature. Furthermore, frequency dependence of breakdown was observed, demonstrating the need for converter-level testing in addition to DPT switching tests. This effect is attributed to trap-related phenomena in the gate structure of the device, which was corroborated by device testing and analysis.

As mentioned previously, the high-frequency behavior of both GaN and SiC has become a focus of attention and systematic investigation by the broader power electronic community. Preliminary behavioral modeling techniques have been proposed to account for this behavior, as recently reported in [25]. In the herein presented work, the observations noted in Sections II and III, and the physical explanation for these observations provided in Section IV can be used to expand the work shown in [25] with more physically descriptive models. That is, the behaviors observed in the herein presented paper can be used to develop models that are physically descriptive of frequency-dependent phenomena. In this way, this paper can help inform modeling, design, and fabrication techniques for future generation wide bandgap semiconductor devices.

REFERENCES

[1] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs—An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[2] D. S. Lee, Z. Liu, and T. Palacios, "GaN high electron mobility transistors for sub-millimeter wave applications," *Jpn. J. Appl. Phys.*, vol. 53, no. 10, Oct. 2014, Art. no. 100212.

[3] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT with 300-GHz f_{max}," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 195–197, Mar. 2010.

[4] N. Ikeda, S. Kaya, J. Li, Y. Sato, S. Kato, and S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse," in *Proc. 20th Int. Symp. Power Semiconductor Devices IC's*, May 2008, pp. 287–290.

[5] M. Kuzuhara and H. Tokuda, "Low-loss and high-voltage III-nitride transistors for power switching applications," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 405–413, Feb. 2015.

[6] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[7] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Oct. 2015.

[8] O. Hilt, F. Brunner, E. Cho, A. Knauer, E. Bahat-Treidel, and J. Wurfl, "Normally-off high-voltage p-GaN gate GaN HFET with carbon-doped buffer," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices ICs*, San Diego, CA, USA, May 2011, pp. 239–242.

[9] L.-Y. Su, F. Lee, and J. J. Huang, "Enhancement-mode GaN-based high-electron mobility transistors on the Si substrate with a P-type GaN cap layer," *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 460–465, Feb. 2014.

[10] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, May 2011.

[11] W. Choi, O. Seok, H. Ryu, H.-Y. Cha, and K.-S. Seo, "High-voltage and low-leakage-current gate recessed normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD-SiN_x/RF-sputtered-HfO_2," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 175–177, Feb. 2014.

[12] W. Shaobing, G. Jianfeng, W. Weibo, and Z. Junyun, "W-band MMIC PA with ultrahigh power density in 100-nm AlGaN/GaN technology," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 3882–3886, Oct. 2016.

[13] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[14] J. Joh, N. Tipirneni, S. Pendharkar, and S. Krishnan, "Current collapse in GaN heterojunction field effect transistors for high-voltage switching applications," in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2014, pp. 6C.5.1–6C.5.4.

[15] S. R. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee, and S. Pendharkar, "Application reliability validation of GaN power devices," in *IEDM Tech. Dig.*, Dec. 2016, pp. 20.5.1–20.5.4.

[16] M. Meneghini, I. Rossetto, C. De Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, and G. Meneghesso, "Reliability and failure analysis in power GaN-HEMTs: An overview," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 3B-2.1–3B-2.8.

[17] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a Gallium-Nitride transistor," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2681–2688.

[18] T.-S. Yeoh, R. S. Nair, and S.-J. Hu, "MOS transistor gate oxide breakdown stress dependence and their related models," in *Proc. 5th Int. Symp. Phys. Failure Anal. Integr. Circuits*, Nov./Dec. 1995, pp. 127–131, doi: 10.1109/IPFA.1995.487609.

[19] J. He, J. Wei, S. Yang, Y. Wang, K. Zhong, and K. J. Chen, "Frequency- and temperature-dependent gate reliability of Schottky-type p-GaN hate HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3453–3458, Aug. 2019.

[20] *EPC8010—Enhancement Mode Power Transistor EPC8010 Datasheet*, Efficient Power Convers. Corp., Aug. El Segundo, CA, USA, 2019

[21] P. Lagger, M. Reiner, D. Pogany, and C. Ostermaier, "Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in GaN based MIS-HEMTs by stress/recovery experiments," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1022–1030, Apr. 2014.

[22] M. Tapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmik, "Gate reliability investigation in normally-off p-type-GaN cap/AlGaN/GaN HEMTs under forward bias stress," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 385–388, Apr. 2016.

[23] G. Meneghesso, M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, A. Chini, and E. Zanoni, "Reliability issues of gallium nitride high electron mobility transistors," *Int. J. Microw. Wireless Technol.*, vol. 2, no. 1, pp. 39–50, Feb. 2010.

[24] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018.

[25] A. J. Sellers, M. R. Hontz, R. Khanna, A. N. Lemmon, B. T. DeBoi, and A. Shahabi, "An automated model tuning procedure for optimizing prediction of transient and dispersive behavior in wide bandgap semiconductor FETs," *IEEE Trans. Power Electron.*, early access, Apr. 13, 2020, doi: 10.1109/TPEL.2020.2986928.

[26] E. J. Miller, X. Z. Dang, H. H. Wieder, P. M. Asbeck, E. T. Yu, G. J. Sullivan, and J. M. Redwing, "Trap characterization by gate-drain conductance and capacitance dispersion studies of an AlGaN/GaN heterostructure field-effect transistor," *J. Appl. Phys.*, vol. 87, no. 11, pp. 8070–8073, Jun. 2000.

[27] L. E. Byrum, G. Ariyawansa, R. C. Jayasinghe, N. Dietz, A. G. U. Perera, S. G. Matsik, I. T. Ferguson, A. Bezinger, and H. C. Liu, "Capacitance hysteresis in GaN/AlGaN heterostructures," *J. Appl. Phys.*, vol. 105, no. 2, pp. 023709-1–023709-4, Jan. 2009.

[28] P. Fiorenza, G. Greco, F. Iucolano, A. Patti, and F. Roccaforte, "Slow and fast traps in metal-oxide-semiconductor capacitors fabricated on recessed AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 106, no. 14, pp. 142903-1–142903-4, Apr. 2015.

[29] I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, C. De Santi, S. Dalcanale, J. Wuerfl, E. Zanoni, and G. Meneghesso, "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016.

[30] A. Lidow, R. Beach, A. Nakata, J. Cao, and G. Y. Zhao, "Enhancement mode GaN transistor with improved gate characteristics," U.S. Patent 8 969 918, Mar. 3, 2015.

[31] A. Lidow, R. Beach, A. Nakata, J. Cao, and G. Y. Zhao, "Enhancement mode GaN HEMT device," U.S. Patent 8 890 168, Nov. 11, 2014.
[32] M. J. Deen and F. Pascal, "Electrical characterization of semiconductor materials and devices," in *Springer Handbook of Electronic and Photonic Materials*, S. Kasap and P. Capper, Eds. Cham, Switzerland: Springer, 2017, p. 1.
[33] S. Dhakal, "Circuit level reliability considerations in wide bandgap semiconductor devices," Ph.D. dissertation, Univ. Toledo, Toledo, OH, USA, Mar. 2020.
[34] M. R. Hontz, Y. Cao, M. Chen, R. Li, A. Garrido, R. Chu, and R. Khanna, "Modeling and characterization of vertical GaN Schottky diodes with AlGaN cap layers," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2172–2178, May 2017.

ROSHAN L. KINI (Member, IEEE) received the B.E. and M.E. degrees in electronics and telecommunication engineering from Mumbai University, Mumbai, India, in 2010 and 2014, respectively, and the Ph.D. degree in engineering from The University of Toledo, Toledo, OH, USA, in Fall 2019. He is currently working with the Pacific Northwest National Laboratory, WA, USA. His current research interests include the management of DER, PV variability mitigation techniques, transactive control techniques, the applications of wide-bandgap semiconductor devices in power electronics, high-frequency power conversion techniques, and maximum power point tracking techniques.

SHANKAR DHAKAL (Member, IEEE) received the B.S. degree in electrical engineering from Morgan State University, Baltimore, MD, USA, in Spring 2014, and the M.S. degree in electrical engineering from The University of Toledo, Toledo, OH, USA, in Summer 2018. He currently works as a Project Design Engineer of American Electric Power. His research interests include the modeling and simulation of wide bandgap semiconductor devices and the applications of those devices on high-frequency power conversion.

SADAB MAHMUD (Member, IEEE) received the B.S. degree in electrical and electronics engineering from the Ahsanullah University of Science and Technology, Dhaka, Bangladesh, in 2016, and the M.S. degree in electrical engineering from The University of Toledo, Toledo, OH, USA, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include maximum power point tracking techniques for aerospace systems, the applications of wideband gap semiconductors in high-frequency power converters, and transactive control techniques for grid modernization.

ANDREW J. SELLERS (Member, IEEE) received the B.S. degree in electrical engineering from Bucknell University, Lewisburg, PA, USA, in 2016, and the Ph.D. degree in electrical engineering from the University of Toledo, Toledo, OH, USA, in 2020.

His current research interests include the semiconductor device modeling of wide bandgap semiconductors for implementation in next generation power electronics, autonomous and algorithmic model generation and optimization, the multi-level integrated modeling of devices, circuits, and systems, the hardware-in-the-loop (HIL) simulation of shipboard power systems, micro-grids, and terrestrial distribution networks, and renewable energy integration.

MICHAEL R. HONTZ (Member, IEEE) received the B.S. degree *(magna cum laude)* in electrical engineering from Bucknell University, Lewisburg, PA, USA, in 2015, and the Ph.D. degree in electrical engineering from The University of Toledo, Toledo, OH, USA, in 2019. He is currently an Electrical Engineer and a Research Scientist with the U.S. Naval Surface Warfare Center Philadelphia Division (NSWCPD), Philadelphia, PA, USA. His research interests include the modeling, design, and implementation of power semiconductors, naval shipboard power systems and power electronics design, control, stability, and robustness, and the integrated probabilistic modeling of power semiconductor devices, circuits, and systems.

CHEIKH A. TINE (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from The University of Toledo, Toledo, OH, USA, in Spring 2015 and Fall 2017, respectively. He currently works as a Power Electronics Design Engineer of GE Appliances. He is also leading the Electronics and Mixing Valve Water-Heater Electronics Department. His research interests include designing inverters and converters for various appliances.

RAGHAV KHANNA (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Pittsburgh, Pittsburgh, PA, USA, in 2007, 2010, and 2014, respectively.

He has worked for several industries including Lockheed Martin, Philadelphia, PA, USA, PPG Industries, Pittsburgh, PA, USA, and HRL Laboratories, Malibu, CA, USA. At the HRL, he was directly involved in the development of GaN-based battery chargers for electric vehicles. In 2015, he joined the Department of Electrical Engineering and Computer Science, UT, as an Assistant Professor. He is also conducting extensive research on control strategies for the integration of distributed energy resources. He recently received grants from the U.S. Department of Defense, the U.S. Department of Energy, and the NASA Jet Propulsion Laboratory to further develop his research activities. His research interests are in the modeling and simulation of wide bandgap semiconductors for applications in next generation power electronics, including renewable energy, electric vehicles, aerospace and maritime systems, and low-power consumer electronics.

Dr. Khanna is a member of the Power Electronics Society, the Power and Energy Society, and the Electron Devices Society. He serves on the technical program committee for flagship international conferences in power conversion such as the Applied Power Electronics Conference (APEC). At the APEC, in 2013, he won the Best Presentation Award for his presentation on the transient performance of silicon carbide transistors.