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Board-Level Lifetime Prediction for Power Board of Balise Transmission Module in High-Speed Railways

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ABSTRACT In high-speed railways, fixed period and failure-induced maintenance lead to extremely high maintenance. Lacking knowledge about device performance degradation is the main reason for high maintenance costs. Power board is the power source of the high-speed railway devices that provides all the energy required from other circuit boards, which is highly associated with the working state of the entire device. However, there is little research on the prognostics for circuit boards, therefore, this paper developed a novel board-level physics-of-failure model to predict the remaining useful life (RUL) of power board. Firstly, the failure modes of the high-speed railway device Balise transmission module (BTM) were analyzed, and board-level physics-of-failure lifetime prediction model for power board was built, then the RULs under the single failure mechanism and multiple failure mechanisms were predicted, finally, the results were verified and validated by Monte Carlo and Simulink respectively. The results show that the multiple failure mechanisms cause more serious degradation, the prediction accuracy of the proposed model can reach 85.48%.

INDEX TERMS High-speed railway, Balise transmission module, power board, multiple failure mechanisms, remaining useful life.

I. INTRODUCTION

High-speed railways (HSRs) are rapidly expanding new transport mode. With the advantages of safety, velocity, capacity, and sustainability, HSRs are often described as the "transport mode of the future". In January 2019, according to a report from the International Union of Railways (UIC) [1], the world-wide length of HSRs was 99,008km. Among them, the lines in China, Japan, and South Korea were 66,347km, in Europe they were 21,901km, in other countries like USA and Morocco were 10,760km. However, high maintenance cost has become a pain point on the sustainable development of high-speed railway. A survey found that maintenance accounts for 15%-40% of manufacturing costs in many industries [2], in the HSR sector, an annual report from UIC [3]pointed out that the maintenance of 1km of a new high-speed line is €90000 per year, and the maintenance of a high-speed train in Europe is €1 million per year.

The root cause of high maintenance costs is the backwardness of maintenance modes. In high-speed railways, corrective maintenance and fixed maintenance are the main maintenance modes. In order to solve the high maintenance cost problem, condition-based maintenance (CBM) is a promising and effective way to change traditional passive maintenance mode to active [4]. Prognostics is the key enabling technology for CBM, and there are different definitions of prognostics [5]. Among them, a more accurate definition is presented by IEEE standard 1856 [6].

As a critical part of an HSR, the BTM is the key device which consists of circuit boards such as power board, emitting board, communication board, decoding board and receiving board. Among them, the power board supplies power to other circuit boards, meanwhile the failure rate is high. The current research only focuses on the functional problems of BTMs,

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for example, the adaptability of the BTM at 380km/h operational speed has been verified [7], the interferences have been assessed in Eurobalise-train communication systems [8], and the cognitive control method has been used to analyze the up-link signal processing [9]. However, research on the internal characteristics and failure mechanisms of BTMs has limited attention. Thus, there is a research gap to build a degradation model of a BTM to obtain the remaining useful life and apply condition-based maintenance. The existing prognostics algorithms are classified as physics-based methods, data-driven methods, hybrid methods, and statistical reliability methods. Physics-based methods assume that a physical model based on the failure mechanism is known, then, the physical model is combined with the measured data and loading condition to build the degradation process of the objective [10]. A lot of research has been done to develop the physical models for fatigue [11], creep [12], corrosion [13] and wear [14], and the physics-based methods are successfully applied in lithium-ion batteries [15], power semiconductors [16], digital electronics components [17], wherein a deep understanding of the system is necessary. Data-driven methods are used to obtain the information from the collected data by in situ monitoring. Based on data mining and machine learning techniques, the degradation state of the system is estimated [18], Ahmadzadeh and Lundberg [19] applied an artificial neural network to predict the remaining useful life (RUL) of grinding mill liners. Widodo *et al.* [20] introduced support vector machines to battery health monitoring. Ferreiro *et al.* [21] used the Bayesian networks to predict the integrated vehicle degradation state. Michael [22] illustrated a fusion approach to combine the strengths of two methods. Hybrid methods integrate physics-based and data-driven methods that can have powerful prognostics capability [23]–[26]. There are different prognostic solutions depending on the characteristics of the field, and more information about the hybrid methods can be found in a review article [27]. Statistical methods are put forward by Byington *et al.* [28]and are based on historical failure data and the distribution of the failure data. Exponential and Weibull functions have been used to describe the distribution of the failure data. Engel *et al.* [29]applied condition monitoring to update the original failure distribution. Several review papers [30], [31]have been published to introduce this method. The statistical methods are easy to exercise, but the prognostics capacity is lower than other methods.

The benefits and challenges of system prognostics are presented [32], and how to select the applicable prognostic method is one of the challenges. The existing prognostic methods are mostly for one specific component, such as a capacitor, an IGBT, or an inductor. There is little research on the prognostics for circuit boards, so there is an emerging need to focus on the board-level prognostic algorithms which is applicable for lifetime prediction of power board of BTM.

This paper is organized as follows. Section II introduces the structure, principles, the main failure modes, and mechanisms of the BTM. In Section III, the board-level prognostics method based on the physical model is used to determine the degradation state of the power board, which is the basis of the remaining useful life. Section IV applies the simulation to show the board-level prognostics methodology and verify the predictive model. Section V presents conclusions and prospects.

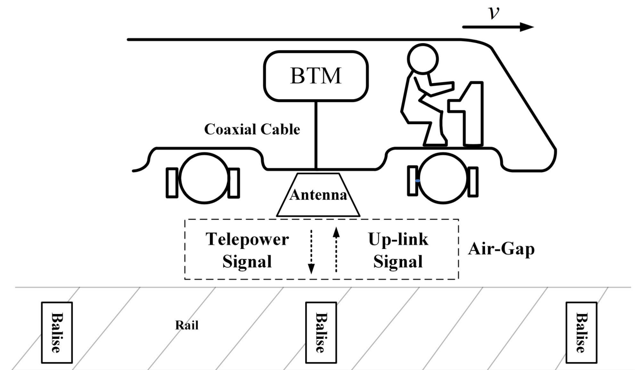


FIGURE 1. Structure of Balise transmission system.

II. BALISE TRANSMISSION MODULE

This section introduces the structure of the Balise transmission system, then presents the functions of different circuit boards of the BTM. The main failure modes of different circuit boards are listed, and the importance of different circuit boards in the BTM is determined.

A. STRUCTURE OF BALISE TRANSMISSION SYSTEM

The Balise transmission system consists of two parts: the on-board part and the ground part [33], as shown in Fig.1.

The ground part includes the Balise, the on-board part includes BTM, antenna, and a cable. The BTM is installed inside the train cabinet, the antenna is installed at the bottom of the train, and the BTM and the antenna are connected by the cable. When the train is running, the BTM generates a 27MHz telepower signal and sends it to the antenna through the cable, then the antenna continuously supplies a 27MHz telepower signal to the Balise by Air-Gap. When the train passes the Balise, the Balise is activated, and the internally stored message in the Balise is transmitted to the antenna by the up-link signal, then the up-link signal is transmitted to the BTM via the cable again, and, finally, the message is sent to the vital computer after demodulating and decoding.

B. STRUCTURE OF BALISE TRANSMISSION MODULE

The BTM is composed of the power board, the emitting board, the receiving board, the decoding board, the communication board, and the recording board. The structure of the BTM from one company is shown in Fig.2.

1) POWER BOARD

The main function of the power board is to convert the DC110V power supply to DC24V power supply. In order to ensure safety in the application, the power board needs

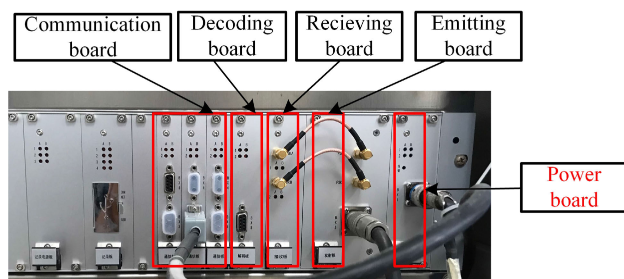


FIGURE 2. Structure of Balise transmission module.

to perform EMC processing and overcurrent protection. The 24V power supply of the whole module is completed by the power board and is mainly used for the emitting board and the receiving board. In order to improve the reliability of the module, the power board is equipped with two independent 110V to 24V DC-DC power modules and two independent 24V to 5V power modules. Two 5V power supplies, respectively, supply power to the two decoding channels of the independent decoding board and cross-power the four communication boards.

2) COMMUNICATION BOARD

A total of four communication boards are set up on the BTM. In order to meet the requirements of security and reliability, the module uses a redundancy system to simultaneously process data, compare the processing results, and output consistent alignment information. The main functions of the communication board include: a. telegram information transmission; b. Balise positioning; c. emitting board power control; d. interface detection; e. decoding information processing, and f. receiving board information processing.

3) DECODING BOARD

The decoding board is configured with a dual-channel structure, and two channels are physically independent. The decoding result is transmitted to the four communication boards through two channels. The main functions of the decoding board include: a. telegram information decoding; b. communication with the communication board; c. module status detection; d. LED display; and e. detection interface.

4) RECEIVING BOARD

The receiving board is designed as a completely independent data processing channel, corresponding to the two signals output by the emitting board. The main function is to receive the signals from the emitting board with a center frequency of 4.23MHz, which is amplified and output to the decoding board.

5) EMITTING BOARD

The emitting board is the main analog function module in the BTM. The main function is to generate a 27MHz telepower signal and transmit it to the antenna. When the train passes the Balise, the Balise is activated. Meanwhile, the emitting board receives the up-link signal from the Balise transmitted from the antenna, and after filtering and preliminary amplification, outputs the information to the receiving board. The emitting board receives the status detection signal sent by the antenna and transmits it to the decoder board.

C. THE MAIN FAILURE MODES OF DIFFERENT BOARDS

The BTM has a self-test function, so the failure modes can be analyzed according to the code, the hardware failure is one of the main failure modes for BTM, the status LED display will be abnormal after the hardware failure occurs, but the fault or hidden danger in the operation cannot be detected by the LED display.

1) POWER BOARD FAILURE

Power board failure will cause the BTM to be powered off. If this happens in the boot self-test stage, communication failure will be reported to the inspector, whereas if this happens during operation, an emergency brake order will be the output.

2) EMITTING AND RECEIVING BOARD FAILURE

There is no fault code for the emitting board, therefore, local failure location can only be performed through the fault code of the receiving board. If this happens in the boot self-test stage, the fault code 4-128-15-03 will be reported, which means the antenna cannot be activated. If this happens during operation, the fault code 6-129-101-1-2 will be reported, which means the BTM cannot receive the up-link signal.

3) DECODING BOARD FAILURE

If the decoding board failure happens in the boot self-test stage, the fault code 4-128-16-03 will be reported. If this happens during operation, the fault code 4-128-16-03 will also be reported.

4) COMMUNICATION BOARD FAILURE

There are four communication boards. If the communication failure happens in the boot self-test stage and operation stage, the fault code 4-128-17-03 will be reported.

D. THE IMPORTANCE OF POWER BOARD

Fig.3 presents the relationship between the different circuit boards. The emitting board activates the Balise, then the Balise transmits the up-link signal to the emitting board, reviving board, and decoding board, and, finally, the uplink signal is processed by the communicating board then sent to the vital computer. The power board provides power to all other circuit boards. So the power board acts as the "heart" of the BTM, meanwhile, from the main failure mode of the BTM, if the failure happens in the power board, the emergency brake will output, which is the most serious failure effects in the system, what's more, "SUBSET 036 FFFIS for Eurobalise" defines the RAMS requirements of the BTM, which requires that its unavailability must be less

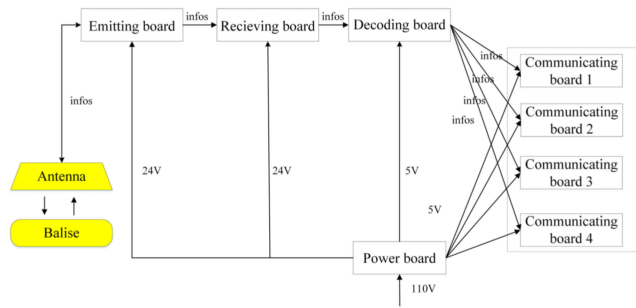


FIGURE 3. Relationship of different circuit boards in BTM.

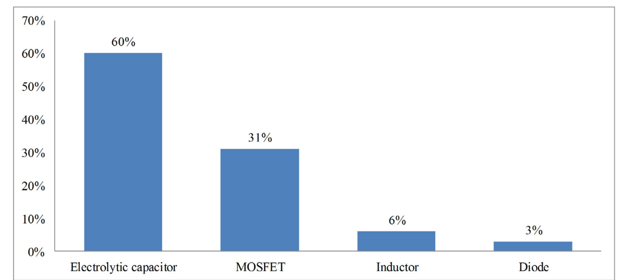


FIGURE 4. Failure rate of critical components in power electronics.

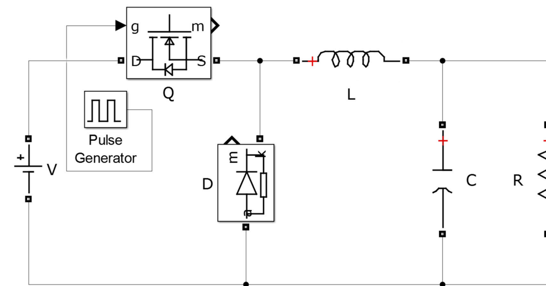


FIGURE 5. The equivalent circuit of power board.

than 1×10^{-6}. After consulting the manufacturer, the power board has a high failure rate in actual application, and the failure rate is close to 1×10^{-6}, which is the limit of BTM unavailability.

In conclusion, the power board is the core part of the BTM, and if it fails, the train will shut down and get delayed, which will lead to the high operation and maintenance cost.

III. PHYSICS-OF-FAILURE MODEL OF POWER BOARD

In this section, the board-level physics-of-failure model of power board was built, firstly, the assumptions need to make in this paper is discussed, then physics-of-failure model of power board is presented, afterward board-level physics-of-failure model was built.

A. ASSUMPTIONS

The assumptions in this paper are as follows: (1) The critical components are the only components that have degraded in the power board, and the degradation is under normal conditions. The BTM had high reliability, so most of the time, the power board components worked at the normal conditions, and a lot of components degrade at the same time, so the degradation of critical components is most representative for true degradation of power board, so this assumption is made. (2) The failure mechanism of the critical component is wear out. There are two categories of the failure mechanisms when the component is working, one is overstress which will lead to the instantaneous and catastrophic failure, the other is wear out, which is a slow degradation process, some intermittent failures will occur before the component completely failed. The main concern in recent research for electronic component is wear out [34], so in this paper, the wear out is the only failure mechanism. (3) The degradation model error and material error are ignorable. Due to the imperfect model and the uncertainty of the component during the manufacturing process, the model error and the component material error will occur. This paper assumes that these errors are negligible, only considering the process errors and measurement errors from degraded data and model parameters, and assumes that they follow a normal distribution.

Based on the assumptions above, first of all, the equivalent model of the power board is built, the potential failure mechanisms and degradation models of critical components are identified; then the board-level physics-of-failure model is derived; finally, the remaining useful life can be predicted.

B. EQUIVALENT MODEL OF THE POWER BOARD

In industry, because the circuit structure is simple and the production cost is low, the DC-DC converters are widely used in mobile phones, MP3s, digital cameras, portable media players [35]. As we mentioned above, the power board is a typical DC-DC converter circuit that converts the DC110V to DC24V power supply. There are numerous components in DC-DC converter circuit but an equivalent model of the power board can be built after identifying the critical components. Pang [36] ranked the failure rate of critical components in power electronics in Fig.4.

We can see that electrolytic capacitors account for the highest failure rate, up to 60% of the total power electronic components. It is followed by metal-oxide-semiconductor field-effect transistors (MOSFET), which account for about 31%. Inductors and diodes follow MOSFETs at 6% and 3%, respectively. So, the electrolytic capacitors, MOSFETs, inductors, and diodes are identified as critical components in the power board. Based on the critical components in the DC-DC converter circuit of a power board, the equivalent circuit of the power board is represented as shown in Fig.5.

V is the DC power supply, Q represents the MOSFET, L is the inductor, D is the diode, C is the capacitor, and R is the resistor. The output voltage of this circuit is lower than the input voltage, and the function is achieved as shown in Fig.6.

There are two states in the circuit: state 1 and state 2. In state 1, the switch Q is driven high, D is driven low, the energy storage inductor is magnetized, the current flowing

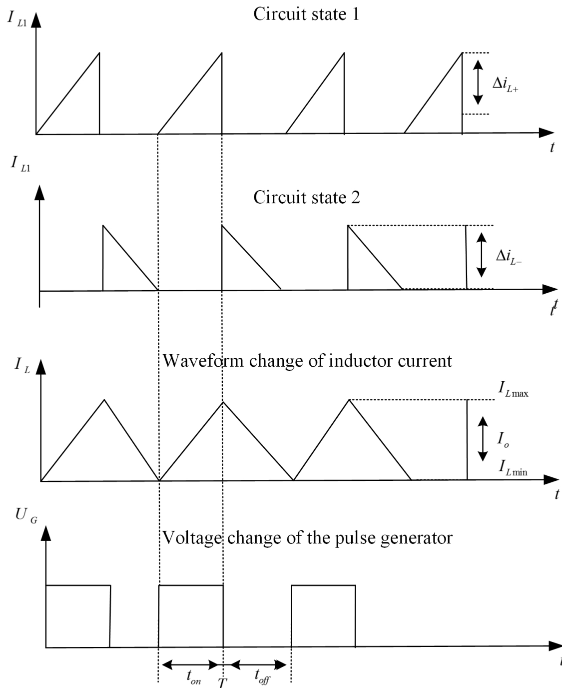


FIGURE 6. The work mode of DC-DC converter circuit.

through the inductor increases, which can charge the capacitor and provide the energy for the resistor.

When the switch Q is driven high, according to the Kirchhoff Voltage Laws (KVL), we get

$$V_{in} - L\frac{\Delta i_{L+}}{\Delta t} - V_o = 0 \tag{1}$$

where V_{in} is the input voltage, V_o is the output voltage, Δi_{L+} is the inductance current increase, L is the inductance, Δt is the conduction time of Q, so we get

$$\frac{\Delta i_{L+}}{\Delta t} = \frac{(V_{in} - V_o)}{L} \tag{2}$$

Let T be the period of the pulse generator and D be the duty cycle, then we are able to derive that

$$\Delta t = T \times D' \tag{3}$$

According to the equation (2) and equation (3), we can get

$$\Delta i_{L+} = \frac{(V_{in} - V_o)TD'}{L} \tag{4}$$

In state 2, the switch Q is driven low, D is driven high, energy storage inductor discharges through the diode, the inductor current decreases, and the output voltage is provided by capacitor discharge.

When the switch Q is driven low, according to the KVL, we get

$$L \times \Delta i_{L-} = V_o \times \Delta t' \tag{5}$$

Δi_{L-} is the inductance current decrease, $\Delta t'$ is the non-conductor time of Q, for the same reason, according to the equation(3), we can derive that

$$\Delta t' = T(1 - D') \tag{6}$$

Combining equations (5) and (6), we get

$$\Delta i_{L-} = \frac{V_o T(1 - D')}{L} \tag{7}$$

According to the equation (4) and equation (7), when the circuit works at steady state, the inductor current waveform changes periodically, which makes inductor current increase, during the on-time, equal to the decrease of the current during the off-time, which means

$$\Delta i_{L+} = \Delta i_{L-} \tag{8}$$

Based on (4), (7) and (8), we can get

$$V_o = V_{in} \times D' \tag{9}$$

Once the switch Q is driven low, the D is driven high, and then we get the relation

$$\Delta i_L = 2I_o \tag{10}$$

$$I_o = \frac{V_o}{R} \tag{11}$$

I_o is the output current, V_o is the output voltage, according to equation (7), equation (10) and equation (11), we get

$$L = \frac{RT(1 - D')}{2} \tag{12}$$

The ripple voltage ΔV_o means the voltage generated by the current flowing through the capacitor, the relationship between the ΔV_o and other parameters is given by:

$$\frac{\Delta V_o}{V_o} = \frac{T^2(1 - D')}{8LC} \tag{13}$$

Then the capacitance is

$$C = \frac{V_o(1 - D')}{8L\Delta V_o}T^2 \tag{14}$$

In this part, the equivalent electrical circuit model of the power board is developed. In the next part, the potential failure mechanisms are identified, and a degradation process of critical components is modeled. Finally, based on degradation model of the critical components, a physics-of-failure model for power board is derived.

C. POTENTIAL FAILURE MECHANISMS AND DEGRADATION MODELS OF CRITICAL COMPONENTS

The critical components of the power board are packaged into a circuit card, so each component is connected to the printed circuit board using tin-lead solder. The details about the critical components are shown in Table 1, the potential failure mechanisms and degradation models of these components will be analyzed assuming the designs mentioned in the Table 1.

1) CAPACITOR

ELNA [37] introduced all the possible failure mechanisms in aluminum electrolytic capacitors and, among them, the main failure mechanism is reduction of electrolyte [38]. There are chemical reactions and electrochemical reactions inside a capacitor which lead to reduction of the electrolyte. As the

TABLE 1. Details about the critical components.

ID	Type	Design
C	Capacitor	Aluminum electrolytic
Q	MOSFET	Power MOSFET
L	Inductor	Wire wound
D	Diode	Schottky diode
R	Resistor	Thin film

working time of the aluminum electrolytic capacitor is prolonged, the electrolyte wears more and more, resulting in the increase of its resistivity. Conversely, the rise in the series resistance of the electrolytic capacitor during the operation of the circuit causes the ripple current in the circuit to rise, and the increase in the ripple current causes the internal temperature of the capacitor to rise, thereby accelerating the evaporation of the electrolyte. As the working hours of aluminum electrolytic capacitors accumulate, the equivalent series resistance increases gradually and the capacitance decreases rapidly. So, the health indicators of aluminum electrolytic capacitor are capacitance and equivalent series resistance. In this paper, capacitance and equivalent series resistance have been used to characterize health of the capacitor in the power board equivalent circuit model. Celaya [39] developed degradation equations to describe the decrease in capacitance and the increase in equivalent series resistance with aging time. The experimental setup was under normal conditions, and they listed all the stress values and environment variables. The collected data under those conditions was used to build the equation:

$$\Delta C(t) = e^{\alpha t} - \beta \tag{15}$$

where α, β are coefficients and t is time.

$$\frac{1}{ESR_t} = \frac{1}{ESR_0}(1 - k \cdot t \cdot \exp(\frac{-E}{T' + 273})) \tag{16}$$

where ESR_t is the ESR value at time t, T' is the temperature, ESR_0 is the initial value at time $t = 0$, k is constant which depends on the design and the construction of the capacitor, E is the Boltzmann's constant.

2) MOSFET

Power MOSFET has obvious advantages such as low power consumption, high input impedance, and high frequency performance. So, it is widely used in various power circuits to function as a switch [40]. The performance degradation of power MOSFET directly affects the temperature, technical performance, and work efficiency of the circuit. As the temperature rises, its cumulative temperature rise will cause the performance of the semiconductor material of the power MOSFET to change. The threshold voltage of the power MOSFET will increase with increasing transconductance, and the on-resistance will increase, finally, the switching function is degraded or even disabled. Vaschenko used the simulation software to determine sensitive parameters in the degradation process [41].The simulation results showed that the gate surface defects cause the threshold voltage of the power MOSFET to change. Therefore, the threshold voltage can be used as a sensitive parameter in the degradation process. Celaya experimentally determined that the channel resistance of a power MOSFET is also a sensitive parameter in the failure process when multiple failure mechanisms work together [42]. Celaya [43] performed an accelerated aging experiment to develop the empirical degradation model of the channel resistance ΔR_w, which is shown as follows:

$$\Delta R_w = a \times (\exp(b \times t) - 1) \tag{17}$$

where a, b are coefficients and t is time.

3) INDUCTOR

Inductors mainly play the role of energy storage and filtering in power electronic circuits. In the power electronic circuit, the inductor works under high frequency conditions. As the inductor operates for longer duration, the temperature of the inductor coil gradually increases and the inductance value decreases, which affects the working performance of the circuit [44]. Therefore, the inductance value is used as the health indicator of the inductor, and deterioration of the inductor is reflected by monitoring the change of the inductance value. The degradation of the inductor can be described by an Arrhenius relationship [45] as equation (18):

$$\ln(\frac{\Delta L}{L_0}) = \ln(At) - \frac{E}{HT'} \tag{18}$$

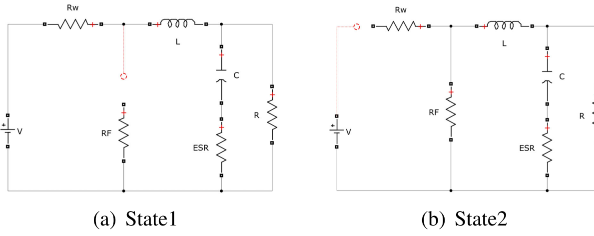
where the change in inductance at time t is ΔL, the initial inductance is L_0, A is a material specific constant, E is the activation energy, H is the gas constant, T' is the absolute temperature.

4) DIODE

Diodes are the most basic electronic components in power electronic circuits and play a vital role in circuit design. There are many types of diodes, among them, Schottky diode has the advantages of small forward voltage drop, fast switch speed, short reverse recovery time, and low power consumption [46]. Based on those advantages, the Schottky diode is widely used in switching power supplies, inverters, etc. During the operation of Schottky diodes, current, voltage, and temperature stresses degrade its performance. At the same time, the power consumption results in the rise of internal temperature, which is one of the reasons for degradation of performance. With the rise in temperature, the reverse leakage current increases, the unidirectional conductivity of the diode becomes worse, and the equivalent resistance R_F increases, which means degradation of the diode is obvious. So, the equivalent resistance R_F is identified to be the health indicator of the diode. The degradation model can be described by an Arrhenius relationship as equation (19):

$$\ln(\frac{\Delta R_F}{R_{F_0}}) = \ln(At) - \frac{E}{HT'} \tag{19}$$

The explanation of this equation refers to the equation (18).



(a) State1 (b) State2

FIGURE 7. Two states in non-ideal DC-DC converter circuit.

5) SOLDER JOINTS

The above-mentioned critical components are soldered to the printed circuit board, so the failure mechanism of the solder joint should also be considered. The failure modes and mechanisms of solder joint are described by Schubert [47]. Crack initiation and propagation is one mechanism that can cause a series of degradation such as grain/phase coarsening; grain boundary sliding; matrix creeps; and micro-void formation and linking. Degradation in solder in most cases is caused by thermal fatigue that leads to cracking of the joints [48]. The degradation process can be described by equation (20) which is the sum of elastic and plastic strain contributions:

$$\begin{cases} W = W_p + W_c = W_{po}(N_{fp})^c + W_{co}(N_{fc})^d \\ \dfrac{1}{N_f} = \dfrac{1}{N_{fp}} + \dfrac{1}{N_{fc}} \end{cases} \tag{20}$$

where W is the total energy, W_p is plastic strain energy density, W_c is creep strain energy density, W_{po}, W_{co}, c and d are material specific constants, N_{fp} is number of failure cycles caused by plastic effects, N_{fc} is number of failure cycles caused by creep effects, and N_f is the final cumulative number of cycles until the solder joint failed.

In this part, the failure mechanisms and degradation models of the critical components are analyzed, and the failure mechanism of the solder joint is also considered. The physics-of-failure model of power board can then be derived.

D. THE PHYSICS-OF-FAILURE MODEL OF THE POWER BOARD

As previously assumed, the critical components are the only components that can degrade in the power board. Among the failure mechanisms of the critical components, only the wear out failure mechanism is considered. The health indicators of the DC-DC circuit board are output voltage and ripple voltage. The DC-DC converter circuit in Fig.5 is the ideal equivalent circuit model, which did not consider the parasitic parameter of the component. Based on the analysis of the potential failure mechanisms and degradation models of each component, the non-ideal DC-DC converter is showed in Fig.7.

As aforementioned work mode for ideal DC-DC converter circuit, there are two states in the circuit. In state1, the switch Q is driven high, D is driven low. The non-ideal circuit for state 1 is shown in Fig.8(a). In state 2, the switch Q is driven low, D is driven high. The non-ideal circuit for state 2 is shown in Fig.8(b) The equation (4) and (7) is rewritten under the non-ideal condition:

$$\Delta i'_{L+} = \frac{(V_{in} - V_o - I_L \cdot R_w)TD'}{L} \tag{21}$$

$$\Delta i'_{L-} = \frac{(V_o - I_L \cdot R_F) \times T(1-D')}{L} \tag{22}$$

The I_L is the inductor current, R_w is channel resistance of power MOSFET, R_F is the equivalent resistance of diode, and other variables have been defined previously. According to equation (21) and (22), we can get:

$$V'_o = D' \cdot V_{in} - I_L \times [D' \cdot R_w + (1-D') \times R_F] \tag{23}$$

In the ideal circuit, the ripple voltage is derived in equation (13) In the non-ideal circuit, the voltage produced by ESR should be considered. The ripple voltage in the non-ideal condition is:

$$\Delta V_o{}' = \frac{V'_o(1-D')}{fL}(ESR + \frac{1}{8fC}) \tag{24}$$

where f is the switching frequency, which equals $1/T$.

Based on above mentioned and the consideration of process errors and measurement errors, the physics-of-failure model of power board can be derived as follows:

$$\begin{cases} V_o{}' = D' \cdot V_{in} - I_L \times [D' \cdot R_w + (1-D') \times R_F] + \varepsilon_v \\ \Delta V_o{}' = \dfrac{V_o(1-D')}{fL}(ESR + \dfrac{1}{8fC}) + \varepsilon_d v \\ \Delta C(t) = e^{\alpha t} - \beta + \omega_c \\ \dfrac{1}{ESR_t} = \dfrac{1}{ESR_0}(1 - k \cdot t \cdot \exp(\dfrac{-E}{T+273})) + \omega_e \\ \Delta R_w = a \times (\exp(b \times t) - 1) + \omega_w \\ \ln(\dfrac{\Delta L}{L_0}) = \ln(At) - \dfrac{E}{LT'} + \omega_l \\ \ln(\dfrac{\Delta R_F}{R_{F_0}}) = \ln(At) - \dfrac{E}{HT'} + \omega_f \\ W = W_p + W_c = W_{po}(N_{fp})^c + W_{co}(N_{fc})^d \\ \dfrac{1}{N_f} = \dfrac{1}{N_{fp}} + \dfrac{1}{N_{fc}} \end{cases} \tag{25}$$

The failure criteria in this model include the health indicators V'_o and $\Delta V_o{}'$. The failure tolerance of the capacitor, MOSFET, inductor, diode and solder joints given in the following part. RUL of power board should be the minimum value t among all critical components.

IV. CASE STUDY

For the power board, there are two DC-DC circuits:110V-24V and 24V-5V. In this paper, we will consider 24V-5V as an example to show the implementation of board-level physics-of-failure model for RUL prediction. So, in the DC-DC converter circuit, $V_{in} = 24V$, $V_o = 5V$, and $R = 10\Omega$, we set the ripple voltage to 5% of output voltage, the switching frequency as 10kHz, in the ideal circuit. Then, according to equation (9)

$$D = 20.83\%$$

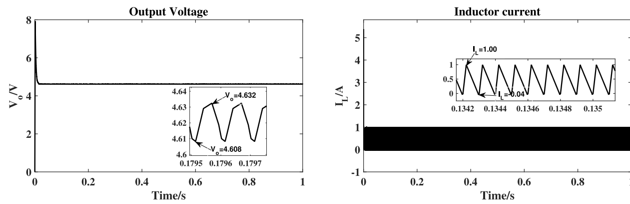


FIGURE 8. Result of the ideal DC-DC converter circuit.

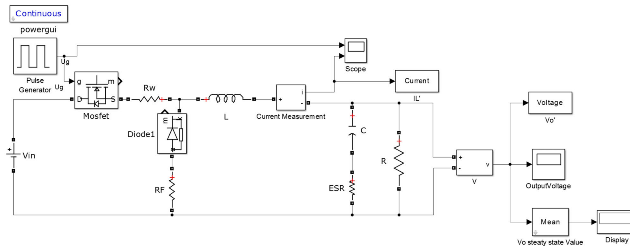


FIGURE 9. Simulink model of the non-ideal DC-DC converter circuit.

The ripple voltage is 5% of output voltage, so

$$\frac{\Delta V_o}{V_o} = 5\%$$

According to equation (12)

$$L = \frac{RT(1-D)}{2} = 3.96 \times 10^{-4} H$$

According to equation (14)

$$C = \frac{V_o(1-D)}{8L\Delta V_o} T_s{}^2 = 5 \times 10^{-4} F$$

With the values obtained, we built the Simulink model of the ideal DC-DC converter circuit based on Fig.6. The simulation algorithm selects ode23tb, the maximum step size is 0.1s, and the duty ratio $D = 20.83\%$, so we can get the output voltage as shown in Fig.8.

We can see that the ripple voltage of the circuit is $\Delta V_o = 0.024V$, $\Delta I_L = 1.04V$, and the mean value of the output voltage is displayed, which is $V_o = 4.62V$, the theoretical value are $V_o = 5V$, $\Delta V_o = 0.025V$, $\Delta I_L = 1A$.

However, in the non-ideal DC-DC converter circuit, the components degrade with the aging time and thermal stress. Based on the analysis of the critical components in Section III, we built the Simulink model of non-ideal DC-DC converter circuit, shown in Fig.9, which considers the degradation of capacitor, MOSFET, inductor, and diode. ESR, R_w, R_F, C and L degraded with the aging time too, the output voltage, ripple voltage and inductor current are measured.

Because the physics-of-failure models of key components in power board were developed under the thermal stress, so when train operates in different temperature bands will cause different RUL prediction results. So case study from specific railways line such as Wuhan-Guangzhou line was studied.

The Wuhan-Guangzhou line connects Wuhan and Guangzhou, the train departed from Wuhan, and then reached

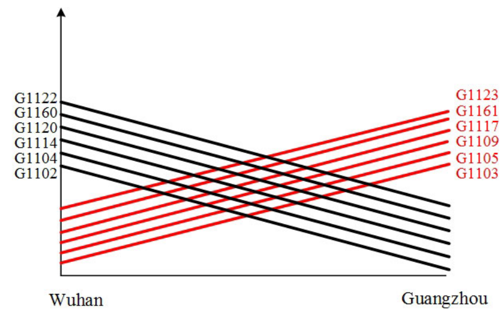


FIGURE 10. Illustration of Wuhan-Guangzhou line operation plan.

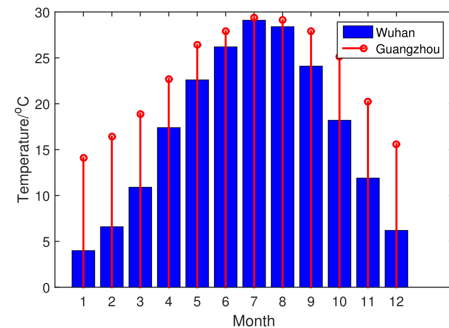


FIGURE 11. Average monthly temperature in Wuhan and Guangzhou.

Guangzhou, time interval is about 4 hours. After staying at the terminal station Guangzhou for some time, according to the dispatch plan, the train number was changed and train departed from the Guangzhou to Wuhan. Fig.10 shows the actual operation plan of the Wuhan-Guangzhou line, the G1103, G1105, G1109, G1117, G1161, and G1123 trains departed from Wuhan and arrived at Guangzhou after 4 hours. After staying in Guangzhou for some time, the train numbers were changed to G1102, G1104, G1114, G1120, G1160, G1122, then train departed from Guangzhou and arrived at Wuhan.

Fig.11 shows the monthly average temperature of two cities, Wuhan and Guangzhou. The statistical data is from 1981-2010 of China Meteorological Administration.

As shown in the Fig.11, the annual temperature changes in Wuhan and Guangzhou are roughly the same. The annual minimum temperature in Wuhan is 4°C in January, the maximum temperature is 29.1°C in July, and the average annual temperature is about 20°C; The annual minimum temperature in Guangzhou is 14.1°C in January, the maximum temperature is 29.4°C in July, and the average annual temperature is about 25°C. Since the two cities of Wuhan and Guangzhou are in southern China, the temperature is high for most of the time. Therefore, the temperature of the operating environment described by the subsequent performance degradation law is set at 25°C based on the annual average temperature of Guangzhou. Under the thermal stress, the remaining effective life of power board predicted.

The simulations were run under the single failure mechanism and multiple failure mechanisms. The health indicators V_o' and $\Delta V_o{}'$ were used to show how the degradation affected

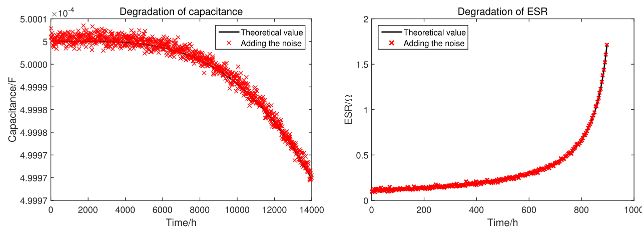


FIGURE 12. Degradation of the capacitor.

the output. Based on the failure criteria of different components, RULs from different components can be calculated.

A. SINGLE FAILURE MECHANISM CONDITION

1) CAPACITOR

In this part, the single failure mechanism condition was simulated. The assumption that other components did not degrade with aging time was made. We take the capacitor UVY1E472M, MOSFET FQA140N10, inductor LQH6PP, and diode MUR1620CT as examples to identify the failure criteria. As we discussed in Section III, capacitance and equivalent series resistance were chosen to be the health indicators of the capacitor. The model and empirical parameter values are given in the Ref [40]. In order to consider the model parameter error, a Gaussian distribution noise is added in the laboratory value. The initial values for the circuit were set as follows: $V_{in} = 24V$, $V_o = 5V$, $R = 10\Omega$, $R_F = 0.03\Omega$, $R_w = 0.01\Omega$, $ESR_0 = 0.11\Omega$, $C = 5 \times 10^{-4}F$, $L = 3.96 \times 10^{-4}H$, and the failure threshold used for $\Delta V_o{}'$ is 5% of output voltage, V_o' was not less or more than 20% of output voltage. According to the equation (21) and (22), we can get $D' = 20.88\%$ in the non-ideal circuit, Assuming the operating temperature of power board to be 25°C [49], then we can get the degradation of C and ESR as shown in Fig.12.

As shown in Fig.12, in the first 900 hours, the capacitance did not show any significant change, but the ESR increases, which will affect the health indicators of the circuit. According to the datasheet of the UVY1E472M capacitor, the failure tolerance is $\pm 20\%$, we can see that within the 14000 hours, the change in capacitance was less than 20%, so the RUL is decided by other failure criteria. In order to consider the degradation data error, a Gaussian distribution noise is added to the C and ESR value, then 2000 samples were drawn using Monte Carlo simulation to express the uncertainty in prediction. So V_o' and $\Delta V_o{}'$ are calculated in theory, then Monte Carlo and Simulink were used to verify and validate the RUL theoretical result respectively, which is shown in Fig.13.

In Fig.13, we can see that the ESR did not have a huge influence on V_o' and I_L, but the $\Delta V_o{}'$ is significantly affected by ESR. As ESR increases, $\Delta V_o{}'$ also increases too. So, ESR can be identified as an important parameter to reflect the health state of the DC-DC converter circuit. We can see that, based on our model, at the 492 hours, the $\Delta V_o{}'$ increases beyond the threshold which is 5% of output voltage 0.25V.

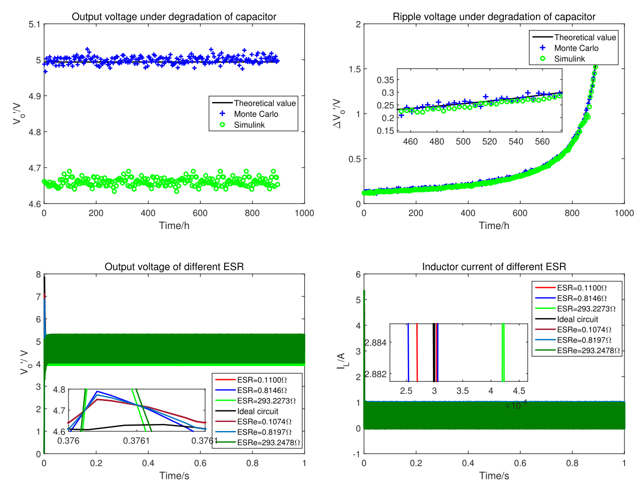


FIGURE 13. DC-DC circuit under degradation of capacitor.

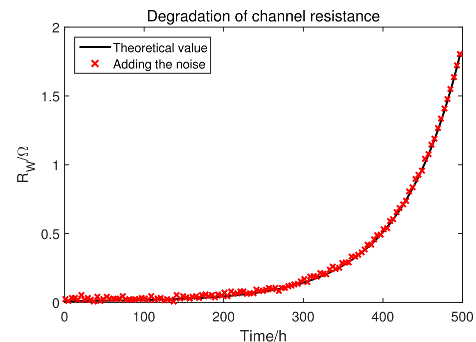


FIGURE 14. Degradation of MOSFET.

So, the RUL is 492 hours, and in the Simulink, the RUL is 516 hours under the capacitor degradation.

2) MOSFET

In Ref [44], the parameters in equation (17) are given. The channel resistance of MOSFET increases with the aging time, and the failure threshold is such that the ΔR_w cannot yield 0.045Ω. Assuming that the MOSFET is the only component degraded in the circuit, so the initial value of the circuit is same as that for the capacitance we discussed above, but according to the equation (21) and (22), the D' is affected by the channel resistance, so,the D' with different channel resistance was calculated to get the degradation of channel resistance in Fig.14.

As shown in Fig.14, the channel resistance changed significantly in the first 300 hours, which will affect the health indicators of the circuit. The ΔR_w cannot yield the threshold, so the RUL from the degradation of MOSFET is 444 hours. Then the V_o' and I_L are compared under the different channel resistance, which are shown in Fig.15.

In Fig.15, we can see that the R_w had a huge influence on V_o', I_L and $\Delta V_o{}'$, with an increase in R_w, the V_o' and $\Delta V_o{}'$ decreased, and when R_w reached a maximum value, current decreased beyond the failure threshold. So,R_w was

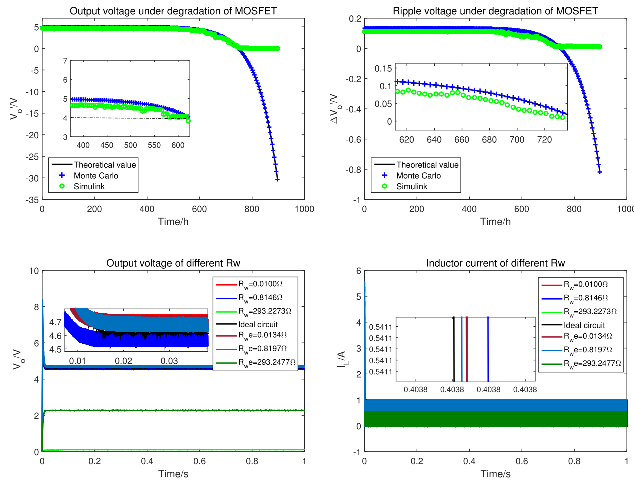


FIGURE 15. DC-DC circuit under the degradation of MOSFET.

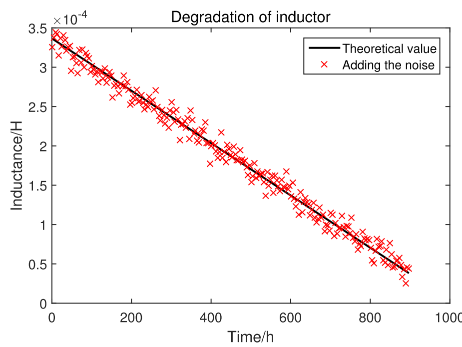


FIGURE 16. Degradation of the inductor.

identified as an important parameter to reflect the health state of the DC-DC converter circuit. In our model, the RUL of the circuit, using the V_o' failure criterion was 628 hours. In the Simulink, it was at 624 hours that the V_o' reached the limitation. Because $\Delta V_o'$ is decreasing, so there is no threshold for this. So based on the three criteria such as degradation of MOSFET, V_o' and $\Delta V_o'$, the RUL of the circuit under the MOSFET degradation is 444 hours.

3) INDUCTOR

The Arrhenius relationship is used to describe the degradation of the inductor and inductance is identified to be the health indicator for the inductor. In the equation (18), the empirical values of the parameters are given [50]. The temperature at which BTM operates is 25°C. The degradation of inductance is obtained as shown in Fig.16.

As shown in Fig.16, the degradation is modeled by the Arrhenius relationship as a linear change and the decrease of inductance will affect the health indicators of the circuit. The failure criterion is found in datasheet which is ±30%, using which the RUL from degradation of inductor comes out to be 660 hours. Then V_o' and $\Delta V_o'$ are calculated, which are shown in Fig.17.

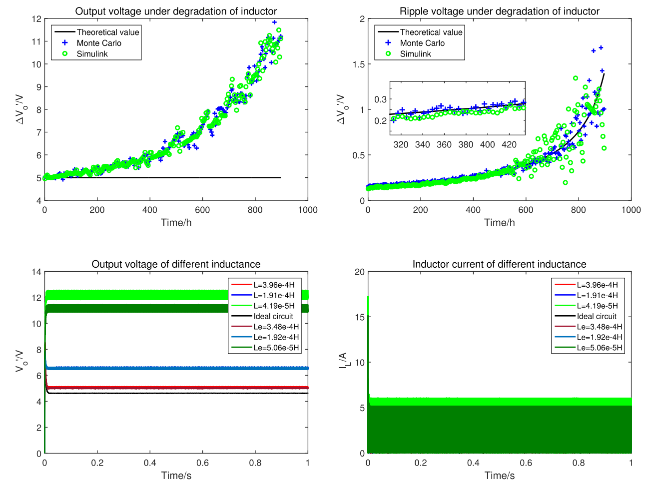


FIGURE 17. DC-DC circuit under degradation of inductor.

In Fig.17, we can see that the L had a huge influence on I_L and $\Delta V_o'$. With a decrease L, the I_L and $\Delta V_o'$ increased, however, the change in V_o' was higher for $\Delta V_o'$ in theory, V_o' is decided by the $\Delta V_o'$ and D', when the D' is identified that means $L \times C$ is fixed. Since it was assumed that the inductor is the only degraded component, so C did not change and that is why the decrease of inductance did not influence V_o' too much in theory. So L was identified as an important parameter to reflect the health state of the DC-DC converter circuit. The RUL from the threshold of V_o' was 346 hours in Simulink, and more than 1000 hours in theory. Since there is a big difference between theory and Simulink, so this is an invalid RUL. From the threshold of $\Delta V_o'$, RUL was 420 hours and 388 hours in Simulink and theory, respectively. Based on all the degradation above, the RUL obtained for the circuit was 388 hours considering inductor degradation.

4) DIODE

Similar to the inductor, the degradation of diode is described by the Arrhenius relationship. The health indicator of the diode is the equivalent resistance R_F. The initial value of $R_F = 0.03\Omega$, and the working temperature is assumed to be 25°C. The degradation of diode with aging time is shown in Fig.18.

As shown in Fig.18, the degradation process for the diode is also linear with respect to time. The equivalent resistance increases with time, which will affect the performance of the circuit. The failure criterion of the diode in the datasheet is that the current cannot decrease by more than 20%, so, the equivalent resistance cannot be more than 5 times of initial value. The RUL from the degradation of the diode is more than 1000 hours. Then the V_o' and $\Delta V_o'$ are calculated in theory and Simulink model, which are shown in Fig.19.

In Fig.19, we can see that the R_F did not have a huge influence on V_o', I_L and $\Delta V_o'$, with the increasing of the R_F, the V_o', I_L and $\Delta V_o'$ did not change in theory too, which means

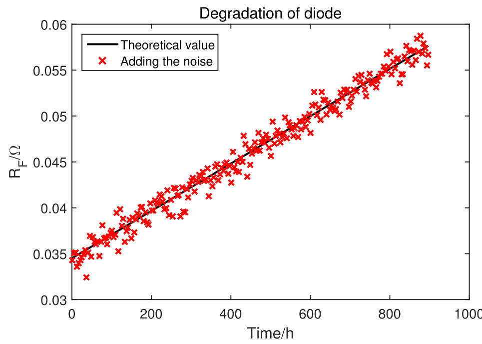


FIGURE 18. **Degradation of diode.**

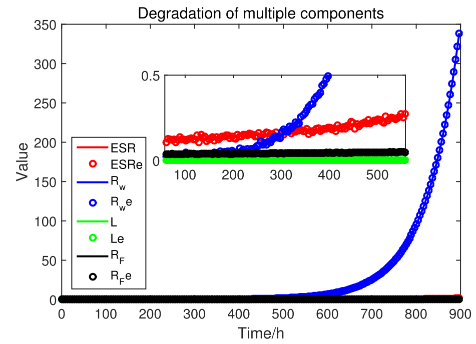


FIGURE 20. **Degradation of multiple components.**

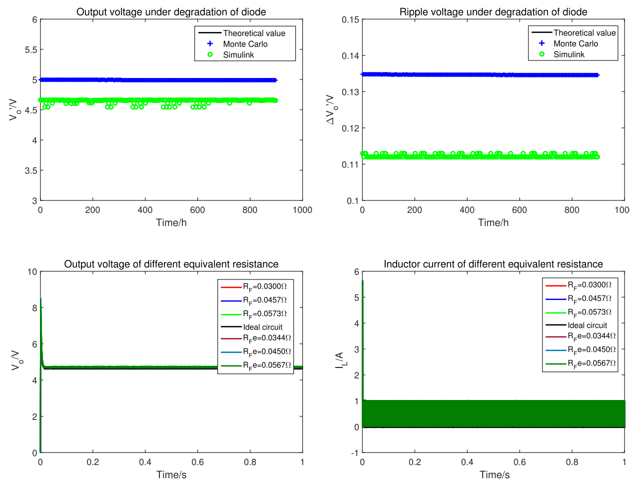


FIGURE 19. **DC-DC circuit under degradation of diode.**

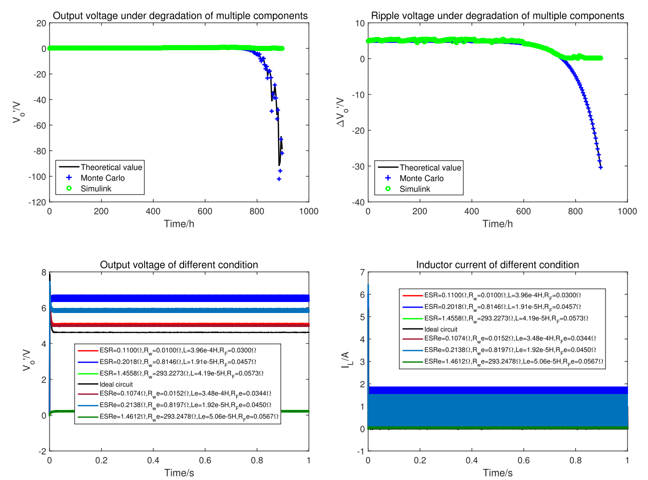


FIGURE 21. **DC-DC circuit under degradation of multiple components.**

R_F can be a reference health indicator for DC-DC converter circuit.

5) SOLDER JOINTS DEGRADATION

The degradation model for the solder joints based on inelastic strain energy density can effectively consider the plasticity and creep strain energy density of multi-chip component solder joints under temperature cyclic loading, and the prediction efficiency and precision are high. Therefore, the model is used to predict the fatigue life of solder joints. The degradation model that is based on inelastic strain energy density is shown in equations (20). For the material parameters in the model, refer to the results of Zhang [51]. The parameters are: $c = -0.8, d = -1.4, W_{po} = 198mJ/mm^3, W_{co} = 1.23 \times 10^4 mJ/mm^3, N_{fc} = 3130, N_{fp} = 27833$, so the $N_f = 2814$. Since it was assumed that one cycle is one hour for BTM, so, the RUL of the DC-DC circuit under the solder joints degradation comes out to be 2814h.

B. MULTIPLE FAILURE MECHANISM CONDITION

The simulations under the single component were discussed in last part. In this part, the outputs of the DC-DC circuit under multiple failure mechanisms are studied. Based on the above-mentioned analysis of degradation of different components, degradation of multiple critical components is shown within the 1000 hours in Fig.20.

In Fig 20, *ESR*, R_w and R_F increased whereas L decreased. Based on these degradations, the V_o' and $\Delta V_o'$ are calculated in theory and Simulink model, and V_o' and I_L are compared under degradation of multiple components, which are shown in Fig.21.

In Fig.21, we can see that the degradation of multiple components has a significant influence on V_o', I_L and $\Delta V_o'$. V_o', I_L and $\Delta V_o'$ increased as the *ESR*, R_F and R_w increased, and the L decreased. There is a mutation point around 800 hours and that is because of the degradation of all components and the DC-DC converter cannot perform function anymore. The result from Simulink validated the result. V_o' yielded the threshold at 628 hours in theory and it was at 624 hours according to the Simulink. $\Delta V_o'$ yielded the threshold at 212 hours, in theory, and at 248 hours in Simulink. In order to consider the uncertainty, Monte Carlo simulation results are shown in Fig.22.

So, according to proposed model, the RUL of the circuit under multiple components degradations is close to the distribution $N(216, 12)$.

Table 2 shows the results above, the relative accuracy (RA), which is the accuracy between the Simulink and theory

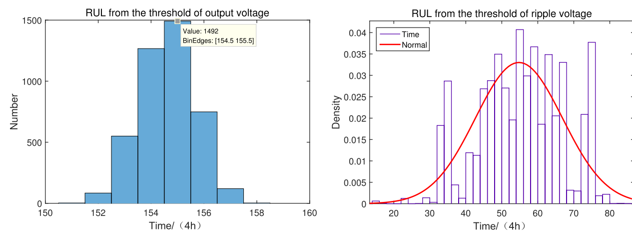


FIGURE 22. RUL results of Monte Carlo simulation.

TABLE 2. RA under different components.

Component	Simulink(h)	Theory(h)	RA(%)
Capacitor	516	492	95.34
MOSFET	624	628	99.35
Inductor	420	388	92.38
Diode	1000	1000	-
Solder joints	-	2814	-
Multiple	248	212	85.48

RUL, can be used to show the precision of the model. RA is expressed as:

$$RA = 1 - \frac{\left|RUL_{Simulink} - RUL_{theory}\right|}{RUL_{Simulink}} \tag{26}$$

RA values are shown in Table 2 for different components. The proposed physics-of-failure model for power board showed good prediction performance. It can also be observed that diode was not a primary indicator for the DC-DC converter circuit. Then the RA under different components are shown in Table 2 too, we can see the physics-of-failure model of power board has a good prediction performance, and the diode is not a primary indicator for the DC-DC converter circuit.

V. CONCLUSION

RUL prediction is a promising way to reduce high maintenance costs for high-speed railways, which can provide the knowledge of the degradation process of equipment in systems. However, for electronic device in high-speed railways, it is difficult to obtain sufficient life-cycle data due to the lack of sensors, and there are multiple components degrade simultaneously, which make it difficult to predict the RUL of high-speed railways. This paper developed a board-level physics-of-failure model for power board in Balise transmission module, the main work includes:

1) Most research discussed fault detection and identification of Balise transmission module, less attention was paid to the failure mode, failure mechanism, so the failure modes of different circuit boards of Balise transmission module were analyzed.

2) We established a board-level physics-of-failure model for power board of Balise transmission module in high-speed railways under the condition that it is hard to build a degradation model for the equipment in complex system and there is insufficient life-cycle data to train the data-driven model.

3) Based on the board-level physics-of-failure model, in this work, the RULs under a single failure mechanism and multiple failure mechanisms are predicted, the results are verified using simulations.

4) Monte Carlo and Simulink simulations were run to verify and validate the proposed model. The results show that the multiple failure mechanisms cause more serious degradation, RA is used to show the prediction performance, the prediction accuracy of the proposed model can reach 85.48%.

In the future, the actual life-cycle data of power board should be collected and validate the proposed model, more accurate method to predict the RUL of the power board should be explored, and more environment parameters such as temperature and humidity should be considered in the model.

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