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Analysis and Design of Bridgeless Continuous Input Current Charge Pump PFC Converter

RUNZE LV AND DONGLEI DAI
School of Electrical Engineering, Southwest Jiaotong University, Chengdu 611756, China
Corresponding author: Runze Lv (rzlv@foxmail.com)

ABSTRACT This paper presents a design methodology for bridgeless continuous input current charge pump power factor correction (PFC) converter. A new fundamental harmonic approximation-based equivalent circuit model is obtained through the Fourier analysis by examining the fundamental behavior of the charge pump. The operating characteristics of the converter are analyzed and the procedure for designing is discussed. To verify the effectiveness of the design method, three simulation circuits under different conditions of operation are designed by the proposed procedure. The characterization of a 55-60 W experimental prototype converter design using the proposed design procedure is presented. Besides, the measured bus voltage is compared with that calculated by the model, and the result shows the good accuracy of the proposed model. The performance of the simulation circuits and the prototype meet the design requirement, showing the validity of the design method.

INDEX TERMS Bridgeless, power factor correction (PFC), charge pump (CP), parameter design.

I. INTRODUCTION

In power theory, harmonics are any variance from the sinusoidal voltage or current waveform typically generated by an ideal voltage source with linear loads [1], and power factor (PF) is the measurement of the economy in power transmission [2].

With the increasing popularity of power electronic devices, the harmonic pollution caused by power electronic devices has been becoming more and more nonnegligible, which would interfere with other devices. To deal with this problem, relevant harmonics standards such as IEC 61000-3-2 [3] limit the harmonic content. Thus, power factor correction technique is widely applied in numerous applications, such as LED driver [4]–[7], induction heating [8] and power supplies [9], [10].

Compared with the two-stage PFC converter, the single-stage PFC converter has the advantages of low cost, small size and high efficiency. Usually, AC-DC single-stage PFC converters are made by integrating the front-end PFC converter and the back-end DC-DC converter. In [11], [12], the Boost-Flyback Single-Stage PFC converter is proposed by integrating the cascading discontinuous-conduction-mode (DCM) Boost converter and Flyback converter. Although the Boost-Flyback Single-Stage PFC converter has the advantages of low cost and small size, several problems exist, including high di/dt, high current stress and insufficient PF.

In [14], the charge pump PFC converters (CPPFC) are very attractive since they use a charge pump composed of a diode operates with zero-current switching (ZCS) and a capacitor in parallel, instead of an inductor to achieve power factor correction, as the capacitor is usually cheaper and smaller than inductor.

Compared with other CPPFC, the current source charge pump PFC converter (CS-CPPFC) has the main advantage of low cost and high efficiency [13]. However, the main disadvantages of the CS-CPPFC converter are high current stresses, narrow range of high PF and that the requirement of a large EMI filter [15]. To solve these problems, the continuous input current charge pump converter (CIC-CPPFC) is developed [14]. Further, based on CIC-CPPFC, [15] integrated the diode in the input side with the diode of the switch to form the bridgeless continuous input current-type charge pump PFC converter (BCIC-CPPFC). Compared with the CIC-CPPFC converter, it has two fewer diodes, which further saves costs and improves efficiency. Compared with the CS-CPPFC converter, the BCIC-CPPFC converter has several advantages: 1) a wider range of unity PF, 2) higher efficiency, 3) smaller current stress, 4) a smaller input filter [15]. Although a practical circuit was proposed, the

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behavior of the converter is still unknown and an effective parameter design method is also needed.

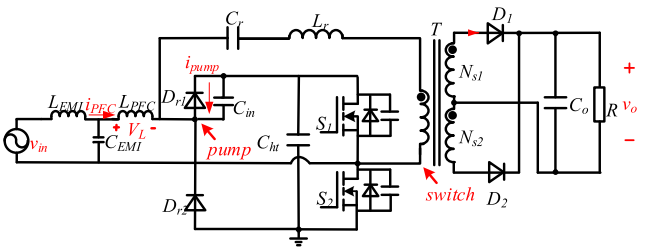


FIGURE 1. Modified BCIC-CPPFC converter.

In this paper, the BCIC-CPPFC converter in [11] is modified into the isolated BCIC-CPPFC converter with DC output which is shown in Fig.1. Taking the application for constant voltage as an example, a fundamental harmonic approximation (FHA)-based equivalent circuit model is established for predicting the behavior of the converter, which is similar to the procedures in [16]. The characteristics of the converter under high PF operating mode with nearly unity PF are analyzed. A design methodology is described and used to design a 55-60 W prototype. Both the model and design method are verified by the experimental measurements taken from the prototype converter.

The paper is organized as followed: Section II gives details of the operating principle of the converter and the FHA equivalent circuit model. Section III describes the details of the FHA equivalent circuit model in different states under the high PF operating mode. Section IV describes the iterative procedure to solve the model. Section V investigates the characteristics of the converter in different states under high PF operating mode. Section VI presents the design procedures. Section VII displays the simulation and experimental results, some are compared with the theoretical prediction. Section VIII concludes the results of the work.

II. PRINCIPLES OF BCIC-CPPFC CONVERTER

The modified BCIC-CPPFC converter is shown in Fig. 1. It consists of four main parts: 1) an input filter formed by a filter inductor L_{EMI} and a capacitance C_{EMI}, 2) a high-frequency dc-ac converter formed by two complementary switched MOSFETs S_1 and S_2, a bus capacitance C_{ht} and the resonant tank formed by resonant inductors and capacitors L_{PFC}, L_r, C_r and C_{in}, 3) a full wave rectifier formed by diodes D_1, D_2, filter capacitor C_o and a transformer T, converting the ac waveform produced in (2) into the isolated dc output, and 4) the charge pump PFC unit formed by D_{r1}, D_{r2}, and C_{in} for PFC function.

A. INPUT CURRENT

The operating waveforms of the converter at one line cycle is shown in Fig.2. It shows that there are two cases of the input current, one operates as a sinusoidal wave, which is the high PF operating mode, as shown in Fig. 2(a), the other operates with a dead-zone, as Fig. 2(b) shows. In detail, there are four

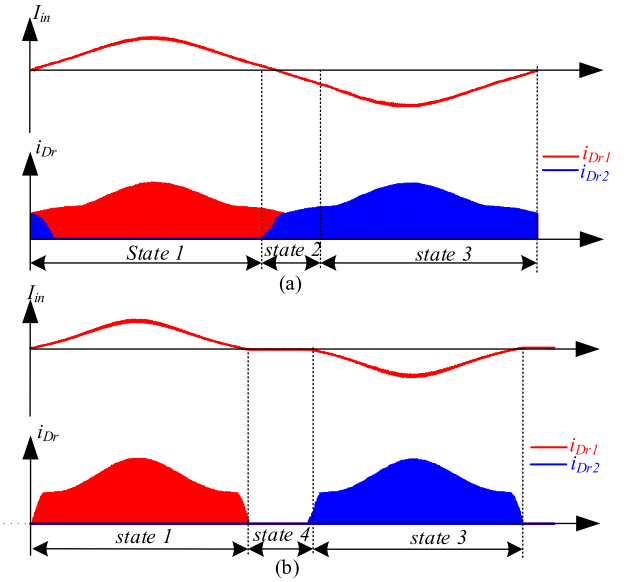


FIGURE 2. Input current under different modes. (a) no dead-zone case (b) dead-zone case.

different states of the converter, while the state 4 operates in the dead-zone. Under unit power factor, the input current i_{in} is given in

$$\begin{cases} i_{in} = I_m \sin(w_0 t) \\ I_m = \dfrac{\sqrt{2} P_o}{\eta V_{in}} \end{cases} \tag{1}$$

where, η is the efficiency of the main circuit, V_{in} is the rms value of input voltage, P_o is the load power.

B. EQUIVALENT CIRCUIT MODEL

While C_{in} is being charged, the converter operates as a fourth-order circuit, which is hard to analyze by time-domain analysis. To solve this problem, assuming that the behavior of the converter is dominated by the fundamental component, a method based on FHA is employed to analyze the converter. The difficulty to analyze the converter by FHA is that the charge pump has the characteristic of diode or capacitor during one switching cycle. So it's necessary to obtain its equivalent model on the fundamental frequency.

To solve this problem, a method similar to [16] is developed. Then, the equivalent circuit model under FHA is established.

First of all, as the voltage across and the current through the transformer T is in phase, the primary side of T can be equivalent as a resister R_{ac}. According to FHA [17], there is

$$R_{ac} = \frac{8N^2}{\pi^2} R \tag{2}$$

where N is the turn ratio of the transformer.

The equivalent circuit of the resonant tank is shown in Fig. 3, which is composed of the charge pump and a linear part in series. In detail, the impedance of the linear part is

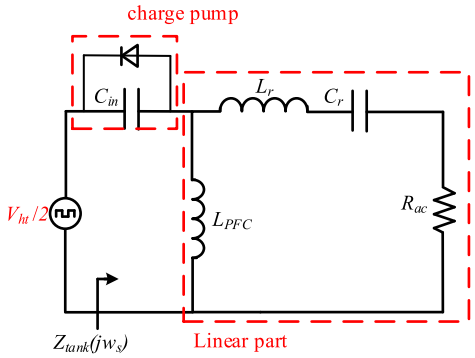


FIGURE 3. Resonant tank equivalent circuit.

given in

$$Z_{linear} = \left(R_{ac} + j(w_s L_r - \frac{1}{w_s C_r})\right) // jw_s L_{PFC}. \quad (3)$$

To obtain the equivalent impedance of the charge pump, first, to simplify analysis, only the fundamental component of the resonant current i_{pump} is considered, which is given in

$$i_{pump} = I_{pump} \sin(w_s t) \quad (4)$$

Then, the expression of the voltage across C_{in}, V_{cin}, is found by examining the fundamental behavior of the charge pump. Further, the fundamental component of V_{cin} is found via Fourier analysis, which is

$$V_{cinf} = V_{cs} \sin(w_s t) + V_{cc} \cos(w_s t) \quad (5)$$

where,

$$\begin{cases} V_{cs} = \dfrac{1}{\pi} \displaystyle\int_0^{2\pi} V_{cin} \sin(w_s t) \cdot d(w_s t) \\ V_{cc} = \dfrac{1}{\pi} \displaystyle\int_0^{2\pi} V_{cin} \cos(w_s t) \cdot d(w_s t) \end{cases} \quad (6)$$

Finally, the fundamental impedance of the charge pump can be obtained by

$$Z_{pump} = Z_{pr} + jZ_{pi} \quad (7)$$

where, $Z_{pr}(Z_{pr} = V_{cs}/I_{pump})$, $Z_{pi}(Z_{pi} = V_{cc}/I_{pump})$ are defined as the real and imaginary parts of the fundamental impedance of the charge pump, respectively. As the time-domain expression of the charge pump is different in each state, the fundamental impedance of the charge pump under different states are given detailly in section III. Moreover, the fundamental impedance of the resonant tank can be obtained as

$$Z_{tank} = Z_{pump} + Z_{linear} \quad (8)$$

Besides, the fundamental component of resonant current I_{pump} can be found in

$$I_{pump} = \frac{2V_{ht}}{\pi Z_{tank}} \quad (9)$$

Furthermore, according to the equivalent circuit model, the bus voltage V_{ht} should satisfy

$$V_{ht} = \left| \frac{2Z_{tank}\left(R_{ac} + j(w_s L_r - \frac{1}{w_s C_r})\right)}{Z_{linear} \cdot R_{ac}} \right| \cdot NV_o \quad (10)$$

C. VOLTAGE STRESS

The mode transitions and equivalent circuits in different states under high PF operating mode are illustrated in Fig.4. When the converter works in state 1, as Fig.4(a) shows, the voltage V_L across the L_{PFC} is found in

$$V_L = \begin{cases} v_{in} + V_{cin}, & [t_0, t_2] \\ v_{in}, & [t_2, t_3] \\ v_{in} - V_{ht}, & [t_3, t_5] \\ v_{in} - V_{ht} + V_{cin}, & [t_5, t_6] \end{cases} \quad (11)$$

According to the volt-second balance, the bus voltage V_{ht} is given in

$$\begin{cases} V_{ht} = 2(v_{in} + V_{cin,ave}) \\ V_{cin,ave} = \dfrac{1}{T_s} \displaystyle\int_0^{T_s} V_{cin} \cdot dt \end{cases} \quad (12)$$

where, $V_{cin,ave}$ is the average value of the voltage across the charge pump during one switching cycle. Besides, V_{ht} is the peak voltage stress of S_1, S_2, D_{r1} and D_{r2}.

D. HIGH PF CONDITION

When the converter works in state 2, the resonant current needs to charge the C_{in} from 0 V to V_{ht}. Thus, in order to make the converter work in high PF operating mode, where the converter always operates in state 2 when $v_{in} = 0$ as shown in Fig. 4(c), C_{in} should satisfy

$$\begin{cases} C_{in} \le C_{PFC} \\ C_{PFC} = \dfrac{2I_{pump}}{V_{ht} \cdot w_s} \end{cases} \quad (13)$$

E. CURRENT STRESS OF SWITCHES

The current flows the switches has two parts, one is the input current, the other is the resonant current. Thus, the current flows through the switches is given in

$$i_s = \begin{cases} i_{pump} - i_{in}, & S_1 \\ i_{pump} + i_{in}, & S_2 \end{cases} \quad (14)$$

III. THE FUNDAMENTAL IMPEDANCE OF CHARGE PUMP IN DIFFERENT STATES

To obtain the specific equivalent circuit model in the high PF operating mode, the expression of Z_{pump} in state 1, state 2, and state 3 are derived as follows.

A. STATE 1

In state 1, the charge pump is operated by D_{r1} and C_{in}, the waveforms of V_{cin} and i_{pump} in state 1 is shown in Fig.5 (a).

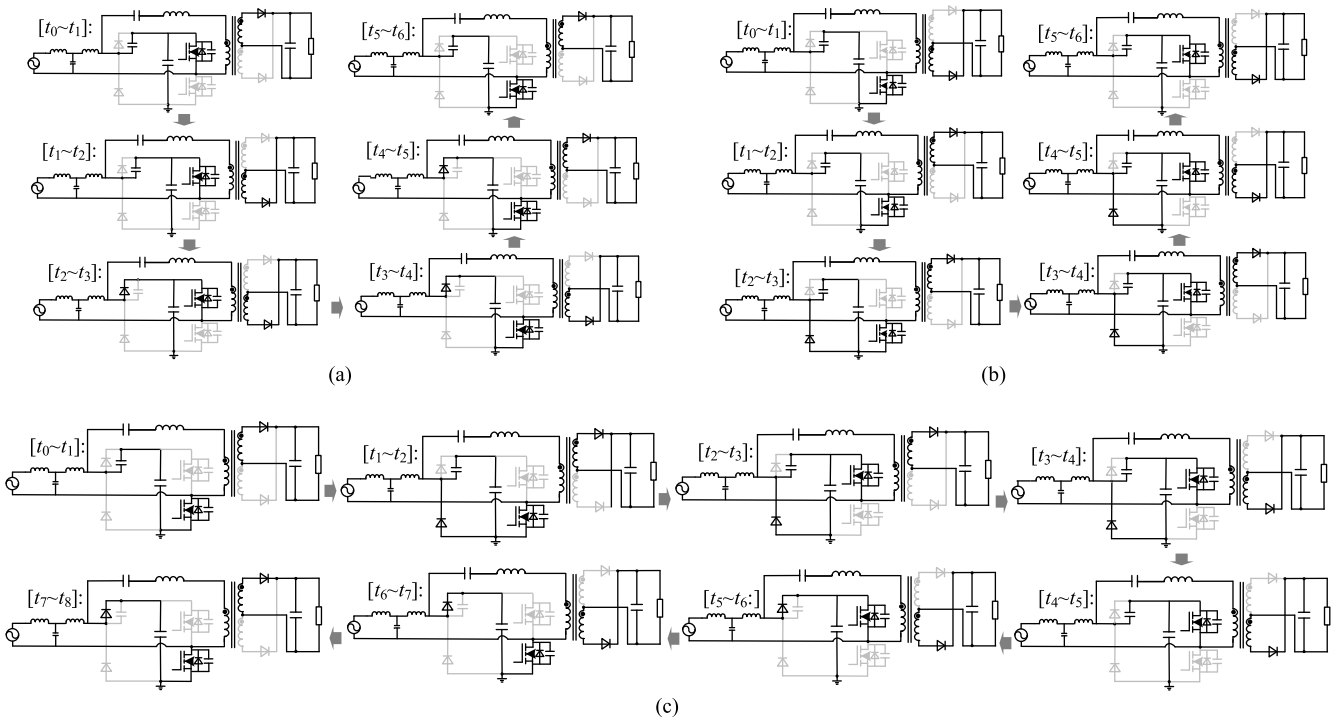


FIGURE 4. Switch-mode transitions and equivalent circuits under high PF operating mode: (a) state 1 and (b) state 2 and (c) state 3.

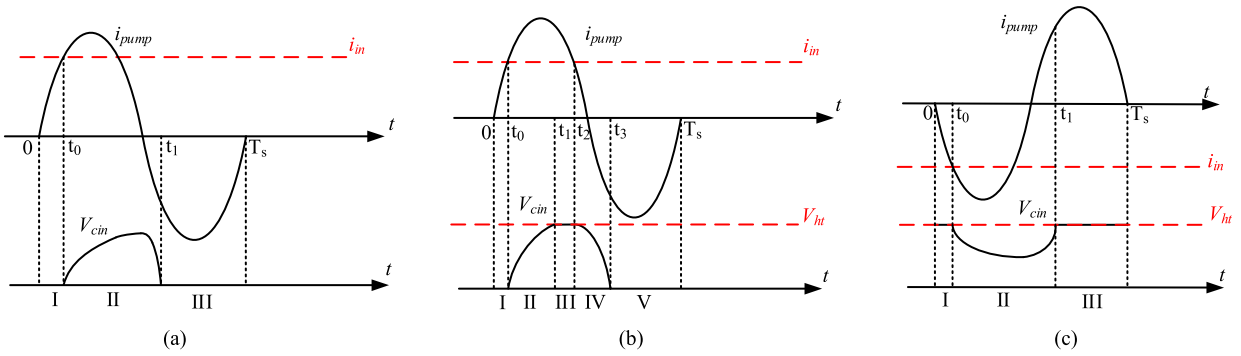


FIGURE 5. Charge pump voltage waveforms. (a) state 1 (b) state 2 (c) state.

Under state 1, the peak value of V_{cin} in a switching cycle, $V_{cin,max}$, can be deduced by

$$V_{cin,max} = \frac{1}{C_{in}}\left[\frac{I_{pump}}{w_s}2\cos w_s t_0 - i_{in}\left(\frac{\pi}{w_s} - 2t_0\right)\right] \quad (15)$$

So, the condition of the converter works in state 1 is that

$$V_{cin,max} < V_{ht} \quad (16)$$

For the interval II($t_0 \le t < t_1$), when the resonant current is greater than the input current at t_0, C_{in} starts to be charged and D_{r1} is turned off. Later, when V_{cin} is equal to 0 V at t_1, D_{r1} turns on again. Thus, the voltage across C_{in} in interval II, V_{II}(t), is given in

$$V_{II}(t) = \frac{I_{pump}}{C_{in}w_s}(\cos w_s t_0 - \cos w_s t) - \frac{i_{in}(t - t_0)}{C_{in}} \quad (17)$$

Thus, the piecewise descriptions of V_{cin} is given in

$$V_{cin}(t) = \begin{cases} V_{II}(t), & t \in [t_0, t_1] \\ 0, & others \end{cases} \quad (18)$$

In detail, t_0 and t_1 are found in

$$t_0 = \frac{1}{w_s} arcsin\left(\frac{i_{in}}{I_{pump}}\right) \quad (19)$$

$$V_{II}(t_1) = 0 \quad (20)$$

Based on the above, substituting (18) into (6) and (7), Z_{pr} and Z_{pi} in state 1 are given in (21) and (22) respectively.

$$Z_{pr} = \left(\frac{\cos(w_s t_0)}{C_{in}\pi w_s} + \frac{i_{in}t_0}{C_{in}\pi I_{pump}}\right)(\cos(w_s t_0) - \cos(w_s t_1)) + \frac{1}{4w_s C_{in}\pi}(\cos(2w_s t)_1 - \cos(2w_s t_0))$$

$$- \frac{i_{in}t_1 \cos(w_s t_1)}{I_{pump}C_{in}\pi} - \frac{i_{in}}{I_{pump}C_{in}\pi} \times \left(\frac{\sin(w_s t_1)}{w_s} + t_0 \cos(w_s t_0) + \frac{\sin(w_s t_0)}{w_s} \right) \quad (21)$$

$$Z_{pi} = \left(\frac{\cos(w_s t_0)}{C_{in}\pi w_s} + \frac{i_{in}t_0}{C_{in}\pi I_{pump}} \right) (\sin(w_s t_1) - \sin(w_s t_0)) + \frac{i_{in}}{I_{pump}C_{in}\pi} \left(\frac{\cos(w_s t_1)}{w_s} - \frac{\cos(w_s t_0)}{w_s} \right) - \frac{i_{in}t_1 \sin(w_s t_1)}{I_{pump}C_{in}\pi} - \frac{\sin(2w_s t_1) - \sin(2w_s t_0)}{4w_s C_{in}\pi} - \frac{t_1 - t_0}{2C_{in}\pi} + \frac{i_{in}t_0 \sin(w_s t_0)}{I_{pump}C_{in}\pi} \quad (22)$$

B. STATE 2

In state 2, the charge pump is operated by D_{r1}, D_{r2}, and C_{in}, the waveforms of V_{cin} and i_{pump} across C_{in} in state 2 is shown in Fig.5 (b).

Under state 2, V_{cin} operates within the two clamping voltage levels, 0 and V_{ht}. As the condition in state 2 is that, $V_{cin,max}$ in state 1 needs to be greater than V_{ht}, which is

$$V_{cin,max} > V_{ht} \quad (23)$$

In interval I($0 \le t < t_0$) and interval V ($t_3 \le t < T_s$), D_{r1} is turning on, V_{cin} is clamped to 0 V, there is

$$V_{cin}(t) = 0 \quad (24)$$

In interval II($t_0 \le t < t_1$), the expression of V_{cin} is the same as V_{II}(t). For the interval III($t_1 \le t < t_2$), D_{r2} turns on, clamping the V_{cin} to V_{ht}, which is

$$V_{cin}(t) = V_{ht} \quad (25)$$

In interval III($t_2 \le t < t_3$), C_{in} is discharged as i_{pump} is less than i_{in}. So, the voltage cross C_{in}, V_{III}, is given in

$$V_{III} = V_{ht} + \frac{I_{pump}}{w_s C_{in}} (\cos w_s t_2 - \cos w_s t) - \frac{i_{in}(t - t_2)}{C_{in}} \quad (26)$$

When $t = t_2$ and $t = t_3$, there is

$$\begin{cases} V_{III}(t_2) = V_{ht} \\ V_{III}(t_3) = 0 \end{cases} \quad (27)$$

To sum up, V_{cin} is given in

$$V_{cin}(t) = \begin{cases} 0, & t \in [0, t_0] \\ V_{II}(t), & t \in [t_0, t_1] \\ V_{ht}, & t \in [t_1, t_2] \\ V_{III}(t), & t \in [t_2, t_3] \\ 0, & t \in [t_3, T_s] \end{cases} \quad (28)$$

By substituting (28) into (6) and (7), Z_{pr} and Z_{pi} in state 2 are found in (29) and (30) as shown at the bottom of the next page.

C. STATE 3

In state 3, the charge pump is operated by D_{r2} and C_{in}, the waveform of V_{cin} and i_{pump} in state 3 is shown in Fig.5 (c), in which the input current and the resonant current are negative.

The condition that the converter works in state 3 is that the minimum value of V_{cin}, $V_{cin,min}$, needs to be greater than zero, which is

$$\begin{cases} V_{cin,min} > 0 \\ V_{cin,min} = V_{ht} + V_{II}(\frac{\pi}{w_s} - t_0) \end{cases} \quad (31)$$

Thus, V_{cin} is given in

$$V_{cin}(t) = \begin{cases} V_{ht} + V_{cin,1}(t), & t \in [t_0, t_1] \\ V_{ht}, & others \end{cases} \quad (32)$$

In detail, t_0 and t_1 is the same as (19) and (20), respectively. By substituting (32) into (6) and (7), Z_{pr} and Z_{pi} in state 3 are the same as (21) and (22), respectively. Thus, the equivalent circuit model in state 3 is the same as the state 1.

IV. SOLVE THE EQUIVALENT CIRCUIT MODEL

Since the equivalent circuit model cannot be solved analytically because the dependence among the expressions of I_{pump}, w_s and V_{ht}. Two iterative procedures are used to find the solution of I_{pump}, w_s, V_{ht} and the maximum output voltage $V_{o,max}$ of the converter respectively, to predict the characteristic of the converter.

A. FIND THE SOLUTION OF RESONANT CURRENT, SWITCHING FREQUENCY AND BUS VOLTAGE

In this section, a search algorithm is employed for the solution of I_{pump}, w_s and V_{ht}, which is given in three steps as follows.

Step1: As I_{pump} is always larger than i_{in} when the converter operates normally, I_{pump} is initated with a value larger than i_{in}. Once the value of $I_{pump}(k)$, w_s, and V_{ht} is given, the refine value for resonant current, $I_{pump,calculate}(k)$, is solved by calculating (4)-(9) sequentially.

To ensure that $I_{pump,calculate}(k) = I_{pump}(k)$, a damping factor α_1 with a value between 0 and 1 should be used to determine the new resonant current value, $I_{pump}(k+1)$, which is similar to [16]

$$\begin{cases} I_{pump}(k+1) = I_{pump}(k) + \Delta I_{pump}(k) \cdot \alpha_I \\ \Delta I_{pump}(k) = I_{pump,caculated}(k) - I_{pump}(k) \end{cases} \quad (33)$$

Step2: After solving I_{pump}, once the value of I_{pump}, w_s and V_{ht} is given, the *error*(*j*) is calculated by (34), as the distance to the target value, namely

$$error(j) = \frac{1}{2}V_{ht} - \left| \frac{Z_{tank}\left(R_{ac} + j\left(w_s(j)L_r - \frac{1}{w_s(j)C_r}\right)\right)}{Z_{linear}R_{ac}} \right| \cdot NV_o \quad (34)$$

As the converter always operates in the inductive area, *error*(*j*) is inversely related to $w_s(j)$. Thus, in order to ensure

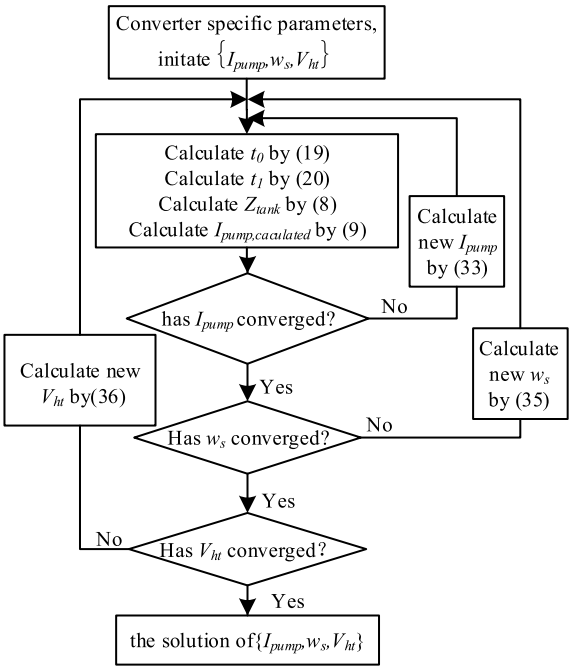


FIGURE 6. Flowchart describing the search algorithm for finding I_{pump}, w_s and V_{ht} under state1.

that $error(j) = 0$, the $w_s(j+1)$ is determined by

$$w_s(j+1) = w_s(j) + \alpha_w \cdot error(j) \tag{35}$$

where α_V is a value larger than 0.

Step3: After solving I_{pump} and w_s, the $V_{ht,calculated}(i)$ is calculated by (11). Similar to step1, the new V_{ht} is found in

$$V_{ht}(i+1) = V_{ht}(i) + \alpha_V \left(V_{ht,caculated}(i) - V_{ht}(i)\right) \tag{36}$$

where α_V is a damping factor with a value between 0 and 1.

As the states work differently from each other, the details of their iterative procedure are different. Taking state1 as an example, the specific algorithm flowchart to solve the solution of I_{pump}, w_s and V_{ht} is shown in Fig. 6.

B. FIND THE MAXIMUM OUTPUT VOLTAGE

Based on the algorithm described in section IV-A, a search algorithm is developed to solve the maximal voltage the converter can output, $V_{o,max}$, which begins with a larger constant step size followed by a smaller constant step size. First, substitute $w(j)$ into (9) to find $V_o(j)$. Then, $w_s(j+1)$ is determine based on the result of $\max\{V_o(j-1), V_o(j)\}$ and the present step size Δw_s. There are three cases as follows.

Case 1:

$$\begin{cases} \max\{V_o(j-1), V_o(j)\} = V_o(j-1) \\ \Delta w_s > \Delta w_{s,\min}, \quad j > 3 \end{cases}$$

Then, there is

$$\Delta w_s = -\Delta w_s/10 \tag{37}$$

$$w_s(j+1) = w_s(j) + \Delta w_s \tag{38}$$

Case 2: $\max\{V_o(j-1), V_o(j)\} = V_o(j)$, j > 3

Then, there is

$$w_s(j+1) = w_s(j) + \Delta w_s \tag{39}$$

Case 3:

$$\begin{cases} \max\{V_o(j-1), V_o(j)\} = V_o(j-1) \\ \Delta w_s = \Delta w_{s,\min}, \quad j > 3 \end{cases}$$

Then, there is

$$V_{o,\max} = V_o(j-1) \tag{40}$$

where, $\Delta w_{s,min}$ is the minimal step size, which is related to the accuracy. When the result is in case 3, $V_{o,max}$ will be solved, the algorithm flowchart is shown in Fig. 7.

V. ANALYSIS OF CONVERTER OPERATING CHARACTERISTICS

As state 1 and state 3 have the same equivalent circuit model, they will have the same operating characteristics, whose characteristics could be given together at the same time. Herein, the characteristics in state 1 and state 2 are analyzed as follows.

$$\begin{aligned} Z_{pr} = {} & \left(\frac{\cos(w_s t_2)}{w_s C_{in}\pi} + \frac{i_{in} t_2}{I_{pump} C_{in}\pi} + \frac{V_{ht}}{I_{pump}\pi}\right)(\cos(w_s t_2) - \cos(w_s t_3)) + \frac{\cos(2w_s t_3) - \cos(2w_s t_2)}{4 w_s C_{in}\pi} + \frac{V_{ht}}{I_{pump}\pi}(\cos(w_s t_1) - \cos(w_s t_2)) \\ & - \frac{i_{in}}{C_{in}\pi I_{pump}}\left(\frac{\sin(w_s t_1)}{w_s} + t_0\cos(w_s t_0) - \frac{\sin(w_s t_0)}{w_s} + \frac{\sin(w_s t_3)}{w_s} + t_2\cos(w_s t_2) - \frac{\sin(w_s t_2)}{w_s} - t_3\cos(w_s t_3) - t_1\cos(w_s t_1)\right) \\ & + \left(\frac{\cos(w_s t_0)}{C_{in}\pi w_s} + \frac{i_{in} t_0}{C_{in}\pi I_{pump}}\right)(\cos(w_s t_0) - \cos(w_s t_1)) + \frac{\cos(2w_s t_1) - \cos(2w_s t_0)}{4 w_s C_{in}\pi} \end{aligned} \tag{29}$$

$$\begin{aligned} Z_{pi} = {} & \left(\frac{\cos(w_s t_2)}{w_s C_{in}\pi} + \frac{i_{in} t_2}{I_{pump} C_{in}\pi}\right)(\sin(w_s t_3) - \sin(w_s t_2)) + \left(\frac{\cos(w_s t_0)}{w_s C_{in}\pi} + \frac{i_{in} t_0}{I_{pump} C_{in}\pi}\right)(\sin(w_s t_1) - \sin(w_s t_0)) + \frac{V_{ht}\sin(w_s t_3)}{I_{pump}\pi} \\ & - \frac{i_{in}}{I_{pump} C_{in}\pi}\left(t_1\sin(w_s t_1) - t_0\sin(w_s t_0) + \frac{\cos w_s t_1}{w_s} - \frac{\cos w_s t_0}{w_s} + t_3\sin(w_s t_3) - t_2\sin(w_s t_2) + \frac{\cos(w_s t_3)}{w_s} - \frac{\cos(w_s t_2)}{w_s}\right) \\ & - \frac{1}{4 w_s C_{in}\pi}[2w_s(t_3 - t_2) + \sin(2w_s t_3) - \sin(2w_s t_2) + 2w_s(t_1 - t_0) + \sin(2w_s t_1) - \sin(2w_s t_0)] - \frac{V_{ht}\sin(w_s t_1)}{I_{pump}\pi} \end{aligned} \tag{30}$$

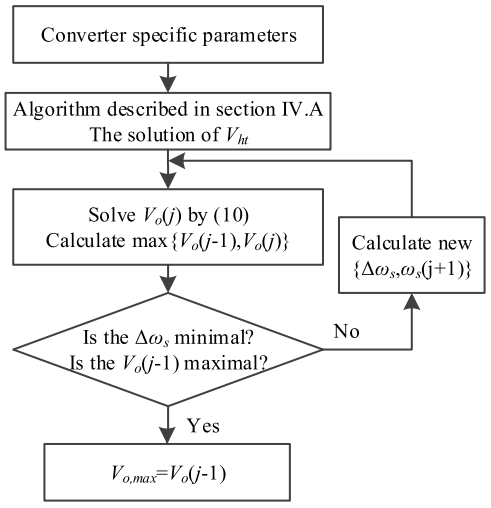


FIGURE 7. Flowchart describing the search algorithm for finding the maximum output voltage.

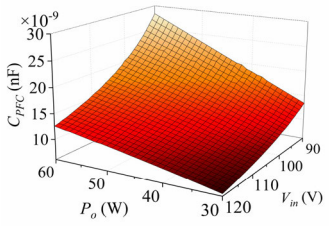


FIGURE 8. Relationship among C_{PFC}, V_{in} and P_o.

A. PFC FUNCTION

Fig. 8 shows the relationship among C_{PFC}, input voltage RMS V_{in} and load power P_o. It is shown that the high PF condition is harder to achieve as V_{in} increases and P_o decreases. Thus, in order to measure the lowest PF in the range of operation, it only needs to measure the point where P_o is the minimal and V_{in} is the maximal.

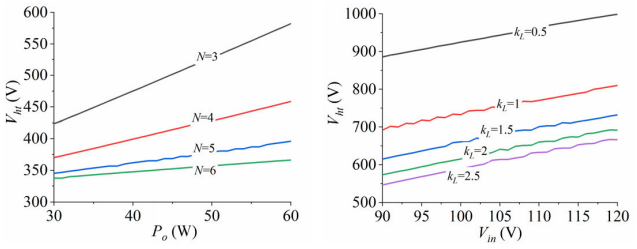


FIGURE 9. Relationship among V_{ht}, k_L, N, V_{in} and P_o.

B. BUS CAPACITOR VOLTAGE STRESS

Fig. 9 shows the bus voltage stress characteristic of the bus capacitor for P_o and V_{in} with different L_{PFC} and N in state 1 and state 2. The figure shows that V_{ht} increases with the increase of the P_o and V_{in}. Moreover, the voltage stress of bus capacitor can be reduced by increasing L_{PFC} and N.

C. SOFT-SWITCHING CONDITION

According to the previous principle analysis, D_{r1} and D_{r2} turn off under the ZCS condition obviously. As for zero-voltage switching (ZVS) condition of switches, under the assumption that the value of parasitic switch capacitances, C_{oss}, and the current flows the switches are unchanged in the dead time, the ZVS condition of S_1 and S_2 is given in

$$\begin{cases} [i_{in} - i_{pump}(t_{on})] \cdot t_s > Q_{oss}, & S_1 \\ [-i_{in} - i_{pump}(t_{on})] \cdot t_s > Q_{oss}, & S_2 \end{cases} \tag{41}$$

where, t_{on} is the time when the switch turns on; C_s is approximated as the sum of C_{oss} and stray capacitance, C_{str} ($C_s = 2C_{oss} + C_{str}$), $i_{pump}(t_{on})$ is given in

$$i_{pump}(t_{on}) = -\frac{2V_{ht}}{\pi} \frac{Z_{tanki}}{|Z_{tank}|^2} \tag{42}$$

where, Z_{tanki} is the imaginary part of Z_{tank}. Thus, to achieve ZVS, C_s/t_s should satisfy

$$\begin{cases} \dfrac{C_s}{t_s} < factor_{ZVS} \\ factor_{ZVS} = \min \dfrac{[\pm i_{in} - i_{pump}(t_{on})]}{V_{ht}} \end{cases} \tag{43}$$

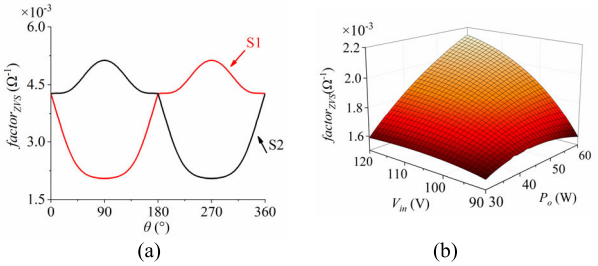
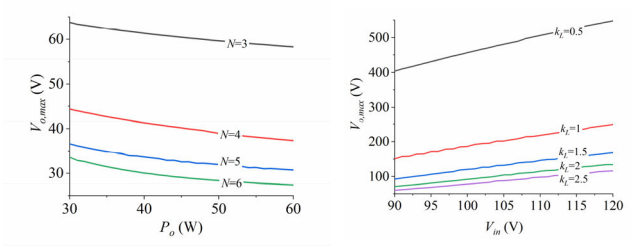


FIGURE 10. $factor_{ZVS}$ characteristic for (a) θ and (b) V_{in} and P_o.

To ensure that ZVS can be achieved in the whole range of operation, it needs to ensure that (34) is satisfied in the given range of input voltage RMS V_{in}, load power P_o and input phase θ. Fig.10(a) shows the relationship between $factor_{ZVS}$ and θ, it is shown that the most difficult input phase of S_1 to achieve ZVS is in 90°, while S_2 is in 270°. Fig.10(b) shows the $factor_{ZVS}$ characteristic of S_1 for V_{in} and P_o under 90°, which is the same as the S_2 under 270°. Thus, to verify whether the converter operates with ZVS in the range of operation, it only needs to verify whether the ZVS condition for S_1 is satisfied when V_{in}, P_o are both the minimal and $\theta = 90°$.

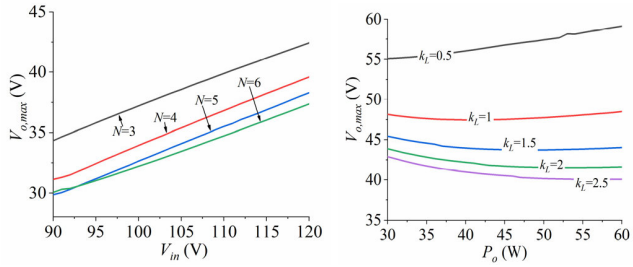
However, in fact, C_{oss} is not a constant, but always decreases as the V_{ds} increases. Thus, previous analysis for ZVS needs to be corrected. First, the equivalent C_s in (43) is given in

$$\begin{cases} C_s = \dfrac{Q_{oss}}{V_{ht}} \\ Q_{oss} = \displaystyle\int_0^{V_{ht}} (2C_{oss}(V) + C_s) \cdot dV \end{cases} \tag{44}$$



(a) (b)

FIGURE 11. Relationship among $V_{o,max}$, k_L, N, V_{in} and P_o under state 1.



(a) (b)

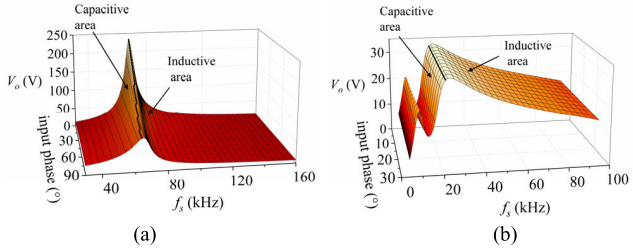
FIGURE 12. Relationship among $V_{o,max}$, k_L, N, V_{in} and P_o under state 2.

From (44), it's easy to know that C_s decreases as V_{ht} increases. Combining the V_{ht} characteristic for P_o and V_{in}, C_s decreases as V_{in} and P_o increase, at the same time, $factor_{ZVS}$ increases. Thus, the ZVS condition is still easier to achieve as V_{in} and P_o increase.

D. OUTPUT VOLTAGE

To ensure that the converter can operate normally, the maximum voltage $V_{o,max}$ it can output, should be larger than the given output voltage V_o. Fig. 11 and Fig. 12 show the maximum output voltage $V_{o,max}$ characteristic for V_{in} and P_o under different $k_L(k_L = L_{PFC}/L_r)$ and N in state 1 and state 2. The figures show that $V_{o,max}$ increases as k_L and N decreases in both state 1 and state 2. Meanwhile, the $V_{o,max}$ decreases as V_{in} decreases and P_o increases when k_L is relatively large.

Hence, if $V_{o,max}$ doesn't satisfy the requirement($V_{o,max} < V_o$), the value of L_{PFC} or N should be reduced. In addition, it only needs to verify whether the $V_{o,max}$ can meet the requirements under the maximum P_o and the minimum V_{in}.



(a) (b)

FIGURE 13. DC characteristic for θ and f_s under state 1 and (b) state 2.

Fig.13 shows the DC characteristic for θ and switching frequency f_s in state 1 and state 2. In addition, the figures also point out the boundary between the capacitive area and the inductive area is approximately at the maximum gain point.

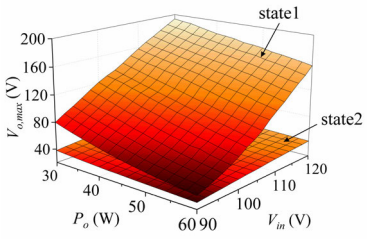
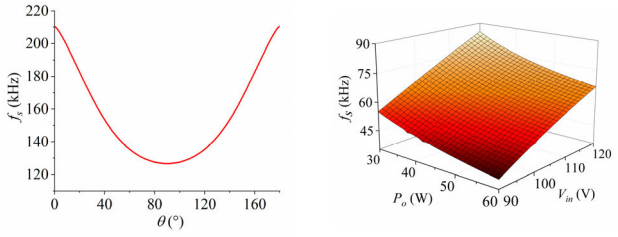


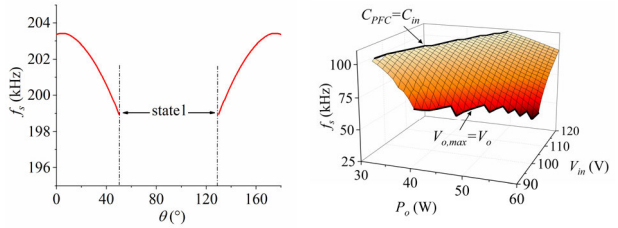
FIGURE 14. Relationship among $V_{o,max}$, V_{in} and P_o under state 1 and state 2.

Fig. 14 shows the comparison of the $V_{o,max}$ between state 1 and state 2. It shows that $V_{o,max}$ in state 1 is always larger than the state 2. Thus, it only needs to verify whether the $V_{o,max}$ satisfies the requirement in state 2.



(a) (b)

FIGURE 15. Relationship among f_s, θ, V_{in} and P_o under state1.



(a) (b)

FIGURE 16. Relationship among f_s, θ, V_{in} and P_o under state2.

E. SWITCHING FREQUENCY

Fig. 15 and Fig. 16 show the switching frequency f_s charac-teristics for θ, V_{in} and P_o. The figures show that the f_s in-creases as P_o decreases and V_{in} increases. Besides, f_s is the maximal when input phase is 0 or 180 degree, and the minimum is under 90 degree. In addition, Fig. 16 points out the area that $C_{PFC} < C_{in}$, $V_{o,max} < V_o$ and $V_{cin,max} < V_{ht}$ where the converter doesn't operate in state 2.

VI. PARAMETER DESIGN PROCEDURE OF BCIC-CPPFC CONVERTER

In this section, a parameter design procedure is illustrated, which guarantees that the converter operates with high PF

and an acceptable peak value of V_{ht} in the given range of operation. Furthermore, it is convenient and effective with the help of MATLAB software.

A. STEP1: DESIGN C_{in} TO ACHIEVE PFC FUNCTION

It can be known from the previous analysis that, if (13) is satisfied, the input current would have no dead zone and the converter operates with high PF. Therefore, in order to achieve high PF in the whole range of operation, (13) should be satisfied under the maximum input voltage RMS $V_{in,max}$ and minimum load power $P_{o,min}$ as shown in previous analysis. So, C_{in} is given in

$$C_{in} \in [\alpha C_{PFC}, C_{PFC}] \tag{45}$$

where α is a value between 0 and 1.

B. STEP2: DESIGN L_{PFC} AND N TO SATISFY THE REQUIREMENT OF OUTPUT VOLTAGE AND ENSURE THE BUS VOLTAGE TO BE ACCEPTABLE

In order to make the converter work normally in the given range of operation, it only needs to design the converter to meet the requirements of output voltage under the minimum input voltage RMS $V_{in,min}$ and maximum load power $P_{o,max}$. Thus, $V_{o,max}$ is given in

$$V_{o,max} \geq \delta V_o \tag{46}$$

where δ is the margin with a value greater than 1.

If (37) is not satisfied, the maximum output voltage of the converter will be increased by reducing N or L_{PFC} as the previous analysis shows. To ensure that the peak bus voltage stress is acceptable, there is

$$V_{ht} < V_{ht,range} \tag{47}$$

where, $V_{ht,range}$ is the maximum acceptable value of V_{ht}.

If (47) is not satisfied, the bus voltage stress can be reduced by increasing the N and L_{PFC} as shown in the previous analysis. In total, the parameter design algorithm flowchart is shown as follows in Fig. 17.

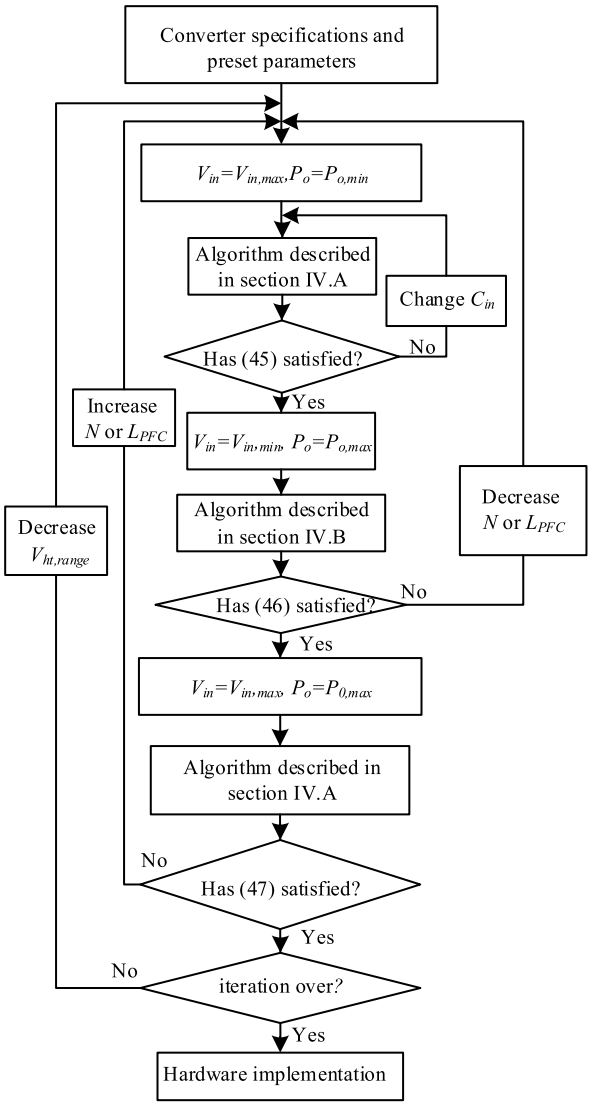


FIGURE 17. Design algorithm flowchart for the analyzed converter.

TABLE 1. The parameter for simulation verification.

Symbol	24 V (55-60 W)	24 V (110-120 W)	18 V (110-120 W)
Lr	500μH	500μH	500μH
L_{PFC}	1mH	1mH	1.3mH
T	N=3.6	N=3.5	N=4.1
C_r	100nF	100nF	100nF
C_{in}	6.8nF	25.3nF	10nF
C_{ht}	40μF	40μF	40μF
C_o	400μF	400μF	400μF
C_{EMI}	0.33μF	0.33μF	0.33μF
L_{EMI}	500μH	500μH	500μH

VII. SIMULATION AND EXPERIMENTAL VERIFICATION

A. SIMULATION VERIFICATION

To verify the universal effectiveness of the design procedure, three simulation circuits under the different conditions of operation have been designed based on the procedure shown in Fig. 17. The design results of different simulation circuits are shown in TABLE 1, herein, $\alpha = 0.95$, $\delta = 1.02$, $V_{ht,range} = 550$ V, and $\eta = 1$.

Fig. 18(a) and Fig. 18(b) show the simulation waveforms of i_{in} and v_{in} with the output voltage of 24 V under $Po = 60$ W, $V_{in} = 90$ V and $Po = 55$ W, $V_{in} = 132$ V respectively. It is shown that the converter operates normally with the minimal PF of 0.969 in the given range. Besides, the maximal value of V_{ht} is 551 V.

Fig. 19(a) and Fig. 19(b) show the simulation waveforms of i_{in} and v_{in} with the output voltage of 24 V under $Po = 120$ W, $V_{in} = 90$ V and $Po = 110$ W, $V_{in} = 132$ V respectively. It is shown that the converter operates normally with the minimal PF of 0.979 in the given range. Besides, the maximal value of V_{ht} is 547 V.

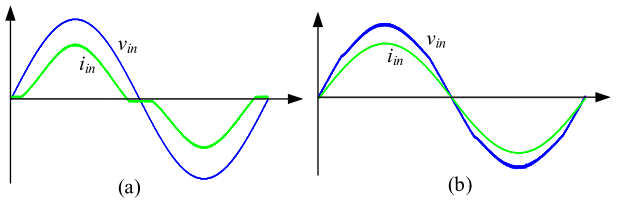


FIGURE 18. Simulation waveforms of input current and voltage with the output voltage of 24 V under (a) $V_{in} = 132$ V, $P_o = 55$ W and (b) $V_{in} = 90$ V, $P_o = 60$ W.

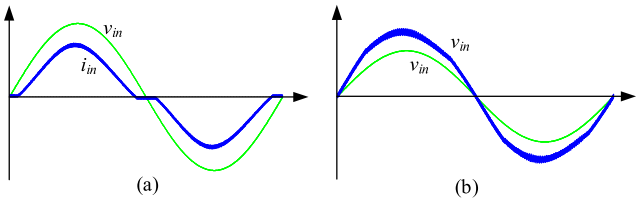


FIGURE 19. Simulation waveforms of input current and voltage with the output voltage of 24 V under (a) $V_{in} = 132$ V, $P_o = 110$ W and (b) $V_{in} = 90$ V, $P_o = 120$ W.

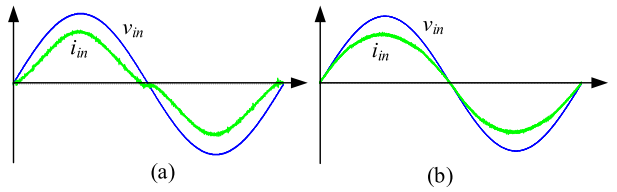


FIGURE 20. Simulation waveforms of input current and voltage with the output voltage of 18 V under (a) $V_{in} = 132$ V, $P_o = 110$ W and (b) $V_{in} = 90$ V, $P_o = 120$ W.

Fig. 20(a) and Fig. 20(b) show the simulation waveforms of i_{in} and v_{in} with the output voltage of 18 V under $Po = 120$ W, $V_{in} = 90$ V and $Po = 110$ W, $V_{in} = 132$ V respectively. It is shown that the converter operates normally with the minimal PF of 0.988 in the given range. Besides, the maximal value of V_{ht} is 586 V.

To sum up, the simulation results show that the converter could always be designed to operate normally with high PF and acceptable bus voltage in the given range of operation by the design procedure.

B. EXPERIMENTAL VERIFICATION

In order to verify the accuracy of the model and the validity of the parameter design, a 55-60 W prototype with 24 V output voltage under the input range of 90-132 V has been designed based on the procedure described in Section IV, built and tested. In detail, the efficiency is assumed as 88%, and L_r, C_r, $V_{ht,range}$, α, δ is selected as 490μH, 100nF, 520V, 0.95, and 1.02. Based on the design procedure, the designed parameter are: $L_{PFC} = 0.8$mH, $C_{in} = 7.8$nF, $N = 3.5$ and the maximal V_{ht} is 512.2V. In addition, $C_{ht} = 15\mu$F, $L_{EMI} = 500\mu$F, $C_{EMI} = 0.33\mu$F. The components make up the converter is given in Table 2.

TABLE 2. Components and parameter value list used in the laboratory prototype.

Symbol	Value	Description
Lr	490μH	PQ26/25(PC95)
L_{PFC}	800μH	Sendust core
L_{EMI}	500μH	Sendust core
T	N=3.5	PQ32/30(PC95)
C_r	100nF	CBB capacitor
C_{in}	7.8nF	Film capacitor
C_{ht}	15μF	Film capacitor
C_o	3×100μF	50V ceramic capacitor
C_{EMI}	0.33μF	CBB capacitor
D_1, D_l	VS-40CPQ060	60V/20A Schottky Rectifier
D_{r1}, D_{r2}	SCS310AP	650V/10A SiC Schottky Diode
S_1, S_2	STW24N60M2	600V/18A $R_{ds(on)}$=0.168Ω
Control Board	TMS320F28335	Drive signal controller
Driver IC	UCC21540	Isolated half-bridge driver

With the component shown in Table 2, the comparison between the V_{ht} calculated by the proposed model and measured bus voltage V_{ht} under $P_o = 55$ W and 60 W is shown in Fig. 21, showing a great agreement between theory and experiment. And the root-mean-square errors are 13.91 V for $P_o = 55$ W and 14.88V for $P_o = 60$ W.

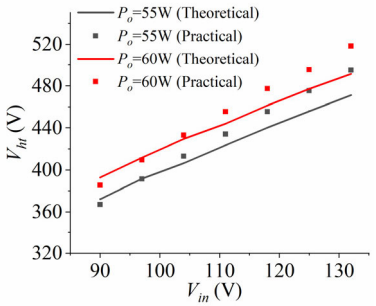


FIGURE 21. Comparison of the theoretical and practical results.

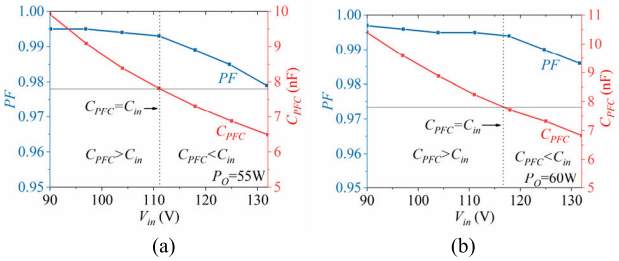


FIGURE 22. Measured PF and calculated C_{PFC} based on the measured efficiency. (a) $P_o = 55$ W and (b) $P_o = 60$ W.

Fig. 22(a) and Fig. 22(b) show the measured PF value and the calculated C_{PFC} value under input voltages RMS from 90 to 132 V with $P_o = 55$ W and 60 W, respectively. As shown in it, PF value remains high under high PF operating mode ($C_{in} < C_{PFC}$), which is always higher than 0.994 and it begins to decrease obviously when $C_{in} > C_{PFC}$, where the input current operates with a dead zone.

Besides, it also shows the accurate prediction of the model and the converter is designed operating with high PF in the given range of operation by the proposed design procedure.

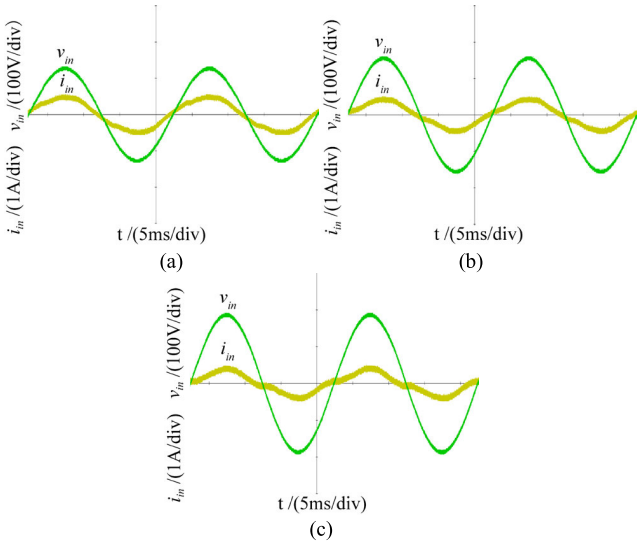


FIGURE 23. Experimental waveforms of input current and input voltage with $P_o = 55$ W under (a) $V_{in} = 90$ V, (b) $V_{in} = 110$ V and (c) $V_{in} = 132$ V.

Specially, Fig. 23 and Fig. 24 show the experimental waveforms of i_{in} and v_{in} under different input voltage RMS with $P_o = 55$ W and 60 W, respectively. It is shown that the input current operates with dead zone gradually as V_{in} increases and P_o decreases, which is the same as theoretical prediction.

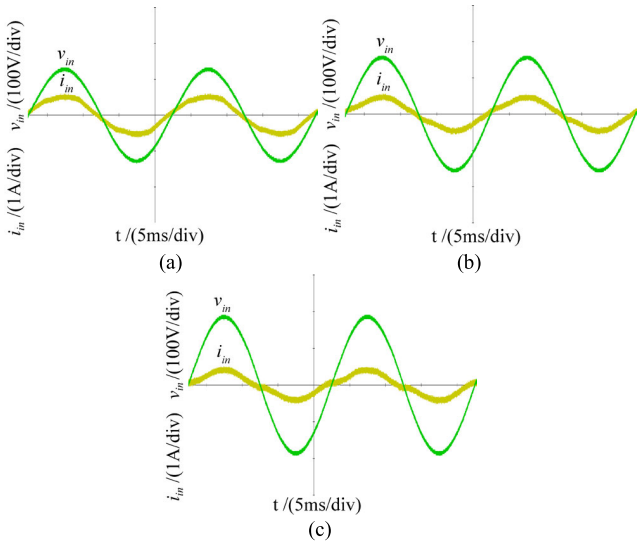


FIGURE 24. Experimental waveforms of input current and voltage with $P_o = 60$ W under (a) $V_{in} = 90$ V, (b) $V_{in} = 110$ V and (c) $V_{in} = 132$ V.

Fig. 25 shows the experimental waveforms of MOSFET S_1 at 90°, 180° and 270° respectively, under the minimal input voltage RMS of 90 V and the minimal load power of 55 W, where is the most difficult of the converter to achieve ZVS in all input phase as the previous analysis shows. As shown in Fig. 25, ZVS is achieved in all input phase. Thus, the converter always operates with ZVS.

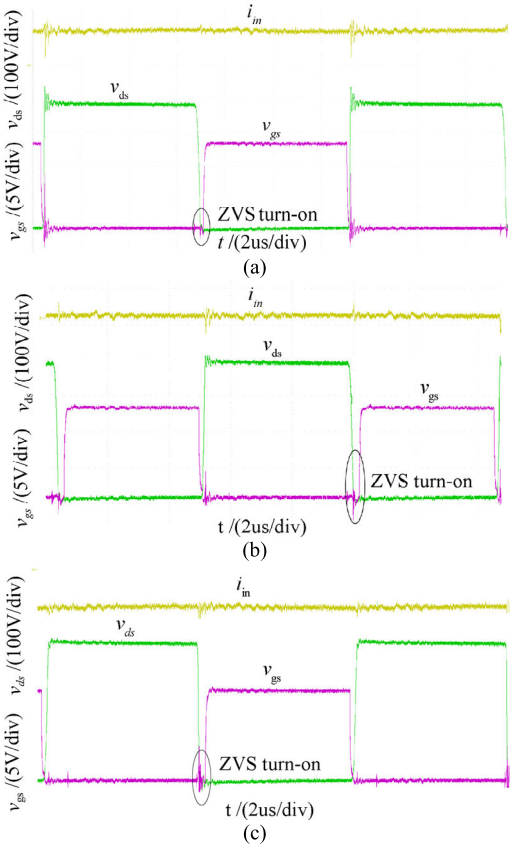


FIGURE 25. Experimental waveforms of S_1 at (a) $\theta = 90°$, (b) $\theta = 180°$, and (c) $\theta = 270°$.

VIII. CONCLUSION

In this paper, an equivalent circuit model based on FHA is established, describing the behavior of BCIC-CPPFC converter. To obtain the equivalent impedance of the charge pump, the fundamental component of its voltage is obtained via Fourier analysis, under the approximation that only the fundamental component of resonant current is considered. Based on the above, the characteristics of the converter under the high PF operating mode are obtained. Further, the design procedure based on the model has been carried out. Three simulation circuits are designed for verifying the design method. A 55-60 W experimental prototype of the converter has been built to verify the validity of the theoretical model and design procedure. From the comparison between theory and experiment, the accuracy of the model is verified. The experimental results also show that the PF remains high and ZVS is achieved in the given range, the bus voltage is always in the given acceptable range as the design procedure.

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RUNZE LV was born in Lishui, Zhejiang, China, in 1999. He is currently pursuing the bachelor's degree with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. His current research interest includes power factor correction converter.

DONGLEI DAI was born in Henan, China, in 1995. He received the B.S. degree in electrical engineering and automation from East China Jiaotong University, Nanchang, China, in 2018. He is currently pursuing the M.S. degree in power electronics and power transmission with Southwest Jiaotong University, Chengdu, China. His current research interest includes dc-dc power converter applied for on-board charger.