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Zinc Tin Oxide Synaptic Device for Neuromorphic Engineering

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ABSTRACT Neuromorphic computing offers parallel data processing and low energy consumption and can be useful to replace conventional von Neumann computing. Memristors are two-terminal devices with varying conductance that can be used as synaptic arrays in hardware-based neuromorphic devices. In this research, we extensively investigate the analog symmetric multi-level switching characteristics of zinc tin oxide (ZTO)-based memristor devices for neuromorphic systems. A ZTO semiconductor layer is introduced between a complementary metal-oxide-semiconductor (CMOS) compatible Ni top electrode and a highly doped poly-Si bottom electrode. A variety of bio-realistic synaptic features are demonstrated, including long-term potentiation (LTP), long-term depression (LTD), and spike timing-dependent plasticity (STDP). The Ni/ZTO/Si device in which the adjustment of the number of states in conductance is realized by applying different pulse schemes is highly suitable for hardware-based neuromorphic applications. We evaluate the pattern recognition accuracy by implementing a system-level neural network simulation with ZTO-based memristor synapses. The density of states (DOS) and charge density plots reveal that oxygen vacancies in ZTO assist in generating resistive switching in the Ni/ZTO/Si device. The proposed ZTO-based memristor composed of metal-insulator-semiconductor (MIS) structure is expected to contribute to future neuromorphic applications through further studies.

INDEX TERMS Neuromorphic, synaptic device, zinc tin oxide, density function theory, neural network.

I. INTRODUCTION

The recent emergence of artificial intelligence (AI), big data, and the Internet of Things (IoT) has defined a new paradigm of digital system alternation that has dramatically increased data processing complexity in terms of represented power, size, the number of gates, the amount of memory, and types of environment [1]. The von Neumann architecture that is most used in a conventional computing system can execute logic processing and arithmetic operations, but it is susceptible to problems due to scaling, power consumption, and device heating [2], [3]. To overcome the problems affecting these conventional computing systems, most studies have concentrated on finding new types of computing architectures, such as a neuromorphic or in-memory computing systems [4], [5]. Neuromorphic systems mimic neurons and synapses of the human brain, in which a variety of arithmetic, logic, learning, and memory activities are conducted using a low amount of

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power. Moreover, parallel computing through adaptive events is suitable for learning and inference [6]–[8]. Neuromorphic systems are more productive for complex tasks, such as speech and image recognition [9]. Several memory devices have been shown to have synaptic functions with a change in weight by recognizing signals from post- and pre-neurons. Two-terminal memristors, phase-change memory (PRAM), conductive bridge memory (CBRAM), and resistive change memory (RRAM) have been widely studied in the literature [10]–[27]. In particular, RRAM offers fast switching ($\sim$100 ns), low current operation ($\sim$1 μA), and a high-density structure with a crossbar array [28]–[33]. To use RRAM as a synapse for a neuromorphic system, it is essential to have multi-level conductance modulation with a pulse at the side of each two-terminal electrode. In contrast with filamentary type devices with abrupt set transitions [34], an interface type device achieves better controllable multilevel states during set and reset events [35]. Furthermore, neuromorphic engineering requires control of the conductance in an analog manner, spike time-dependent plasticity (STDP), and a CMOS compatible with neuron circuits.

Researchers have frequently reported on material approaches to improve the synaptic characteristics, including using a bilayer structure, such as HfO_2/Al_2O_3 [36], layered two-dimensional materials such as graphene, MoS_2, and h-BN [37], and semiconducting materials such as IGZO and ITO [38], [39].

Here, we conduct comprehensive experiments and simulations to evaluate the suitability of CMOS compatible ZTO-based memristor as synaptic device for neuromorphic hardware applications. We fabricated CMOS-compatible Ni/ZTO/Si devices and studied their analog synaptic behavior to emulate neuromorphic systems. When manufacturing memristor devices, there are several advantages in using silicon bottom electrodes instead of conventional metal electrodes. Since the memristor can be connected directly to the source or drain terminal of the transistor, the 1T1R structure can be easily used for embedded memory applications [40]. Moreover, an anisotropic wet etching process can be used to readily scale the silicon bottom electrode [41], and the dopant concentration in the silicon surface can be adjusted to efficiently obtain nonlinear I-V curves [42]. We demonstrate the performance of the LTP and LTD for the change in conductance state and STDP as biological synaptic features to realize the Hebbian learning rule. Different pulse schemes are used for multiple conductance states. Furthermore, we obtain the pattern recognition accuracy with a neural network considering the variation in conductance by using the proposed neuromorphic circuit. Finally, the role of the oxygen vacancies that are related to the conduction mechanism are discussed using density functional theory (DFT).

II. EXPERIMENTS

The Ni/ZTO/Si synaptic device was fabricated as follows. Doped n-type Si BE was deposited via LPCVD by reacting SiH_4 and PH_3 on an SiO_2/Si substrate. The base pressure in the sputter chamber was 1.0×10^{-4} Torr, and the target was sputtered in an argon atmosphere for the ZTO film. The temperature of the substrate was 25 °C. The working pressure and RF power were maintained at 2.1×10^{-2} Torr and 50 W, respectively. A Ni top electrode (TE) with a thickness of 100 nm was deposited via DC sputtering and was then patterned by a shadow mask with a diameter of 100 μm. X-ray photoelectron spectroscopy (XPS) analysis was performed using an XPS system with Thermo Fisher Scientific K-Alpha operating at 15 kV and 100 W with a monochromatic Al-Ka radiation source. The crystal structure of the synaptic devices was analyzed by a grazing angle X-ray diffraction (XRD) that was performed using a diffractometer (SmartLab, Rigaku Corporation). The cross-sectional structure of the Ni/ZTO/n^+-Si device was characterized using high-resolution transmission electron microscopy (HRTEM, JEM-2100F). DC I-V sweep and pulse measurements were performed with a Keithley 4200-SCS semiconductor parameter analyzer and 4225-PMU ultrafast I-V module, respectively. During device operation, the Si BEs were grounded, and the Ni TE bias was controlled.

III. THEORETICAL METHODOLOGY

A theoretical confirmation of the formation of the conducting filaments, geometry optimizations and electronic density of states (DOS) was performed using a generalized gradient approximation, Hubbard parameters (GGA + U), and Perdew, Burke and Ernzerhof (PBE) functionals [43]–[45] to produce accurate calculation that include the Coulomb effect with non-local exchange and exchange correlation functionals. The values of the Hubbard parameters U for Zn and Sn were 5.0 eV [46] and 4.0 eV respectively, as reported in earlier findings [47]. All these calculations were carried out with the help of the Vienna ab initio simulation package (VASP) [48], [49] based on density functional theory. The ZTO supercell was modeled with the following atomic ratio of Zn 4% and Sn 1%, which is very close to our experimental sample ratio, so it contains a total number of 64 atoms (Zn = 24, Sn = 6 and O = 34). Convergence tests for the total energy of the system with respect to electron wave functions were conducted using plane waves with a cut-off energy of 400 eV. The ionic positions, cell volume and lattice parameters of the system were fully relaxed with the conjugate gradient (CG) method until Hellmann Feynman forces became smaller than 0.02 eV/Å while the energy convergence criteria was met at 1×10^{-5} eV [50]. The most popular scheme for these calculations is the Monkhorst Pack (MP) [51], [52] which was applied for k-point sampling. The MP grid was chosen to be 10 × 10×10. In addition, the formation energy (ΔE) of the Ni/ZTO/Si-based memory device was calculated using the following equation [53]:

$$\Delta E = E_{\text{tot}}(\text{defect} + \text{host}) - E_{\text{tot}}(\text{host}) + n_a\mu_a + E_V \quad (1)$$

where E_{tot}(defect + host) is the total energy of the system with defects in the host material, E_{tot}(host) is the total energy of the host material (ZTO), E_V is the valence band maximum (VBM) of the host material (ZTO), n_a is the number

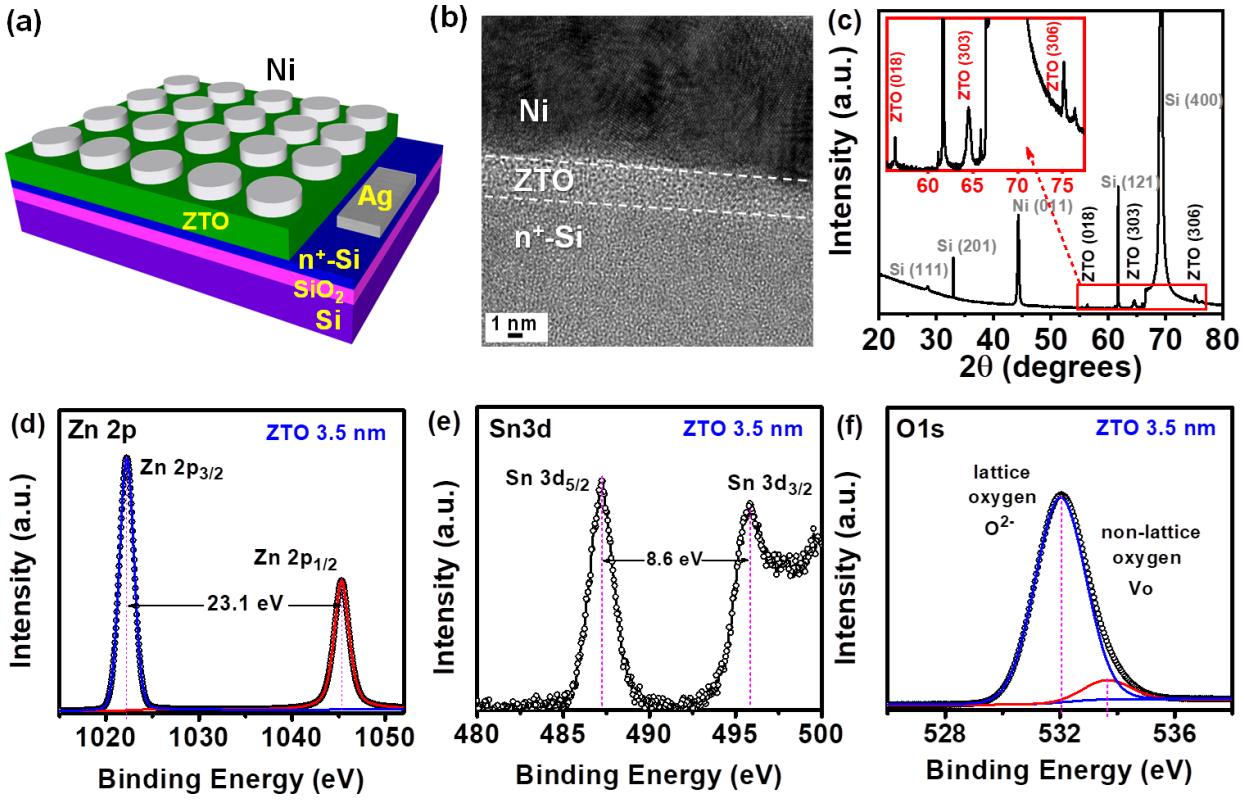

FIGURE 1. (a) Schematic and (b) HRTEM image of the Ni/ZTO/Si device. (c) Three peaks (018, 303, and 306) of Zn_2SnO_4 by XRD. XPS spectra of ZTO: (d) Zn 3d, (e) Sn 2p, (f) O 1s.

of atoms being removed (oxygen vacancy generation) during defect formation in the host material, and μ_a is the chemical potential of the oxygen vacancy.

IV. RESULTS AND DISCUSSION

Fig. 1(a) shows the schematic structure of a device composed of top electrodes/switching layer/bottom electrode as a Ni/ZTO/Si device. Fig. 1(b) displays a cross-sectional TEM image of the Ni/ZTO/Si device where the overall thickness of the ZTO is 3.5 nm. The structure of the deposited ZTO film was investigated via XRD. Fig. 1(c) shows the XRD analysis of the Ni/ZTO/Si device. The three peaks appearing at 56.33°, 64.50° and 75.16° correspond to the characteristic peaks of Zn_2SnO_4, as shown in the inset of Fig. 1(c). The XRD pattern shows that the structure of the ZTO film is the cubic inverse spinel phase (JCPDS card NO.1381) of Zn_2SnO_4 [54]. An XPS analysis was performed to confirm the chemical composition and surface chemical state of the ZTO thin film. Fig. 1(d)–(f) displays the corresponding high resolution XPS spectra of Sn 3d, Zn 2p, and O1s of the ZTO film. Fig. 1(d) shows the Zn2p core-level spectra with two distinct peaks corresponding to Zn $2p_{3/2}$ and Zn $2p_{1/2}$ at 1045.30 eV and 1022.2 eV, respectively. The spin orbit split between $2p_{3/2}$ and Zn $2p_{1/2}$ photoelectrons is 23.1 eV, which reflects strong bonding between Zn atoms and oxygen ions, which is consistent with previously reported result [55]. Fig. 1(e) shows Sn $3d_{5/2}$ and Sn $3d_{3/2}$ doublet peaks centered at 488.6 eV and 495.2 eV (Sn^{4+} and Sn^0), which is ascribed to the formation of Sn-O bonding. Spin orbit splitting of the doublet peaks Sn $3d_{5/2}$ and Sn $3d_{3/2}$ is 8.4 ± 0.2 eV [56]. The Sn cations can be regarded as Sn^{4+} and Sn^0 oxidation states. In addition, the peak intensity for Sn^{4+} is obviously higher than that of Sn^0 [57]. Fig. 1(f) shows that the XPS spectra of the O1s s-edge of the ZTO layer is deconvoluted into two peaks equivalent to lattice oxygen (oxygen ions) and non-lattice oxygen (oxygen vacancies or defects) [58]. We can see that the binding energy peaks at 532.03 eV are due to oxygen ions while the higher energy at 533.7 eV corresponds to oxygen vacancies in the ZTO film. Fig. 2(a) show the current-voltage (I-V) characteristics of the Ni/ZTO/Si device. The basic I-V curve follows the typical interface type switching with I_{ON}/I_{OFF} ratio (~67.5) and R_{ON} (~0.16 MΩ) at 0.1 V. To compare with the superior performance of the previously reported memristor devices, it is necessary to further improve resistive switching memory characteristics through various approaches, such as stack, material, and structural engineering in ZTO-based memristors [59].

The SET and RESET operation occur at a positive voltage and at a negative voltage, respectively, indicating typical bipolar operation. When a Ni/ZTO/Si device is used as a synaptic device to obtain multilevel states, the SET and RESET stop voltages in the DC sweep mode are controlled. Fig. 2(a) (inset) shows the device-to-device distribution of the SET voltage and RESET voltage, which is defined as the

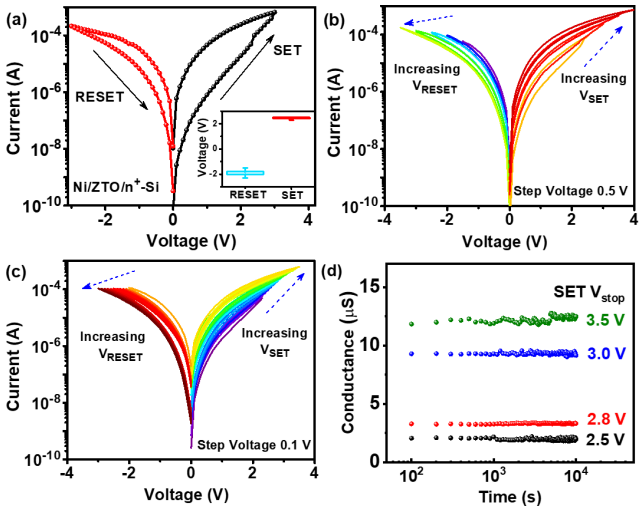

FIGURE 2. **(a) Typical interface-type I-V characteristics of a Ni/ZTO/Si device. Multilevel I-V curves by stop voltage control by (b) step voltage of 0.5 V and (c) 1 V. Retention of 4 levels controlled by SET stop voltage for 10000 s.**

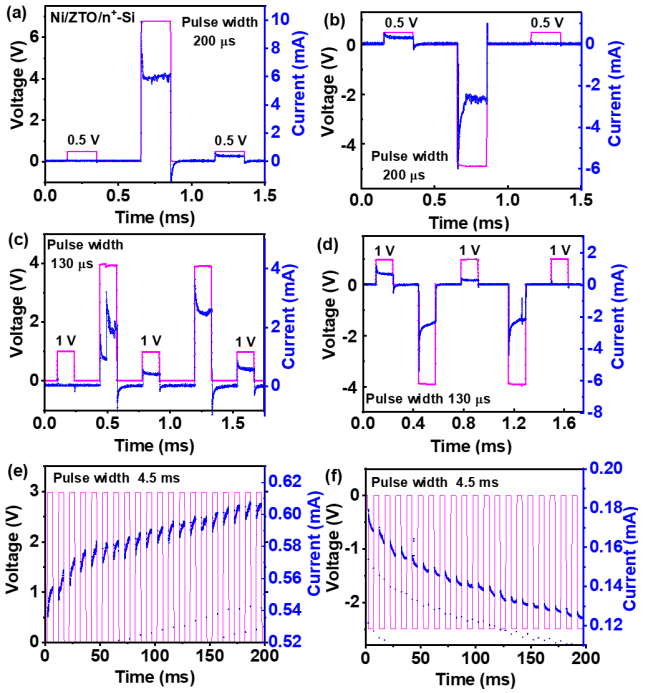

FIGURE 3. **Pulse response of the Ni/ZTO/Si device: (a) program and (b) erase transient characteristics of one SET pulse and RESET pulse. (c) Program and (d) erase of two SET pulses and RESET pulses. (e) Program and (f) erase of 20 consecutive SET pulses and RESET pulses.**

starting voltage for the transition. The device has an advantage in that the voltage and sweep range at which the current changes begin for SET and RESET are nearly symmetrical. Fig. 2(b) and (c) shows multilevel I-V characteristics of the Ni/ZTO/Si device by changing the voltage steps of 0.5 V and 0.1 V. The current can be controlled very precisely according to the stop voltage for SET and RESET. Fig. 2(d) shows the retention property of the Ni/ZTO/Si device with different current states obtained by adjusting the SET stop voltages (2.5 V, 2.8 V, 3 V, and 3.5 V). Note that four current states can be distinguished at room temperature at up to 10000 s.

To demonstrate the synapse features of the Ni/ZTO/Si devices, it is essential to apply optimized pulses to the device. To implement the multiple conductance in the same way as in applying the DC voltage, we use the designed pulse scheme. Fig. 3(a) and (b) show the transient characteristics when applying one SET pulse and one RESET pulse response between read pulses. After the SET pulse or RESET pulse is applied to the device, a current rise or decrease is noticeable in the read voltage of 0.5 V. There was a significant current overshoot in the voltage transition of the rising and falling time. Fig. 3(c) and (d) show three states of the current levels during a pair of pulse response for the SET and RESET operations, respectively. Moreover, we observe a gradual increase and decrease in the multi-level current by 20 consecutive identical pulses with identical voltage responses in Fig. 3(e) and (f).

Here, 20 distinctive states were controlled with precision for the synapse array in hardware-based neuromorphic engineering.

To further emulate a biological system, we design more sophisticated pulse schemes. The LTP and LTD characteristics of the conductance were obtained by applying repetitive pulses to Ni/ZTO/Si devices in Fig. (4).

The conductance is extracted from a DC read voltage of 0.5 V after each pulse response. Fig. 4(a) shows a gradual conductance increase and decrease by applying a series of identical pulses with different amplitudes to achieve LTP and LTD properties. The conductance of an initial minimum state was from 0.586 μS to 0.75 μS, and for the maximum conductance state, the conductance value was tunable according to the pulse amplitude with the same pulse width of 0.5 ms. The final conductance values after 40 identical pulses controlled by 2.3 V, 2.5 V, 2.8 V, and 3 V were 1.34 μS, 2.61 μS, 5.56 μS, and 8.68 μS, respectively. Similarly, the LTD characteristics are observed in the same way as for LTP.

A larger pulse voltage during the depression created a significant reduction in conductance at the first pulse response. Fig. 4(b) shows 3 cycles including LTP and LTD from identical pulses with potentiation at 3 V and a depression at –2.8 V.

To obtain further conductance states, the pulse amplitude and pulse width gradually change. Fig. 4(c) shows LTP and LTD with a larger dynamic range by pulse amplitude modulation with an increase from 1.8 V to 3 V for LTP and –1.8 V to –3 V for LTD with a fixed pulse width of 5 ms. The maximum conduction reaches 12 μS. The number of conductance states gradually vary by about 280 potentiation pulse events and 180 depression pulse events. Similarly, the pulse width was varied to obtain an increase in the number of conductance states. Fig. 4(d) shows the conductance as a function of potentiation and depression pulses. The pulse amplitude is fixed at 3 V and –3 V for potentiation and depression, respectively, and the pulse width gradually increased from 50 μs to 5 ms. The improved symmetric and linear conductance

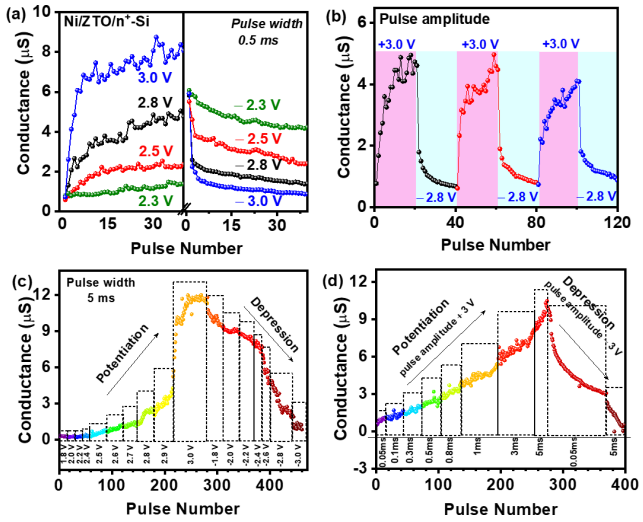

FIGURE 4. Potentiation and depression of the Ni/ZTO/Si device: (a) LTP and LTD by an identical pulse condition. (b) 3 consecutive LTP and LTD by identical pulse responses. LTP and LTD with a large dynamic range by (c) an incremental pulse amplitude and (d) incremental pulse width.

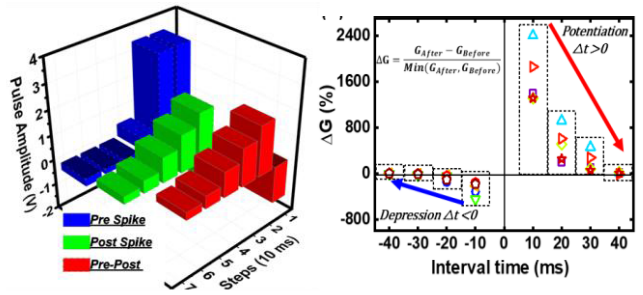

FIGURE 5. STDP characteristics of the Ni/ZTO/Si device: (a) pre-spike and post-spike pulse train scheme. (b) conductance change as a function of interval time for 5 cells.

change between the potentiation and depression process was achieved via width and amplitude modulation of the pulse conditions.

One of the most important synaptic behaviors in Hebbian learning of a spiking neural network (SNN) is STDP. The synaptic weight change is modulated by timing differences between the pre-synaptic spike and post-synaptic spike in Fig. 5(a).

Note that the pulse scheme needs to be systematically designed to demonstrate the optimal STDP behavior. The pre-spike and post-spike are set according to changes in conductance with the designed pulse train. The pulse voltage is defined as the pre-spike minus the post-spike. It is applied with 6 different pulse amplitudes, –1.5 V, 2 V, 1.5 V, 1 V, 0.5 V, and 0.3 V, in series in both the pre-spike and post-spike. Fig. 5(b) shows STDP-like curves including potentiation and depression.

Both the pulse width and interval were fixed at 5 ms where G_{After} is the conductance of the device after applying the pulse train to the device at each time interval, and G_{Before} is the conductance before applying the pulse train to the

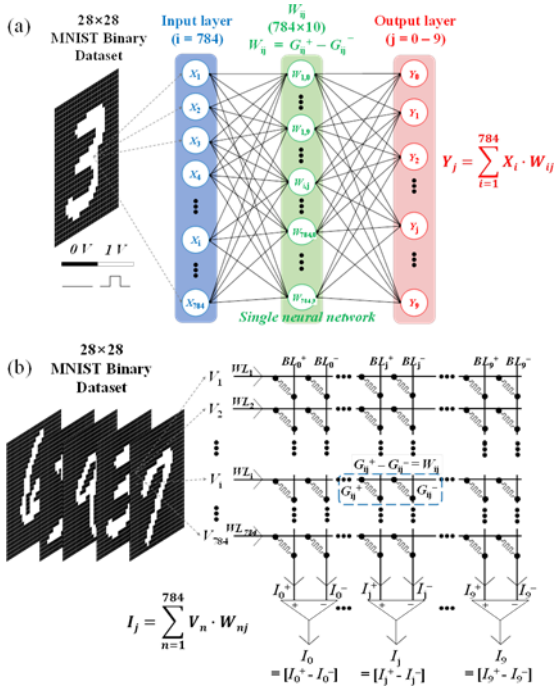

FIGURE 6. Neural network simulation for hardware-based neuromorphic system: (a) Single-layer neural network including input layer and output layer. (b) Single-layer neuromorphic circuit containing the weight of the memristor.

device at each interval. The result reveals a change in the conductance value from –449% for depression to 2401% for potentiation in the 5 devices. The smaller difference between the pre spike and post spike, a larger effective pulse results in a larger change in conductance.

Based on the measured characteristics of the Ni/ZTO/Si device, we simulate a pattern recognition test with a single layer neural network (one hidden layer) including input and output neurons in Fig. 6(a). To classify image patterns, a Modified National Institute of Standards and Technology (MNIST) dataset is used, which corresponds to the input neurons. Fig. 6(b) shows single layer neuromorphic circuit.

It consists of word lines (WL_i, i = 1 ∼ 784) for 784 input neurons and bit lines (BL_j, j = 0 ∼ 9) for 10 output neurons. The Ni/ZTO/Si device is used to connect the input and output layers so that the conductance of the device corresponds to the weight of the synaptic device.

We use two memristor devices as one synaptic device to implement the negative value of the weight. Each synaptic device consists of an exhibitory device and an inhibitory device that are responsible for the exhibitory weight G^+ and inhibitory weight G^-, respectively. The weight of the synaptic device is defined as $W_{ij} = G^+ – G^-$. The inference scheme of this neuromorphic system is as follows: a feature in a binary MNIST image (white pixel) is a 1 V pulse voltage, and the background (black pixel) is a 0 V pulse voltage, and this is applied to the crossbar array through WL_i.

All simulations train 60,000 training images in a single-layer neuromorphic system and save the weight map for every 100 training images. The test is conducted by inputting

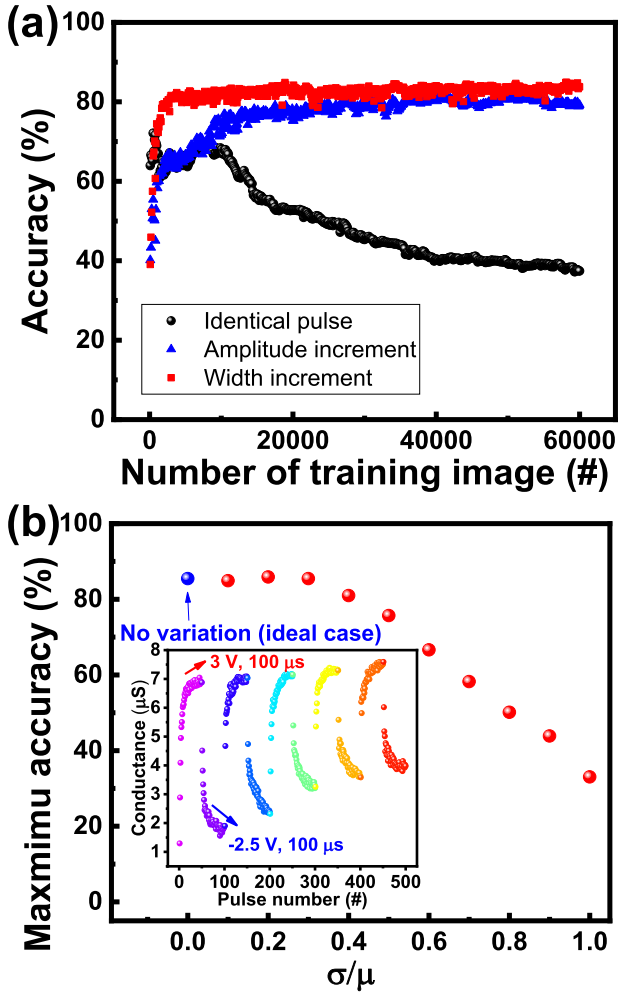

FIGURE 7. (a) MNIST pattern accuracy of three different pulse modes (identical pulse, pulse amplitude incremental, and pulse width incremental). (b) Maximum accuracy of relative standard deviation.

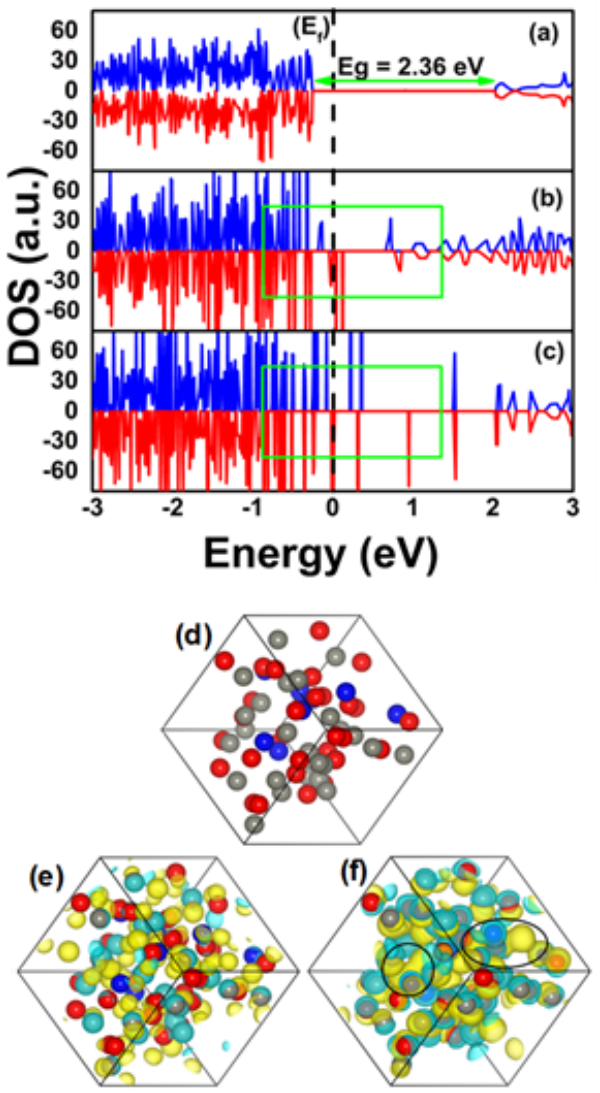

FIGURE 8. DOS of (a) ZTO, (b) single-oxygen vacancy, (c) di-oxygen vacancy. The dashed black vertical line at E = 0 eV represents Fermi level E_f and the green rectangle indicates the charge / defects states of electrons. Iso-surface charge density plots for ZTO (d) pure (e) single oxygen vacancy f) and di-oxygen vacancy. The blue spheres represent Sn atoms, grey spheres Zn atoms, red spheres oxygen atoms; yellow and sky-blue colors reveal charge accumulation and depletion respectively while the oval and circular shape box indicates the conducting channels.

10,000 test images into the stored weight map, and the number of correct images among the 10,000 test images is expressed as the recognition accuracy percentage. Fig. 7(a) shows the accuracy as a function of the number of training images for different pulse measurement conditions (identical, amplitude incremental, and width incremental methods). The width adjustment method shows the highest recognition rate because pulse width-controlled potentiation/depression can perform conductance updates linearly and symmetrically, as shown in Fig. 2(a)–(d). To examine the effects of the variation on the Ni/ZTO/Si device, we observe 5 additional consecutive potentiation/depression cycles in the inset of Fig. 7(b). As the potentiation/depression cycle continues, the maximum and minimum conductance values change. This has a disadvantage in that it is difficult to maximize the dynamic range in the cross-point array structure. Fig. 7(b) shows the maximum accuracy as a function of the relative standard deviation (RSD, σ/μ). As the RSD is greater than 0.3, the recognition rate starts to noticeably decrease. Therefore, additional approaches including materials tuning and measurement methods and a new learning algorithm in the neural network simulation to reduce the distribution of the memristor parameters will be required.

To understand the switching mechanism of the Ni/ZTO/Si device, we focus on a theoretical study to reveal the charge transport of ZTO. The results of the density of states (DOS), isosurface charge density, and formation energy of ZTO with single and di oxygen vacancies for deep analysis of the charge transformation mechanism. The value of the bandgap of the ZTO calculated by GGA + U was 2.36 eV, as shown in Fig. 8(a), which is consistent with the values obtained from the literature (2.95–3.07 eV) [60]. Fig. 8(b) and (c) show that in the case of single- and di-oxygen vacancies, the band-gap shrinks with many localized electronic states transferred from the valence band to the conduction band while crossing over

the Fermi level (E_f) as indicated by the green rectangular box. Sharing of the *2p*-electrons of Zn and *1s*-electrons of O is expected to result in sp^2 hybridization. Fig. 8 shows that the oxygen vacancy in ZTO is able to enhance the conductivity by generating the conducting oxygen vacancies. Moreover, this is supported by the calculated values of the formation energy of single and di oxygen vacancies. The value of the formation energy for the di-oxygen vacancy in ZTO (3.05 eV) is smaller than the value of single-oxygen vacancy (5.04 eV), which indicates that the di-oxygen vacancy is more favorable in terms of the formation of oxygen-based conducting defects. The lowest formation energy of the di-vacancy in the ZTO device is also evident, which is responsible for the large concentration of oxygen vacancies. Hence, the maximum charge transfer occurs as depicted. Therefore, Zn can be expected to extract oxygen from the ZTO to form a Zn oxide layer due to the strong bonding between the Zn and oxygen atoms.

This accumulation of charges also helps increase the conductance, and it can help charges/electrons to transport during switching phenomena caused by these defect states, as shown in Fig. 8(b) and (c). Fig. 8(d)–(f) show iso-surface charge density plots for a pure, single-oxygen vacancy and a di-oxygen vacancy in ZTO. Many charges are accumulated at the inter-sites between the oxygen atoms and around the oxygen vacancy as a result of a large number of conducting channel formations, which is responsible for high conductivity.

V. CONCLUSION

We demonstrate synaptic behaviors in a CMOS compatible ZTO memristor. Interface-type synaptic Ni/ZTO/Si devices with good retention are capable of fine gradual conductance control, making them well-suited for biological plasticity for hardware-based neuromorphic computing. The implementation of potentiation, depression, and STDP was realized by the pulse responses, and the conductance value were controlled well. The pattern accuracy was calculated using the MNIST data set in the neural network configuration. The behavior of the electronic density of states, formation energy, and isosurface charge density of the ZTO device was studied to propose the controllability of conductance by the oxygen vacancies model.

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