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An IEGT Model for Analyzing the High Current Turn-off Characteristics in DC Circuit Breaker Applications

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ABSTRACT The direct current (DC) circuit breaker based on semiconductor power devices is one of the critical components in multiterminal flexible high voltage DC transmission technology. A press pack injection enhanced gate transistor (IEGT) can realize a low on-state voltage similar to a gate turn-off (GTO) thyristor while achieving better high current turn-off capability and wider safety operating area than an IGBT. Therefore, an IEGT is a promising candidate for high voltage DC circuit breaker applications. The fault current conducted by devices in DC circuit breaker applications is 4∼6 times the device rated current, which brings great risks to reliable operation. Optimizing the device turn-off characteristics and then realizing reliable operation are indispensable parts of DC circuit breaker design. For analyzing the high current turn-off characteristics under the working conditions of a DC circuit breaker, an IEGT model is proposed in this paper. In the model, a simple method for predicting the static-state I-U characteristics is established. In addition, based on the differences in the gate structures of IEGTs and IGBTs and the influence of the gate structure on the nonlinear capacitances between device terminals, the nonlinear capacitances are greatly improved to better describe the turn-off transient process. Subsequently, the model is verified by experiments. The model is expected to be a convenient simulation tool for designing a high voltage DC circuit breaker with IEGTs.

INDEX TERMS High voltage direct current (DC) circuit breaker, high current turn-off characteristics, press pack injection enhanced gate transistor (IEGT), IEGT model, static-state output characteristics, nonlinear capacitance.

I. INTRODUCTION

The development of multiterminal flexible high voltage direct current (HVDC) projects puts forward urgent demands for high voltage direct current (DC) circuit breaker technology. A fully controlled DC circuit breaker based on power semiconductor devices is one of the main technical development directions and has already realized successful engineering applications [1]–[3].

As power semiconductor devices are the key components of a DC circuit breaker, the working reliability of devices directly affects the working reliability of the breaker, and how to select suitable devices is critical for high voltage DC circuit breaker design [4]. The press pack injection enhanced gate transistor (IEGT) can realize a low on-state voltage similar to a gate turn-off (GTO) thyristor while achieving better high current turn-off capability and wider safety operating area than an insulated gate bipolar transistor (IGBT) [5]. The current density of a fabricated 4500 V IEGT with multiple trench gates at a 2.5 V forward voltage drop is over ten times that of the conventional trench gate IGBT [6], [7]. The use of a double-sided heat dissipation packaging structure can cool down both the collector and emitter sides and bring about good heat dissipation characteristics. Because of the low conduction loss and good heat dissipation characteristics, a 4.5 kV/3kA IEGT is able to conduct and turn off 20 kA for 5 ms with the junction temperature is only 100 °C [4]. In addition, the press pack structure and short-circuit failure mode can also provide convenience for series connection of multiple IEGTs, which is very critical for high-voltage

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applications [4], [8]. Therefore, due to these advantages, an IEGT is suitable for very high current interruption and is a promising candidate for high-voltage DC circuit breakers.

Under the working conditions of a high voltage DC circuit breaker, the fault current conducted by power semiconductor devices is 4∼6 times the rated current, and the devices are working in the near desaturation state when turning off the fault current, which brings great risks to reliable operation of devices [9]. Optimizing the turn-off characteristics and then realizing reliable operation of devices are indispensable parts of circuit breaker design. This paper focuses on the analysis of the high current turn-off characteristics of an IEGT in high voltage DC circuit breaker applications.

An IEGT simulation model is necessary for revealing the relevant influencing parameters and corresponding influencing laws for the turn-off characteristics of devices and is helpful for reducing the risk of device damage and economic losses, especially for high-power devices. Based on an analysis of the static-state and dynamic turn-off transient characteristics of an IEGT in DC circuit breaker applications, the requirements for the IEGT model are analyzed as follows.

The fault current conducted by power semiconductor devices in a high voltage DC circuit breaker is above ten thousand ampere, which is far larger than the rated collector current (at most 3000 A), and the devices are working in the near desaturation state when turning off the fault current. In addition, to reduce the conduction losses and make full use of the current conduction ability of devices, the selected driving voltage is approximately 18∼20 V in engineering, which is larger than that under other application conditions. Therefore, the near desaturation region of the static-state I-U characteristic curve, especially under large driving voltages, is an indispensable focus point for high voltage DC circuit breaker engineering, and it is the basis for analyzing the conduction loss and maximum breaking current.

However, the parameters offered by IEGT datasheets are mainly focused on the working conditions of converters or inverters, and the static-state I-U characteristic curves offer no values for the near desaturation or desaturation regions [10]–[12], which brings difficulties to the applications of IEGTs in DC circuit breakers. In addition, adopting test methods directly in the lab puts high requirements on the experimental equipment, and it is easy to damage devices. As a result, modeling the I-U characteristic curve, especially the characteristics in near desaturation regions under large driving voltages, is significant for the application of IEGTs in high voltage DC circuit breakers.

Calculating the excess carrier distribution by solving the ambipolar diffusion equation and then obtaining the electron and hole currents are the main parts of the static-state modeling. As a special type of IGBT, an IEGT has many similar features to an IGBT from the perspective of the chip structure, working mechanism and so on. Meanwhile, an IEGT has deeper and wider trench gate electrodes than those of an IGBT, which increases the carrier density inside the device and prevents carriers from passing to the emitter electrode [7], [13]. Consequently, carrier accumulation occurs, and the N-base carrier distribution increases on the emitter electrode side. That is, an injection enhancement (IE) effect occurs. As a result, adopting the carrier distribution calculation methods based on the one-dimensional carrier distribution approximation, for example, the Hefner and Kraus models, will result in large errors [14]–[18]. For describing the IE effect and then calculating the electron and hole currents accurately, the two-dimensional effects in the N-channel region should be considered when solving the ambipolar diffusion equation [19]–[29]. However, regardless of whether numerical iteration methods or approximate analytical derivations are used, some chip structure parameters, such as the distance from the bottom of the trench gate to the P-base, cell half-width and intercell half-width, are needed in the calculations. In addition, determining these structure parameters for IEGTs in DC circuit breaker engineering is difficult and impractical, which limits the application of these methods. Therefore, a simple method for modeling the static-state output characteristics is necessary for the application of IEGTs in DC circuit breakers.

Modeling the turn-off transient process of a device is also essential for the analysis of turn-off transient voltage overshoots, turn-off losses, influences of the driving circuit and stray inductances on the turn-off process and so on. The nonlinear capacitances between device terminals are key parts of the transient model and have an important influence on the increase rate of the collector-emitter voltage during the turn-off process [30]–[33]. In addition, the nonlinear capacitances are closely related to the gate structure. As mentioned above, an IEGT has a deeper and wider trench gate structure than that of an IGBT. This feature of an IEGT indeed affects the calculations of nonlinear capacitances. The nonlinear capacitances were improved in [33]. This improved model is used to reproduce the target device port characteristic waveforms that have been previously obtained based on experiments. In addition, the electromagnetic disturbance problems in the application circuit can then be predicted using the model. This model cannot realize predictions about the port characteristics of the device itself. Therefore, it is not applicable to the problems faced in this paper, where the high current turn-off characteristics need to be predicted to complement experimental approaches. Therefore, the nonlinear capacitances still should be of strong concern for the turn-off transient modeling.

Thus, to analyze the high current turn-off characteristics of an IEGT under the working conditions of a DC circuit breaker, the IEGT model is still needs to be further studied. This paper is organized as follows. In section II, the high current turn-off process of an IEGT in DC circuit breaker applications is analyzed. Then, the key aspects for modeling the device to describe the working process are determined. In section III, we derive a new IEGT model based on semiconductor device theory and the features of an IEGT. In the model, a simple method for modeling the static-state I-U characteristics is proposed, and the nonlinear capacitances

between device terminals is greatly improved for adaption to the deeper and wider gate structure of an IEGT. In section IV, first, we establish an experimental platform in the laboratory according to the equivalent working circuit of the device under the working conditions of a high voltage DC circuit breaker. Second, the proposed model is verified by a comparison between the simulation and experimental results. In section V, some conclusions are presented.

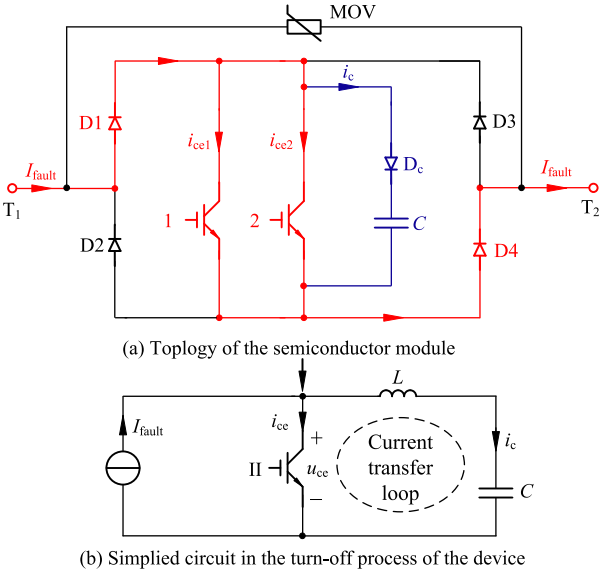


FIGURE 1. Diode full bridge topology of the semiconductor module and equivalent circuit during device turn off.

II. ANALYSIS OF THE HIGH CURRENT TURN-OFF PROCESS AND REQUIREMENTS FOR THE IEGT MODEL

This paper takes the diode full-bridge topology [1]–[3] shown in Fig. 1(a) as an example. This topology has been successfully implemented in engineering. In the topology, D1, D2, D3 and D4 are current conduction power diodes, 1 and 2 are two parallel fully controlled semiconductor devices, D_c and C form the current transfer branch, a metal oxide varistor (MOV) forms the fault current cut-off branch, and T_1 and T_2 refer to the two terminals of the topology.

Assuming that the fault current is conducted from T_1 to T_2, the power devices D1, D4, 1 and 2 conduct the fault current first. When the fault current increases to some degree, devices 1 and 2 turn off, and the fault current is transferred to the high power capacitor in parallel with devices 1 and 2. The transfer process from devices 1 and 2 to the capacitor results in an increase in the voltage in the module. When the voltage increases to some degree, the MOV in parallel with the module conducts the fault current and completes the cut-off of the fault current.

According to Fig. 1(a) and its working process described above, a simplified circuit representing the turn-off process of device 1 or 2 is derived and shown in Fig. 1(b), where C is the parallel capacitance; L is the stray inductance in the current transfer loop formed by device 1 or 2 and the parallel capacitor, which mainly refers to the stray inductances in the connecting conductor; u_{ce} is the collector-emitter voltage of the IEGT; i_{ce} is the collector current of the IEGT; and i_c is the current of the capacitor branch. In addition, considering that the duration of the device turn-off process (μs level) is much shorter than that of the fault current conduction process (ms level) in the modules, a constant current source I_{fault} is used in Fig. 1(b). The MOV does not work in the turn-off process of the device, so the MOV is not included in Fig. 1(b).

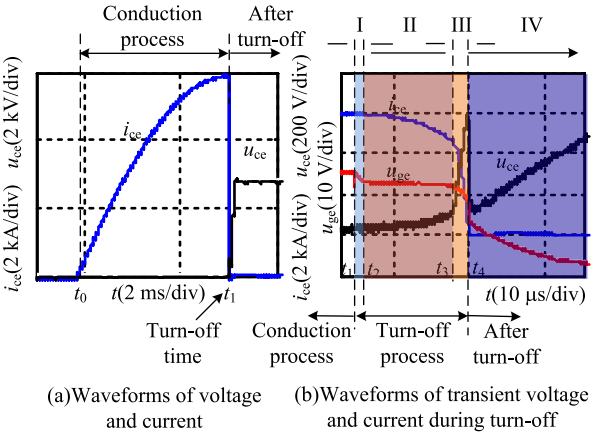


FIGURE 2. Typical turn-off current and voltage waveforms.

Fig. 2 shows the typical current i_{ce} and voltage u_{ce} waveforms of the IEGT during the conduction and turn-off processes in the laboratory. Referring to Fig. 2(a), the IEGT conducts and turns off the fault current at t_0 and t_1, respectively. Considering that the breaking current at t_1 is far larger than the rated current of the device and the device is working in the near desaturation state when turning off the fault current, the static-state model should focus on the near desaturation and desaturation regions of the I-U curve. Based on the static-state model, the conduction losses and saturation currents can be predicted. Then, the maximum breaking current and device selection can be determined.

Fig. 2(b) shows the details of the turn-off transient collector current and collector-emitter voltage waveforms. The turn-off process is divided into four stages in this paper according to the turn-off mechanism of the IEGT.

Stage I ($t_1 - t_2$): In the first stage, the IEGT is working in the saturation state, and with decreasing gate voltage u_{ge}, the IEGT approaches the desaturation state.

Stage II ($t_2 - t_3$): The device starts to work in the desaturation state at t_2. In this stage, the depletion region expands with the excess carriers outflowing from the base. Fig. 3 shows the chip cross-section structure and expansion of the depletion region. In Fig. 3, D_g is the distance from the bottom of the trench gate to the P-base; W_d is the width of the depletion region; C_{gd} is the gate-drain nonlinear capacitance; and C_{dsj} is the drain-emitter nonlinear capacitance. The width W_d increases with increasing voltage u_{ce} during the turn-off

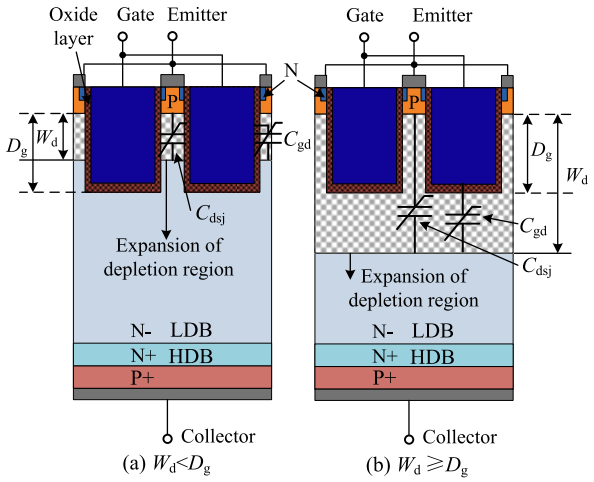


FIGURE 3. Chip cross-section structure and expansion of the depletion region in the IEGT during turn off.

process. Fig. 3(a) and Fig. 3(b) show the depletion region for $W_d < D_g$ and $W_d \geq D_g$, respectively.

This stage corresponds to Fig. 3(a), where W_d is less than D_g. The increase rate of voltage u_{ce} in this stage is relatively small because the capacitances C_{gd} and C_{dsj} for the case shown in Fig. 3(a) are relatively large.

In terms of the device, the voltage drop in the N-base shows a small change, and the increase in voltage u_{ce} is mainly determined by the expansion of the depletion region. Meanwhile, according to Fig. 1(b), the voltage u_{ce} and current i_{ce} satisfy the relation shown in (1). From (1), we know that the change in current i_{ce} is coupled with the change in voltage u_{ce}, so the expansion of the depletion region will also result in a simultaneous decrease in current i_{ce}.

$$u_{ce}(t) = L\frac{\mathrm{d}\left[I_{fault} - i_{ce}(t)\right]}{\mathrm{d}t} + \frac{1}{C}\int_{t_2}^{t_3}\left[I_{fault} - i_{ce}(t)\right]\mathrm{d}t. \quad (1)$$

Stage III ($t_3 - t_4$): When W_d is greater than D_g, which is shown as Fig. 3(b), the capacitances C_{gd} and C_{dsj} become relatively small, and the collector-emitter voltage starts to increase rapidly. When the collector current becomes zero at t_4, the device turns off completely.

Stage IV (after t_4): A current oscillation or a tail current will occur in this stage. The current characteristics after t_4 have a close relation with the N-base excess carriers. If few or no N-base excess carriers remain when current i_{ce} is close to zero, then current oscillation will occur easily [13]. Otherwise, the slow recombination of the remaining excess carriers will result in a tail current [13]. The waveforms shown in Fig. 2(b) indicate that the current oscillation phenomenon is not obvious for the tested IEGT.

There is a waveform phenomenon that should be of concern. As we all know, for the turn-off process of a device in converter or inverter applications, the current i_{ce} remains constant before the voltage u_{ce} reaches the bus voltage. However, according to the current waveforms in stages II and III shown in Fig. 2(b), we can find that current i_{ce} will decrease with a simultaneous increase in voltage u_{ce} because there is no clamping voltage in the circuit. Therefore, the nonlinear capacitances affect both voltage u_{ce} and current i_{ce} in DC circuit breaker applications. In addition, for converter or inverter applications, the nonlinear capacitances only affect voltage u_{ce} before it reaches the DC-side bus voltage. Therefore, the effect of nonlinear capacitances on the turn-off process in DC circuit breaker applications is greater than that in converter or inverter applications.

In summary, the variations in voltage u_{ce} and current i_{ce} in stages II and III have a close relation with the nonlinear capacitances C_{gd} and C_{dsj}. The capacitance values directly affect the increase rate of the collector-emitter voltage during the turn-off process. The characteristics of current i_{ce} in stage IV are mainly determined by the N-base excess carriers. The nonlinear capacitances between device terminals and N-base excess carriers have a great impact on the turn-off transient process of devices.

III. ESTABLISHMENT OF THE IEGT MODEL

According to the above analysis, the IEGT model is established from two aspects: the static-state output characteristics and dynamic turn-off transient process.

A. STATIC-STATE MODELING

The static-state I-U characteristic curve is the basis for determining the conduction losses and saturation currents at different driving voltages.

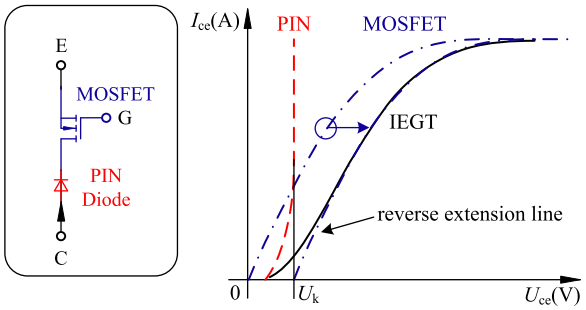
The existing methods for modeling the static-state I-U characteristic curve require many chip structure parameters and are not suitable for DC circuit breaker engineering applications. In terms of the near desaturation or desaturation regions of the static-state I-U characteristic curve, which are the device characteristics of special concern in high voltage circuit breaker applications, the on-state forward voltage drops and hole/electron currents in the device all have some certain change laws. Based on these change laws, the static-state IEGT model can be simplified.

The on-state voltage, electron current I_n and hole current I_p are three parts of the static-state model.

1) ON-STATE VOLTAGE

First, the metal oxide semiconductor field-effect transistor (MOSFET)/PIN rectifier model shown in Fig. 4(a) is used to analyze the on-state voltage drops in the device [31]. The device consists of a PIN rectifier connected in series with a MOSFET operating in its near desaturation region.

In terms of the PIN diode, the on-state voltage drop increases logarithmically with the conduction current due to the conductivity modulation effect [31], that is, $U_{PIN} = 2kT/q \times \ln(FJ)$, where k is Boltzmann's constant; T is temperature; q is the electric charge; F is a function related to the chip parameters of the device; and J is the conduction current density. Therefore, with a conduction current increase, the change in the voltage on the PIN diode decreases.



(a) MOSFET/PIN model (b) On-state voltage drops in IEGT

FIGURE 4. MOSFET/PIN rectifier model, and on-state forward voltage drops in the IEGT.

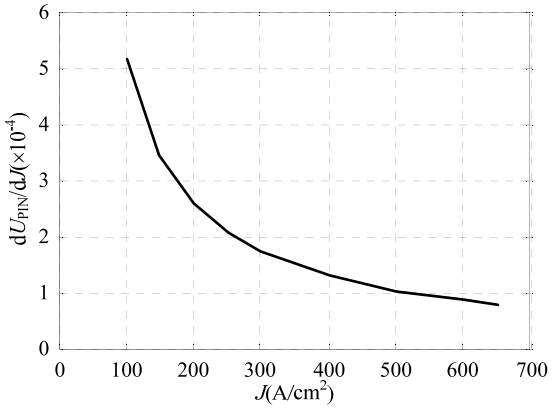


FIGURE 5. Derivative of U_{PIN} with respect to J under different conduction current densities J (T = 300 K).

Fig. 5 shows the calculation results for the derivative of U_{PIN} with respect to J under different conduction current densities J at $T = 300$ K, where the 2D static-state model for a high voltage trench IGBT in [28], [29] and the chip parameters of a 4500 V IEGT in [22] are used. From the results, the differential value is already less than 5×10^{-4} when J is above 100 A/cm^2. As a result, the voltage drop across the PIN diode remains approximately constant at a large conduction current density, which is applicable to DC circuit breaker applications.

According to the voltage drops shown in Fig. 4(b), at a low conduction current density with a large gate bias voltage, the voltage drop across the PIN diode becomes dominant, and the IEGT conduction current increases exponentially with the on-state voltage [31]. At larger conduction current densities, the voltage drop across the MOSFET becomes significant, and the IEGT conduction current starts to increase linearly with the on-state voltage [31]. Therefore, the approximate PIN diode voltage at large current density U_k can be obtained using the intersection of the reverse extension line and the abscissa, as shown in Fig. 4(b).

2) ON-STATE ELECTRON AND HOLE CURRENTS IN THE DEVICE

The MOSFET/PIN rectifier model shown in Fig. 4(a) cannot simulate the hole current in the device. Using the current transport equations, the electron and hole current densities J_n and J_p around the N-channel can be obtained as

$$J_n(W) = \frac{D_n}{D_n + D_p} J_{ce} + 2q \frac{D_n D_p}{D_n + D_p} \frac{dn}{dx}\bigg|_{x=W}$$
$$J_p(W) = \frac{D_p}{D_n + D_p} J_{ce} - 2q \frac{D_n D_p}{D_n + D_p} \frac{dp}{dx}\bigg|_{x=W}, \quad (2)$$

where D_n and D_p are the electron and hole diffusivities, respectively; n and p are the electron and hole concentrations, respectively; J_{ce} is the conduction current density, with $J_{ce} = J_n + J_p$; and W refers to the end of the drift region or N-channel region in the device.

The hole current $I_p(W)$ consists of two components, one for recombination in the accumulation layer, $I_{rec}(W)$, and the other for flow through the P-well to the emitter, αJ_{ce}, where α is the electron injection efficiency. That is,

$$J_p(W) = J_{rec}(W) + \alpha J_{ce}. \quad (3)$$

The recombination current $J_{rec}(W)$ is converted to an electron current in the vicinity of the accumulation layer. That is, the electron current density at the emitter side is $J_{Ee} = J_n(W) + J_{rec}(W)$.

The MOSFET model in [34] is used to model the electron current I_{Ee}. Meanwhile, considering that the voltage drop across the PIN diode remains approximately constant in DC circuit breaker applications, the on-state voltage of the device at a large current density can be obtained by adding a certain value to the voltage drop across the MOSFET. Therefore, a coefficient U_k is introduced in (4) to approximately describe the PIN diode voltage, which can simplify the model.

$$I_{mos} = \beta \left(U_{ge} - U_T\right)^{\gamma} \tanh\left[\theta \left(U_{ce} - U_k\right)\right], \quad (4)$$

where β is a parameter related to the transconductance; U_{ge} is the driving voltage; U_T is the equivalent MOSFET gate channel threshold voltage; γ is a power-law parameter; and θ is a parameter to scale the collector-emitter voltage U_{ce}.

The IE effect of the IEGT can be characterized by the electron injection efficiency $\alpha = J_{Ee}/J_{ce}$ [35]–[37]. In addition, according to the experimental results shown in [35], the electron injection efficiency α under different conduction current density is shown in Fig. 6. According to the results, we can see that the relation between α and J_{ce} is nonlinear for an IEGT.

3) STATIC-STATE I-U RELATION OF THE IEGT

To conform to this nonlinear change law for the relation of α to J_{ce} and the fact that the IEGT and equivalent MOSFET part in the device are working in the desaturation state at the same time, the voltage part in (4) is improved as the nonlinear function $\theta(U_{ce} - U_K)^{\lambda}$, and the I-U relation of the IEGT is described as

$$I_{ce} = \beta \left(U_{ge} - U_T\right)^{\gamma} \tanh\left[\theta \left(U_{ce} - U_k\right)^{\lambda}\right], \quad (5)$$

where λ is a model coefficient to be extracted.

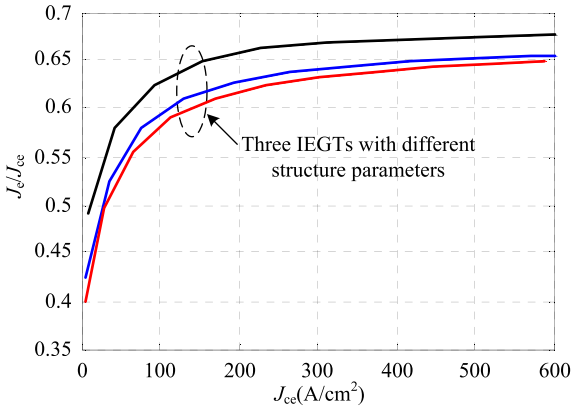


FIGURE 6. Ratio of the electron current to the total current under different conduction current densities.

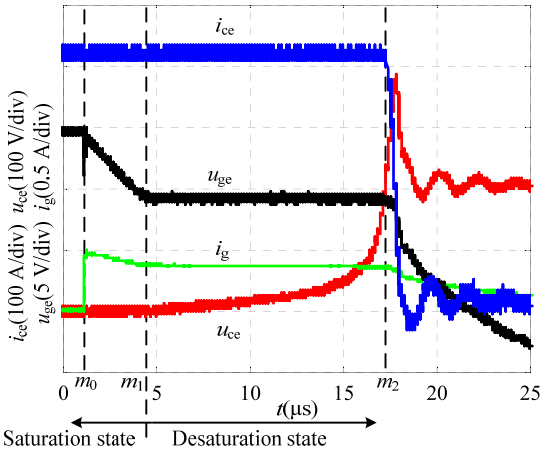


FIGURE 7. Typical turn-off transient current and voltage waveforms based on the clamped inductive load circuit or double-pulse circuit.

When U_{ce} reaches the desaturation voltage U_{ce-s}, the hyperbolic tangent function is approximately equal to 1. That is,

$$\theta \left(U_{\text{ce-s}} - U_{\text{k}}\right)^{\lambda} = arc\tan\text{h}\left(0.999\right). \tag{6}$$

According to the approximate relation of a quadratic function between I_{mos} and U_{ds} [23], we derive the relation $I_{mos} = \beta \left(U_{ge} - U_T\right)^{\gamma/2} U_{ds} - \beta U_{ds}^2/2$, with $I_{sat} = \beta(U_{ge} - U_T)^{\gamma}$. In addition, the desaturation voltage is

$$U_{\text{ce-s}} = \left(U_{\text{ge}} - U_{\text{T}}\right)^{\gamma/2} + U_{\text{k}}. \tag{7}$$

4) DETERMINATION OF STATIC-STATE MODEL PARAMETERS

Determining the static-state model coefficients is an essential step for the model. The extraction methods for parameters β and γ can follow [34]. According to the methods in [34], some saturation current values at different driving voltages are needed. However, for high power IEGTs, the datasheets do not offer the desaturation region in the I-U characteristic curve, so it is difficult to obtain the saturation current values. In addition, directly measuring the saturation currents at different driving voltages will bring a great risk of device damage and put forward high requirements for the test conditions. This paper proposes an easy and safe experimental method for obtaining some saturation current values at different driving voltages and then determining the static-state model coefficients. The details are shown in the following.

Fig. 7 shows typical current and voltage waveforms based on the clamped inductive load circuit [15] or double-pulse test circuit. As shown in Fig. 7, the device starts to turn-off at m_0, and with the decrease in the gate voltage, the IEGT approaches the desaturation state. When the gate voltage remains constant at m_1, the device starts to work in the desaturation state. Therefore, the collector current after m_1 is the desaturation current at the corresponding gate voltage.

This can be further qualitatively explained using the typical static-state output characteristics of the device shown in Fig. 8, where the dotted line is the saturation currents at

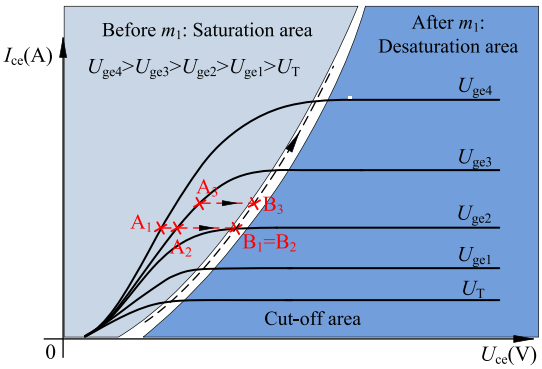


FIGURE 8. Typical static-state output characteristics.

different driving voltages. Referring to Fig. 8, the device is working in the saturation area before m_1 (A1, A2, or A3), and with the decrease in the gate voltage, the device starts to work in the desaturation area at m_1 (B1, B2, or B3).

Therefore, the collector currents at the points of A1, A2, and A3 are equal to the desaturation currents corresponding to the gate voltages at the points of B1, B2, and B3. Then, some desaturation currents at different driving voltages can be obtained from the turn-off current and voltage waveforms based on the clamped inductive load circuit or double-pulse test circuit.

The parameters θ and λ can be easily determined from (6), (7) and some data in the linear region provided by the datasheet of the device. In addition, it should be noted that the two parameters vary with the driving voltage.

B. TURN-OFF TRANSIENT MODELING

A model describing the turn-off transient process of the device is a convenient and powerful tool for revealing the relevant influencing parameters and corresponding influencing laws for the turn-off characteristics of the device.

The equivalent circuit of the IEGT in this paper is shown in Fig. 9, where the IEGT is modeled as a controlled current

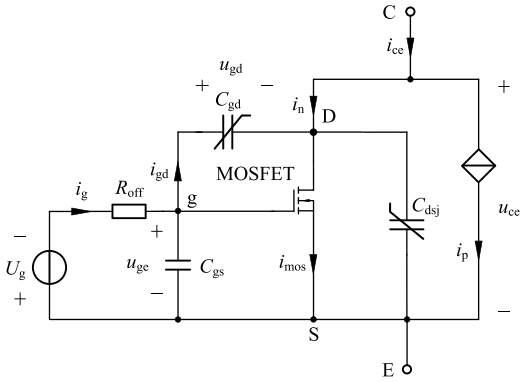


FIGURE 9. Transient turn-off equivalent circuit of the IEGT.

source i_p and a MOSFET to describe the hole and electron currents, respectively; C, E, and G refer to the collector, emitter, and gate, respectively; D refers to the drain of the equivalent MOSFET; u_{gd} is the gate-drain voltage; C_{gs} is the gate-emitter capacitance; R_{off} is the driving resistance when the IEGT turns off; U_g is the pulse driving source; i_n is the electron current; and i_g and i_{gd} are the gate current and the current between the gate and drain, respectively.

According to the equivalent circuit shown in Fig. 9, the circuit can be divided into three main parts: the MOSFET part, the capacitances between device terminals part and the hole current source part.

The modeling of the MOSFET part is the same as that in [15]. In terms of the hole current source part, it is determined by the excess carrier distribution in the device. The excess carriers in the N-channel region will decrease to approximately zero when the collector-emitter voltage increases above approximately 50 V for a typical IEGT with a voltage rating of 4500 V. Therefore, at the beginning of the switching transient, the width of the N-channel $D_g - W_d$ decreases to zero, and the 2D effects are eliminated [24]. The one-dimensional approximate analytical solution for the N-base carrier distribution during turn-off shown in [19] is adopted in this paper. Combining the carrier distribution and current transport equation shown in (2), the hole current can be obtained.

According to the analysis shown in section II about the turn-off process of an IEGT in DC circuit breaker applications, the nonlinear capacitances between device terminals have a great impact on the increase rate of the collector-emitter voltage during the turn-off process, and the calculations of the nonlinear capacitances are the emphases of the model [33], [38]. Considering the difference in the gate structure between IEGTs and IGBTs, the nonlinear capacitances between terminals are greatly improved as shown below.

IEGTs have a deeper and wider gate structure than that of IGBTs, which brings about the difference in the modeling of the capacitance C_{gd} between the gate and drain terminals during the turn-off process shown in Fig. 3(a), where W_d is less than D_g.

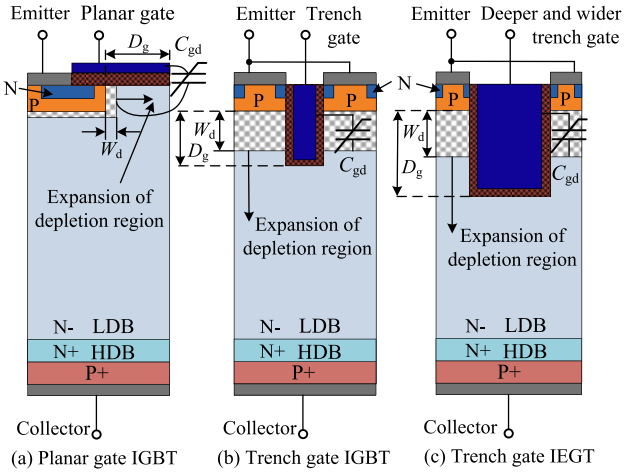


FIGURE 10. Diagram of changes in capacitance C_{gd} in the turn-off process ($W_d < D_g$).

Fig. 10 shows the changes in the capacitance C_{gd} for different gate structures with $W_d < D_g$. The capacitance C_{gd} between the gate and drain terminals consists of an oxide capacitance C_{oxd} and a depletion region capacitance C_{gdj} in series. That is,

$$C_{gd} = C_{oxd}C_{gdj}/\left(C_{oxd} + C_{gdj}\right). \tag{8}$$

Strictly speaking, considering that an IEGT has a wider and deeper trench gate, the effective oxide capacitances C_{oxd} and C_{gdj} will both change with changing contact area between the depletion layer boundary and oxide layer for $W_d < D_g$. In addition, the two capacitances are closely related to the gate structure, but the structure of the trench gate is complex and not regular in shape, resulting from the chip manufacturing process [39], which brings difficulties for calculating C_{gd} precisely.

For the planar and trench gate IGBTs shown in Fig. 10(a) and (b), the width W_d is small, and C_{gdj} is much larger than C_{oxd}. Therefore, according to (8), the value of C_{gd} is mainly determined by C_{oxd}. Although C_{gdj} will decrease with increasing W_d, the change in W_d is limited and small for $W_d < D_g$ owing to the short gate. C_{gd} approximately equals C_{oxd} when W_d is less than D_g for the IGBT. Many IGBT circuit models, for example, the Hefner model, employ this approximate method to calculate C_{oxd} for $W_d < D_g$. However, this approximate calculation method is not applicable to IEGTs. The trench gate IEGT shown in Fig. 10(c) has a wider and deeper trench gate than that of the trench IGBT. The increase in the gate structure size will lead to a definite increase in C_{oxd} and result in a larger decrease in C_{gdj} with expansion of the depletion region. The capacitance C_{gd} is determined by both C_{oxd} and C_{gdj}, and an increase in W_d can result in a larger change in C_{gd}, which can be seen in Fig. 16(b) in the appendix. Therefore, the nonlinear capacitance C_{gd0} is proposed in this paper to describe this feature of an IEGT.

Based on the analysis, the capacitance C_{gd} is given as

$$C_{gd} = \begin{cases} C_{gd0} & u_{ce} \le U_{Td} \\ C_{oxd}C_{gdj}/\left(C_{oxd} + C_{gdj}\right) & u_{ce} > U_{Td}, \end{cases} \quad (9)$$

where U_{Td} is the threshold voltage when $W_d = D_g$.

As described above, the irregular gate shape and the change in the contact area between the depletion layer boundary and oxide layer bring difficulties for calculating C_{gd} precisely. This paper proposes an experimental method for extracting it, and the details are shown in the following.

Based on the typical current and voltage waveforms shown in Fig. 7, when voltage u_{ce} is smaller than the clamped voltage, current i_{ce} and gate voltage u_{ge} remain constant. Gate current i_g equals the current i_{gd} due to the Miller effect. Therefore, the capacitance C_{gd0} can be obtained by

$$C_{gd0}\left(u_{gd}\right) = \frac{\mathrm{d}}{\mathrm{d}\left(u_{ce} - u_{ge} - U_k\right)} \int_{m_1}^{m_2} i_g\left(t\right) \mathrm{d}t, \quad (10)$$

where U_k is used again to describe the voltage drop across the equivalent PIN diode in the device.

The nonlinear capacitance C_{gdj} is [15]

$$C_{gdj} = A_{gd}\varepsilon / W_{gdj}, \quad (11)$$

where ε is the dielectric constant of silicon; A_{gd} is the gate-drain overlap area; and W_{gdj} is the width of the depletion region between the gate and drain and is calculated as follows:

$$W_{gdj} = W_d - \sqrt{2\varepsilon U_{Td}/q/N_L}, \quad (12)$$

where N_L is the doping concentrations in the low doped base (LDB) region.

Based on Gauss's law, the electrostatic field distribution in the depletion region can be easily obtained. Then, by integrating the electric field in the depletion layer, the width W_d under different voltages u_{ce} is obtained as follows:

If $u_{ce} \le U_{Td}$,

$$W_d = \sqrt{2u_{ce}\varepsilon/\left(qN_L\right)}. \quad (13)$$

If $U_{Td} < u_{ce} \le U_{rt}$,

$$W_d = \sqrt{\frac{A^2 - A_{ds}^2}{A_{ds}^2}\frac{2\varepsilon U_{Td}}{qN_L} + \frac{2\varepsilon u_{ce}}{qN_L}} + \frac{A - A_{ds}}{A_{ds}}\sqrt{\frac{2\varepsilon U_{Td}}{qN_L}}, \quad (14)$$

where A is the device active area; $A_{ds} = A - A_{gd}$; and U_{rt} is the corresponding voltage when the depletion region expands to the high doped base (HDB) region.

If $u_{ce} > U_{rt}$,

$$W_d = \sqrt{\begin{array}{l}\left(W_L + \dfrac{A}{A_{ds}}\sqrt{\dfrac{2\varepsilon}{qN_L}U_{Td}}\right)^2 \\ - \left(\dfrac{2AW_LN_L}{N_HA_{ds}}\sqrt{\dfrac{2\varepsilon}{qN_L}U_{Td}} \right. \\ \left. + \dfrac{N_LW_L^2}{N_H} - \dfrac{2\varepsilon}{qN_H}\left(u_{ce} - U_{Td}\right)\right)\end{array}} - \frac{A}{A_{ds}}\sqrt{\frac{2\varepsilon}{qN_L}U_{Td}}, \quad (15)$$

where N_H is the doping concentrations in the HDB region; W_L is the width of the LDB region.

The corresponding voltage U_{rt} when the depletion region extends to the HDB region is

$$U_{rt} = \frac{qN_L}{2\varepsilon}\left(W_L + \frac{A - A_{ds}}{A_{ds}}\sqrt{\frac{2\varepsilon}{qN_L}U_{Td}}\right)^2 - \frac{A^2 - A_{ds}^2}{A_{ds}^2}U_{Td}. \quad (16)$$

The nonlinear capacitance C_{dsj} is [15]

$$C_{dsj} = A_{ds}\varepsilon / W_d. \quad (17)$$

The related parameters in the proposed equations can be obtained following the corresponding methods in [40]–[42].

IV. EXPERIMENTS AND MODEL VERIFICATION

Based on experiments, the correctness of the proposed model is verified from two aspects: the static-state output characteristics and the high current turn-off transient process.

A. ESTABLISHMENT OF THE TEST PLATFORM

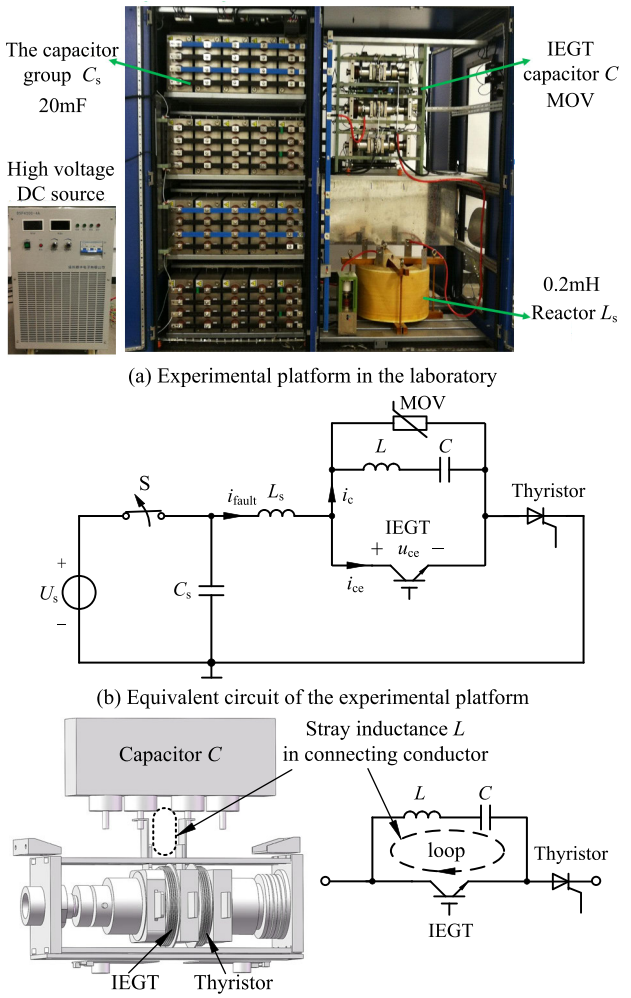
Based on the working conditions of the DC circuit breaker shown above and the equivalent circuit shown in Fig. 1(b), we establish an experimental platform, shown in Fig. 11(a). Fig. 11(b) displays the equivalent circuit of the experimental platform, and Fig. 11(c) shows the IEGT and parallel capacitor.

The selected type of IEGT is a TOSHIBA ST2100GXH24A, which has the maximum breakdown voltage tolerance and conduction current among all available commercial IEGTs. The C and L in Fig. 11(b) and (c) are the same as those in Fig. 1(b). The stray inductance L in the experiment is extracted using ANSYS Q3D Extractor, $L = 150$ nH. The value of the parallel capacitance C is 220 μF.

In the experimental platform, $C_s = 20$ mF, $L_s = 0.2$ mH, and the thyristor is the main circuit switch and is used to prevent the capacitor C from being charged before the IEGT conducts the current. First, the capacitor C_s is charged by a high voltage DC source, and then, the breaker S turns off. Next, the IEGT and thyristor turn on, and fault current i_{fault} is generated by the resonance of C_s and L_s. The resonant period is approximately 12 ms, and the peak value of the resonant current is approximately ten times the charge voltage U_s. Referring to [3], the duration of the fault current conduction in the IEGT is approximately 3 ms. Therefore, the IEGT conducts the fault current for 3 ms and then turns off in the experiment. The turn-on and turn-off driving voltages are 15 V and −9 V in a hard switching mode. Meanwhile, a Tektronix MDO3034 digital oscilloscope, a PEM CWT 300 current probe and a Tektronix THDP0110 high voltage differential probe are applied for data acquisition.

B. VERIFICATION OF THE OUTPUT CHARACTERISTICS OF THE MODEL

The static-state output characteristics are the basis for analyzing the conduction losses and the desaturation current values



(a) Experimental platform in the laboratory

(b) Equivalent circuit of the experimental platform

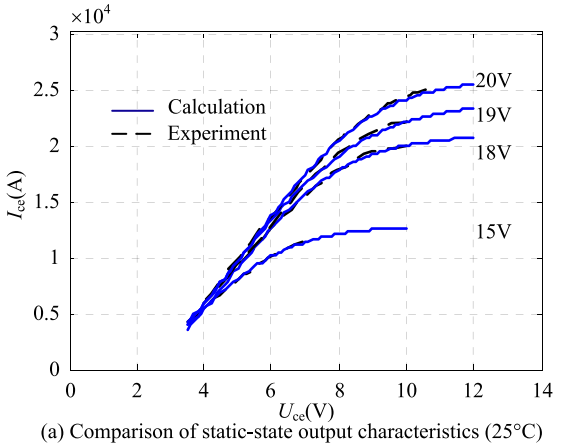
(1) 3D assembly drawing (2) Equivalent circuit

(c) 3D assembly drawing and equivalent circuit of the IEGT and capacitor

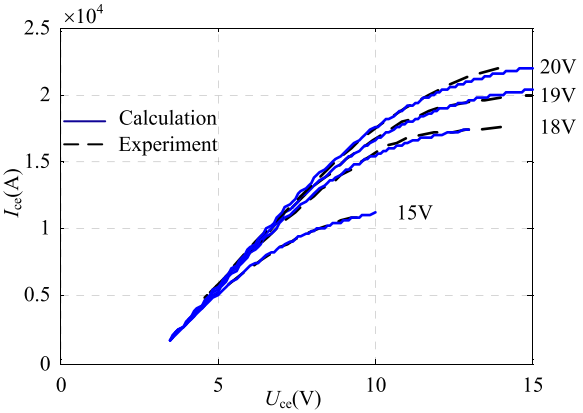
FIGURE 11. Experimental platform and equivalent circuit.

at different driving voltages. Fig. 12 compares the static-state I-U curve obtained by the model (blue solid lines) with the data measured in the lab (black dashed lines) at temperatures of 25°C and 125°C. A good agreement can be obtained, especially in the near desaturation region where the IEGT is normally operated under the working conditions of a DC circuit breaker. Therefore, the analysis of the change laws of the voltage drops and hole/electron currents in the IEGT is proved to be correct, and the accuracy of the proposed simple model is verified.

Fig. 13 shows a comparison of transfer characteristic curves when voltage U_{ce} is 20 V. The agreement between the calculation and experimental results verifies the accuracy of the proposed method. By calculating the derivative of current I_{ce} with respect to voltage U_{ge}, we obtain that the transconductance g_{fs} of the IEGT can be above 1300 S when the conduction current is above 5000 A. And Fig. 13 shows that the maximum saturation current is above 20 kA, which proves the good high current conduction ability and advantages of the IEGT in DC circuit breaker applications.



(a) Comparison of static-state output characteristics (25°C)



(b) Comparison of static-state output characteristics (125°C)

FIGURE 12. Comparison of static-state output characteristics.

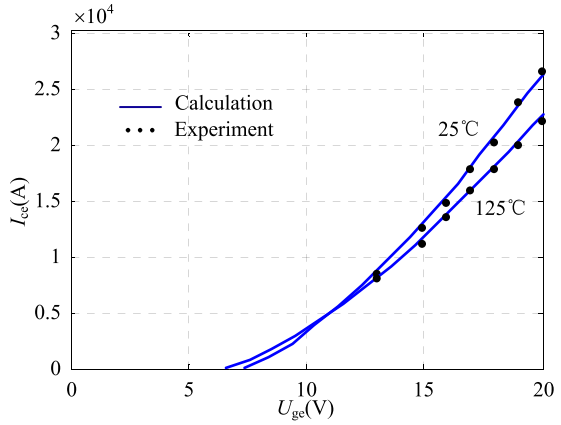


FIGURE 13. Comparison of transfer characteristics (U_{ce} = 20 V).

C. VERIFICATION OF THE TURN-OFF TRANSIENT MODEL

To further verify the turn-off dynamic transient model, this paper calculates the turn-off transient collector-emitter voltage and collector current based on the proposed model and Newton–Raphson method.

Fig. 14 shows the turn-off transient voltage and current waveform comparison when the breaking current is 3863 A and the turn-off driving resistance is 15 Ω/33 Ω/51 Ω.

According to the comparison shown in Fig. 14, good agreement can be obtained between the simulation and measurement waveforms. The proposed model can accurately describe the influence of the turn-off driving resistance on the turn-off process. That is, with increasing turn-off driving resistance, the duration of the turn-off process increases (50 μs > 33 μs > 17 μs) and the voltage overshoot formed during the turn-off process decreases (220 V < 310 V < 430 V). The experimental results verify the correctness of the transient model.

Table 1 shows the comparison of the turn-off loss results. According to Table 1, the maximum difference between the measured and calculated turn-off losses is 6.4%. Therefore, the model meets the engineering requirements.

TABLE 1. Comparison of turn-off losses.

$R_{off}(\Omega)$	15		33		51	
	Exp.	Simulation	Exp.	Simulation	Exp.	Simulation
W(J)	1.72	1.83	3.39	3.26	5.43	5.77
Error(%)	6.4		3.8		6.3	

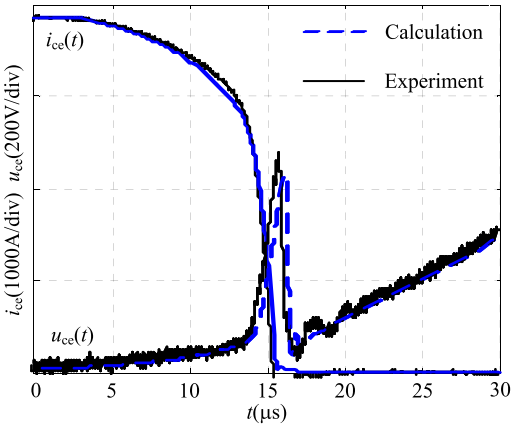
The Hefner model of an IGBT is a relatively mature mechanism model [15] that can comprehensively describe the electrical/thermal characteristics and damage mechanism of an IGBT. It has been successfully applied in the software PSpice and Saber. Therefore, for making a comparison, the Hefner model is used to calculate the collector-emitter voltage and collector current. Fig. 15 compares the voltage and current waveforms when the breaking current is 4240 A/8455 A/11570 A and the turn-off gate resistance is 15 Ω.

It can be seen from Fig. 15 that the voltage and current waveforms of the proposed model are closer to the measured waveforms than those of the Hefner model. Therefore, the proposed model can well describe the high current turn-off characteristics under different breaking currents.

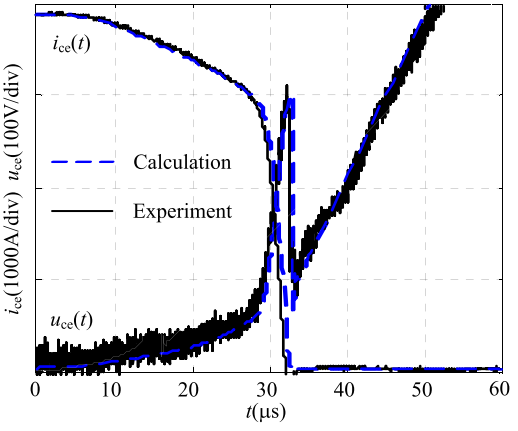
Admittedly, the differences between the proposed IEGT model and Hefner model do not lie in just a single aspect, and the factors affecting the model accuracy are complex. As mentioned above, the equivalent circuit shown in Fig. 9 can be divided into three main parts: the MOSFET part, the capacitances between device terminals part and the hole current source part. Focusing on the three parts, the accuracy of the proposed model is analyzed qualitatively as follows.

The modeling for the MOSFET part is the same for the proposed model and Hefner model, and the differences between the two models lie in the other two aspects: the capacitances between device terminals part and the hole current source part. In addition, the hole current source is determined by the distribution of N-base excess carriers.

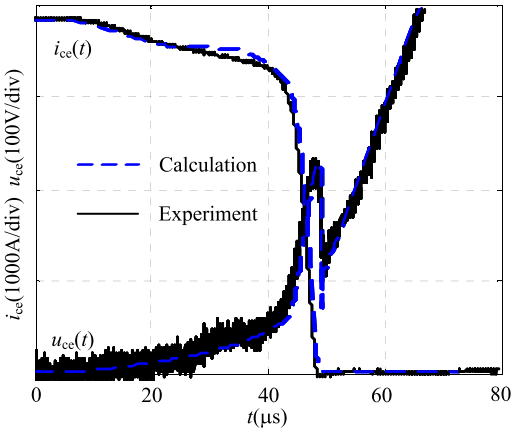
Taking Fig. 15(a) as an example, the device starts and completes the turn-off process at t_1 and t_4, respectively, and the different stages in the turn-off process are exactly the same as in Fig. 2(b). According to the analysis of the main influencing factors in different stages in section II, the waveforms



(a) Comparison of turn-off transient waveforms (R_{off}=15 Ω)



(b) Comparison of turn-off transient waveforms (R_{off}=33 Ω)

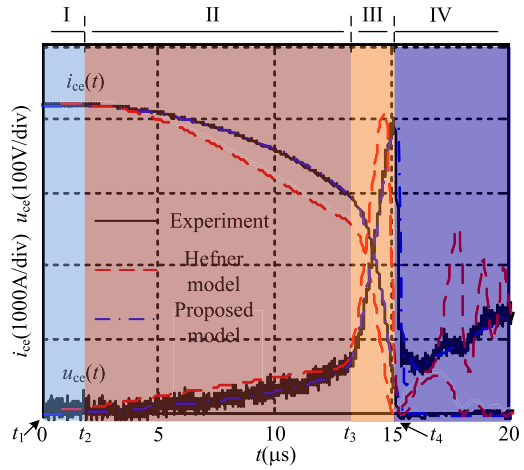


(c) Comparison of turn-off transient waveforms (R_{off}=51 Ω)

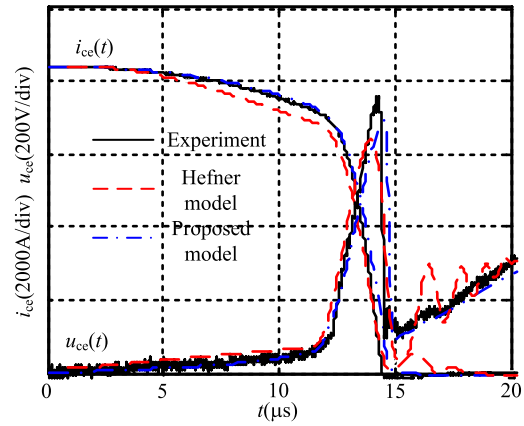
FIGURE 14. Comparison of turn-off transient current and voltage waveforms under different driving resistances (I_{break} = 3863 A).

in stages II/III and stage IV can qualitatively reflect the calculation accuracy of the nonlinear capacitances and the distribution of N-base excess carriers, respectively.

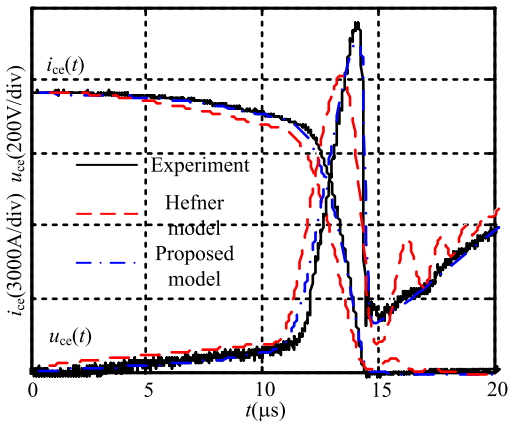
The voltage u_{ce} in stages II and III increases with the expansion of the depletion region, and the increase rate of voltage u_{ce} is mainly determined by the expansion speed of the depletion region [31]. The expansion of the depletion region is reflected by the nonlinear capacitances between



(a) Comparison of turn-off transient waveforms (I_{break}=4240 A)



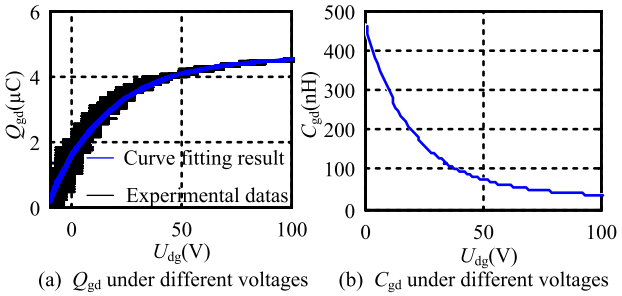
(b) Comparison of turn-off transient waveforms (I_{break}=8455 A)



(c) Comparison of turn-off transient waveforms (I_{break}=11570 A)

FIGURE 15. Comparison of turn-off transient current and voltage waveforms under different breaking currents.

device terminals in the model. The depletion region expansion means charging of the capacitances, and the expansion speed of the depletion region is determined by the values of the capacitances. Therefore, the higher calculation accuracy of the proposed model for the voltage u_{ce} and current i_{ce} in stages II and III indicates that improving the nonlinear capacitances in the model proves to be necessary and effective.



(a) Q_{gd} under different voltages (b) C_{gd} under different voltages

FIGURE 16. Charge Q_{gd} and capacitance C_{gd} under different gate-drain voltages.

The stage IV part of Fig. 15(a) shows the waveforms after the device completes the turn-off process. It is universally known that the variation characteristics of current i_{ce} near zero are closely related to the N-base excess carriers. If few or no N-base excess carriers remain when current i_{ce} is close to zero, then the current oscillation phenomenon will occur easily [8]. In contrast, a large number of remaining excess carriers will result in a tail current. The experimental results in Fig. 14 show that the current oscillation phenomenon is not obvious. Therefore, the current oscillation phenomenon predicted by the Hefner model in stage IV in Fig. 15 indicates that the modeling of the excess carrier distribution is not accurate. The agreement between the proposed model and measured results validates the reasonability and accuracy of the calculations for the N-base excess carrier distribution. Table 2 shows a comparison of the measured and simulated turn-off losses.

TABLE 2. Comparison of turn-off losses.

I_{break}(A)	4240			8455			11570		
	Exp.	IEGT	Hefner	Exp.	IEGT	Hefner	Exp.	IEGT	Hefner
W(J)	1.91	1.84	2.25	6.35	6.52	7.53	13.85	13.48	15.53
Error(%)	-	3.7	17.8	-	2.6	18.6	-	2.7	12.1

As seen in Table 2, the turn-off loss differences between the experiment and proposed model are within 5%, while the Hefner model results in a large error (above 10%) for the measured turn-off losses. Therefore, the proposed model can well describe the turn-off characteristics of the IEGT.

In summary, the simulated results of both the static-state I-U characteristic curve and dynamic turn-off transient process agree well with the test results. Hence, the proposed model can accurately describe the high current turn-off characteristics of an IEGT under the working conditions of a DC circuit breaker, and it is suitable for engineering applications.

V. CONCLUSION

To analyze the high current turn-off characteristics of IEGTs in high voltage DC circuit breaker applications, an IEGT model is proposed in this paper. The model contains two innovations.

TABLE 3. Parameters used in proposed model of ST2100GXH24A.

Parameters	Values	Parameters	Values	Parameters	Values
W_H(cm)	0.0004	β(25 °C)	593.8	C_{gs}(nF)	220
N_H(cm^{-3})	2.0×10^{17}	β(125 °C)	575.7	C_{oxd}(nF)	420
W_L(cm)	0.0205	γ(25 °C)	1.46	I_{sne}(A)	1.88×10^{-13}
N_L(cm^{-3})	7.5×10^{13}	γ(125 °C)	1.41	τ_L(μs)	2
U_{Td}(V)	50	U_k(V/25 °C)	2.3	τ_H(μs)	0.1
A(cm^2)	30	U_k(V/125°C)	2.7	A_{gd}(cm^2)	24
U_T(V/25 °C)	7.5	U_T(V/125 °C)	6.7		

First, (1) The on-state voltage drop across the equivalent PIN diode in the IEGT approximately remains constant for a large conduction current density, which is consistent with DC circuit breaker applications. (2) The relation of electron injection efficiency α and conduction current density J_{ce} is nonlinear for an IEGT. (3) The equivalent MOSFET part in the device and the IEGT itself start to work in the desaturation state at the same time with increasing conduction current. Based on the above laws, a simple method for modeling the static-state output characteristics is proposed. The proposed simple method is suitable for analyzing the conduction losses and predicting desaturation currents especially under large driving voltages, which are exactly the device characteristics of concern in DC circuit breaker engineering.

Second, an IEGT has a deeper and wider gate structure than that of an IGBT. As a result, in the turn-off process, the nonlinear capacitance C_{gd} between gate and collector terminals will show large changes when the width of the depletion region W_d is less than the distance from the bottom of the trench gate to the P-base D_g, while the capacitance C_{gd} shows a relatively small change or even remains approximately constant for an IGBT under the same conditions. Based on this conclusion, the nonlinear capacitances between terminals are greatly improved to better describe the transient turn-off process.

The model shows good agreement in the static-state output characteristics and the dynamic behavior during turn-off between the experimental and simulated results. This successful validation indicates that this model can be a convenient tool for analyzing the high current turn-off characteristics of IEGTs in DC circuit breaker applications.

APPENDIX

The parameters used in the model of ST2100GXH24A are listed in Table 3. Fig. 16(a) shows the extracted charge Q_{gd} under different gate-drain voltages u_{gd}. Based on the curve fitting results and (20), the extracted results can be obtained as in Fig. 16(b), and the curve fitting result for C_{gd0} is

$$C_{gd0}\left(u_{gd}\right) = 392e^{-0.05797u_{gd}} + 72e^{-0.007u_{gd}}. \quad \text{(A1)}$$

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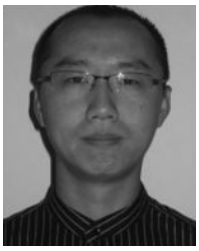

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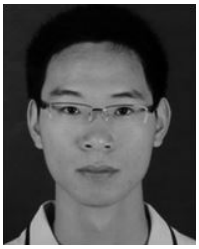

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