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Three-Phase Embedded Modified-Z-Source Three-Level T-Type Inverters

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ABSTRACT Two topologies are designed by combining a modified-Z-source (MZS) network consisting of three diodes, two inductors and four capacitors to a traditional three-level T-type inverter (3LTI), and embedding either one or two dc sources in the impedance network, which are named as asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI). The proposed topologies provide a highly boosted ac output voltage with five voltage levels and ensure a continuous dc source current by adopting the embedded concept. Operating analysis is performed and a comparison of the two proposed topologies with five different topologies combining the impedance network and 3LTI or neutral-point-clamped (NPC) inverter is provided. A novel modulation technique is proposed for effectively controlling the upper and lower shoot-through states with a simple logic circuit and balancing a neutral-point voltage. The validity of the proposed topologies and the modulation technique is demonstrated through simulation and experimental results.

INDEX TERMS Boost capability, embedded dc source, Z-source impedance network, modulation technique, three-level T-type inverter (3LTI).

I. INTRODUCTION

Nowadays, multilevel inverters have been widely employed in various industrial applications such as medium-voltage ac motor drives [1] and wind turbine or photovoltaic (PV) generation systems [2], [3]. Compared to conventional two-level inverters, multilevel inverters can provide a staircase output waveform with lower total harmonic distortion (THD) and decrease the voltage stress on inverter power semiconductor switches. Among the various multilevel topologies, some popular selections include the neutral-point-clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB) [4], [5]. The three-level T-type inverter (3LTI), a relatively recent three-level inverter topology, is implemented by connecting active bidirectional switches between the dc-link midpoint and three-phase outputs of the conventional two-level inverter [6]–[15]. Compared to the three-phase three-level NPC inverter, 3LTI can provide lower conduction losses and fewer diodes while retaining the benefit of the three-level inverter such as the stepped output voltage waveform. In [6] and [7], the switching and conduction losses of 3LTI for low-voltage applications were analyzed and compared to a three-level NPC inverter or two-level inverter. The fault-tolerant control strategies for a 3LTI under an open-circuit fault condition are proposed by measuring the bridge voltage or neutral-point voltage [8]–[11]. The 3LTI can be applied in various industrial applications such as photovoltaic (PV) generation [12], permanent-magnet synchronous motor (PMSM) drives [13], [14], and energy storage systems [15].

However, 3LTI and the three highly popular topologies perform only a buck dc-ac voltage conversion because they are unable to output ac voltage greater than the dc source voltage. Some applications like renewal energy generation with a low voltage renewal energy source demand 3LTIs with higher voltage gain to obtain a desired ac output voltage. To enhance the voltage boosting ability with a single power conversion stage, the concept of the (quasi-)Z-source impedance network is introduced to the 3LTI. The Z-source inverter (ZSI) or quasi-Z-source inverter (qZSI) can raise the dc-link voltage by shorting any phase leg of the inverter [16]–[18], which can achieve a buck-boost operation with a single

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power conversion stage. The reliability is improved because dead-time of the inverter can be avoided due to the possible shoot-through state.

Several topologies integrating the (quasi-)Z-source impedance network to the 3LTI have been proposed to attain the benefits of (q)ZSI as well as those of 3LTI. The topology and modulation method for the three-phase or single-phase Z-source three-level T-type inverters (ZS-3LT^{2}Is), which are implemented by combining a single Z-source impedance and three- or single-phase 3LTI, are described in [19], [20]. These inverters have a discontinuous dc source current. The space vector modulation scheme and carrier level shifted modulation method of the quasi-Z-source 3LTI (qZS-3LT^{2}I) topology realized by combining two symmetrical quasi-Z-source networks and three-phase 3LTI are proposed to reduce the common-mode voltage by balancing the neutral-point voltage [21]–[23]. The normal operation behavior and open-loop failure condition of the qZS-3LT^{2}I are studied in [24]. An efficiency study to compare the qZS-3LT^{2}I and qZS-NPC inverter was realized by simulation [25]. The qZS-3LT^{2}I has a continuous source current. However, it requires a large number of passive components that results in increased weight, volume, and cost of the power converter. Although both the ZS-3LT^{2}I and qZS-3LT^{2}I have a boost capability, their boost factor is not high.

To improve the boost capability while reducing the number of passive components, the three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I) topology was introduced in [26]–[28]. The 3L-qSBT^{2}I topology is designed by replacing the quasi-Z-source impedance network in qZS-3LT^{2}I with the quasi-switched boost network proposed in [29], [30]. The 3L-qSBT^{2}I can provide a high voltage gain and reduce the number of passive components. However, it requires two additional switching devices and its modulation technique is complex. An active impedance-source 3LTI with reduced component count (RC^2-AIS-3LTI) topology has been introduced to reduce the number of active and passive switches [31], which can save two diodes and one active switch compared to the 3L-qSBT^{2}I.

In this paper, three-phase embedded modified-Z-source three-level T-type inverter topologies are proposed. The proposed topologies are designed by attaching the single modified-Z-source (MZS) impedance network proposed in [32], [33] to 3LTI, and embedding either one or two dc sources at the MZS network, which are named asymmetrical embedded MZS-3LTI (AEMZS-3LTI) and symmetrical embedded MZS-3LTI (SEMZS-3LTI), respectively. They can improve the boost ability and ensure a continuous dc source current without an extra capacitor or filter by employing the embedded concept. The operations for the shoot-through and non-shoot-through states of both the AEMZS-3LTI and SEMZS-3LTI are analyzed. A novel modulation technique based on an alternative phase opposition disposition (APOD) for the proposed topologies is proposed to produce boosted ac output voltage with five voltage steps and achieve a neutral-point voltage balance by balancing the two series capacitor voltages. The performance of the proposed topologies and modulation technique is demonstrated through simulation and experimental results.

II. OPERATION ANALYSIS OF ASYMMETICAL AND SYMMETRICAL EMZS-3LTIs

The operation analysis for the proposed AEMZS-3LTI and SEMZS-3LTI topologies was performed with the assumption that all components adopted at the proposed topologies are ideal for simplification. Fig. 1 shows the structures of the proposed AEMZS-3LTI and SEMZS-3LTI topologies. The AEMZS-3LTI topology shown in Fig. 1(a) is designed by combining the MZS network [32], [33] and 3LTI, and placing a single dc source in series with the inductor L_1 of the upper cell in the impedance network [34]. The SEMZS-3LTI topology shown in Fig. 1(b) is implemented by combining the MZS network and 3LTI, and placing two dc sources V_{dc1} and V_{dc2} at the upper and lower cells in the MZS network, respectively. Therefore, a continuous dc source current can be achieved without any additional filters or capacitors. The MZS network contains three diodes, two inductors, and four capacitors. Three-phase bidirectional active switches are connected between the mid-point of two series capacitors C_1 and C_2 and the three-phase output bridges of the two-level inverter.

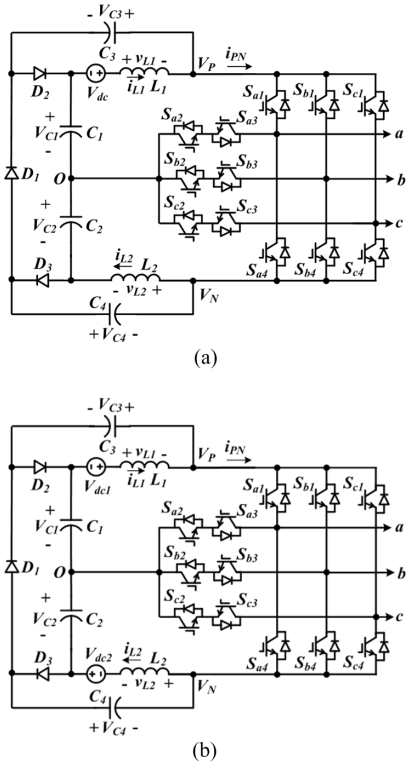

FIGURE 1. Proposed three-phase embedded modified-Z-source three-level T-source inverters: (a) AEMZS-3LTI topology, (b) SEMZS-3LTI topology.

The proposed topologies, like traditional ZSI, have two operating states: the shoot-through (ST) state and the non-shoot-through (NST) state. There are three types of

shoot-through states available for the proposed topologies, including a full shoot-through (FST) state, an upper shoot-through (UST) state and a lower shoot-through (LST) state. The FST state can be accessed by switching on the upper and lower switches in any phase leg. Zero output voltage during the FST state results in a distorted ac output voltage. Both the UST and LST states can be achieved by switching on the upper or lower switch while connecting the dc-link mid-point and output bridge. Because the output voltage can be generated during both the UST and LST states, the quality of the output voltage waveform is improved.

The steady-state operations of the two proposed topologies are analyzed through their equivalents circuits.

A. OPERATING PRINCIPLES OF AEMZS-3LTI

The steady-state operating principle of the AEMZS-3LTI is explained, assuming $V_{C1} = V_{C4}$ and $V_{C2} = V_{C3}$ due to symmetry of the MZS network [34].

1) SHOOT-THROUGH STATE

In the UST state shown in Fig. 2(a), the short circuit condition of the upper impedance cell can be accessed by turning on switches S_{1x}, S_{2x}, and S_{3x} ($x = a$, b, or c). The diodes D_1 and D_3 are conducting, whereas diode D_2 is blocking. Both the dc input source and capacitor C_1 deliver energy to the inductor L_1. Both the inductor L_2 and capacitor C_3 supply energy to the load side. The voltages across two inductors and dc-link voltage are given by

$$v_{L1} = V_{dc} + V_{C1}, \quad v_{L2} = -V_{C4} \tag{1}$$

$$V_{PN} = V_{C2} + V_{C4}. \tag{2}$$

In the LST state shown in Fig. 2(b), the short circuit condition of the lower impedance cell can be instigated by turning on switches S_{2x}, S_{3x}, and S_{4x} ($x = a$, b, or c). The diodes D_1 and D_2 are conducting, whereas diode D_3 is blocking. The inductor L_2 charges the energy from the capacitor C_2. The dc input source V_{dc1}, the inductor L_1, and capacitor C_4 supply energy to the ac load side. The voltages across two inductors and dc-link voltage are given by

$$v_{L1} = V_{dc} - V_{C3}, \quad v_{L2} = V_{C2} \tag{3}$$

$$V_{PN} = V_{C1} + V_{C3}. \tag{4}$$

2) NON-SHOOT-THROUGH STATE

Fig. 2(c) shows the equivalent circuit of the NST state, which is divided into an active state and a zero state. The AEMZS-3LTI operates like the traditional 3LTI. The diodes D_2 and D_3 are conducting, whereas diode D_1 is blocking. In the active state, the switches S_{1x} and S_{2x} are turned on at the positive x-phase reference signal, and the switches S_{3x} and S_{4x} are turned on at the negative x-phase reference signal. The voltages across inductors and dc-link voltage are given by

$$v_{L1} = V_{dc} - V_{C3}, \quad v_{L2} = -V_{C4} \tag{5}$$

$$V_{PN} = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \hat{V}_{PN}. \tag{6}$$

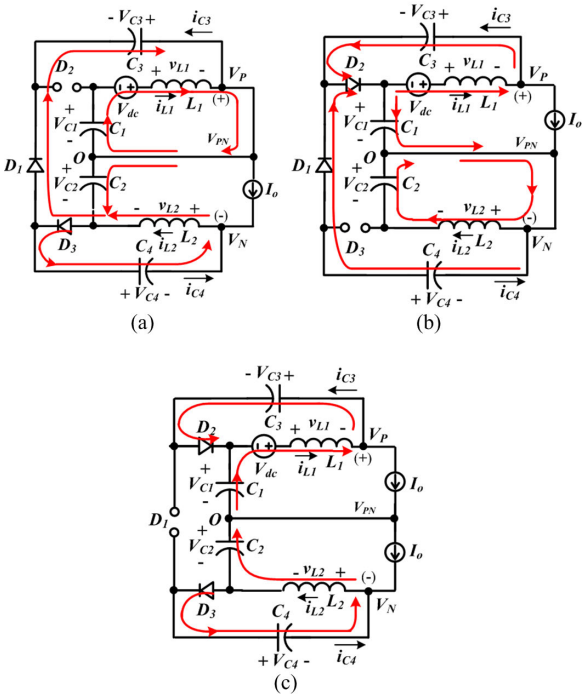

FIGURE 2. Equivalent circuits for the three-phase AEMZS-3LTI: (a) UST state, (b) LST state, (c) NST state.

The dc-link voltage in the active state, which is a peak voltage, can be established by adding four capacitor voltages. When only S_{2x} and S_{3x} are turned on, the AEMZS-3LTI operates in the zero state and the output voltage becomes zero due to the dc-link open circuit.

3) BOOST FACTOR

The average values of the UST and LST periods are the same over one period of the inverter frequency due to symmetrical operation of the modulation technique. Therefore, the period of UST and LST is represented as T_{ST}.

By utilizing the volt-second balance principle on the inductors (L_1 and L_2) from (1), (3), and (5) over one switching period T, the four capacitor voltages are expressed as a function of the shoot-through duty ratio D, which is defined as $D = T_{ST}/T$.

$$V_{C1} = V_{C4} = \frac{D}{1-2D} V_{dc}, \quad V_{C2} = V_{C3} = \frac{1-D}{1-2D} V_{dc} \tag{7}$$

The voltage across capacitors C_1 and C_4 is lower than the voltage across capacitors C_2 and C_3 by the value of the dc input voltage due to embedding the dc source at the upper impedance cell. By substituting (7) into (6), the boost factor B, defined as the ratio of the peak dc-link voltage to the dc input voltage, is given by

$$B = \frac{\hat{V}_{PN}}{V_{dc}} = \frac{2}{1-2D}. \tag{8}$$

B. OPERATING PRINCIPLES OF SEMZS-3LTI

The steady-state operating principle of the SEMZS-3LTI is explained, assuming $V_{C1} = V_{C2} = V_{C3} = V_{C4}$ due to

symmetry of the impedance network. The equivalent circuits for the three-phase SEMZS-3LTI in the two shoot-through states and non-shoot-through state are shown in Fig. 3. The on/off switching devices and dc-link voltage of the SEMZS-3LTI topology are the same as those of the AEMZS-3LTI topology in all of the three operating states.

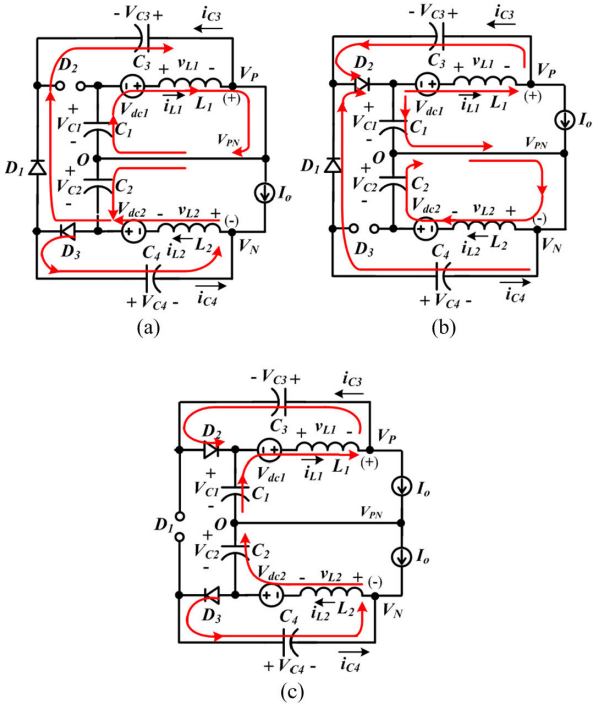

FIGURE 3. Equivalent circuits for the three-phase SEMZS-3LTI: (a) UST state, (b) LST state, (c) NST state.

1) SHOOT-THROUGH STATE

In the UST state shown in Fig. 3(a), both the dc input source V_{dc1} and capacitor C_1 delivery energy to the inductor L_1. The dc input source V_{dc2}, inductor L_2, and capacitor C_3 supply energy to the ac load side. The capacitors C_2 and C_4 are charged. The voltages across two inductors and the capacitor currents can be written by

$$v_{L1} = V_{dc1} + V_{C1}, v_{L2} = V_{dc2} - V_{C4} \tag{9}$$

$$i_{C4} = i_{L2} - I_O, i_{C2} + i_{C3} = i_{C4} - i_{L2} = -I_O \tag{10}$$

In the LST state shown in Fig. 3(b), both the dc input source V_{dc2} and capacitor C_2 deliver energy to the inductor L_2. The dc input source V_{dc1}, inductor L_1, and capacitor C_4 supply energy to the ac load side. The capacitors C_1 and C_3 are charged. The voltages across two inductors and the capacitor currents can be written by

$$v_{L1} = V_{dc1} - V_{C3}, \; v_{L2} = V_{dc2} + V_{C2} \tag{11}$$

$$i_{C2} = -i_{L2}, \; i_{C3} = i_{L1} - I_O. \tag{12}$$

2) NON-SHOOT-THROUGH STATE

Fig. 3(c) shows the equivalent circuit of the NST state. In the active state, the switching states for the x-phase four switching devices are dependent on the polarity of the x-phase reference signal dc-link voltage is a peak dc-link voltage as in the AEMZS-3LTI topology. The voltages across inductors and the capacitor currents are given by

$$v_{L1} = V_{dc1} - V_{C3}, \; v_{L2} = V_{dc2} - V_{C4} \tag{13}$$

$$i_{C1} = i_{C2} = -I_O, \; i_{C3} = i_{L1} - I_O. \tag{14}$$

3) BOOST FACTOR

By utilizing the volt-second balance principle on inductors (L_1 and L_2) from (9), (11), and (13) over one switching period T, assuming $V_{dc1} = V_{dc2} = V_{dc}$, the four capacitor voltages are expressed as a function of D as follows:

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{1}{1-2D} V_{dc} \tag{15}$$

By applying the charge-second balance principle to capacitors C_2 and C_3 from (10), (12), and (14) over one switching period T, assuming $i_{L1} = i_{L2}$, the averages of two inductor currents are expressed as

$$\bar{i}_{L1} = \bar{i}_{L2} = \frac{2(1-D)}{1-2D} I_o. \tag{16}$$

By substituting (15) into (6), the boost factor is given by

$$B = \frac{\hat{V}_{PN}}{V_{dc1} + V_{dc2}} = \frac{\hat{V}_{PN}}{2V_{dc}} = \frac{2}{1-2D}. \tag{17}$$

The boost factor of the SEMZS-3LTI topology is the same as that of the AEMZS-3LTI topology.

C. OPERATION OF TWO TOPOLOGIES WITHOUT THE SHOOT-THROUGH STATE

The operation of the two proposed topologies when a shoot-through duty ratio $D = 0$ is different from the operation in the NST state. Therefore, the four capacitor voltages derived as (7) and (15) are not valid when $D = 0$ because the two topologies do not have a shoot-through state. Fig. 4 shows the equivalent circuits for the two proposed topologies when $D = 0$. Three diodes D_1, D_2 and D_3 are conducting and the switching states for all of switches of the 3LTI are the same as those in the NST state.

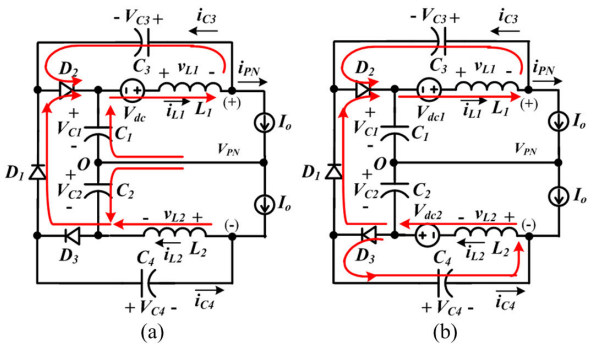

FIGURE 4. Equivalent circuits for two proposed topologies when $D = 0$: (a) AEMZS-3LTI, (b) SEMZS-3LTI.

Based on Fig. 4(a), four capacitor voltages and the dc-link voltage of the AEMZS-3LTI are given by

$$V_{C1} = -\frac{V_{dc}}{2}, V_{C2} = \frac{V_{dc}}{2}, V_{C3} = V_{dc}, V_{C4} = 0 \quad (18)$$

$$V_{PN} = V_{C1} + V_{C2} + V_{C3} + V_{C4} = V_{dc}. \quad (19)$$

From Fig. 4(b), four capacitor voltages and dc-link voltage of the SEMZS-3LTI are given by

$$V_{C1} = V_{C2} = 0\ , \quad V_{C3} = V_{C4} = V_{dc} \quad (20)$$

$$V_{PN} = V_{C1} + V_{C2} + V_{C3} + V_{C4} = 2V_{dc}. \quad (21)$$

Table 1 describes the pole phase voltage V_{xo} ($x = a$, b, or c) and the turn-on switching devices and diodes according to the operating states of the two proposed topologies.

TABLE 1. Switching states of the two proposed topologies ($x = a$, b, or c).

State Type	ON switches	ON diodes	V_{xo}
UST	S_{1x}, S_{2x}, , S_{3x}	D_1, D_3	0
LST	S_{2x}, S_{3x}, S_{4x}	D_1, D_2	0
NST 1	S_{1x}, S_{2x}	D_1, D_2, D_3	V_{C1}+V_{C3}
NST 2	S_{3x}, S_{4x}	D_1, D_2, D_3	-(V_{C2}+V_{C4})
NST 3	S_{2x}, S_{3x}	D_2, D_3	0

III. COMPARISON WITH OTHER TOPOLOGIES COMBINING IMPEDANCE NETWORK AND 3LTI OR NPC INVERTER

The proposed AEMZS-3LTI and SEMZS-3LTI topologies are compared to other topologies combining the impedance network and 3LTI such as ZS-3LT^{2}I [19], qZS-3LT^{2}I [21], 3L-qSBT^{2}I [26], RC^2-AIS-3LTI [31], and combining the impedance network and NPC inverter named MZS-NPC inverter [33].

A. COMPARISON OF THE BOOST FACTOR

Fig. 5 shows the plots of the boost factors of the two proposed topologies and five different topologies. Both the ZS-3LT^{2}I and qZS-3LT^{2}I have the lowest boost factor, and the boost factor of the 3L-qSBT^{2}I varies in the range of the lowest value and twice the lowest value. The boost factor of the proposed two topologies is twice as large as that of the three different topologies, and it is same as the SC^2-AIS-3LTI and MZS-NPC inverter.

B. COMPARISON OF THE NUMBER OF COMPONENTS

Table 2 summarizes the number of passive and active components used in the impedance network. The proposed topologies require two more diodes than the ZS-3LT^{2}I. However, ZS-3LT^{2}I has a discontinuous dc source current. Compared to qZS-3LT^{2}I, the proposed topologies use two less inductors and one additional diode and dc source (in case of SEMZS-3LTI). The 3L-qSBT^{2}I uses fewer inductors and capacitors

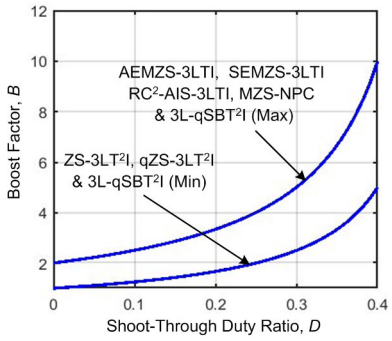

FIGURE 5. Boost factor with a variation of D.

TABLE 2. Number of components used at impedance network.

Components	ZS-3LT^{2}I	qZS-3LT^{2}I	3L-qSBT^{2}I	RC^2-AIS-3LTI	MZS-NPC	AEMZS-3LTI	SEMZS-3LTI
Inductors	2	4	1	1	2	2	2
Capacitors	4	4	2	2	4	4	4
Diodes	1	2	4	2	3	3	3
Switches	0	0	2	1	0	0	0
DC sources	1	1	1	1	1	1	2

than the proposed topologies. However, 3L-qSBT^{2}I needs one more diode and two additional active switches. The RC^2-AIS-3LTI topology uses fewer inductors, capacitors, and diodes, and requires one more active switch. The MZS-NPC inverter has the same number of components as the AEMZS-3LTI.

C. COMPARISON OF THE VOLTAGE AND CURRENT STRESSES

The voltage stress across the capacitors in the impedance network varies with the boost factor and dc input voltage. For a fair comparison of the capacitor voltage stresses of the seven topologies, the ratio of the voltage stress to the root means square (RMS) value of the ac output voltage is adopted to consider the cost to produce a desired output voltage.

The dc-ac voltage gain G is defined by

$$G = \frac{\sqrt{2}\, v_{o(rms)}}{V_{dc}/2} = M \cdot B \quad (22)$$

where $v_{o(rms)}$ and M are the RMS of the output phase voltage and modulation index. A simple boost control method is used, in which $M = 1-D$. Substituting $M = 1-D$ into (22), the dc input voltage can be expressed as the output phase voltage.

$$V_{dc} = \frac{2\sqrt{2}}{(1-D)B} v_{o(rms)} \quad (23)$$

The ratios of the voltage stress across capacitors and diodes to the RMS value of the ac output voltage using (23) and the inductor current stress for the seven topologies are described in Table 3. The capacitor voltage stress ratio of the proposed

TABLE 3. Comparison of voltage stress across capacitors and diodes, and the inductor current stress.

	ZS-3LT^{2}I		qZS-3LT^{2}I		qSBT^{2}I	SC^2-AIS-3LTI	MZS-NPC		AEMZS-3LTI		SEMZS-3LTI
Capacitor Voltage Stress Ratio	C_1, C_2	$\frac{\sqrt{2}(1-2D)}{1-D}$	C_1, C_4	$\frac{\sqrt{2}D}{1-D}$	$\frac{\sqrt{2}}{1-D}$	$\frac{\sqrt{2}}{1-D}$	C_1, C_2	$\sqrt{2}$	C_1, C_4	$\frac{\sqrt{2}D}{1-D}$	$\frac{\sqrt{2}}{1-D}$
	C_3, C_4	$2\sqrt{2}$	C_2, C_3	$\sqrt{2}$			C_3, C_4	$\frac{\sqrt{2}D}{1-D}$	C_2, C_3	$\sqrt{2}$	
Diode Voltage Stress Ratio	$\frac{2\sqrt{2}D}{1-D}$		$\frac{\sqrt{2}}{1-D}$		$\frac{\sqrt{2}}{1-D}$	$\frac{\sqrt{2}}{1-D}$	$\frac{\sqrt{2}}{1-D}$		$\frac{\sqrt{2}}{1-D}$		$\frac{2\sqrt{2}}{1-D}$
Inductor Current Stress	$\frac{1-D}{1-2D}I_o$		$\frac{1-D}{1-2D}I_o$		$\frac{1-D}{1-2D}I_o \sim \frac{2(1-D)}{1-2D}I_o$	$\frac{2(1-D)}{1-2D}I_o$	$\frac{2(1-D)}{1-2D}I_o$		$\frac{2(1-D)}{1-2D}I_o$		$\frac{2(1-D)}{1-2D}I_o$

AEMZS-3LTI is less than qSBT^{2}I and SC^2-AIS-3LTI and equal to qZS-3LT^{2}I. The capacitor voltage stress ratio of the proposed SEMZS-3LTI is the same as qSBT^{2}I and SC^2-AIS-3LTI. The diode voltage stress ratio of the proposed AEMZS-3LTI (or SEMZS-3LTI) is the same as (or higher than) qZS-3LT^{2}I, qSBT^{2}I and SC^2-AIS-3LTI. The current stress on the inductors of the proposed two topologies is equal to the SC^2-AIS-3LTI, and higher than the ZS-3LT^{2}I, qZS-3LT^{2}I, and qSBT^{2}I. The voltage stress across capacitors and diodes, and inductor current stress of the proposed AEMZS-3LTI is the same as MZS-NPC inverter.

IV. MODIFIED MODULATION TECHNIQUE

A. OPERATIONS OF THE MODIFIED MODULATION TECHNIQUE

Fig. 6 depicts the modified modulation technique based on an alternative phase opposition disposition (APOD) [35] for the a-phase of the two proposed topologies to generate a boosted ac output voltage. As shown in Fig. 6(a), there are two carrier signals V_{tri1} and V_{tri2} with a 180° phase shift and the shoot-through envelope signal V_{sh}. From the three-phase sinusoidal reference signals V_{ref_x} ($x = a$, b, or c), the three-phase positive and negative modulation signals V_{px} and V_{nx}($x = a$, b, or c) can be obtained as

$$V_{px} = \frac{1}{2}(|V_{ref\_x}| + V_{ref\_x}) \tag{24}$$

$$V_{nx} = \frac{1}{2}(|V_{ref\_x}| - V_{ref\_x}). \tag{25}$$

The pairs S_{1x}/S_{3x}, which are switched complementarily, are generated by comparing the signal V_{px} with a carrier signal V_{tri1}. When the signal V_{px} is lower than V_{tri1}, the switch S_{3x} is turned on and switch S_{1x} is turned off. The pairs S_{2x}/S_{4x}, which are switched in a complementary way, are generated by comparing the signal V_{nx} with a carrier signal V_{tri2}. When signal V_{nx} is lower than V_{tri2}, the switch S_{2x} is turned on and switch S_{4x} is turned off. The UST and LST signals ST_U and ST_L can be produced by comparing the signal V_{sh} with V_{tri1} and V_{tri2}, respectively. The UST state is inserted into the pulse width modulation (PWM) signal of S_{1a} in the positive reference signal period, and the LST state is inserted into the PWM signal of S_{4a} in the negative reference signal period to achieve a neutral-point voltage balance by balancing two series capacitor voltages.

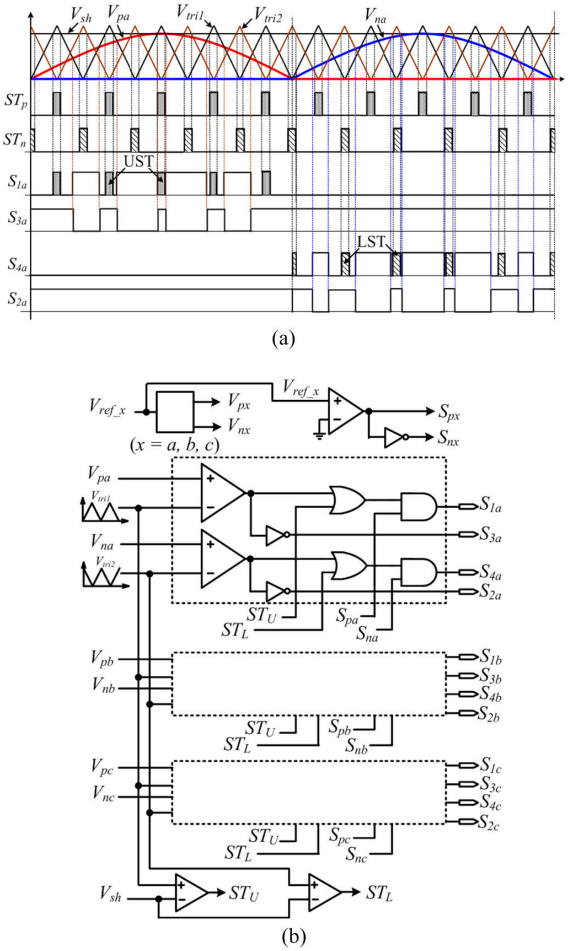

FIGURE 6. Modified modulation technique: (a) switching patterns, (b) circuit diagram for PWM generation.

Fig. 6(b) shows a logic circuit for generating 12 PWM signals from the three-phase reference signal V_{ref_x} and the shoot-through envelope signal V_{sh}. The signals S_{px} and S_{nx} ($x = a$, b, or c) are utilized to insert the UST or LST state according to the polarity of the reference signal of each phase. The proposed modulation technique for the proposed topologies can be easily implemented by a simple logic circuit.

B. NEUTRAL-POINT VOLTAGE BALACING SCHEME

The dc-link neutral-point voltage balance in the proposed topologies can be achieved by balancing the two series capacitor voltages V_{C1} and V_{C2}. Fig. 7 shows the upper and lower shoot-through states and two series capacitor voltages V_{C1} and V_{C2}. The UST and LST states are evenly distributed over one switching period. The capacitor C_2 is only charged during the UST state and capacitor C_1 is only charged during the LST state, as regarding Figs. 2 and 3. The two series capacitor voltages V_{C1} and V_{C2} can be balanced due to the same charging/discharging time of the two capacitors.

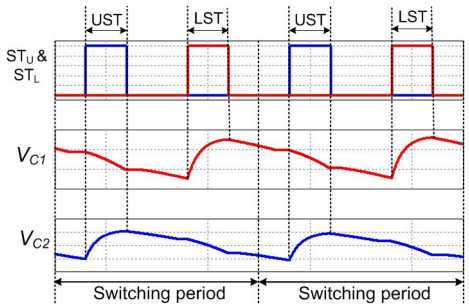

FIGURE 7. Neutral-point voltage balancing technique.

The modified modulation technique proposed in this paper can provide a higher voltage gain with a simple implementation, and can achieve the neutral-point voltage balance condition by balancing the two series capacitor voltages.

V. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the two proposed topologies is demonstrated with simulation and experimental results. One or two dc sources of 40 V are embedded and the switching frequency of the 3LTI is 5 kHz. The list of the circuit parameters used for the simulation and experimental verification of the proposed topologies is given as:

- MZS network: $C_1 = C_2 = 1000\ \mu$F, $C_3 = C_4 = 500\ \mu$F, $L_1 = L_2 = 1$ mH
- Three-phase LC filter: $L_f = 0.6$ mH, $C_f = 50\ \mu F$
- Three-phase RL load: $R_L = 50\Omega$, $L_L = 1.2$ mH

A. SIMULATION RESULTS

The simulations were carried out using the PSIM program. Fig. 8 shows the simulation results of the proposed SEMZS-3LTI topology when the modulation index $M = 0.8$ and $D = 0.2$. As shown in Fig. 8(a), the unfiltered ac output line-to-line voltage has five voltage steps, and the ac output

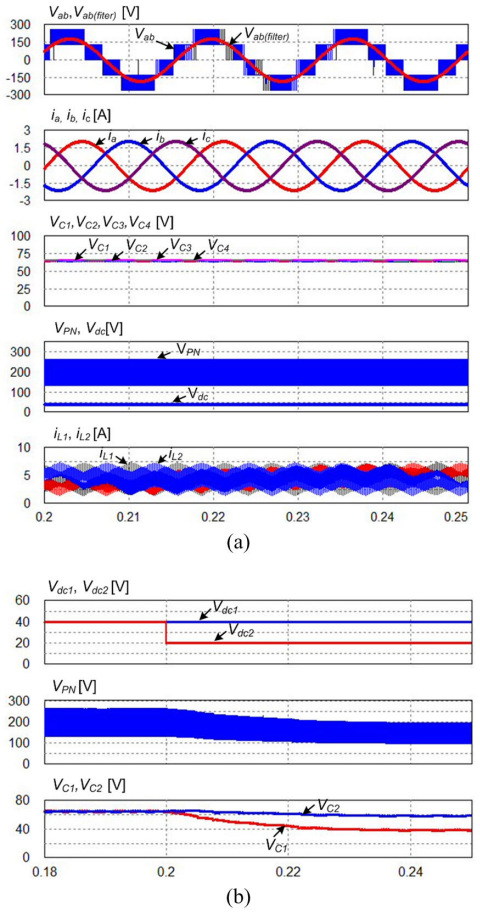

FIGURE 8. Simulation results of SEMZS-3LTI when $M = 0.8$ and $D = 0.2$: (a) when $V_{dc1} = V_{dc2} = 40$ V, (b) when V_{dc2} changes to 20 V.

voltage filtered by the LC filter of 126 V_{RMS} is generated. Four capacitors have nearly the same average voltage of 65 V. The dc-link voltage is boosted to 260 V from the two dc sources of 40 V. Two inductor currents i_{L1} and i_{L2}, which are identical to the two dc input currents, are continuous. Fig. 8(b) shows the dc-link voltage and two series capacitor voltages when the dc input voltage V_{dc2} only decreases from 40 V to 20 V. When two dc source voltages are different, the peak dc-link voltage and relationship between the two series capacitor voltages and two dc source voltages for balancing the dc-link voltage are expressed, respectively, as

$$\hat{V}_{PN} = \frac{2}{1-2D}(V_{dc1} + V_{dc2}) \tag{26}$$

$$V_{dc1} + V_{C1} = V_{dc2} + V_{C2}. \tag{27}$$

Therefore, the peak dc-link voltage is reduced from 260 V to 195 V, and the capacitor voltage V_{C1} is 20 V less than V_{C2} as V_{dc2}decreases from 40 V to 20 V.

Fig. 9 shows the simulation results of the proposed AEMZS-3LTI topology when $M = 0.8$ and $D = 0.2$. The RMS value of the filtered ac output voltage and peak dc-link voltage are 64 V and 130 V, respectively, which are half of those of the SEMZS-3LTI topology. The average value of the two capacitor voltages V_{C2} and V_{C3} is 52 V. The average

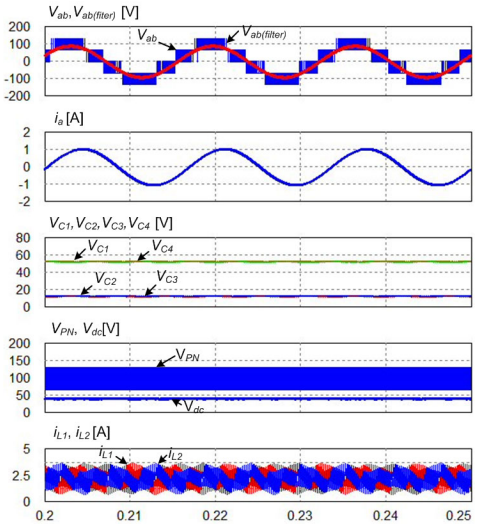

FIGURE 9. Simulation results of AEMZS-3LTI when $M = 0.8$ and $D = 0.2$.

voltage of C_1 and C_4 is 12 V, which is equivalent to less the value of dc input voltage (40 V) than the average voltage of C_2 and C_3.

Fig. 10 demonstrates the operations of the neutral-point voltage balancing scheme in conditions of imbalance of the two series capacitor voltages of the two proposed topologies, in order to validate the performance of the proposed voltage balancing scheme. As shown in Fig. 10(a), the two series capacitor voltages V_{C1} and V_{C2} of the SEMZS-3LTI are intentionally changed to 50 V and 75 V, respectively, at $t = 0.2$ s while maintaining the voltage balance across the two series capacitors. After $t = 0.21$ s, the two series capacitor voltages converge to the same value as 62 V. As shown in Fig. 10(b), the voltages across the two capacitors C_1 and C_2 of the AEMZS-3LTI converge back to 12 V and 52 V when V_{C1} and V_{C2} are intentionally changed to 35 V and 40 V, respectively, at $t = 0.2$ s. The capacitor voltage V_{C2} is balanced with the voltage, adding V_{C1} and dc input voltage V_{dc} (40 V) as outlined in (27).

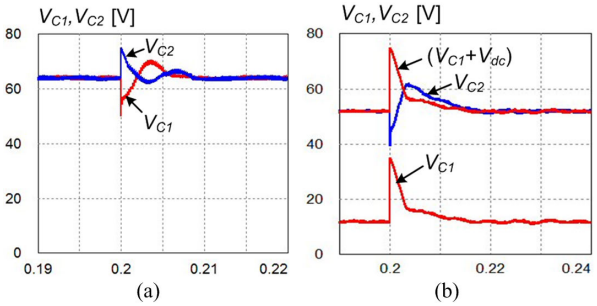

FIGURE 10. Simulation results for the neutral-point voltage balance method: (a) SEMZS-3LTI, (b) AEMZS-3LTI.

B. EXPERIMENTAL RESULTS

Fig. 11 depicts an experimental prototype built in the laboratory to further verify the performance of the proposed topologies. The prototype consists of a control board implemented by the 32-bit DSP TMS320F28335, 3LTI

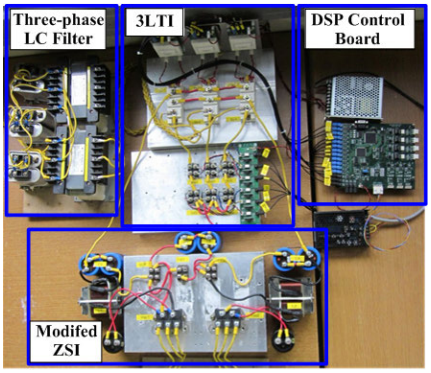

FIGURE 11. Photograph of the experimental setup.

with 12 insulated gate bipolar transistors (IGBTs), the modified Z-source impedance network, the three-phase LC filter, and a resistive-inductive load. Two dc voltage sources are built using a separate ac voltage source and diode rectifier.

Fig. 12 shows the experimental results of the SEMZS-3LTI topology at the same operating conditions as the simulation

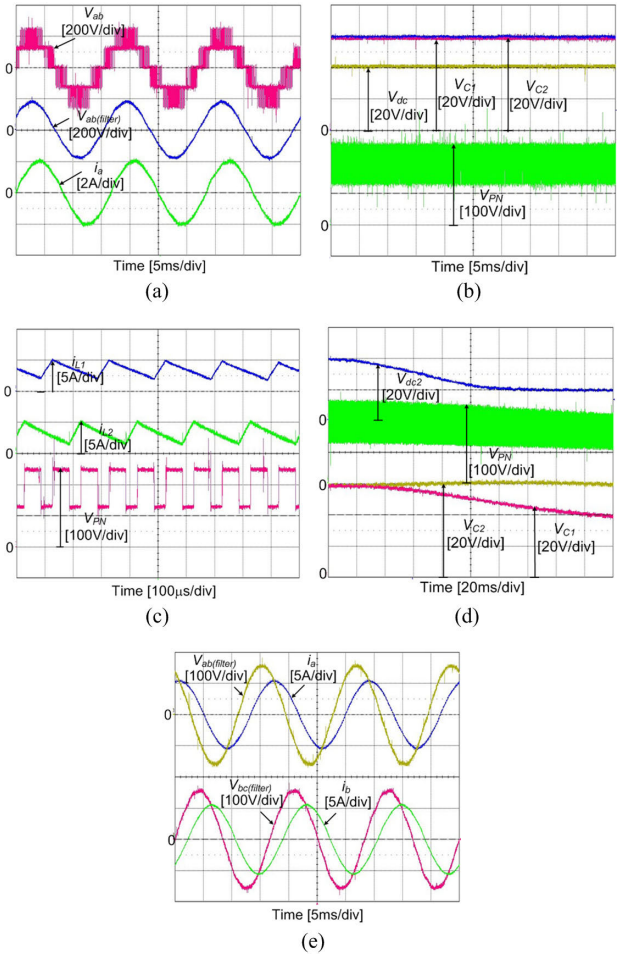

FIGURE 12. Experimental results of SEMZS-3LTI when $M = 0.8$ and $D = 0.2$: (a) ac output voltage and current, (b) two series capacitor voltages and dc-link voltage, (c) two inductor currents and dc-link voltage, (d) when V_{dc2} changes from 40 V to 20 V, (e) ac output voltage and current at $R_L = 15\Omega$ and $L_L = 8$ mH.

results shown in Fig. 8. The generated line-to-line ac output voltage is 123 V_{RMS} and the dc-link voltage is boosted to 245 V, which is 3.06 times the two dc input voltages of 80 V. Two series capacitor voltages V_{C1} and V_{C2} are balanced with 60 V. From Fig. 12(c), the inductor currents i_{L1} and i_{L2} increase during the UST and LST states, respectively, thus the charging energy for each inductor. The dc-link voltage during the two shoot-through states is half of the peak dc-link voltage. The two dc source currents are continuous. Fig. 12(d) shows the two series capacitor voltages and dc-link voltage, when the dc input voltage V_{dc2} decreases from 40 V to 20 V. The capacitor voltage V_{C1} becomes 20 V less than V_{C2}, and the peak dc-link voltage is reduced as V_{dc2} decreases to 20 V, which are nearly the same as the simulation result shown in Fig. 8(b). Fig. 12(e) displays two line-to-line ac output voltages and currents when the load resistance decreases from 50 Ω to 15 Ω and the load inductance increases from 1.2 mH to 8 mH for achieving a more inductive load.

Fig. 13 shows the experimental results of the SEMZS-3LTI topology when M increases from 0.8 to 0.9 and D decreases from 0.2 to 0.1. Despite the increase of M, the decrease of D by 0.1 reduces the ac output voltage to 101 V_{RMS}. The balanced three-phase ac output voltages are shown in Fig. 13(b). Fig. 14 shows the experimental results of the AEMZS-3LTI topology when $M = 0.8$ and $D = 0.2$. Both the ac output voltage and dc-link voltage are nearly half those of the SEMZS-3LTI topology under the same M and D shown in Fig. 12. The average values of V_{C1} and V_{C2} are 10 V and 50 V, respectively. The voltage difference between the two capacitors C_1 and C_2 is identical to the dc input voltage embedded at the upper shell of the MZS network. The dc-link, ac output, and capacitor voltages of the experimental results are slightly lower than those of the simulation results under the same operating conditions due to the forward voltage drops of IGBTs and diodes as well as the equivalent series resistances (ESRs) of the capacitors and inductors.

Fig. 15 shows the experimental results of the two proposed topologies when $D = 0$ and $M = 1$. The capacitor voltages and dc-link voltage are nearly identical with voltages calculated from (18), (19), (20) and (21). It can be seen that the dc-link voltage is not boosted, because there is no ST state.

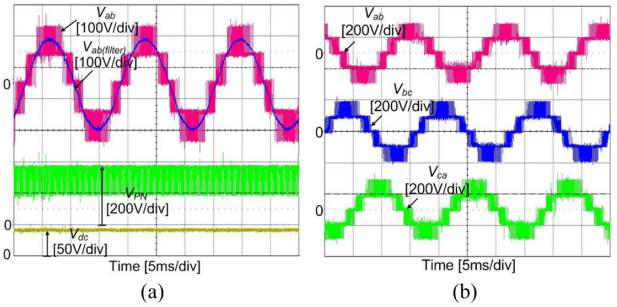

FIGURE 13. Experimental results of SEMZS-3LTI when $M = 0.9$ and $D = 0.1$: (a) ac output voltage, dc-link and dc input voltages, (b) three-phase ac output voltages.

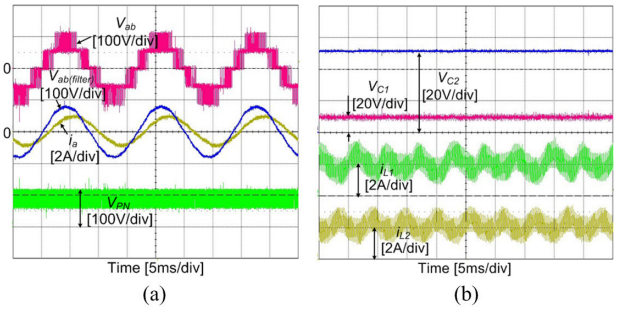

FIGURE 14. Experimental results of AEMZS-3LTI when $M = 0.8$ and $D = 0.2$: (a) ac output voltage and current, dc-link voltage, (b) two series capacitor voltages and two inductor currents.

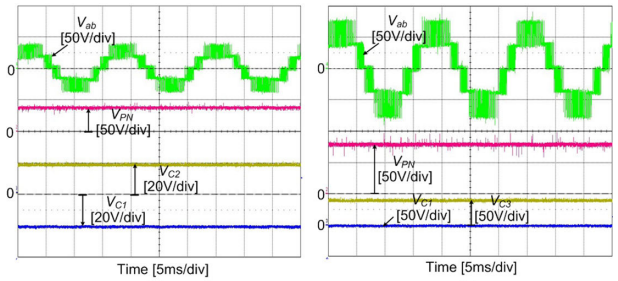

FIGURE 15. Experimental results of two proposed topologies when $M = 1.0$ and $D = 0$: (a) AEMZS-3LTI (b) SEMZS-3LTI.

Fig. 16 describes the a-phase gating signals with the modulation signals and UST state. Fig. 16(a) shows the positive and negative modulation signals and gating signals S_{1a} and S_{4a}. The switches S_{1a} and S_{4a} are only modulated their pulse width when a reference signal is positive/negative. As shown in 16(b), the pairs S_{1x}/S_{3x} are switched complementarily and the UST state is only inserted at the signal S_{1a}.

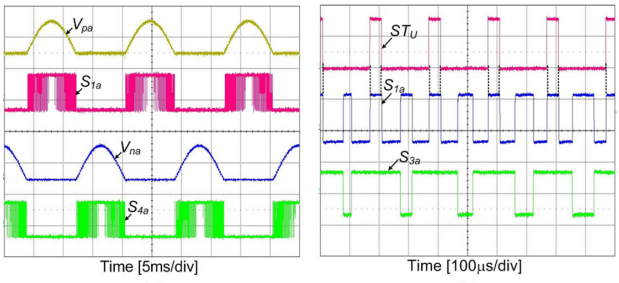

FIGURE 16. A-phase gating signals: (a) positive and negative modulation signals and gating signals S_{1a} and S_{4a}, (b) UST state and gating signals S_{1a} and S_{3a}.

Fig. 17 shows the spectrum analysis of the filtered ac output voltage. The total harmonic distortion (THD) of the filtered ac output voltage is calculated as 2.5 %. Fig. 18 depicts the efficiency of the SEMZS-3LTI topology, which ranges from 79.5 % to 85.1 % with a variation of the output power.

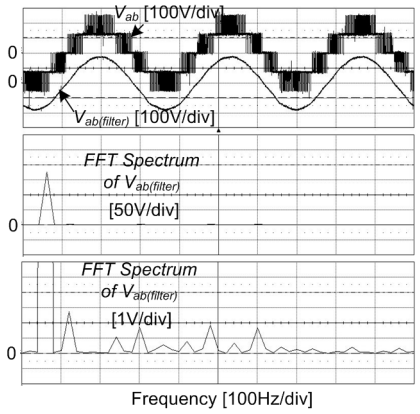

FIGURE 17. FFT spectrum analysis of filtered ac output voltage.

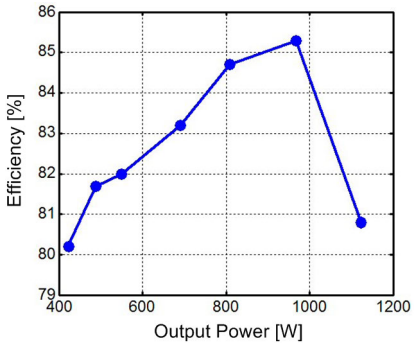

FIGURE 18. Efficiency of SEMZS-3LTI when $M = 0.8$ and $D = 0.2$.

VI. CONCLUSIONS

This paper proposed two types of topologies, AEMZS-3LTI and SEMZS-3LTI, designed by integrating a modified-Z-source impedance network to the traditional 3LTI, and embedding either one or two dc sources in the impedance network. The proposed topologies provide a highly boosted ac output voltage with five voltage levels, even though there is not an active switch in the impedance network. Additionally, they ensure a continuous dc source current by embedding the dc source(s) without an extra filter. Compared to five different topologies combining the impedance network and 3LTI or NPC inverter, the number of components, the boost factor, and voltage stress ratio on capacitors are kept in an acceptable range except for a higher voltage stress on the diode of the SEMZS-3LTI. The upper and lower shoot-through states are effectively adjusted and two series capacitor voltages are balanced using a modified modulation technique implemented with a simple logic circuit. An experimental prototype was built and the experimental results validate the performance of the two proposed topologies and the modulation technique.

REFERENCES

[1] D. Mohan, X. Zhang, and G. H. B. Foo, "A simple duty cycle control strategy to reduce torque ripples and improve low-speed performance of a three-level inverter fed DTC IPMSM drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2709–2721, Apr. 2017.

[2] J. S. Lee and K. B. Lee, "Open-switch fault tolerance control for a three-level NPC/T-type rectifier in wind turbine systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1012–1021, Feb. 2015.

[3] H. Xiao and S. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[4] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[5] R. S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[7] S.-M. Shin, J.-H. Ahn, and B.-K. Lee, "Maximum efficiency operation of three-level T-type inverter for low-voltage and low-power home appliances," *J. Electr. Eng. Technol.*, vol. 10, no. 2, pp. 586–594, Mar. 2015.

[8] D. Chen, Y. Liu, and S. Zhang, "Open-circuit fault diagnosis method for the T-type inverter based on analysis of the switched bridge voltage," *IET Power Electron.*, vol. 12, no. 2, pp. 295–302, Feb. 2019.

[9] T. L. Lee, B. F. Li, M. Y. Yang, and Y. T. Tsai, "A carrier-based PWM for three-level T-type inverter to tolerate open-circuit fault," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8787–8796, Oct. 2018.

[10] U. M. Choi, F. Blaabjerg, and K. B. Lee, "Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2660–2673, May 2015.

[11] J. Chen, C. Zhang, A. Chen, and X. Xing, "Fault-tolerant control strategies for T-Type three-level inverters considering neutral-point voltage oscillations," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2837–2846, Apr. 2019.

[12] X. Wang, J. Zou, L. Ma, J. Zhao, C. Xie, K. Li, and L. Meng, "Model predictive control methods of leakage current elimination for a three-level T-type transformerless PV inverter," *IET Power Electron.*, vol. 12, no. 2, pp. 295–302, 2018.

[13] S. Bhattacharya, D. Mascarella, G. Joos, J.-M. Cyr, and J. Xu, "A dual three-level T-NPC inverter for high-power traction applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 668–678, Jun. 2016.

[14] Z. Wang, X. Wang, J. Cao, M. Cheng, and Y. Hu, "Direct torque control of T-NPC inverters-fed Double-Stator-Winding PMSM drives with SVM," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1541–1553, Feb. 2018.

[15] D. Zhang, J. G. Jiang, B. N. Wang, Z. Z. Zhou, and H. L. Li, "Research on seamless switching control strategy for T-type three-level energy storage inverter based on virtual synchronous generator," *J. Eng.*, vol. 2017, no. 13, pp. 1524–1527, 2017.

[16] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[17] J. Anderson and F. Z. Peng, "A class of Quasi-Z-Source inverters," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 2008, pp. 1–7.

[18] D. Panfilov, O. Husev, F. Blaabjerg, J. Zakis, and K. Khandakji, "Comparison of three-phase three-level voltage source inverter with intermediate DC–DC boost converter and quasi-Z-source inverter," *IET Power Electron.*, vol. 9, no. 6, pp. 1238–1248, May 2016.

[19] X. Xing, C. Zhang, A. Chen, J. He, W. Wang, and C. Du, "Space-vector-modulated method for boosting and neutral voltage balancing in Z-source three-level T-type inverter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1621–1631, Mar./Apr. 2016.

[20] H.-T. Luong, M.-K. Nguyen, and T.-T. Tran, "Single-phase five-level Z-source T-type inverter," *IET Power Electron.*, vol. 11, no. 14, pp. 2367–2376, Nov. 2018.

[21] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "A space vector modulation scheme of the quasi-Z-source three-level T-type inverter for common-mode voltage reduction," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8340–8350, Oct. 2018.

[22] C. Qin, C. Zhang, X. Xing, X. Li, A. Chen, and G. Zhang, "Simultaneous common-mode voltage reduction and neutral-point voltage balance scheme for the Quasi-Z-Source three-level T-Type inverter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1956–1967, Mar. 2020.

[23] C. Roncero-Clemente, E. Romero-Cadaval, M. Ruiz-Cortes, and O. Husev, "Carrier level-shifted based control method for the PWM 3L-T-type qZS inverter with capacitor imbalance compensation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8297–8306, Oct. 2018.

[24] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Martins, "Quasi-Z-source inverter with a T-type converter in normal and failure mode," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7462–7470, Nov. 2016.
[25] M. Ruiz-Cortes, E. Romero-Cadaval, C. Roncero-Clemente, E. Gonzalez-Romera, and O. Husev, "Evaluation of losses in three-level neutral-point-clamped and T-type quasi-Z-source inverters with modified carrier based modulation method," in *Proc. 11th IEEE Int. Conf. Compat., Power Electron. Power Eng. (CPE-POWERENG)*, Apr. 2017, pp. 638–642.
[26] D. T. Do and M. K. Nguyen, "Three-level quasi-switched boost T-type inverter: Analysis, PWM control, and verification," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8320–8329, Oct. 2018.
[27] D.-T. Do, M.-K. Nguyen, T.-H. Quach, V.-T. Tran, C.-B. Le, K.-W. Lee, and G.-B. Cho, "Space vector modulation strategy for three-level quasi-switched boost T-Type inverter," in *Proc. IEEE 4th Southern Power Electron. Conf. (SPEC)*, Dec. 2018, pp. 1–5.
[28] D.-T. Do, M.-K. Nguyen, T.-H. Quach, V.-T. Tran, F. Blaabjerg, and M. Vilathgamuwa, "A PWM scheme for a fault-tolerant three-level quasi-switched boost T-Type inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jun. 13, 2019, doi: 10.1109/JESTPE.2019.2922687.
[29] M.-K. Nguyen, T.-V. Le, S.-J. Park, and Y.-C. Lim, "A class of quasi-switched boost inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1526–1536, Mar. 2015.
[30] M.-K. Nguyen, T.-T. Tran, and Y.-C. Lim, "A family of PWM control strategies for single-phase Quasi-Switched-Boost inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1458–1469, Feb. 2019.
[31] M.-K. Nguyen, T.-T. Tran, and F. Zare, "An active impedance-source three-level T-Type inverter with reduced device count," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jul. 10, 2019, doi: 10.1109/JESTPE.2019.2927727.
[32] A.-V. Ho and T.-W. Chun, "Single-phase modified Quasi-Z-Source cascaded hybrid five-level inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5125–5134, Jun. 2018.
[33] A. V. Ho and T. W. Chun, "Topology and modulation scheme for three-phase three-level modified Z-source neutral-point-clamped inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11014–11025, Nov. 2019.
[34] A. V. Ho, A. T. Huynh, and T. W. Chun, "Three-phase modified Z-source three-level T-type inverters with continuous source current," in *Proc. Int. Aegean Conf. Elect. Mach. Power Electron. (ACEMP) Int. Conf. Optim. Elect. Electron. Equip. (OPTIM)*, Aug. 2019, pp. 1–6.
[35] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.

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