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Stability Investigation of Bidirectional AC-DC Converter Considering Operating Conditions

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ABSTRACT This paper investigates the stability performances of bidirectional ac-dc converters considering operating conditions based on the small-signal impedance model. It finds that the converter has different stability margins when working in different operating conditions (including inverter mode and rectifier mode, as well as generating/absorbing reactive power), which should be taken into account in the design of the converter for bidirectional energy conversions. To have an intuitive understanding of the instability mechanisms of bidirectional converters in different operating conditions, the concept of positive feedback is used. It finds that with phase-lock loop (PLL) and dc-link voltage control loop (VCL), positive feedback effects appear when the converter operating in different conditions; and the influencing mechanisms of the parameters, including control parameters of PLL, inner current and outer voltage controllers and power ratings, on the converter's stability can be explicitly identified by the positive feedback gains. And it indicates that reducing the values of the parameters along the positive feedback paths will be a practical way to enhance the converter's stability. The theoretical stability analysis results are verified by simulations and experiments.

INDEX TERMS Stability, small-signal model, bidirectional converter, positive feedback, operating conditions.

I. INTRODUCTION

Power electronic converters have been widely used in power systems for energy conversions between renewable energy sources and grid/loads [1], [2]. The voltage source converter (VSC) can deliver power in bidirectional way thanks to its control flexibility, and VSCs have been applied for bidirectional energy conversions in some instances, such as battery energy storage systems [3], double-fed wind generation systems [4], and hybrid ac-dc power systems [5]–[7] (known as interlinking converter in [5]), etc. However, the interactions among the converters' complicated control loops and passive components of the power systems possibly result in instability issues and thus impair the safe operation of these converters [8], [9]. As a result, stability analysis for parameter designs of the bidirectional converters is important, particularly for hybrid ac-dc systems in which the bidirectional converters used as key equipment that links ac systems and dc systems.

Recent researches showed that the stability performances of the converters are affected by their power flow directions (or their operation modes, i.e., inverter mode and rectifier mode) [9]–[11]. Ref. [9] revealed that the converter with dc-link voltage control may suffer from low-frequency oscillations in the rectifier mode, but high-frequency oscillations in the inverter mode. In [10], [11], it was reported that VSC-HVDC system is stable when the power flows from the power-controlled converter to the dc-voltage-controlled converter, but it becomes unstable when the power flow direction alters. Ref. [10] showed that the control bandwidth of the dc voltage control loop has an impact on the converter's operational modes, and Ref. [11] used the Nyquist plot of impedance ratio to predict the system stability for the two power flow directions. However, the influence mechanism of power flow direction on the converter's stability—an important consideration that is supposed to be taken into account

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in the design of the bidirectional converters—has not been further explored.

Much work has engaged in stability analysis of VSCs [8], [12]–[17]; however, less attention has been paid on the differences of stability margins of VSCs when working in different modes. Ref. [12] indicated that the dynamics of control loops (inner current control loop (CCL), and outer control loops such as dc-link voltage control loop (VCL) and phase-lock loop (PLL)) and time delay in a digital system are the causes of the negative-conductance behavior of a VSC, which possibly leads to resonance destabilization. The instability problems caused by PLL is due to, as indicated in [13], that PLL leads to *q*-*q* channel impedances of grid-tied inverters behave as negative incremental resistors. Wang, *et al*., in a reporter pointed out that PLL bridges voltage disturbance to the converter's output current, and the loop at the q-axis is a positive feedback in the inverter (i.e., active power current $I_d > 0$) [8]. The PLL behaviors of VSCs under different grid-tied and islanded conditions have been investigated in [14], in which the PLL model interacting with the grid has been studied. It showed that the self-synchronization loop tends to drive the PLL output out of the steady state, and the loop characteristics greatly rely on multiple system parameters. The outer dc-link voltage control loop makes the instability issues of the converter more complex. In [16], it showed that, when connected to a weak ac grid, the dc-bus voltage control stability of VSCs will be affected by ac-bus voltage control, which provides dc-bus voltage control with additional negative damping and positive restoring components. The study of low-frequency instability for a single-phase rectifier (controlled in *d*-*q* frame) shows that the current and voltage controls both have influences on the negative impedance shaping the rectifier with a low switching frequency [17].

Most of researches aforementioned so far focus on the stability of the converter operating as a pure rectifier or inverter. The differences of the stability margins of a converter in rectifier and inverter operation modes are not sufficiently investigated. Besides, the grid-tied converter may participate in adjusting the reactive power of the grid, so the effect of the converter's output reactive power on stability performance of the converter should also be studied. Moreover, the conventional impedance-based analysis method can determine whether the converter is stable or not by simply using Generalized Nyquist Criterion (GNC) [9]–[17], but it cannot intuitively explain why the stability margins of a converter in different operating conditions are distinct; this is one of the motivations of this paper.

The main objective of this paper is to investigate the instability mechanism of bidirectional converters considering operating conditions by a comprehensive investigation that involves CCL, PLL and VCL of the converter, and be helpful for the design of the bidirectional converters. Although Ref. [15] investigated the effect of control-loops interactions on power stability limits of the VSC, the bidirectional power conversion of a VSC has not been considered, thus lacking of discussions about the distinctions of stability performances of VSC when working in different operation modes. And our work focuses on not only the effects of operating points [18]–[20] on stability performance of the converter but also instability mechanism of the converter in different operation modes. In [21] it was found that the PLL of VSC in inverter mode results in negative conductance, while the dc voltage loop has an opposite effect, which destabilizes the VSC in the rectification mode; and in this paper, it will indicate that positive feedback introduced by PLL and VCL is the essential reason of negative conductance of VSC.

The main contributions of this paper are three-fold: 1) we systematically investigate the stability performances of bidirectional ac-dc converters considering operating conditions, and reveal that converter has different stability margins when works in different operating conditions, 2) the instability mechanisms of bidirectional converters in different operating conditions are intuitively revealed by using the concept of *positive feedback*, and 3) this study also indicates that the stability of the converter can be effectively enhanced by reducing the values of the parameters along the positive feedback paths.

The rest of this paper is organized as follows. First, a unified small-signal impedance model of a bidirectional converter that works in both rectifier and inverter operation modes is presented in Section II. Based on the proposed model, the instability mechanisms of CCL and PLL of the converter are studied in Section III. And then, the stability analysis of the converter with VCL is investigated in Section IV. Finally, the experimental results are presented in Section V, and Section VI concludes this paper.

II. SMALL-SIGNAL IMPEDANCE MODEL OF BIDIRECTIONAL AC-DC CONVERTER

A. SYSTEM DESCRIPTION

The VSC that works for bidirectional energy conversions between ac- and dc-sides needs the support of steady dc-link voltages, which is realized by either dual-loop control strategy (i.e., CCL for current tracking and VCL for dc-link voltage regulation) [9] or dc systems (whose bus voltage is maintained by distributed generations and energy storage) [5]. In the latter cases, the reference current of the converter's current loop is provided by power control loops with much lower control bandwidth for energy conversions between ac and dc systems, and the converter' power control loops could be neglected. In this paper, the typical bidirectional ac-dc converters with dual-loop control strategy will be used as the object of study.

The structure of the bidirectional ac-dc converter studied in this paper is shown in Fig. 1, where L and R_L denote the inductor and resistor of the inverter output filter; d_d, d_q are the duty ratios. The ac-side of the converter is connected to the ac system that is simplified to a voltage source in series with impedance; L_g and R_g denote the equivalent inductor and resistor of the ac grid. The dc-side of the converter

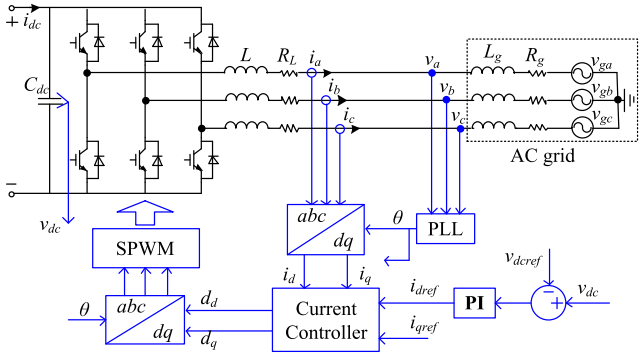

FIGURE 1. Structure of bidirectional ac-dc converter.

can be connected to dc loads [15], dc microgrids [5], ac-dc converters [10], [11], and etc. VCL is used for the dc-link voltage regulation of the converter. As the grid-tied converter is controlled in *d-q* frame, the typical PLL strategy is used for synchronization [22]. In [30] it showed that the voltage feed-forward compensation control (VFCC) on stability of grid-tied converter has negative effects on stability of grid-tied converter and VFCC will make the control system more complex. For simplicity [9], [12]–[14], [22]–[24], VFCC has not been considered in this paper.

B. SMALL-SIGNAL MODEL OF THE CONVERTER

Fig. 2 shows the small-signal circuit of a converter [23]. To illustrate the influence of PLL on the converter, two *d-q* frames are defined, i.e., system *d-q* frame and controller *d-q* frame, [13], [22]. The symbolic "$\sim$" denotes the small-signal perturbation of a variable, and superscript "s" denotes variables in the system *d-q* frame.

According to Fig.2, one can get the converter output currents on ac-side in s-domain as follows

$$\begin{aligned}\tilde{\boldsymbol{i}}^{s} &= \begin{bmatrix}\tilde{i}_d^s\\ \tilde{i}_q^s\end{bmatrix} = \begin{bmatrix}sL+R_L & -\omega_1 L\\ \omega_1 L & sL+R_L\end{bmatrix}^{-1}\left\{\frac{V_{dc}}{2}\begin{bmatrix}\tilde{d}_d^s\\ \tilde{d}_q^s\end{bmatrix}\right.\\ &\quad\left.-\begin{bmatrix}\tilde{v}_d^s\\ \tilde{v}_q^s\end{bmatrix}+\frac{1}{2}\begin{bmatrix}D_d & 0\\ D_q & 0\end{bmatrix}\begin{bmatrix}\tilde{v}_{dc}\\ 0\end{bmatrix}\right\}\\ &= \boldsymbol{Y_{out}}\tilde{\boldsymbol{d}}^{\boldsymbol{s}} - \boldsymbol{Y_{in}}\tilde{\boldsymbol{v}}^{\boldsymbol{s}} + \boldsymbol{Y_{dci}}\tilde{\boldsymbol{v}}_{\boldsymbol{dc}}\end{aligned} \tag{1}$$

where ω_1 is fundamental frequency of the grid. Capital letters of variables, e.g., V_{dc}, D_d and D_q, denote the values of the variables in steady state. Transfer function matrices, $\boldsymbol{Y_{out}}$ and $\boldsymbol{Y_{in}}$ are open loop output and input admittances, respectively, and $\boldsymbol{Y_{dci}}$ represents the transfer function matrix that relates the small-signal perturbation of the dc-link voltage to the converter output currents.

And for dc-side, one can get the expression (2)

$$\begin{aligned}\tilde{\boldsymbol{v}}_{\boldsymbol{dc}} &= \frac{1}{sC_{dc}}\begin{bmatrix}\tilde{i}_{dc}^s\\ 0\end{bmatrix} - \frac{3}{s\cdot 4C_{dc}}\begin{bmatrix}I_d & I_q\\ 0 & 0\end{bmatrix}\begin{bmatrix}\tilde{d}_d^s\\ \tilde{d}_q^s\end{bmatrix}\\ &\quad - \frac{3}{s\cdot 4C_{dc}}\begin{bmatrix}D_d & D_q\\ 0 & 0\end{bmatrix}\begin{bmatrix}\tilde{i}_d^s\\ \tilde{i}_q^s\end{bmatrix}\\ &= \frac{1}{sC_{dc}}\tilde{\boldsymbol{i}}_{\boldsymbol{dc}}^{\boldsymbol{s}} - \boldsymbol{G_{ddc}}\tilde{\boldsymbol{d}}^{\boldsymbol{s}} - \boldsymbol{G_{idc}}\tilde{\boldsymbol{i}}^{\boldsymbol{s}}\end{aligned} \tag{2}$$

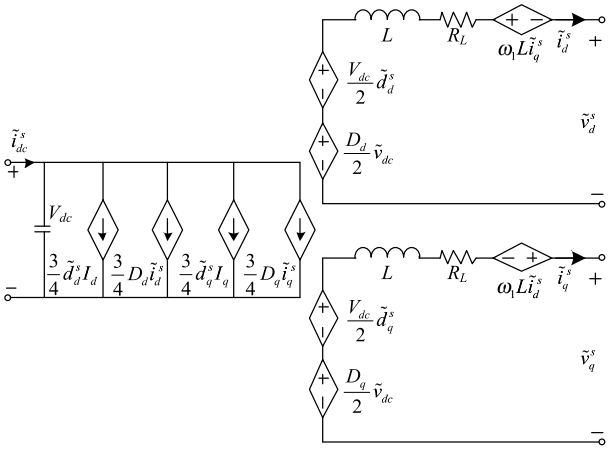

FIGURE 2. Small-signal circuit of converter in d-q frame.

where I_d and I_q denote converter output currents in steady state. When $I_d > 0$, the converter works in inverter mode; otherwise the converter works in rectifier mode. $\boldsymbol{G_{ddc}}$ is the transfer function matrix that links duty cycle to dc-link voltage, and $\boldsymbol{G_{idc}}$ links output currents to dc-link voltage.

Fig. 3 shows the small-signal block diagram of the converter with dual-loop control in *d-q* frame. Superscript "c" denotes variables in controller *d-q* frame. $\boldsymbol{G_{plli}}$ and $\boldsymbol{G_{plld}}$ denote voltage perturbations introduced into converter output currents and duty ratio, respectively, in controller *d-q* frame by PLL. $\boldsymbol{G_{del}}$ is the time delay [24], and $\boldsymbol{G_{nor}}$ is the normalization matrix that normalizes modulation signals to duty ratio. Diagonal matrix $\boldsymbol{G_{cv}}$ is voltage PI controller and $\boldsymbol{G_{ci}}$ is current PI controller. Sub-diagonal matrix $\boldsymbol{G_{dec}}$ is current decoupling term.

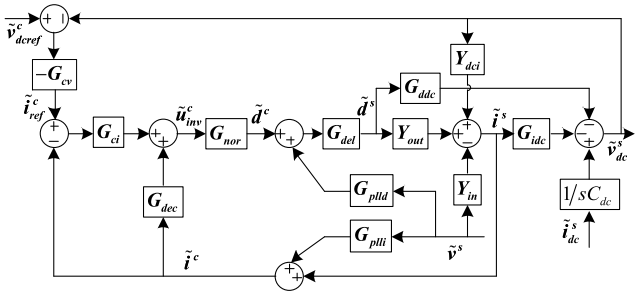

FIGURE 3. Unified small-signal block diagram of bidirectional converter with dual-loop control in d-q frame.

III. STABILITY ANALYSIS OF THE CONVERTER IN TERMS OF INNER CURRENT CONTROL LOOP (CCL) AND PLL

Firstly, considering that the converter's dc-side is supplied by a stiff dc voltage source to get rid of the interaction between PLL and VCL, the instability mechanisms of CCL and PLL are studied in this section. Fig. 4 demonstrates the small-signal block diagram of the converter without VCL.

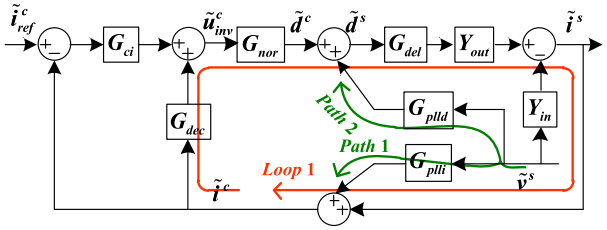

FIGURE 4. Small-signal block diagram of the converter without voltage control loop.

A. STABILITY ANALYSIS OF INNER CURRENT CONTROL LOOP (CCL)

Firstly, the stabilities of inner CCL will be studied because it is the precondition of the stability of outer control loops of the converter. According to Fig.4, the open loop transfer function matrix of the CCL can be expressed as

$$\boldsymbol{G_{opi}} = \boldsymbol{Y_{out}}\boldsymbol{G_{del}}\boldsymbol{G_{nor}}\left(\boldsymbol{G_{ci}} - \boldsymbol{G_{dec}}\right) \tag{3}$$

where $\boldsymbol{G_{del}} = [G_{del}, 0; 0, G_{del}]$, $\boldsymbol{G_{nor}} = [2/V_{dc}, 0; 0, 2/V_{dc}]$, $\boldsymbol{G_{ci}} = [G_{ci}, 0; 0, G_{ci}]$ and $\boldsymbol{G_{dec}} = [0, -\omega_1 L; \omega_1 L, 0]$. G_{del} and G_{ci} are expressed as

$$G_{del} = e^{-sT_d}, \quad G_{ci} = k_{pi} + \frac{k_{ii}}{s} \tag{4}$$

where k_{pi} and k_{ii} are proportional gain and integral gain of the current PI controller. Time delay function e^{-sT_d} can be approximated by [20]

$$e^{-sT_d} \approx \frac{1 - 0.5T_d s + 1/12T_d^2 s^2}{1 + 0.5T_d s + 1/12T_d^2 s^2} \tag{5}$$

with $T_d = 1.5/f_s$ (f_s is the sampling frequency).

The stability of CCL can be analyzed by the transfer function matrix $\boldsymbol{G_{opi}}$ and the GNC [25], [26]. It was acknowledged that time delay in a digital system and parameters of a current PI controller have impacts on the stability of CCL [12]. An interesting phenomenon claimed in [27] is that the decoupling term introduces positive feedback into CCL, as shown in Fig. 4, and it can be found that there exists positive feedback in q-d channel (see expression of $\boldsymbol{G_{dec}}$) in *loop 1*, which brings the negative effects of the coupling terms to the system's stability.

Fig. 5 shows the GNC plots of $\boldsymbol{G_{opi}}$ with different parameters (marked as Case I_{in}, Case II_{in}, Case III_{in}, and Case IV_{in}), and the parameters of the converter are given in Table 1. It can be found that with too large k_{pi} and longer time delay, the GNC plots of $\boldsymbol{G_{opi}}$ encircles $(-1, 0)$ and the system is unstable. To illustrate the negative effects of the decoupling terms on the converter's stability, an extreme decoupling coefficient is employed and the converter becomes unstable indeed. G_{dec} cannot be $10\omega_1 L$ in practice, so the decoupling term is reasonably neglected for inner current loop controller design [24]. Fig. 6 shows the simulation results of output currents in PSCAD/EMTDC, which is consistent with theoretical analysis in Fig. 5.

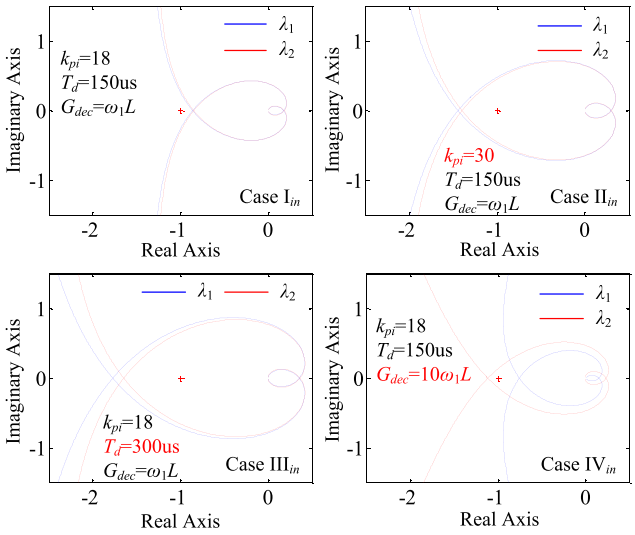

FIGURE 5. GNC plots of $\boldsymbol{G_{opi}}$ with different parameters.

TABLE 1. Parameters of converter system.

Parameters	Value
Converter dc-link voltage V_{dc}	750 V
Grid fundamental frequency ω_1	50 Hz
Grid voltage	380 V
Sampling frequency f_s	10 kHz
Inductance of inverter filter inductor L	2 mH
Inductance of grid equivalent inductor L_g	1 mH
Proportional gain of current controller k_{pi}	18
Integral gain of current controller k_{ii}	300
Proportional gain of voltage controller k_{pv}	2
Integral gain of voltage controller k_{iv}	5
Proportional gain of PLL k_{pPLL}	2
Integral gain of PLL k_{iPLL}	200

B. STABILITY ANALYSIS OF CONVERTER'S PLL CONSIDERING OPERATING CONDITIONS IN WEAK GRID

According to Fig. 4, the output admittance of the converter without VCL can be expressed as

$$\boldsymbol{Y_{eqi}} = \boldsymbol{G_{cli}}\boldsymbol{Y_{pcci}} = \boldsymbol{G_{cli}}\left(\boldsymbol{Y_{in}} - \boldsymbol{Y_{out}}\boldsymbol{G_{del}}\boldsymbol{G_{pllx}}\right) \tag{6}$$

where $\boldsymbol{G_{cli}} = (\boldsymbol{I} + \boldsymbol{G_{opi}})^{-1}$, and $\boldsymbol{G_{pllx}}$ is given as follow

$$\boldsymbol{G_{pllx}} = \boldsymbol{G_{plld}} - \boldsymbol{G_{nor}}\left(\boldsymbol{G_{ci}} - \boldsymbol{G_{dec}}\right)\boldsymbol{G_{plli}} \tag{7}$$

and transfer function matrices $\boldsymbol{G_{plli}}$ and $\boldsymbol{G_{plld}}$ are given as [13], [18]

$$\boldsymbol{G_{plli}} = \begin{bmatrix} 0 & I_q G_{PLL} \\ 0 & -I_d G_{PLL} \end{bmatrix}, \quad \boldsymbol{G_{plld}} = \begin{bmatrix} 0 & -D_q G_{PLL} \\ 0 & D_d G_{PLL} \end{bmatrix} \tag{8}$$

with

$$G_{PLL} = \frac{sk_{pPLL} + k_{iPLL}}{s^2 + sV_d k_{pPLL} + V_d k_{iPLL}} \tag{9}$$

where k_{pPLL} and k_{iPLL} are proportional gain and integral gain of the PI controller of PLL. At operating point, we can obtain that $D_d^* V_{dc}/2 = V_d + R_L I_d - \omega_1 L I_q$, and $D_q^* V_{dc}/2 = R_L I_q + \omega_1 L I_d$.

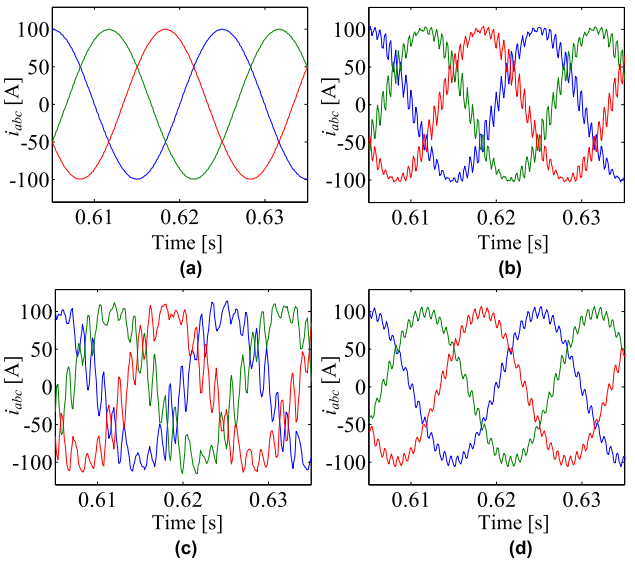

FIGURE 6. Simulation results of output currents with different control parameters: (a) case I_{in}, (b) case II_{in}, (c) case III_{in}, and (d) case IV_{in}.

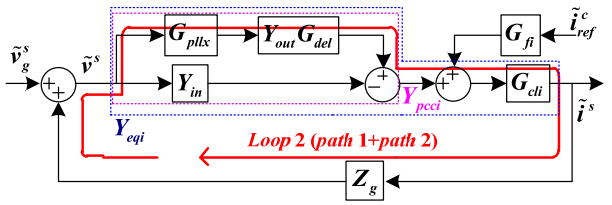

FIGURE 7. Small-signal block diagram of the converter in weak grid.

In a weak grid (the grid equivalent impedance $\boldsymbol{Z_g} \neq 0$) with the small-signal perturbation of grid source $\tilde{\boldsymbol{v}}_{\boldsymbol{g}}^{\boldsymbol{s}}$, one can get that

$$\tilde{\boldsymbol{v}}^{\boldsymbol{s}} = \tilde{\boldsymbol{v}}_{\boldsymbol{g}}^{\boldsymbol{s}} + \boldsymbol{Z_g}\tilde{\boldsymbol{i}}^{\boldsymbol{s}} \tag{10}$$

Fig. 7 shows the small-signal block diagram of the converter in a weak grid. The stability of the converter output current can be judged by return ratio matrix, $\boldsymbol{L_i} = \boldsymbol{Y_{eqi}Z_g}$, i.e., if $\boldsymbol{L_i}$ satisfies GNC, the converter will be stable.

For *loop 2* (introduced by PLL through *path 1* and *path 2*, as shown in Fig. 4), ignoring the resistor of the filter inductor, i.e., $R_L \approx 0$, then one can have

$$\boldsymbol{Y_{out}G_{del}G_{pllx}} = \frac{G_{del}G_{PLL}}{(sL)^2+(\omega_1 L)^2}\begin{bmatrix} 0 & -sLG_{ci}I_q \\ & +\omega_1 L\,(V_d + G_{ci}I_d) \\ 0 & \omega_1 LG_{ci}I_q \\ & +sL\,(V_d + G_{ci}I_d) \end{bmatrix} \tag{11}$$

According to (11) and Fig. 7, it can be found that when $I_d > 0$, *loop 2* introduces positive feedback into the system, which will deteriorate the system's stability. This means that the stability of the converter working in rectifier mode ($I_d < 0$) will be better than that of the converter in inverter mode ($I_d > 0$).

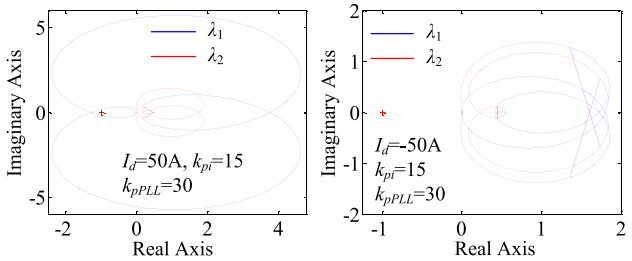

FIGURE 8. GNC plots of L_i with different values of I_d.

Fig. 8 shows that in a weak grid with short circuit ratio (SCR) of 3.18 (parameters in Table 1 are used), when $I_d = 50$A, one of the system's characteristic loci (λ_1) encircles the critical point $(-1, 0j)$, which indicates that the system is unstable; but when $I_d = -50$A, none of the system's characteristic loci encircles the critical point, and the system is stable. Fig. 9 shows the simulation results of output currents and it is consistent with theoretical analysis in Fig. 8.

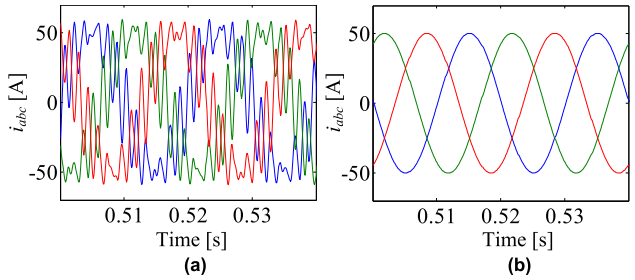

FIGURE 9. Simulation results of output currents with different values of I_d: (a) $I_d = 50$ A, and (b) $I_d = -50$ A.

Now it can be concluded that, according to (11) and Fig. 7, a weak grid with $\boldsymbol{Z_g} \neq 0$ provides a path (depending on the power flow direction of the converter) that may introduce positive feedback via PLL into the system. It can be observed that the feedback gain, along *loop 2* shown in Fig. 7 together with the specific expression in (11), is determined by the grid equivalent impedance $\boldsymbol{Z_g}$, power rating (magnitude of I_d) and the parameters of PLL and current PI controllers. So attempts to decline the feedback gain along *loop 2* will be benefit to the stability of the converter. However, reducing the control parameters of PLL and current PI controller is perhaps the best choice for stability improvement of the converter, especially when the converter is connected to a weak grid and with high power ratings. As a matter of fact, the interaction between CCL and PLL can be intuitively revealed by the feedback gain of *loop 2*.

The influences of the feedback gain of *loop 2* on converter's stability can also be revealed by the output admittances of the converter. Note that $\tilde{v}_q^s$ is introduced into the control system by PLL, thus the feedback gain only has impact on the converter output admittances Y_{eqidq} and Y_{eqiqq}. Fig. 10 shows the admittance Y_{eqiqq} of the converter with different parameters. It indicates that when the converter

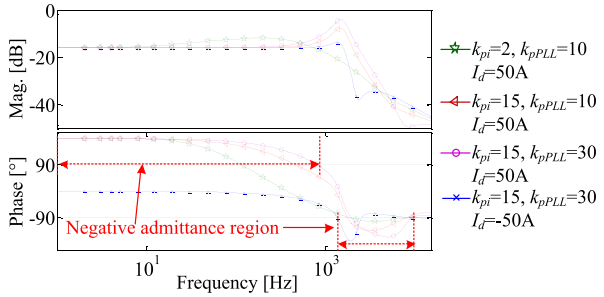

FIGURE 10. Admittance Y_{eqiqq} of the converter with different parameters.

working in inverter mode ($I_d > 0$) and with larger k_{pi} and k_{pPLL}, the admittance Y_{eqiqq} will have a wider negative admittance behavior (i.e., namely negative damping effects, as discussed in [12]–[14], [21]) both in relatively low and high frequency region, in which negative admittance behavior in relatively low frequency region is due to active power flows from dc-side to ac-side of the converter, and in relatively high frequency region due to the time delay in digital control systems. When the converter working in rectifier mode ($I_d < 0$), the frequency range of negative admittance behavior of Y_{eqiqq} decreases—or rather, the negative admittance behavior in relatively low frequency region disappears. Thus the converter in rectifier mode has a better stability. It should be noted that due to the time delay in digital control systems, the negative feedback system (e.g., the converter in rectifier mode) will also become unstable with inappropriate control parameters, and for example, when $I_d = -50$A (rectifier mode), Y_{eqiqq} in Fig 10 still has negative admittance region in relatively high frequency range due to the time delay.

According to (11), when $I_q > 0$, *loop 2* introduces partial positive feedback via diagonal element and partial negative feedback via off-diagonal element into the system. Normally the diagonal element is dominant in feedback control, thus the positive feedback via diagonal element will be dominant on the system's stability. So the stability of the converter that absorbs reactive power ($I_q < 0$) will be better than that of the converter that generates reactive power ($I_q > 0$).

In fact, the converter's outputs I_d and I_q are limited by its capacity, namely $D_d^2 + D_q^2 \leq 1$. Fig. 11 (a) shows the stable regions of the converter in a weak grid. Curve 1 denotes the capacity boundary of the converter; curve 2 denotes the stability boundary of the converter with parameters $k_{pi} = 10$ and $k_{pPLL} = 40$. So the "stable region" refers to the areas surrounded by curve 1 and curve 2. It indicates that the converter's stable region in a weak grid is much smaller than its capacity region (curve 1).

Fig. 11 (a) also shows that the converter's stable region is asymmetric with respect to line $I_d = 0$ and $I_q = 0$. Due to the converter's capacity limitation, there is no much meaning to discuss its asymmetry with respect to line $I_q = 0$. In terms of its asymmetry with respect to line $I_d = 0$, we can find that the converter working in rectifier mode ($P < 0$) has much larger stable region areas than working in inverter mode ($P > 0$);

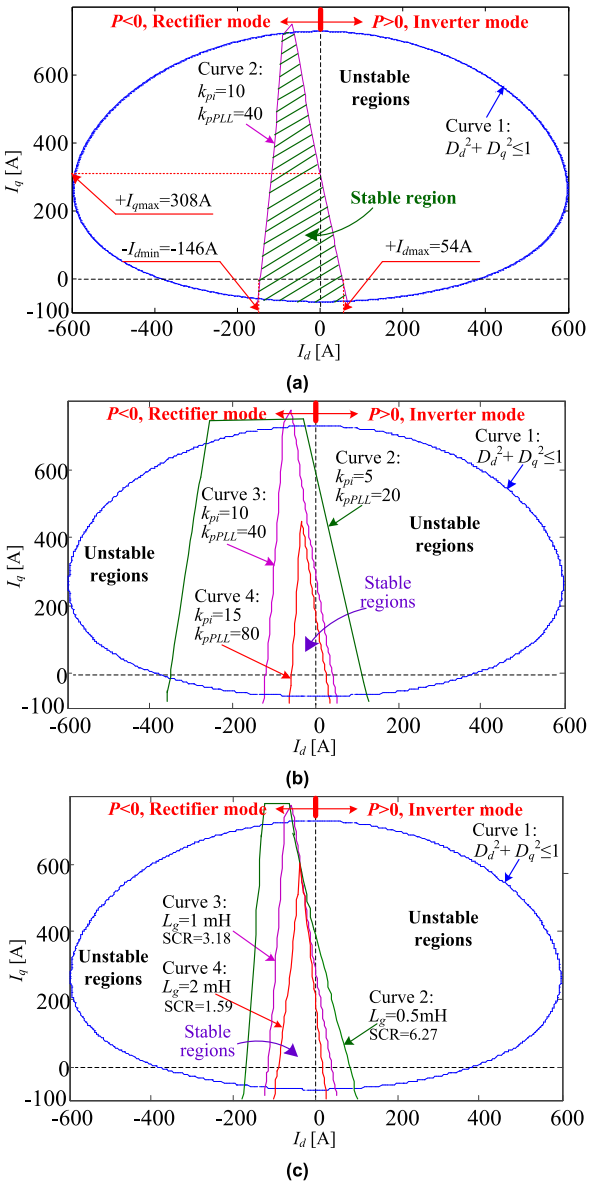

FIGURE 11. Stable region of the converter in weak grid with different parameters: (a) $k_{pi} = 10$, $k_{pPLL} = 40$, $L_g = 1$mH (SCR = 3.18), (b) different control parameters of the converter and $L_g = 1$mH (SCR = 3.18), and (c) $k_{pi} = 10$, $k_{pPLL} = 40$, and different grid impedance.

it means that the converter working in rectifier mode will have more stability margins than working in inverter mode.

Figs. 11 (b) and (c) show the stable regions of the converter in a weak grid with different control parameters and grid impedance, respectively. It can be found that, although the system's stable regions vary with different parameters, they are all asymmetric, and the converter working in rectifier mode ($P < 0$) has much larger stable region areas than working in inverter mode ($P > 0$). It means that the positive feedback effects exist in the system no matter what parameters of the system are. In fact, the detailed interpretation of the positive feedback introduced by PLL in a weak grid also indicates that the existence of positive feedback effects is the

intrinsic property of the bidirectional ac-dc converter when connected to a weak grid, and determined by the operating mechanism of the converter rather than the values of the parameters, but the influences of positive feedback on the system's stability are determined the values of the parameters.

The stable region shown in Fig. 11 (a) could provide some advice for the grid-tied converter's design. For example, in low voltage ride through (LVRT) operation for grid-tied inverters [27], in order to keep the grid voltage and frequency stable, the inverter ($P > 0$) is required to provide extra power for the grid, which possibly makes the inverter run to unstable regions. So the inverter's output power should be set reasonably according to its stable region.

Additionally, from Fig. 11 (a) it can be seen that, when the converter operates with a unity power factor ($I_q = 0$), the upper limit value $I_{d\max}$ (54A) is smaller than the lower limit value $I_{d\min}$ (146A). This also means that the stability margin of the converter working in rectifier mode is better than that of the converter working in inverter mode. On the other hand, it can be seen that the upper limit value $I_{q\max}$ (308A, and $I_d = 0$) is much larger than the upper limit value $I_{d\max}$ ($I_q = 0$), which indicates that reactive power has a slighter negative influence on the converter's stability than active power. Working in different operating conditions the bidirectional converters will have different stability margins, and therefore the converters should be designed properly according to their stable regions.

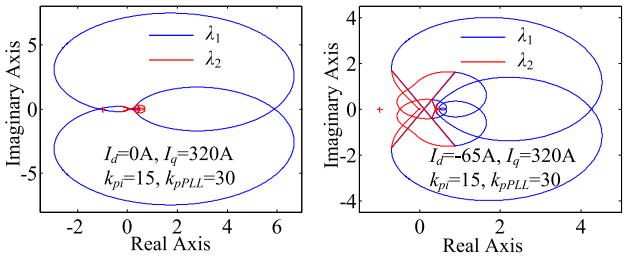

FIGURE 12. GNC plots of Li with different values of I_d and I_q.

An interesting phenomenon can be found in Fig. 12. It shows that when $I_d = 0$A and $I_q = 320$A, the system is unstable; but when $I_d = -65$A and $I_q = 320$A, the system becomes stable. This means that the positive feedback effect introduced by too large I_q could, to some extent, be offset by the negative feedback effect introduced by minus I_d. Fig. 13 shows the simulation results of the output currents that are consistent with the theoretical analysis in Fig. 12.

Based on the analysis above, it can be seen that by using the concept of positive feedback, signals (output current or voltage of the converter) can be traced along the positive feedback, and interpreted physically, to provide an intuitive understanding of the instability mechanisms of bidirectional converters in different operating conditions. Such merits cannot be directly realized by the impedance-based analyzing (as shown in Figs. 8 and 12, for example) that simply based on GNC.

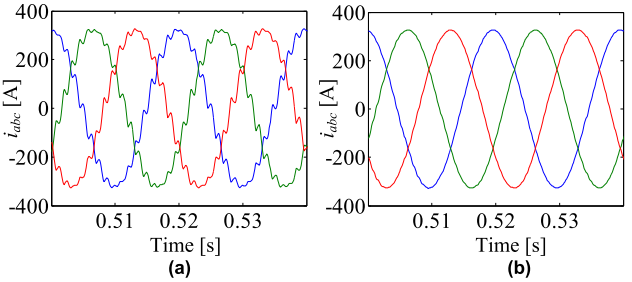

FIGURE 13. Simulation results of output currents with different values of I_d and I_q: (a) $I_d = 0$ A, $I_q = 320$A, and (b) $I_d = -65$ A, $I_q = 320$A.

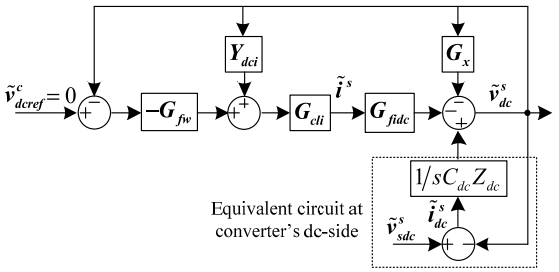

FIGURE 14. Small-signal block diagram of the converter with VCL.

IV. STABILITY ANALYSIS OF THE CONVERTER IN TERMS OF VOLTAGE CONTROL LOOP (VCL)

In this section, first of all, the stability analysis of VCL of the converter will be investigated by assuming that the converter is connected to a strong grid to get rid of the interaction between PLL and VCL, too. Subsequently, based on the full order small-signal impedance model that combines PLL and VCL of the converter, the influence of VCL on the stability of the converter in a weak grid is studied.

A. STABILITY ANALYSIS OF CONVERTER'S VCL CONSIDERING OPERATING CONDITIONS

When the dc-side of a converter is not supplied by a stiff dc voltage source, supposing that $\tilde{\boldsymbol{v}}^{\boldsymbol{s}}_{\boldsymbol{sdc}} = \begin{bmatrix} \tilde{v}^s_{sdc} & 0 \end{bmatrix}^T$ is the small-signal perturbation on converter's dc-side with the equivalent impedance Z_{dc}, then one can get that

$$\tilde{\boldsymbol{i}}^{\boldsymbol{s}}_{\boldsymbol{dc}} = \frac{1}{Z_{dc}} \left(\tilde{\boldsymbol{v}}^{\boldsymbol{s}}_{\boldsymbol{sdc}} - \tilde{\boldsymbol{v}}^{\boldsymbol{s}}_{\boldsymbol{dc}} \right) \tag{12}$$

Fig. 14 shows the small-signal block diagram of the converter with a voltage control loop when the converter is connected to a strong grid. It can be found that the reflection of the dc-side impedance Z_{dc} in the ac-side control system is mainly influenced by dc-link capacitor C_{dc}, and a large capacitance will result in decoupling between ac- and dc-sides of the converter. When the converter operates as a constant power load, the dc-side impedance Z_{dc} will be equal to the load impedance R_{load}.

Fig. 15 shows the structure and small-signal block diagram of a bidirectional ac-dc converter, in which an ideal current source is connected to the dc-side of the converter to control

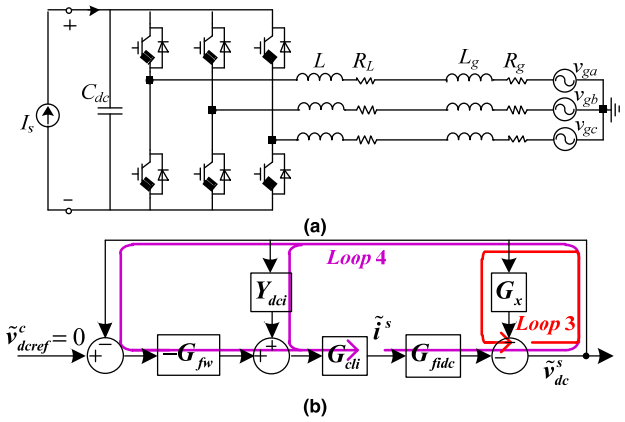

FIGURE 15. Bidirectional ac-dc converter with an ideal current source: (a) structure, and (b) small-signal block diagram.

its power flow direction, thus the control part related to the dc-side impedance Z_{dc} is not included.

According to Fig. 15, the open loop transfer function matrix of the converter's voltage loop can be expressed as

$$\boldsymbol{G_{opv}} = (\boldsymbol{I} + \boldsymbol{G_x})^{-1}\, \boldsymbol{G_{fidc}} \boldsymbol{G_{cli}} \left(\boldsymbol{Y_{dci}} + \boldsymbol{G_{fw}}\right) \tag{13}$$

where matrices $\boldsymbol{G_x}$, $\boldsymbol{G_{fidc}}$ and $\boldsymbol{G_{fw}}$ are given as follows

$$\boldsymbol{G_x} = \boldsymbol{G_{ddc}} \boldsymbol{G_{del}} \boldsymbol{G_{nor}} \boldsymbol{G_{ci}} \boldsymbol{G_{cv}} \tag{14}$$

$$\boldsymbol{G_{fidc}} = \boldsymbol{G_{idc}} - \boldsymbol{G_{ddc}} \boldsymbol{G_{del}} \boldsymbol{G_{nor}} \left(\boldsymbol{G_{ci}} - \boldsymbol{G_{dec}}\right) \tag{15}$$

$$\boldsymbol{G_{fw}} = \boldsymbol{Y_{out}} \boldsymbol{G_{del}} \boldsymbol{G_{nor}} \boldsymbol{G_{ci}} \boldsymbol{G_{cv}} \tag{16}$$

Assume that $G_{opv} = [\boldsymbol{G_{opv}}]_{1,1}$, where "$[\ ]_{1,1}$" denotes the 1st row and the 1st column element of a matrix. The stability of the converter's voltage loop can be judged by Bode diagram of G_{opv}, i.e., the magnitude of G_{opv} is supposed to be always negative when the phase crosses $-180°$.

For *loop 3* in Fig. 15, $\boldsymbol{G_x}$ is expressed as

$$\boldsymbol{G_x} = \frac{3}{s \cdot 4C_{dc}} \frac{2}{V_{dc}} G_{del} G_{ci} G_{cv} \begin{bmatrix} I_d & I_q \\ 0 & 0 \end{bmatrix} \tag{17}$$

For *loop 4*, assuming that $G_{del} \approx 1$, and then $\boldsymbol{G_{fidc}}$ can be expressed as

$$\boldsymbol{G_{fidc}} \approx \frac{3}{s \cdot 4C_{dc}} \frac{2}{V_{dc}} \begin{bmatrix} V_d - G_{ci} I_d & -G_{ci} I_q \\ 0 & 0 \end{bmatrix} \tag{18}$$

Similarly, the influences of the interactions between VCL and CCL on the stability of VCL can be revealed by positive feedback gains. From (17) and (18), it can be found that, when $I_d < 0$, partial positive feedback is introduced by *loop 3* and partial negative feedback is introduced by *loop 4* into the control system. The feedback gain of *loop 3* is determined by G_{ci}, G_{cv}, C_{dc} and V_{dc}—these parameters will indeed have effects on the stability of VCL; the feedback gain of *loop 4* is determined not only by G_{ci}, C_{dc} and V_{dc}, but by G_{ci} and G_{cv} contained in $\boldsymbol{G_{fw}}$ [see its specific expression in (16)], thus parameter G_{ci} will have double effect on *loop 4* than on *loop 3*.

It can be perceived that when $I_d < 0$, the positive feedback effect introduced by *loop 3* will be offset by the negative feedback effect introduced by *loop 4*. Whether the stability of VCL in rectifier mode is worse than in inverter mode will depend on whether the strength of feedback effect of *loop 3* is stronger than that of *loop 4*. But with parameters of G_{ci} increasing, the positive feedback effect introduced by *loop 3* could be completely offset and even over offset, then the stability of VCL in inverter mode could be worse than in rectifier mode. Note that the converter's VCL mainly relates to active current I_d, thus the influence of reactive current I_q on VCL can be neglected.

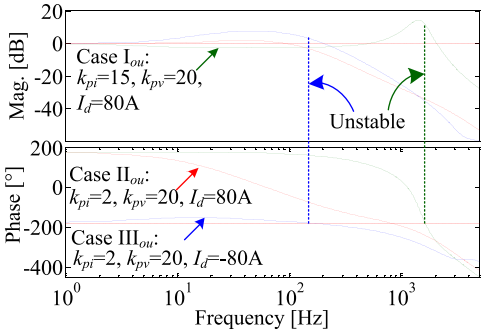

FIGURE 16. Bode diagram of G_{opv} with different values of I_d and $I_q k_{ii} = 300$, $k_{iv} = 5$.

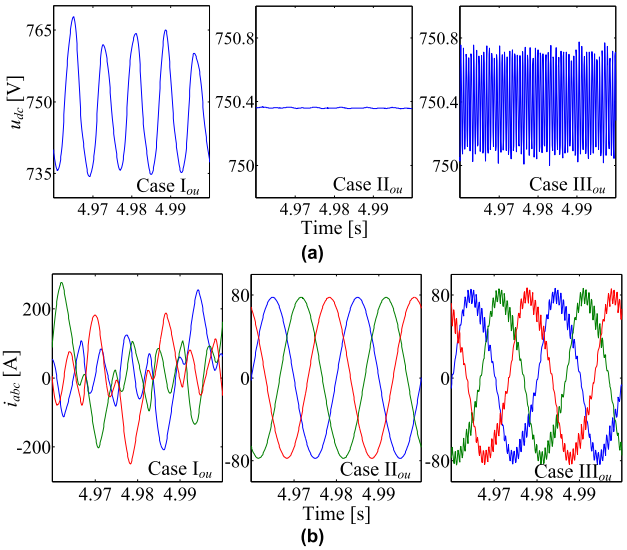

FIGURE 17. Simulation results of the converter: (a) dc-link voltage and (b) output currents.

The above theoretical analyses can be validated by the stability analysis in Fig. 16 and simulations in Fig 17 (the parameters of the voltage control loop of converter are also given in Table 1). Fig. 16 shows the Bode diagram of G_{opv} with different control parameters. It can be seen that with $k_{pi} = 2$ and $k_{pv} = 20$, when $I_d = -80$A the magnitude of G_{opv} is positive when the phase crosses $-180°$, and it means that the system is unstable; but when $I_d = 80$A the system is stable. However with k_{pi} increasing to 15, the system becomes unstable. The simulation results of dc-link voltage and output currents shown in Fig. 17 are consistent with the stability analysis in Fig. 16.

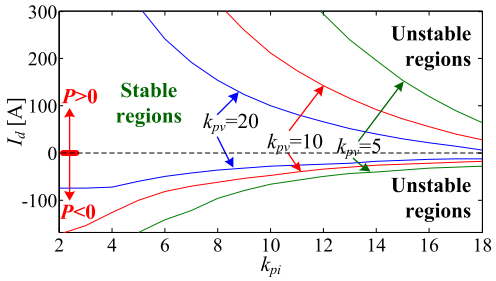

FIGURE 18. Stable regions of the converter's VCL.

Fig. 18 shows the stable regions of the VCL with different control parameters. It can be found that with k_{pv} increasing, the stable regions of the converter's outer voltage control loop become small. And with relatively small k_{pi}, the stability of the converter in inverter mode ($I_d > 0$) is better than that of the converter in rectifier mode ($I_d < 0$); but when k_{pi} is increasing, the stability of the converter in inverter mode becomes worse, and even worse than that of the converter working in rectifier mode, which is due to the double effect of G_{ci} on *loop 4*. Thus, against [21], VCL of the converter not always has worse negative effect in rectifier mode than that of inverter mode.

The stable dc-link voltage of the converter is the guarantee of achieving pulse width modulation to generate standard sine wave, so the VCL of the converter should also be designed properly when working in different operating conditions. And the investigation of instability mechanism of VCL in this paper would be helpful for the converters' parameters design.

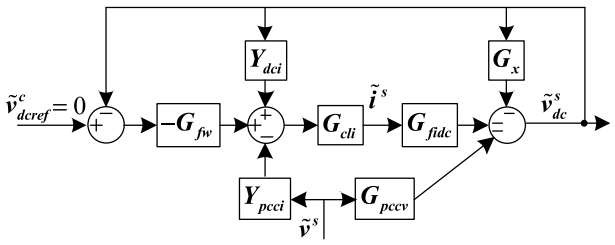

FIGURE 19. Small-signal block diagram of the converter with VCL.

B. INFLUENCE OF VCL ON CONVERTER'S STABILITY IN WEAK GRID

Fig. 19 shows the small-signal block diagram of the converter with VCL. The full order small-signal output admittance of the converter with VCL can be expressed as

$$\boldsymbol{Y_{eqv}} = \boldsymbol{G_{clv}}\left\{\boldsymbol{Y_{eqi}} + \boldsymbol{G_{cli}}\left(\boldsymbol{Y_{dci}} + \boldsymbol{G_{fw}}\right)(\boldsymbol{I} + \boldsymbol{G_x})^{-1}\boldsymbol{G_{pccv}}\right\} \quad (19)$$

where $\boldsymbol{G_{clv}}$ and $\boldsymbol{G_{pccv}}$ are given by

$$\boldsymbol{G_{clv}} = \left\{\boldsymbol{I} + \boldsymbol{G_{cli}}\left(\boldsymbol{Y_{dci}} + \boldsymbol{G_{fw}}\right)(\boldsymbol{I} + \boldsymbol{G_x})^{-1}\boldsymbol{G_{fidc}}\right\}^{-1}\boldsymbol{G_{cli}} \quad (20)$$

$$\boldsymbol{G_{pccv}} = \boldsymbol{G_{ddc}}\boldsymbol{G_{del}}\boldsymbol{G_{pllx}} \quad (21)$$

From (20) we can see that the output admittance $\boldsymbol{Y_{eqi}}$ is actually included in the output admittance $\boldsymbol{Y_{eqv}}$, and the differences between $\boldsymbol{Y_{eqi}}$ and $\boldsymbol{Y_{eqv}}$ is due to the existence of VCL. Fig. 20 shows the admittance of the converter with different voltage control parameters and dc-link capacitor. In Fig. 20, the curves with and without marks denote the admittance $\boldsymbol{Y_{eqi}}$ and $\boldsymbol{Y_{eqv}}$, respectively. It can be observed that the differences between $\boldsymbol{Y_{eqi}}$ and $\boldsymbol{Y_{eqv}}$ are relatively obvious in low frequency range, and their differences reduce as k_{pv} decreases (i.e., the control bandwidth of voltage loop decreasing) or dc-link capacitor increases. From Fig.20, it can also be found that VCL has no influence on *q-q* channel admittance. So in terms of influence path, VCL has influence on the converter's stability mainly through *d-d* channel admittance, in contrast with PLL affecting converter's stability mainly through *q-q* channel admittance.

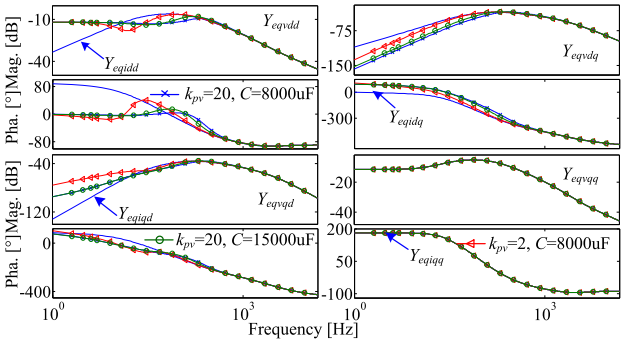

FIGURE 20. Admittance of the converter with/without VCL.

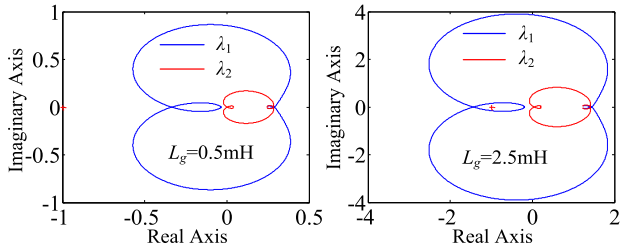

FIGURE 21. GNC plots of L_v with different grid impedance. $k_{pi} = 2$, $k_{pv} = 10$, $I_d = -80$ A and $k_{pPLL} = 2$.

For the grid-tied converter with a VCL, the stabilities of CCL and VCL are the preconditions of the converter's stability. Then the stability of the converter in a weak grid can be judged by using GNC through the matrix $\boldsymbol{L_v} = \boldsymbol{Y_{eqv}}\boldsymbol{Z_g}$. Fig. 21 shows GNC plots of $\boldsymbol{L_v}$ with different grid impedance. It can be seen that when the converter is connected a grid with $L_g = 0.5$mH (SCR = 6.27), it is stable; but when connected to the grid with $L_g = 2.5$mH (SCR = 1.27), the converter becomes unstable. Fig. 22 shows the simulation results of output currents of the converter. It can be found that without voltage control loop, i.e., the converter's dc-side is supplied by a stiff dc voltage source (i.e., without VCL), the converter is stable with SCR = 1.27; and with VCL, the converter is stable with SCR = 6.27; but when SCR decreases to 1.27, the converter becomes unstable. This means that the converter's stability could be impaired by VCL in a weak grid.

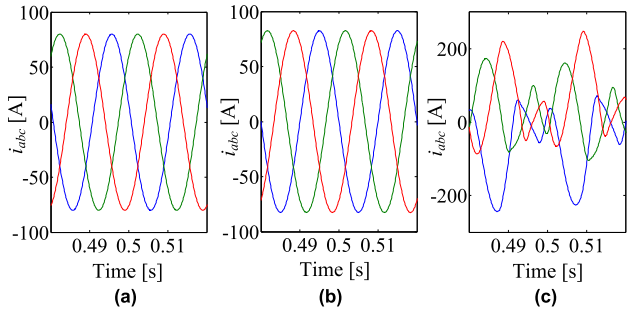

FIGURE 22. Simulation results of converter's output currents with/without VCL in a weak grid: (a) $L_g = 2.5$ mH (SCR = 1.27) without VCL, (b) $L_g = 0.5$ mH (SCR = 6.27) with VCL, and (c) $L_g = 2.5$ mH (SCR = 1.27) with VCL.

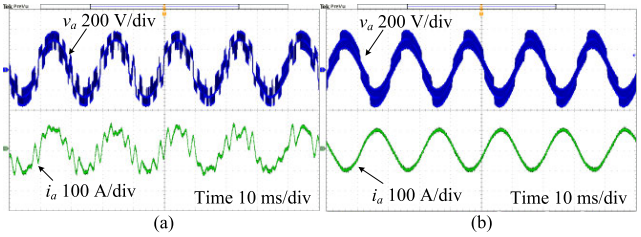

FIGURE 23. Output current of the converter and PCC voltage without voltage control loop with $L_g = 1$ mH (SCR = 3.18), $k_{pi} = 10$ and $k_{pPLL} = 20$: (a) $I_d = 100$ A, $I_q = 0$ A (inverter mode), and (b) $I_d = -100$ A, $I_q = 0$ A (rectifier mode).

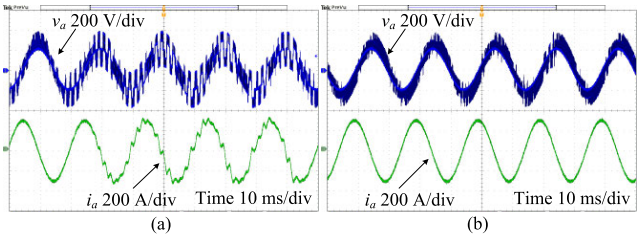

FIGURE 24. Output current of the converter and PCC voltage without voltage control loop with $L_g = 1$ mH (SCR = 3.18), $k_{pi} = 10$ and $k_{pPLL} = 20$: (a) $I_d = 0$ A, $I_q = 300$ A, and (b) $I_d = -50$ A, $I_q = 300$ A.

V. EXPERIMENTAL VERIFICATION

The control hardware in the loop (CHIL) [2], [29] experiments of the grid-tied converter are carried out, as shown in Figs. 23-26, to validate the theoretical analysis and simulations, and the parameters listed in Table 1 are used.

Fig. 23 shows the output current of the converter and PCC voltage (phase A's current i_a and voltage v_a are taken as examples). It can be seen that in a weak grid, the stability of the converter in rectifier mode is better than that of the converter in inverter mode. Fig. 24 shows that with too large I_q the converter is unstable, but the converter becomes stable when the converter output $I_d = -50$A, which means that minus I_d can offsets positive feedback e ffect introduced by large positive I_q.

Fig. 25 indicates that with a small k_{pi}, the stability of the converter working in inverter mode is better than that of the converter working in rectifier mode; but when k_{pi} increased to 15, the system becomes unstable, which indicates that a larger k_{pi} can lead to instability of the converter.

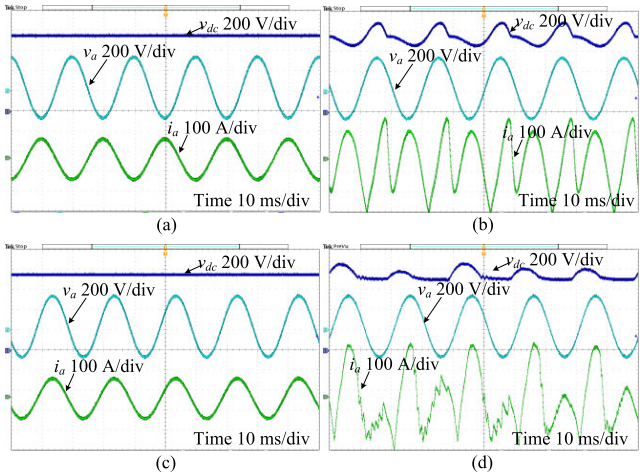

FIGURE 25. Output current and dc-link voltage of the converter and PCC voltage with $L_g = 0$ mH and $k_{pPLL} = 2$: (a) $k_{pi} = 2$, $k_{pv} = 5$, $I_d = -100$ A, $I_q = 0$ A (rectifier mode), (b) $k_{pi} = 2$, $k_{pv} = 20$, $I_d = -100$ A, $I_q = 0$ A (rectifier mode), (c) $k_{pi} = 2$, $k_{pv} = 20$, $I_d = 100$ A, $I_q = 0$ A (inverter mode), and (b) $k_{pi} = 15$, $k_{pv} = 20$, $I_d = 100$ A, $I_q = 0$ A (inverter mode).

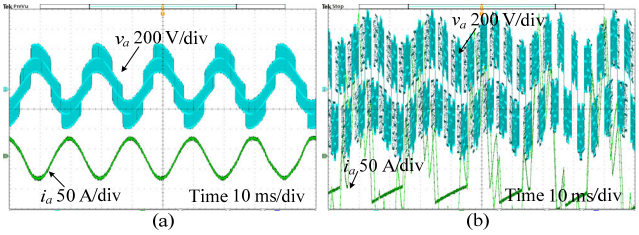

FIGURE 26. Output current of the converter and PCC voltage with $L_g = 2.5$ mH (SCR = 1.27), $k_{pi} = 2$, $k_{pv} = 5$ and $k_{pPLL} = 2$: (a) $I_d = -50$ A, $I_q = 0$ A without VCL, and (b) $I_d = -50$ A, $I_q = 0$ A with VCL.

Fig. 26 shows that in a weak grid, the converter without VCL can be stable, but will become unstable if the VCL is included. This means that VCL has negative effects on the converter's stability.

VI. CONCLUSION

This paper presents a unified small-signal impedance model of the bidirectional ac-dc converter to investigate the stability performances of the bidirectional converters considering operating conditions. The concept of positive feedback is used to analyze the converter's instability mechanisms. It reveals that positive feedback effects are introduced by PLL and VCL of converters in weak ac grids, which could deteriorate the converter's stability. The positive feedback effect is basically depending on power the converters' flow directions; the converters will have different stability margins when working in different operating conditions. The positive feedback gains along positive feedback loops can intuitively reveal the influencing mechanisms of the parameters on the converter's stability. For the design of a converter used for bidirectional energy conversions, the traditional design criterion of converters [31] is still the footstone, but the operating conditions should be taken into account in the design of the bidirectional converters, and considering the positive feedback introduced by PLL and VCL, the values of the

parameters along the positive feedback paths are suggested to be reduced properly to enhance the converter's stability.

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