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A Novel Impedance-Network-Based Electric Spring

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ABSTRACT An electric spring (ES) can well maintain the balance between supply and demand to compensate for the intermittent nature of small-scale renewable energy resources (RES). Despite its popularity, the second generation of ES (ES-2) is deemed to have a few practical problems. The most conspicuous one is the requirement of accurate dead-time control is in the ES circuit to avoid bridge shoot-through problem, which is necessitated by the series-connection of multiple voltage sources and/or converters to realize a wide voltage range. This however could cause output voltage waveform distortions. In this study, inspired by the Z-source network structure, we propose a novel ES topology with a specifically designed impedance network, i.e., an impedance-network-based (i.e., a network of passive devices such as inductors and capacitors) ES (IN-ES), which intrinsically has a wide voltage range and is immune to the bridge shoot-through issue (i.e., switch tubes on the same bridge arm of the inverter are turned ON/OFF at the same time). Detailed theoretical derivation, simulation and experimentation are conducted in this study, which verify the unique advantageous features of the proposed IN-ES, demonstrating a wide voltage operation range, undistorted waveforms and safe operations.

INDEX TERMS Impedance-network-based electric spring, novel ES structure, bridge shoot-through, terminal voltage control.

NOMENCLATURE

V_{in}	DC input voltage of ESs
L_{s}	Inverter filter inductor
C_{s}	The penalty function
V_{g}	Voltage of emulated power grid
Z_{line}	Line impedance of emulated power grid
r_{line}	Line resistance of emulated power grid
x_{line}	Inductive reactance of DC emulated power grid
V_{es}	Compensation voltage of ESs
V_{nc}	Voltage across non-critical load
V_R	Resistance voltage of non-critical load
V_L	Reactance voltage of non-critical load
Z_{nc}	Non-critical load
Z_{c}	Critical load
V_{c}	Voltage across critical load
$I_{L_{\text{s}}}$	Filtered inductor current of inverter
I_{es}	Current through non-critical load
V_{C_1}	Voltage across DC side capacitance
V_{p}	Voltage across the inverter bridge
$E_{C_{\text{s}}}$	Capacitor stores energy
I_{i}	Equivalent current source current
P	Inverter AC side output power
$V_{\text{s-ref}}$	Nominal terminal voltage
$V_{\text{dc-load}}$	DC load voltage
V_{L_1}, V_{L_2}	Voltage of inductors L_1 and L_2
I_{L_1}, I_{L_2}	Current of inductors L_1 and L_2
$I_{\text{dc-load}}$	Current of DC Load
i_{C_1}	Current of capacitor C_1
$R_{\text{dc-load}}$	Resistance of DC Load
V_{CE}	IGBT turn-on voltage drop
P_D	Diode power loss
P_{r_L}	Inductor power loss
P_{r_c}	Capacitor power loss
P_{Loss}	Total power loss of the IN-ES
P_{S}	IGBT power loss

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RES	Renewable energy resources
SBI	Switched boost inverter
PLL	Phase lock loop
IN-ES	Impedance-network-based electric spring
ESR	Equivalent series resistance
RMS	Root mean square

I. INTRODUCTION

In recent years, renewable energy resources such as wind and solar have been widely recognized as a favorable alternative to mineral-based energy resources, due to their environmentally friendliness and inexhaustible availability [1], [2]. Enabled by the rapid development of power electronics technology, which reduces the side effects of their intermittent nature, an increasing amount of RESs are being integrated with the power grid. However, this new energy industry is facing many problems and obstacles. For instance, the low efficiency of renewable energy power generation is currently the main problem restraining its development. In addition, renewable energy power generation would cause energy waste due to its poor power quality. Both problems are mainly caused by the intermittency of wind and solar RESs, which makes heavily RES-integrated grids difficult to balance load demands and power supply. One of the traditional solutions is to mitigate this problem by employing demand-side energy management techniques such as energy storage [3], real-time pricing [4], [5], load scheduling [6]–[8] and direct on-off load control [9].

In 2012, researchers proposed a novel hardware-based demand-side energy management strategy, i.e., the electric spring, trying to tackle the same problem. The invented ESs are able to reduce voltage and frequency fluctuations [10]–[12], improve power quality [12], [13], enhance demand-side energy management of the power grid [14], and diminish energy imbalance in built environments [15]. To date, three versions of ES have been proposed. The first generation of ES (ES-1) includes capacitors and power inverters as shown in Fig. 1(a) [16], which collectively can provide reactive power regulation to non-critical loads (i.e., loads that can work under a certain range of voltage levels) connected in series with the ES. The second generation of ES (ES-2) is also connected in series with non-critical loads as shown in Fig. 1(b), where ES-2 replaces the capacitor in ES-1 with a battery storage system [17], which makes it possible to compensate both active and reactive power. The third generation of ES (ES-B2B) consists of two half-bridge back-to-back converters as shown in Fig. 1(c), which, in addition to ES-2's functions, can extract power from the power grid [18].

The above-mentioned ES structures have been experimentally proven to be able to maintain the supply and demand balance in RES-integrated power systems. However, the DC side of the most popular ES-2 requires a high DC voltage to achieve a wide range of voltage compensation and operate in an environment with electromagnetic interference, causing shoot-through of inverter bridges and subsequent damages.

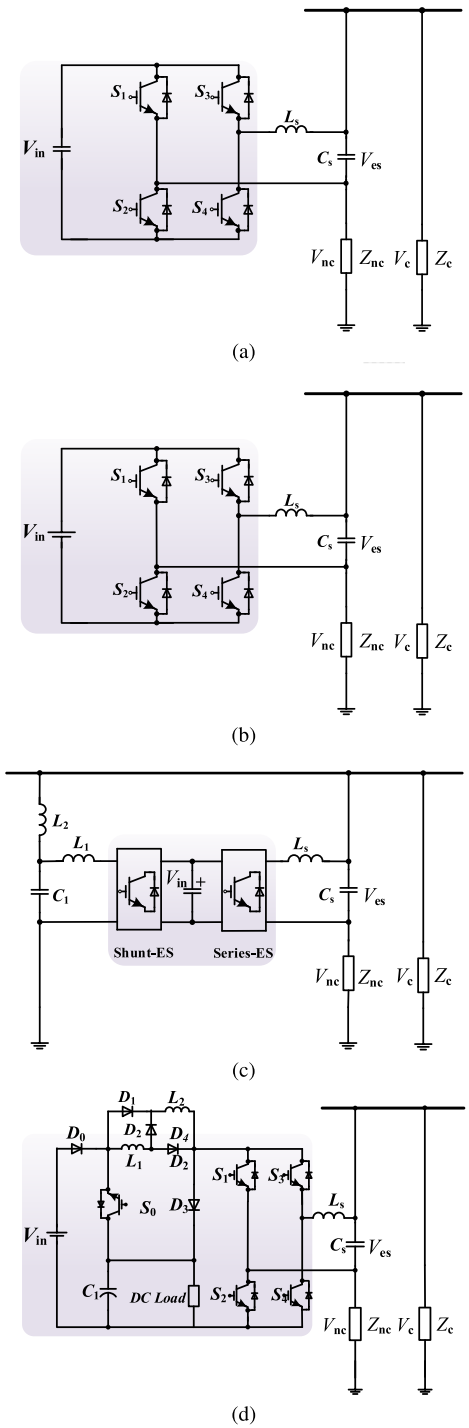

FIGURE 1. Schematics of electric springs: (a) ES-1; (b) ES-2; (c) ES-B2B (third generation); and (d) the proposed IN-ES.

To achieve a high DC voltage for ES-2, traditionally, a number of batteries or boost converters are employed and installed on the DC side to increase the DC voltage, thereby increasing the output voltage of the ES-2. High voltage gain boost converters may also be used, which can be achieved using various methods, e.g., [19] and [20]. However, using the above methods to increase the DC side voltage of ES may

result in shoot-through of the inverter bridge. The traditional solution is to insert a dead-time in the drive signal to avoid shoot-through of the inverter bridge, but the insertion of the dead-time control will cause the distortion of the output voltage waveform [21], [22].

To solve the problems in the existing ES structures, expanding from the design ideas from [23]–[26]. In this paper, we propose a novel impedance-network-based ES, as shown in Fig.1(d), and the IN-ES topology is analyzed with reference to the analytical methods of quasi Z-source inverter topologies in [27]–[29]. The impedance network resembles a quasi-Z-network, which is connected to the DC side of the existing inverter. Compared with the second generation of electric spring, the proposed IN-ES is able to boost the DC side input voltage by the introduced impedance network and avoid the loss caused by the two-stage converter, which can easily achieve a wide range of voltage compensation with a lower DC input voltage. It does not need many batteries or boost converters to be installed on the DC side. So the size of the battery can be reduced, which attests cost-effectiveness. In other words, the function of a wide output range facilitates the design of power supply systems to achieve small size and low costs. In addition, with the specifically designed inductor in the IN-ES, inverter bridges are immune to shoot-through issues, which therefore does not require the conventional dead-time control, thus preventing waveform distortion of the output voltage. The IN-ES can also increase system stability. In conclusion, the proposed IN-ES with the quasi-Z-network has high engineering and application values. To verify the efficacy of the proposed IN-ES structure, theoretical analyses, software simulation and hardware experimentation are conducted in this study, and the results agree well with the expected features of the proposed IN-ES.

The rest of the paper is organized as follows. In Section II, the topology, working principle and operation modes of the proposed IN-ES are illustrated, which is followed by the closed-loop control design in Section III. Simulation and experimentation are reported in Sections IV and V, respectively. Finally, this paper concludes in Section VI.

II. THE PROPOSED IN-ES

This section explains the topology, working principle and operation modes of the proposed IN-ES, and its superiority over its conventional counterparts.

A. TOPOLOGY OF IN-ES

As briefly mentioned in the introduction, typical topologies of existing ESs include half-bridge inverter, a full-bridge inverter, and a three-phase inverter. The ES-1 has the advantage of a simple structure and easy implementation, but it can only provide reactive power compensation [30]. With battery storage system, ES-2 has the capability to provide both active and reactive power compensation, which has been widely used for voltage stabilization and power factor correction [31]. The back-to-back converter topology enables ES-B2B to connect to the electric grid, and export and import electric power to and from the grid. In addition to active and reactive power compensation, ES-B2B can also suppress harmonics, improving power quality [18].

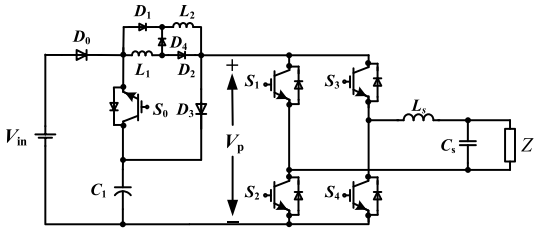

FIGURE 2. Schematic of SBI (Z: AC Load).

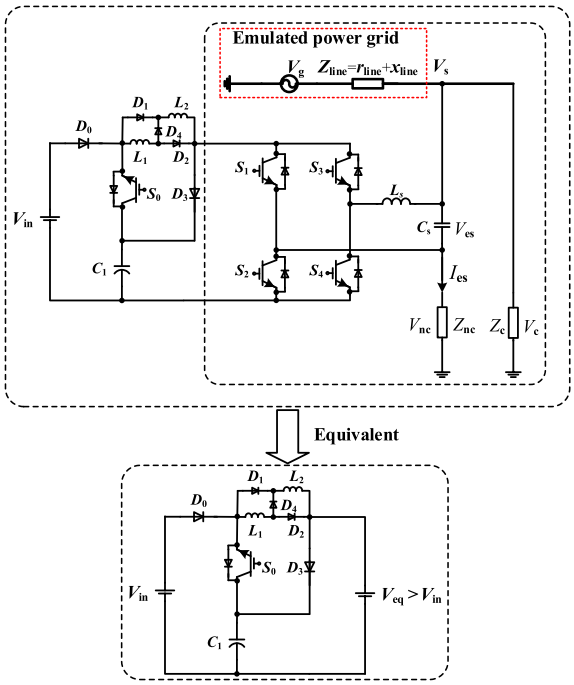

FIGURE 3. Application of SBI as ES in power grid and its equivalent model.

A switched boost inverter (SBI) that provides power to AC load is shown in Fig. 2. The SBI as ES application circuit with power grid and the equivalent model are shown in Fig. 3, it can be clearly seen that the voltage of the DC-side boost capacitor at this time may be disturbed by the energy rectified from the backward power flow of AC inverter bridge, causing the capacitor V_{C_1} damaged and then further make the boost converter failed. The circuit of the proposed IN-ES connected with power grid is shown as Fig. 4, which couples a switch-boost quasi-Z-network and DC load. The DC load will pave an energy path for bidirectional energy consumption at the boost stage, and further for grid terminal voltage control. When the critical load voltage is unstable, the proposed IN-ES will boost DC input voltage V_{in} to compensate for active or reactive power of the power grid, which will stabilize the critical load Z_c voltage.

TABLE 1 summarizes the advantages and disadvantages of the proposed IN-ES and the existing ESs.

TABLE 1. Advantages and disadvantages of ESs.

Topology	Advantage	Disadvantage
ES-1	Low cost, small volume	Bridge cannot shoot-through
ES-2	Compensation for active and reactive power	Large volume and high cost, bridge cannot shoot-through
ES-B2B	Wide range of voltage regulation	Bridge cannot shoot-through
IN-ES	Wide range of voltage regulation, bridge shoot-through	DC power loss

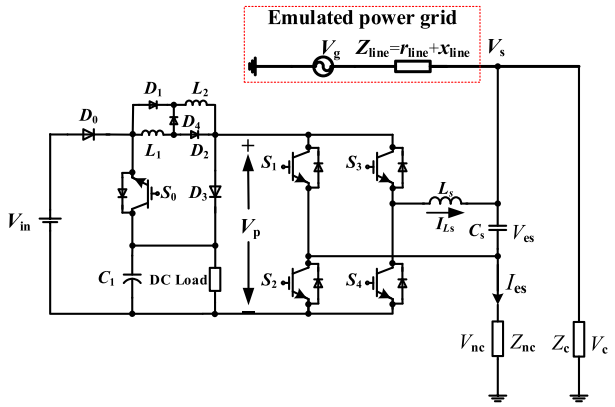

FIGURE 4. Circuit of the proposed IN-ES (Z_c: critical load, and V_c: voltage across the critical load, i.e., loads that need to work at a constant voltage).

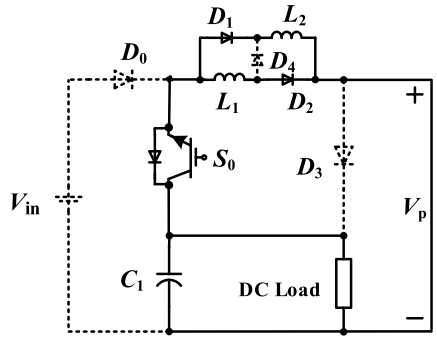

FIGURE 5. Equivalent circuit of the proposed IN-ES in shoot-through state.

B. OPERATING PRINCIPLE

The proposed IN-ES has two operational states, as shown in Figs. 5 and 6, where the dotted line represents line disconnection. Fig. 5 shows the equivalent circuit with shoot-through state, and Fig. 6 depicts the equivalent circuit in the non-shoot-through state, where $L_1 = L_2$.

As shown the shoot-through state time (last T_0) of the proposed IN-ES in Fig. 5, the diodes D_1, D_2 and switch S_0 are on, the diodes D_0, D_3 and D_4 are off. At the same time, current flows from capacitor C_1 to inductor, load and shoot-through switch S_0, and the corresponding equations for the shoot-through state are

$$\begin{cases} -V_{C_1} + V_{L_1} = -V_{C_1} + V_{L_2} = 0, \\ V_{\rm p} = 0. \end{cases} \tag{1}$$

$$\begin{cases} I_{L_1} = I_{L_2}, \\ i_{C_1} = I_{L_1} + I_{L_2} + I_{\rm dc-load} = 2I_{L_1} + I_{\rm dc-load}. \end{cases} \tag{2}$$

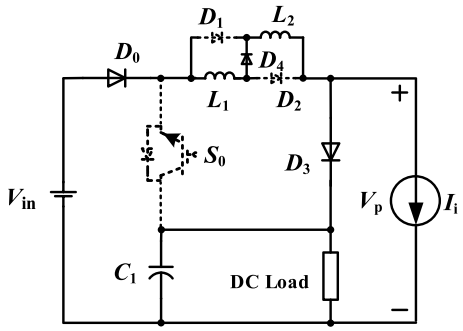

FIGURE 6. Equivalent circuit of non-shoot-through state of the proposed IN-ES.

According to (1), we have

$$\begin{cases} V_{C_1} = V_{L_1} = V_{L_2}, \\ V_{\rm p} = 0. \end{cases} \tag{3}$$

When it works in the non-shoot-through state as shown in Fig. 6, during the non-shoot-through time T_1, D_0, D_3 and D_4 are on, while D_1, D_2 and S_0 are off. Similarly, current flows from voltage source $V_{\rm in}$ and inductors L_1 and L_2 to capacitor C_1 and the load, which results in equations as

$$\begin{cases} -V_{\rm in} + V_{L_1} + V_{L_2} + V_{C_1} = 0, \\ V_{\rm p} = V_{C_1}. \end{cases} \tag{4}$$

$$\begin{cases} I_{L_1} = I_{L_2}, \\ i_{C_1} = I_{L_1} - I_{\rm dc-load} - I_{\rm i} = I_{L_2} - I_{\rm dc-load} - I_{\rm i}. \end{cases} \tag{5}$$

The switching interval between these two states is negligible, and thus one can assume voltage of inductors L_1 and L_2, namely V_{L_1} and V_{L_2} are approximately equal, and one has

$$\begin{cases} V_{L_1} = \dfrac{V_{\rm in} - V_{C_1}}{2}, \\ V_{\rm p} = V_{C_1}. \end{cases} \tag{6}$$

The above two states operate alternatively during one switching period, i.e., $T = T_0 + T_1$. According to the volt-second balance and ampere-second balance principle, we have

$$V_{L_1} = \bar{v}_{L_1} = \frac{T_0 V_{C_1} + \dfrac{1}{2} T_1 \left(V_{\rm in} - V_{C_1}\right)}{T} = 0. \tag{7}$$

$$\left(I_{L_1} - I_{\rm dc-load} - I_{\rm i}\right) T_1 = \left(2I_{L_1} + I_{\rm dc-load}\right) T_0. \tag{8}$$

If shoot-through duty ratio is

$$d = \frac{T_0}{T}, \tag{9}$$

then we can have

$$dV_{C_1} + \frac{1}{2}(1-d)\left(V_{\text{in}} - V_{C_1}\right) = 0,$$
$$\Rightarrow V_{C_1} = \frac{1-d}{1-3d} \cdot V_{\text{in}}. \tag{10}$$

$$I_{L_1} = I_{L_2} = \frac{(1-d)\, I_{\text{i}} + d I_{\text{dc-load}}}{1-3d}. \tag{11}$$

The DC link voltage through the inverter bridge can be expressed as

$$V_{\text{p}} = V_{C_1} = V_{\text{dc-load}} = BV_{\text{in}}, \tag{12}$$

where

$$B = \frac{1-d}{1-3d}. \tag{13}$$

The peak voltage can then be obtained as the boost factor due to the shoot-through state, and the peak voltage is

$$\hat{V}_{\text{ac}} = V_{\text{es}} = MBV_{\text{in}}. \tag{14}$$

In Figs. 1(a)-(d), the grid reactive power is compensated by capacitor C_{s}, whose stored energy can be expressed as

$$E_{C_{\text{s}}} = \frac{1}{2} C_{\text{s}} V_{\text{es}}^2, \tag{15}$$

where V_{es} is the voltage across capacitor C_{s}.

According to (14), the magnitude of voltage V_{es} can be controlled by the modulation ratio M and the shoot-through boost factor B. Under the condition that the rated voltage of the capacitor C_{s} is not exceeded, according to (15), the energy stored in capacitor C_{s} can be increased by changing modulation ratio M and shoot-through boost factor B, thus enhancing the reactive power compensation capacity of the C_{s}. This theoretical analysis justifies the superiority of the proposed IN-ES over traditional ES structures and can provide a wider range of voltage control through reactive power compensation, owing to the controllable capacitor energy.

According to the aforementioned analyses, the DC link voltage of the inverter can be derived from the capacitor voltage V_{C_1}, and the DC link output power equals the capacitor's output power. In terms of the power constant principle, one can get

$$P = V_{\text{p}} I_{\text{i}} = V_{C_1} I_{\text{i}} = V_{\text{es}} \sin(\omega t)\, I_{L_{\text{s}}} \sin(\omega t + \theta)$$
$$= \frac{1}{2} V_{\text{es}} I_{L_{\text{s}}} \left[\cos(2wt + \theta) - \cos(\theta)\right], \quad (\theta \in [0, 2\pi]), \tag{16}$$

where P is output power at the AC side, V_{es} is the magnitude of the AC side output voltage and I_{Ls} is the magnitude of the AC side output current. According to (16), it can be seen that there is a secondary low-frequency pulsation due to the output power of the inverter and the electrical energy provided by the DC side. Therefore, the twice low-frequency ripple also exists on the DC side, i.e., V_{C1} and V_{p} have twice low-frequency ripples.

C. EFFICIENCY ANALYSIS

Parasitic parameters in power electronics circuits can make the actual voltage gain deviate from the theoretical value. In this subsection, the efficiency of the proposed IN-ES converter is investigated. In order to obtain the practical gain, parasitic resistances of the power electronics components used in this study are taken into account. This includes diode forward voltage (V_{F}), diode conduction resistor (R_D), winding resistor of inductor (R_{LS}), equivalent series resistance of capacitor (R_C), the drain-source on-resistance of IGBT (R_{CE}), and the turn-on and turn-off time of IGBT denoted as t_{on} and t_{off}.

The currents flowing through the diodes can be obtained as

$$i_{D_{0,3,4}} = \begin{cases} I_{L_1}, & \text{Converter non-shoot-through,} \\ 0, & \text{Converter shoot-through,} \end{cases} \tag{17}$$

and

$$i_{D_{1,2}} = \begin{cases} I_{L_1}, & \text{Converter shoot-through,} \\ 0, & \text{Converter non-shoot-through,} \end{cases} \tag{18}$$

and the RMS value and average value of the current of diode can be deduced as

$$I_{D_k(\text{RMS})} = \sqrt{\frac{1}{T}\int_0^T i_{D_k}^2 dt}, \tag{19}$$

and

$$I_{D_k(\text{AVG})} = \frac{1}{T}\int_0^T i_{D_k} dt. \tag{20}$$

The total power loss in diode D_k ($0 \le k \le 4$) is the summation of the power loss in R_D and the power loss associated with the voltage source V_D. Assuming that all diodes are identical, according to (19) and (20), the total power loss of the diodes can be obtained as

$$P_D = P_{R_{D_k}} + P_{V_{D_k}}$$
$$= I_{D_{k(\text{RMS})}}^2 R_{D_k} + V_{F_{D_k}} I_{D_{k(\text{AVG})}}$$
$$= (3-d) R_D \left(\frac{(1-d)\frac{P}{V_{C_1}} + \frac{dV_{C_1}}{R_{\text{dc-load}}}}{1-3d}\right)^2$$
$$+ (3-d) V_{F_D} \left(\frac{(1-d)\frac{P}{V_{C_1}} + \frac{dV_{C_1}}{R_{\text{dc-load}}}}{1-3d}\right). \tag{21}$$

Total conduction loss in the inductor due to their equivalent series resistance (ESR) is given by

$$P_{r_L} = 2 I_{L_{1(\text{RMS})}}{}^2 R_{LS} = 2R_{LS} \left(\frac{(1-d)\frac{P}{V_{C_1}} + \frac{dV_{C_1}}{R_{\text{dc-load}}}}{1-3d}\right)^2. \tag{22}$$

It can be easily seen from the above analysis that the current flowing through the capacitor can be represented as

$$i_{C_1} = \begin{cases} 2I_{L_1} + I_{\text{dc-load}}, & \text{Converter non-shoot-through,} \\ I_{L_1} - I_{\text{dc-load}} - I_{\text{i}}, & \text{Converter shoot-through,} \end{cases} \tag{23}$$

The RMS value of the capacitor current is given by

$$\begin{aligned} I_{C_{1(\mathrm{RMS})}} &= \sqrt{\frac{1}{T}\int_0^T i_{C_1}^2 dt} \\ &= \sqrt{\frac{1}{T}\int_0^{dT} i_{C_1}^2 dt + \frac{1}{T}\int_{dT}^T i_{C_1}^2 dt} \\ &= \sqrt{d(2I_{L_1}+I_{\mathrm{dc-load}})+(1-d)\left(I_{L_1}-I_{\mathrm{dc-load}}-I_{\mathrm{i}}\right)^2}. \end{aligned} \tag{24}$$

The total conduction loss in the buffer capacitors due to their ESRs can be obtained as

$$\begin{aligned} P_{rc} &= I_{C_{1(\mathrm{RMS})}}^2 R_{C_1} \\ &= \left(\frac{(1-d)(1+4d)\frac{P}{V_{C_1}} + d(6-4d)\frac{V_{C_1}}{R_{\mathrm{dc-load}}}}{1-3d}\right)^2 R_{C_1}. \end{aligned} \tag{25}$$

It can be easily deduced from the above analysis that the current flowing through the IGBT switch S_0 to S_4 can be obtained as

$$i_{S_0} = \begin{cases} 2I_{L_1}, & \text{Converter shoot-through,} \\ 0, & \text{Converter non-shoot-through.} \end{cases} \tag{26}$$

$$i_{S_{1,2,3,4}} = \begin{cases} 2I_{L_1}, & \text{Converter shoot-through,} \\ I_{\mathrm{i}}, & \text{Converter non-shoot-through.} \end{cases} \tag{27}$$

Hence the RMS value of the currents of the S_0 and $S_{1,2,3,4}$ can be obtained as

$$\begin{aligned} I_{S_{0(\mathrm{RMS})}} &= \sqrt{\frac{1}{T}\int_0^T i_{S_0}^2 dt} \\ &= \sqrt{\frac{1}{T}\int_0^{dT} (2I_{L_1})^2 dt} \\ &= \sqrt{4d\left(\frac{(1-d)I_{\mathrm{i}} + dI_{\mathrm{dc-load}}}{1-3d}\right)^2}. \end{aligned} \tag{28}$$

$$\begin{aligned} I_{S_{1,2,3,4(\mathrm{RMS})}} &= \sqrt{\frac{1}{T}\int_0^T 2i_{S_{1,2,3,4}}^2 dt} \\ &= \sqrt{\frac{1}{T}\int_0^{dT} (2I_{L_1})^2 dt + \frac{1}{T}\int_{dT}^T I_{\mathrm{i}}^2 dt} \\ &= \sqrt{4d\left(\frac{(1-d)I_{\mathrm{i}} + dI_{\mathrm{dc-load}}}{1-3d}\right)^2 + (1-d)I_{\mathrm{i}}^2}. \end{aligned} \tag{29}$$

Considering the switching loss and conduction loss of inverter bridge, the power loss in the IGBT is thus

$$\begin{aligned} P_S &= P_{Q_{(\mathrm{con})}} + P_{Q_{(\mathrm{swi})}} \\ &= 5R_{\mathrm{CE}} I_{S_{0(\mathrm{RMS})}}^2 + \frac{4V_{\mathrm{CE}} I_{S_{1,2,3,4(\mathrm{RMS})}}(t_{\mathrm{on}}+t_{\mathrm{off}})f}{2} \\ &\quad + \frac{V_{\mathrm{CE}} I_{S_{1,2,3,4(\mathrm{RMS})}}(t_{\mathrm{on}}+t_{\mathrm{off}})f_{S_0}}{2} \\ &= 10dR_{CE}\left(\frac{(1-d)\frac{P}{V_{C_1}} + \frac{dV_{C_1}}{R_{\mathrm{dc-load}}}}{1-3d}\right)^2 \\ &\quad + \frac{\sqrt{2d\left(\frac{(1-d)\frac{P}{V_{C_1}} + \frac{dV_{C_1}}{R_{\mathrm{dc-load}}}}{1-3d}\right)^2 + (1-d)\left(\frac{P}{V_{C_1}}\right)^2}}{2} \\ &\quad \cdot V_{\mathrm{CE}}(t_{\mathrm{on}}+t_{\mathrm{off}})(4f+f_{S_0}), \end{aligned} \tag{30}$$

where $P_{Q_{(\mathrm{con})}}$ and $P_{Q_{(\mathrm{swi})}}$ are conduction and switching power losses of switches and V_{CE} is the drain-source voltage of S_0 to S_4 being off. Then the total energy efficiency of the proposed converter can be calculated as,

$$\eta = \frac{P}{P+P_{\mathrm{Loss}}} = \frac{P}{P+P_{rL}+P_{rC}+P_{\mathrm{S}}+P_D}. \tag{31}$$

Under the same operation conditions, the efficiency curve of IN-ES and converters (a) in [32] following the change in duty cycle are shown in Fig. 7. When the input voltage of IN-ES is $V_{\mathrm{in}} = 15V$ and $d = 0.25$, the efficiency is 84.31%, and is higher than the converter (a) of [32], which is 81.23%.

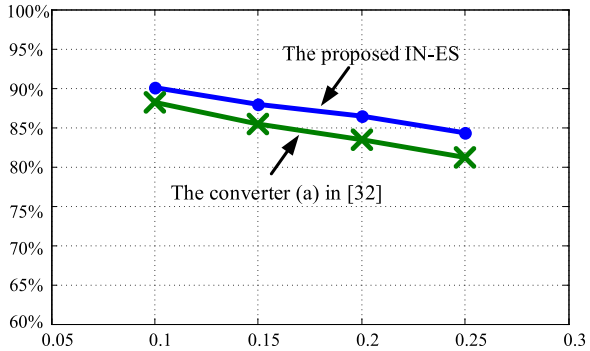

FIGURE 7. Efficiency curve of the proposed IN-ES and converter (a) in [32].

D. OPERATION MODES OF THE PROPOSED IN-ES

The proposed ES structure with a high-step-up ratio and immunity of bridge shoot-through has eight operation modes, which resembles ES-2, i.e., (i) inductive mode, (ii) capacitive mode, (iii) resistive mode, (iv) negative-resistive mode, (v) inductive plus resistive mode, (vi) capacitive plus resistive mode, (vii) inductive plus negative-resistive mode and (viii) capacitive plus negative-resistive mode. This section mainly introduces the voltage regulation function when the proposed IN-ES provides pure reactive power compensation (non-critical load is assumed to be a RL load).

1) VOLTAGE SUPPORT

As shown in Fig. 8, when the mains voltage $V_{\mathrm{s}} = V_{\mathrm{nc}} + V_{\mathrm{es}}$ is lower than the nominal value $V_{\mathrm{s-ref}}$, the proposed IN-ES operates in the inductive status, i.e., absorbing reactive power from the grid. The phase of the output voltage V_{es} leads its current I_{es} by 90°, as shown in Fig. 8.

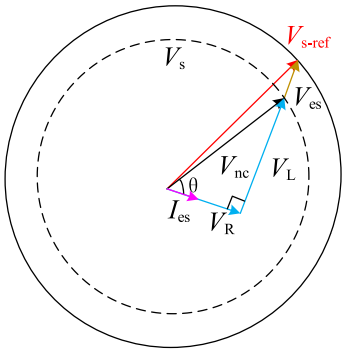

FIGURE 8. Relation among electric variables of the proposed IN-ES: Inductive mode.

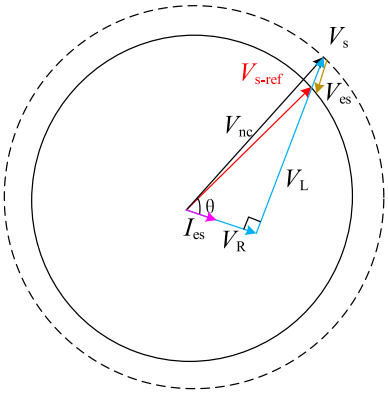

FIGURE 9. Relation among electric variables of the proposed IN-ES: Capacitive mode.

2) VOLTAGE SUPPRESSION

As shown in Fig. 9, when terminal voltage is higher than the nominal value, the proposed IN-ES operates in the capacitive mode, and the output voltage V_{es} of the IN-ES lags its current I_{es} by 90°. In this mode, IN-ES provides reactive power to the grid to decrease the magnitude of the terminal voltage.

Conclude that the proposed IN-ES can well stabilize the terminal fluctuation voltage both in voltage support and suppression to the nominal value.

III. CONTROL STRATEGY AND STABILITY ANALYSIS OF THE PROPOSED IN-ES

A. CONTROL STRATEGY

In order to realize the advanced features of the proposed IN-ES, corresponding control purposes are listed as follow.

1) Control the modulation ratio M and the boost factor B through controlling the switches, so as to extend the voltage regulation range; and

2) Stabilize the terminal voltage at its nominal value.

The control scheme shown in Fig. 10 is established in MATLAB/Simulink to achieve the above control objectives. With the battery storage system (denoted as V_{in}), the phase angle of the compensation voltage V_{es} and the phase angle of the current, namely I_{es}, flowing through the proposed IN-ES can produce complex power with an arbitrary angle, thereby stabilizing the voltage fluctuations.

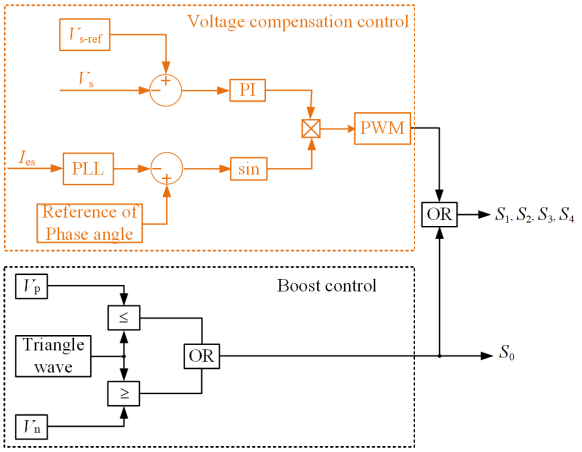

FIGURE 10. Control strategy for the proposed IN-ES.

This control scheme uses a single-phase phase lock loop (PLL) to determine the phase angle of I_{es}, and then changes the phase angle of output voltage in terms of required reactive power compensation. In Fig. 10, driving signals for switches $S_0 \sim S_4$ are described.

In Fig. 10, a simple boost control method is utilized to achieve the DC side voltage. The method controls the ON and OFF of the DC side switch S_0 while inserting the shoot-through signal into the modulation signal of the traditional SPWM full bridge inverter, and finally balance DC side voltage. Detailed control waveforms is shown in Fig. 11 which is generated from Fig. 10.

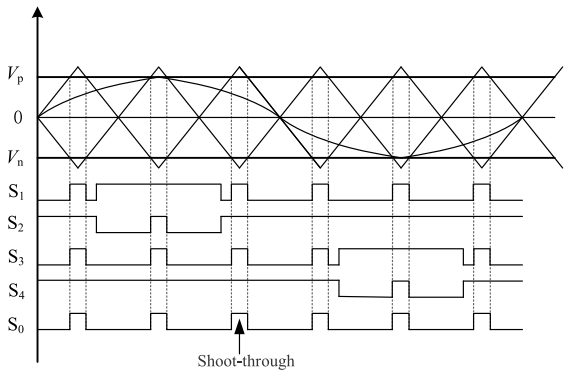

FIGURE 11. Driving waveforms of switches $S_0 \sim S_4$.

B. STABILITY ANALYSIS

Suppose the overall system operates around the steady-state point with a small perturbation. Considering perturbation $\hat{v}_{in}$ to the nominal input voltage V_c and $\hat{d}$ to the nominal duty ratio d, the relationship among state variables of the IN-ES converter impedance network can be expressed as

$$\begin{cases} i_{L_1} = I_{L_1} + \hat{i}_{L_1}, \\ v_{C_1} = V_{C_1} + \hat{v}_{C_1}, \\ v_{in} = V_{in} + \hat{v}_{in}, \\ d = D + \hat{d}. \end{cases} \tag{32}$$

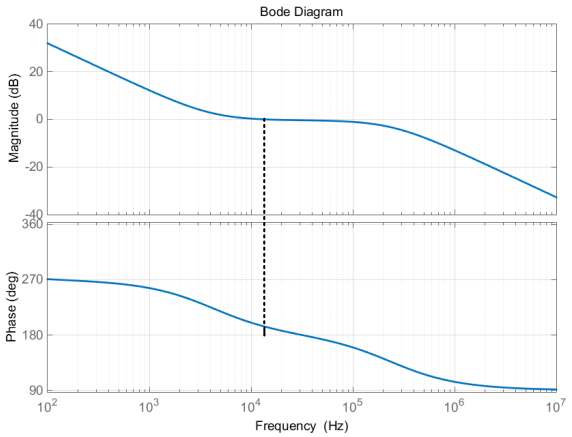

FIGURE 12. Bode plots of the transfer functions $G_{V_{C_1}}(s)$ of IN-ES.

Since the perturbation of the input voltage $\hat{v}_{\text{in}}$ negligible, the transfer function can be deduced as

$$G_{V_{C_1}}(s) = \frac{b_0 s + b_1}{a_0 s^2 + a_1 s + a_2}, \tag{33}$$

where

$$\begin{cases} b_0 = L_1 \left(I_{\text{i}} - 2I_{L_1}\right), \\ b_1 = (1 - 3d)\left(2V_{C_1} - V_{\text{in}}\right), \\ a_0 = L_1 C_1, \\ a_1 = \dfrac{L_1 (1 - 2d)}{R_{\text{dc-load}}}, \\ a_2 = (1 - 2d)(1 - 3d). \end{cases} \tag{34}$$

Bode plots of the transfer functions $G_{V_{C_1}}(s)$ is shown in Fig. 12. It can be seen from the bode diagram that the phase margins of the transfer function are higher than 0, so the IN-ES is a stable system.

The IN-ES output port is represented by a variable voltage source V_{i}, then the equivalent s-domain circuit diagram of Fig. 13 can be drawn. According to Norton's theorem, we can have

$$\begin{cases} Z_0 = \dfrac{Z_{\text{line}} Z_{\text{c}} + Z_{\text{c}} Z_{\text{nc}} + Z_{\text{nc}} Z_{\text{line}}}{Z_{\text{line}} + Z_{\text{c}}}, \\ I_0(s) = V_{\text{g}}(s) \dfrac{Z_{\text{c}}}{Z_{\text{line}} Z_{\text{c}} + Z_{\text{c}} Z_{\text{nc}} + Z_{\text{nc}} Z_{\text{line}}}. \end{cases} \tag{35}$$

According to the Kirchhoff's laws

$$\begin{cases} sC_{\text{s}} V_{\text{es}}(s) = I_L(s) + \dfrac{V_{\text{s}}(s) - V_{\text{es}}(s)}{Z_{\text{nc}}}, \\ sL_{\text{s}} I_L(s) = V_{\text{i}}(s) - V_{\text{es}}(s), \\ sC_{\text{s}} V_{\text{es}}(s) = I_L(s) + I_0(s) - \dfrac{V_{\text{es}}(s)}{Z_0}. \end{cases} \tag{36}$$

According to formula (36)

$$V_{\text{s}}(s) = G_1(s) V_{\text{i}}(s) + G_2(s) V_{\text{g}}(s), \tag{37}$$

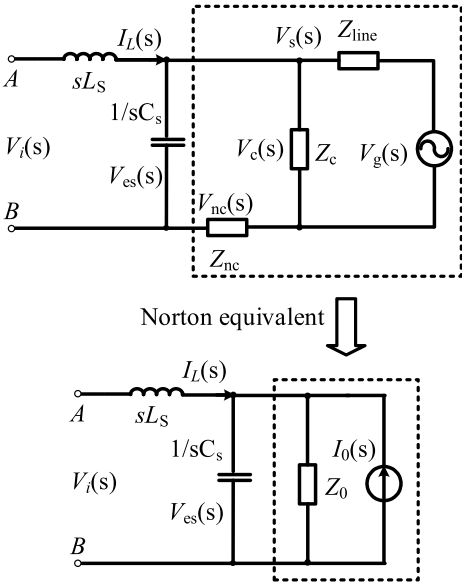

FIGURE 13. *S*-domain equivalent model of IN-ES application circuit.

where

$$\begin{cases} G_1(s) = \dfrac{Z_{\text{line}} Z_{\text{c}}}{(Z_{\text{line}} + Z_{\text{line}})\left(Z_0 L_{\text{s}} C_{\text{s}} s^2 + L_{\text{s}} s + Z_0\right)}, \\ G_2(s) = \dfrac{Z_{\text{c}}\left(Z_{\text{nc}} L_{\text{s}} C_{\text{s}} s^2 + L_{\text{s}} s + Z_{\text{nc}}\right)}{(Z_{\text{line}} + Z_{\text{line}})\left(Z_0 L_{\text{s}} C_{\text{s}} s^2 + L_{\text{s}} s + Z_0\right)}. \end{cases} \tag{38}$$

From formulas (35), (37) and (38), the transfer function of the system is

$$G_0(s) = K_{\text{pwm}} \frac{Z_0 - Z_{\text{nc}}}{(Z_{\text{line}} + Z_{\text{line}})\left(Z_0 L_{\text{s}} C_{\text{s}} s^2 + L_{\text{s}} s + Z_0\right)}, \tag{39}$$

where K_{pwm} is the ratio of the DC voltage V_{p} of the inverter to the amplitude of the triangular carrier.

The Bode diagram of the transfer function of the system is shown in Fig. 14, and its phase angle margin is higher than zero, hence a stable system. Because the fluctuation of voltage V_{s} will affect the stability of the system, in order to achieve a stable operation and improve the dynamic response, a voltage control strategy with a PI controller is used. The expression of the PI controller is

$$G_{\text{PI}}(s) = k_{\text{p}} + \frac{k_{\text{i}}}{s} = 0.1 + 300\frac{1}{s} \tag{40}$$

It can be seen from Fig. 14 that the phase angle margin of the system is greatly increased after compensation, so this control strategy can ensure stable operations of the system.

IV. SIMULATION STUDY

In order to verify the effectiveness of the proposed IN-ES, in this section we conduct simulations in MATLAB/Simulink environment, which is compared to the popular ES-2 under different input voltages. Simulation parameters are shown in TABLE 2. The simulation employs the control strategy shown in Fig. 10 to control the circuit in Fig. 4 for verification.

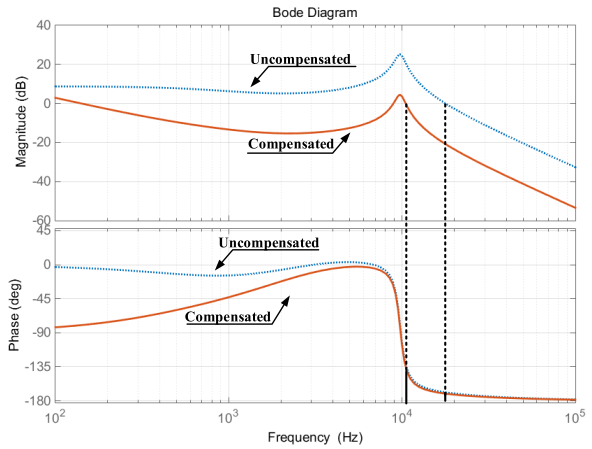

FIGURE 14. Bode plot of the control-to-output transfer function of the proposed IN-ES.

TABLE 2. Simulation parameters.

Parameters	Value
Nominal terminal voltage	$V_{\mathrm{s-ref}}$=220V
DC input voltage of IN-ES, ES-2	$V_{\mathrm{in(IN-ES)}}$=100V, $V_{\mathrm{in(ES-2)}}$=140V
Inductance	L_1=L_2=3mH, L_{s}=330μH
Capacitance	$C_1 = 2200\mu$F, $C_{\mathrm{s}} = 10\mu$F
DC Load	100Ω
Noncritical load	$Z_{\mathrm{nc}} = 20 + j31.4\Omega$
Critical load	$Z_{\mathrm{c}} = 60\Omega$
Line impedance	r_{line}=2Ω, $x_{\mathrm{line}} = 0.69\Omega$
Switching frequency of S_0, inverter IGBT	40kHz, 20kHz
Shoot-thought duty	$d = 0.25$

TABLE 3. Experimental equipments.

Equipment	Type
Oscilloscope	KEYSIGHT DS9104A
Current Probe	KEYSIGHT 1147A
Differential Probe	Agilent N2790A
DC Power Supply	KIKUSUI PWR800L
DC Power Supply	UNI-T UTP3305
AC Power Suppoly	PCR1000LE
dSPACE	DS1103

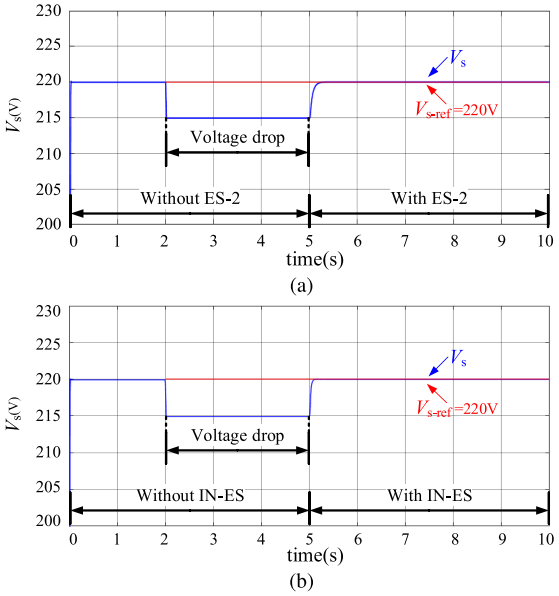

FIGURE 15. Terminal voltage V_s for voltage support (a) ES-2, and (b) the proposed IN-ES.

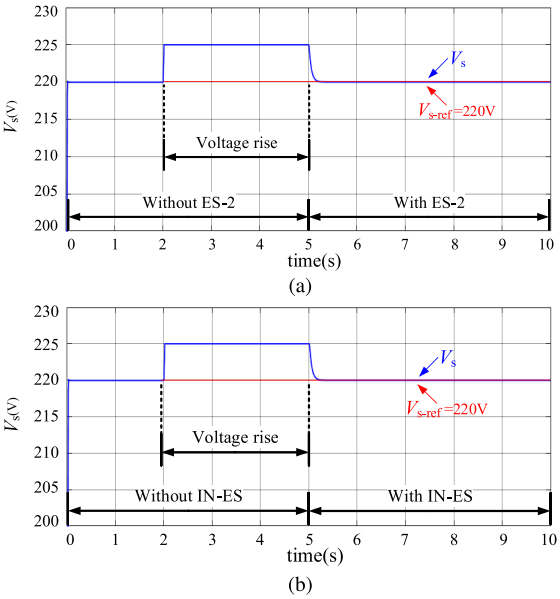

FIGURE 16. Terminal voltage V_s for voltage suppression: (a) ES-2, and (b) the proposed IN-ES.

As shown in Figs. 15∼18, in the simulation, voltage V_{s} suddenly changes to 215V or 225V when $t = 2$s, which is lower or higher than its nominal value 220V. Under this condition, the proposed IN-ES and ES-2 start the control duty at $t = 5$s. Their control results are plotted in Figs. 15∼18, respectively. We can see that the proposed IN-ES and ES-2 are able to regulate V_s to the nominal value.According to the formula $V_{\mathrm{es}} = MV_{\mathrm{in}}$ of the output voltage of the full-bridge inverter, the DC side voltage of the ES-2 needs to be $95\sqrt{2}$V(=134.33V), while the IN-ES only requires 100V to do so, which demonstrates that under the same voltage, the proposed IN-ES has a wider voltage regulation range than the existing ES-2. This agrees well with our previous theoretical analyses.

In addition, as shown in Fig. 19(a), when the proposed IN-ES is not regulating the terminal voltage ($t = 0 \sim 5$s), it can provide a constant DC voltage. At $t = 5$s, the IN-ES starts operating in voltage support mode and the DC side capacitance voltage is 294.5 ± 1V. This fluctuation is caused

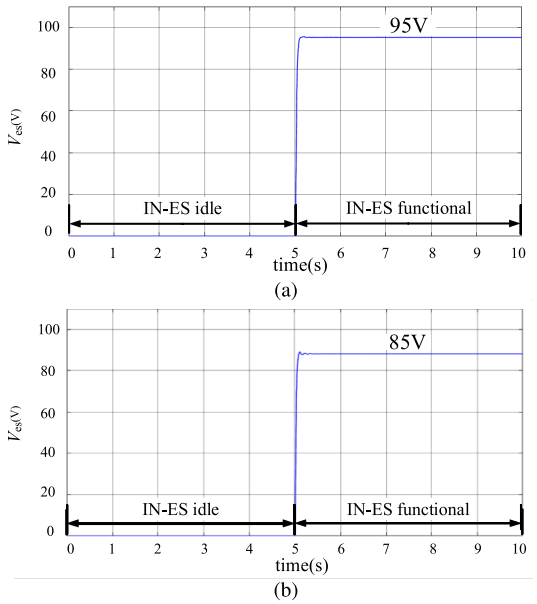

FIGURE 17. Compensation voltage V_{es} of the proposed IN-ES in voltage: (a) support mode and (b) suppression mode.

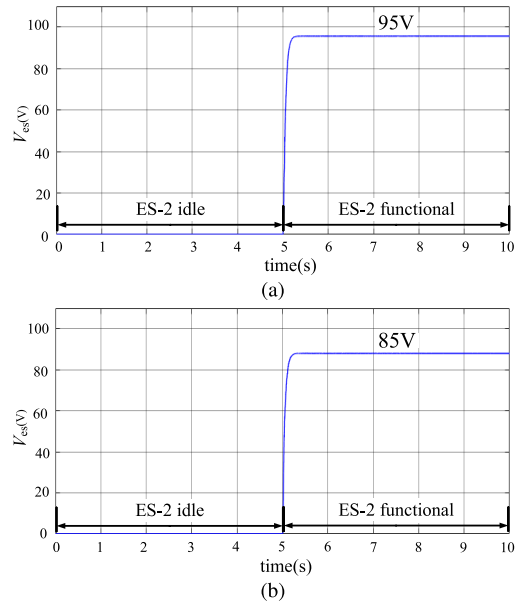

FIGURE 18. Compensation voltage V_{es} of the proposed ES-2 in voltage (a) support mode and (b) suppression mode.

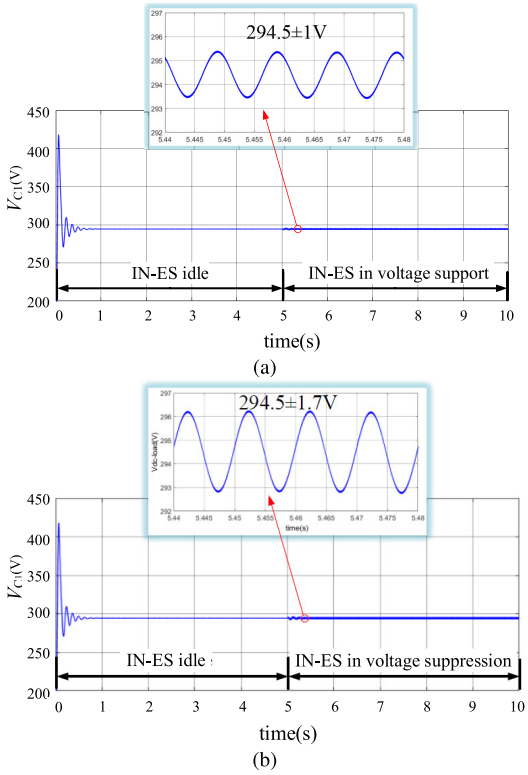

FIGURE 19. Voltage across V_{C_1}: (a) IN-ES is idle for the first 5 seconds and operates in voltage support mode from 5 to 10 seconds, (b) IN-ES is idle for the first 5 seconds and operates in voltage suppression mode from 5 to 10 seconds.

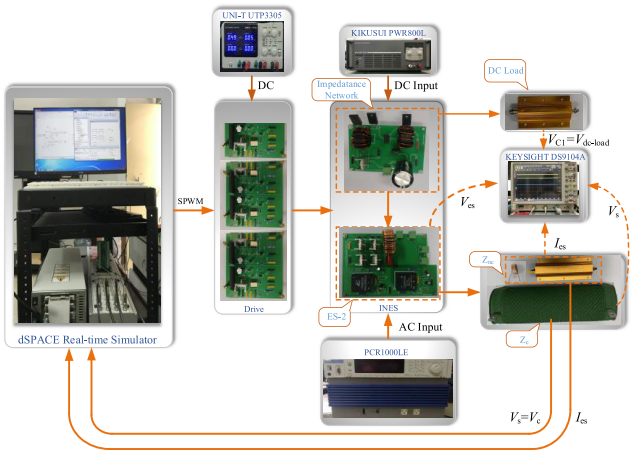

FIGURE 20. Prototype and experimental setup.

by the output power on the AC side and the turn-on voltage drop of the diode and IGBT transistors. Because the voltage fluctuations sit within the 0.4% range, the IN-ES is considered to be able to provide stable DC voltage while absorbing reactive power from the grid. Similar conclusion can be drawn for IN-ES working in voltage suppression mode as in Fig. 19(b), where the DC side capacitance voltage is 294.5±1.7V (below 0.6% of the DC component) when IN-ES is providing reactive power to the grid.

From the simulation results shown in Figs. 15∼19, we can see that the proposed IN-ES is able to provide a higher compensation voltage to regulate the terminal voltage to its nominal value, hence a wider voltage control range. It also suggests that the ES-2 is not able to cope with such voltage deviations when the input DC voltage source is 100V. It is thus safe to conclude that the proposed IN-ES has a superior voltage regulation capability over the existing ES-2 for compensating the terminal voltage deviations.

TABLE 4. Experimental parameters.

Parameters	Value
Power source	V_{s-ref}=30V
Input DC voltage of IN-ES, ES-2	$V_{in(IN-ES)}$=15V, $V_{in(ES-2)}$=45V
Inductance	L_1=L_2=3mH, L_s=330uH
Capacitance	C_1=2200μF, C_s=10μF
DC load	100Ω
Noncritical load	Z_{nc}=20+j31.4Ω
Critical load	Z_c=60Ω
Line impedance	r_{line}=2Ω, x_{line}=0.69Ω
Switching frequency of S_0, inverter IGBT	40kHz, 20kHz
Shoot-through duty	d=0.25

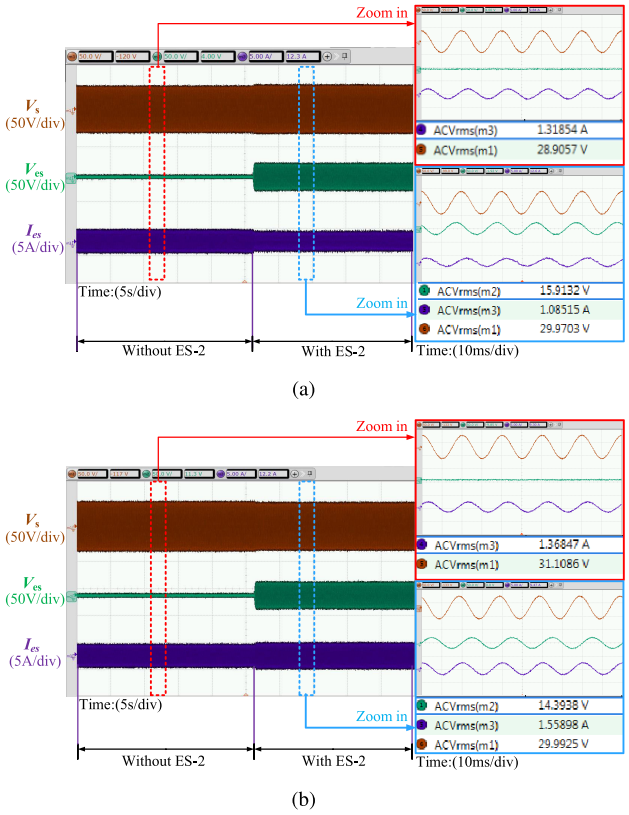

FIGURE 21. Experimental waveforms of ES-2 in (a) voltage support mode and (b) voltage suppression mode.

V. EXPERIMENTAL VERIFICATION

In order to further verify the validity of the proposed IN-ES, a hardware prototype is established in this paper, which is shown in Fig. 20. The parameters used in the experiment are shown in TABLEs 3 and 4 for IN-ES and peripheral devices, respectively.

As shown in Figs. 21(a) and (b), when ES-2 operates in voltage support (inductive) mode, it is able to stabilize the terminal voltage from 28.9V to 30V, and the compensation

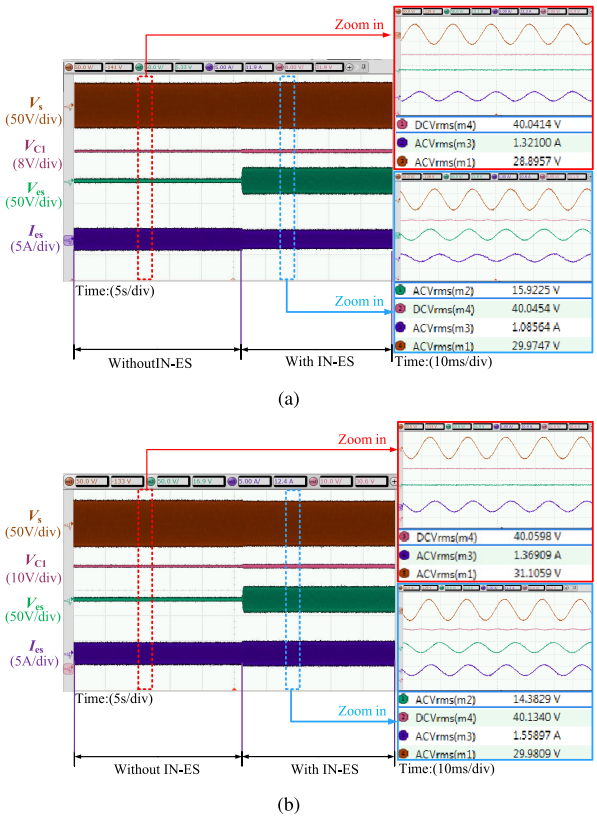

FIGURE 22. Experimental waveform of the proposed IN-ES in voltage (a) support mode and (b) suppression mode.

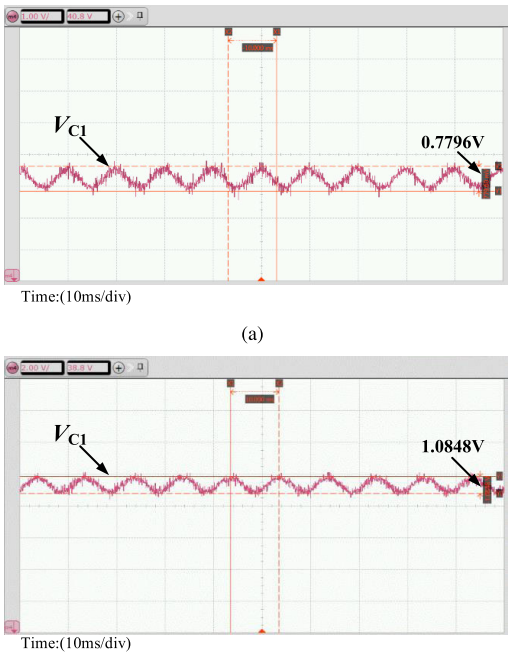

FIGURE 23. Magnified results of V_{C_1} voltage with the proposed IN-ES in: (a) voltage support mode and (b) voltage suppression mode.

voltage V_{es} of the ES-2 is 16V. Similarly, ES-2 is able to regulate the terminal voltage from 31.1V down to its nominal

value, with the V_{es} being 14.4V. Through further experiments we know that if the terminal voltage is to be stabilized under ±1.1V, ES-2 requires the DC input voltage to be at least 23V, which is greater than the input voltage, and ES-2 cannot satisfy this condition.

On the other hand, we can see from Figs. 22(a) and (b), the capacitor voltage V_{C_1} and the inverter bridge DC side voltage V_p can be increased from 15V to 40V. When the proposed IN-ES regulates the terminal voltage, it is able to stabilize the voltage of critical load at its nominal value 30V. Compared with the traditional ES-2, its DC side voltage only requires 15V, and adjusting the shoot-through duty d can further reduce the DC input voltage requirement. According to (16) and the results in Fig. 23, we can observe that when IN-ES conducts voltage control, voltages V_{C_1} and V_p have the twice low-frequency ripples. Conclude that IN-ES is superior to ES-2.

VI. CONCLUSION

In this study, we have proposed a novel impedance-network-based electric spring structure, and we have conducted thorough analysis, simulation and experimentation, which verified the efficacy of the proposed IN-ES. Unlike previous versions of electric springs, the proposed IN-ES has an additional switch-boost quasi-Z-network to the DC side. Compared with the ES-2, this structure has been proven to be able to reduce the requirement of the DC side voltage level and corresponding requirements for battery system, increase input-to-output voltage ratio, and expand electric spring's voltage compensation range. Furthermore, without needing dead-time control, the proposed IN-ES is intrinsically immune to the inverter bridge shoot-through issue. All these features are absent in the existing ES topologies.

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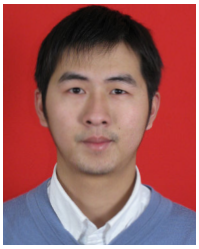

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