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A High Performance Adaptive Digital LDO Regulator With Dithering and Dynamic Frequency Scaling for IoT Applications

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ABSTRACT In this paper, a high performance adaptive digital low-dropout voltage regulator (ADLDO) is proposed for Internet-of-Things (IoT) applications. In the proposed ADLDO, a fully synthesizable adaptive digital controller is designed. It automatically senses load variations and adaptively controls multi-loop architecture to reduce quiescent current, minimize output voltage ripples and achieve fast transient response. The multi-loop architecture with hill climbing reduces the total bi-directional shift registers length which results in the reduced leakage current in the transistor-switch-array (TSA), and improves the recovery time and output DC voltage accuracy. A dithering technique is introduced to eliminate the limit cycle oscillation (LCO) and improve the performance of the regulator. The dynamic frequency scaling (DFS) mechanism is proposed for reducing controller power consumption in steady state. In order to reduce the offset and output voltage error, a dynamic latch comparator is utilized. When the input supply voltage is varied from 0.5 V to 1 V, the measured output voltage ranges from 0.45 V to 0.95 V with 50 mV dropout voltage. The operating frequency is 10 MHz with fast transient response and quiescent current of 350 ns and 3.7 μA, respectively. The maximum measured power and current efficiencies are 89.7 % and 99.97 %, respectively, with 1.9 mV output voltage ripples. Measured load and line regulations are 2.2 mV/mA and 9.5 mV/V respectively. The proposed circuit is implemented in 28 nm CMOS process and occupies 0.016 mm^2 chip area.

INDEX TERMS Adaptive, dithering, digital LDO, dynamic frequency scaling (DFS), fully synthesizable, fast transient, hill climbing, limit cycle oscillation (LCO), low power, multi-loop.

I. INTRODUCTION

Recently, the Internet-of-Things (IoT) technology is being adopted rapidly for connecting wireless electronic devices such as sensors, RFIDs, and medical implanted devices, etc through internet [1]. The IoT and battery operated devices demand more and more functionalities in a smaller area with high power efficiency. In all wireless devices power is supplied by the batteries having limited lifetime. In order to increase system standby time, it is extremely important to guarantee the operation of the wireless devices for longer period without charging [2], [3]. Therefore, low power consumption of wireless devices is vital for operating in the ideal IoT applications. In any IoT device, for high power

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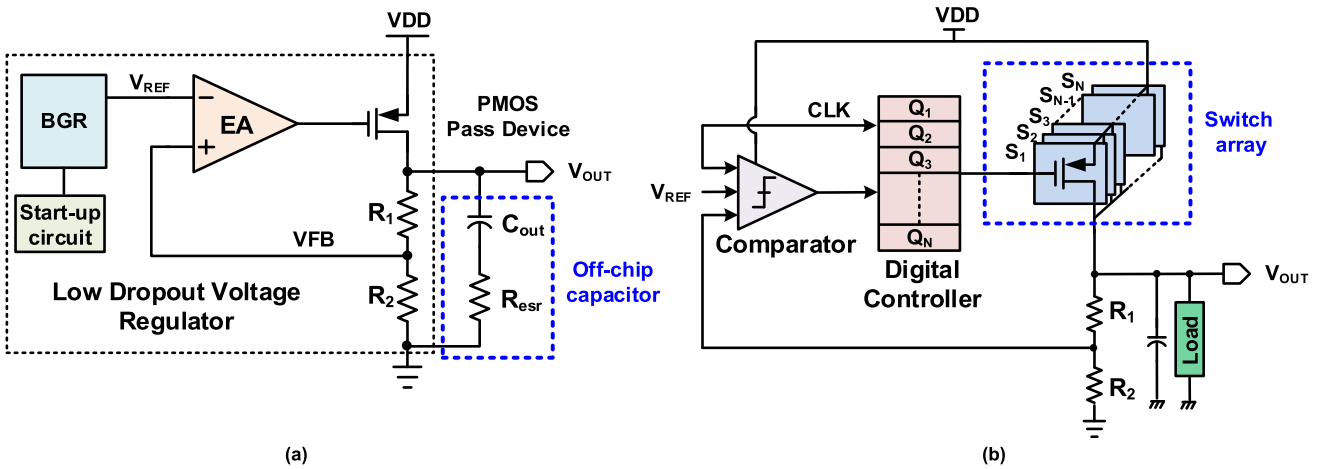

FIGURE 1. Block diagram of a conventional (a) analog LDO regulator, and (b) digital LDO regulator.

efficiency, it is important to minimize the power consumption and area of each building block. The analysis shows that a high power efficiency is achieved by operating the circuits at close/sub-threshold region [4]–[7].

Normally, an LDO provides a smooth voltage for supply power to the sub-circuits in a system-on-chip (SOC). An analog LDO is suitable for noise sensitive load circuits but it does not provide sufficient loop gain at low supply voltages due to process, voltage temperature (PVT) variations [8]–[10]. Moreover, these technology dependent regulators also suffer from slow load regulation due to limited bandwidth of the error amplifier and poor power noise rejection [11], [12].

Recently, digital LDO (D-LDO) has drawn significant attention for low power and area constrained applications. It provides regulated supply voltages to sub-systems by integrating asynchronous or synchronous control methods. The digital LDO has advantages over analog LDO due to less stability issues, smaller power transistor area, and improved process stability [13], [14]. The basic analog and digital LDO structures are elaborated in Fig. 1. An analog LDO mainly consists of error amplifier (EA), bandgap reference (BGR), PMOS pass devices and feed-back loop as shown in Fig. 1(a). The D-LDO is composed of switch array, comparator and a digital controller [15] as shown in Fig. 1(b). In D-LDO regulator, an error amplifier is replaced with a comparator and it senses the difference between feed-back loop and the main reference voltage. The comparator output controls the PMOS switch array with a shift register depending upon the load variations. However, the conventional D-LDO faces the fundamental tradeoffs such as power consumption, output current resolution, and transient response [16], [17]. The LDO efficiency (η) is given in (1).

$$\eta = \frac{I_{OUT} V_{OUT}}{(I_{OUT} + I_Q) V_{IN}} \times 100 \tag{1}$$

Recently, numerous DLDO structures, such as flash ADC-DLDO [14], analog-assisted digital LDO (AA-DLDO) [18], dual-loop combined synchronous and asynchronous (CO-SA-DLDO) regulator [19] and discrete-time digital LDO [20] are discussed in literature. The flash ADC-DLDO architecture uses flash ADC with baseline D-LDO. This LDO requires an additional digital controller and reference selection circuit for flash ADC. Because of flash ADC, its power consumption is high and it occupies huge area. The AA-DLDO uses combined analog and digital circuits. It suffers large power consumption and high output voltage ripples. In D-LDO regulator, an asynchronous controller is used for achieving fast transient response without increasing the quiescent current [19]. Due to PVT variations, the asynchronous circuit increases delay, creates DC offsets and decreases overall efficiency. Thus, it is difficult to design a high-performance system with asynchronous logic [17], [21].

Similarly, intrinsic output ripples, also known as limit cycle oscillations (LCO), are found in D-LDO. Several works have been carried out for LCO reduction in the past literature. To reduce LCO, a high-resolution ADC is introduced in [18] is called freeze mode and by using multiple comparators a dead-zone is added to the comparator stage in [22]. These techniques result in an increased circuit complexity, power consumption and area. In D-LDO, the most important challenges are to limit the output ripples during steady-state time, reduce the quiescent current, diminish the output voltage spikes and minimize the response time during the transition period [23].

In this paper, a multi-loop adaptive digital low-dropout voltage regulator (ADLDO) for IoT applications is proposed. The adaptive digital LDO operates at low supply voltage near sub-threshold region. In order to achieve higher power and current efficiencies with fast transient response and output ripple reduction, some key strategies are introduced in the proposed circuit. A fully synthesizable ADLC controller is designed for sensing load variations, automatically reference voltage control and employing an adaptive hill-climbing scheme with multi-loop architecture. For fast transient response, low power consumption and less quiescent current, the MOS switch array with three loops is designed.

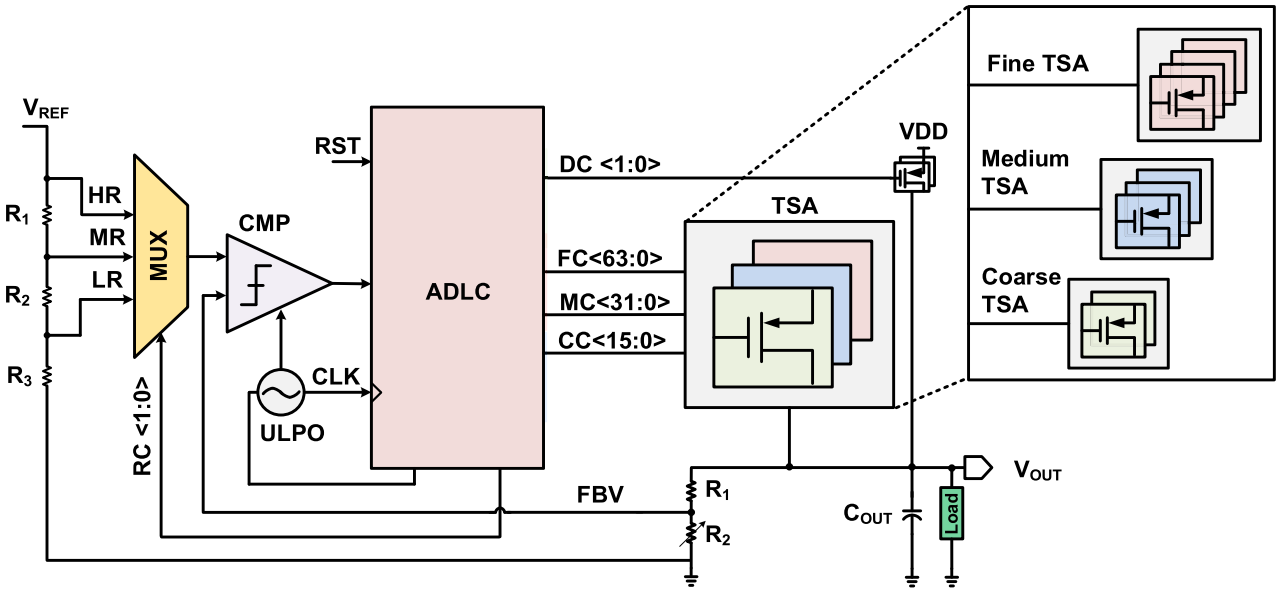

FIGURE 2. Block diagram of the proposed adaptive digital LDO regulator (ADLDO).

To eliminate the LCO, a dithering control mechanism is incorporated to enhance the overall performance during the steady-state condition. The DFS improves power consumptions and reduces V_{OUT} ripple frequency. Furthermore, a dynamic latch comparator is introduced to reduce voltage error between reference and feedback loop voltages.

The rest of the paper is organized as follows: Section II provides architecture and main design concept of the proposed circuit. Section III explains the sub-block circuits and the corresponding working principle. Experimental results are discussed in Section IV. Finally, the paper is concluded in Section V.

II. PROPOSED ADAPTIVE DIGITAL LDO

In the baseline digital LDO, the comparator compares V_{OUT} with V_{REF}, generating a binary output and feeds to the digital controller. The digital controller turns-on/off the switches in the MOS array depending upon the comparator output [8]. The comparison is performed either by a 1-bit analog to digital converter (ADC), comparator, or time to digital converter (TDC) [24]–[26]. To decrease the circuit complexity, unpredictability, offset and quiescent current, a dynamic latch comparator with a strong-arm is incorporated in the presented DLDO structure. The top architecture of the proposed ADLDO regulator is depicted in Fig. 2. It consists of an adaptive digital LDO controller (ADLC), a transistor switch array (TSA), a synchronous dynamic comparator (CMP) and a reference voltage selection multiplexer (MUX). For reducing power consumption and achieving fast transient response with more accurate and stable output voltage, a multi-loop (coarse, medium, and fine) ADLDO architecture including a dithering control (DC), dynamic frequency scaling (DFS) with configurable ultra-low power oscillator (ULPO) is proposed.

A. WORKING TECHNIQUE

The concept of the ADLC controller can be well understood, if we first discuss the hill-climbing algorithm. Fig. 3, shows the N numbers of switches controlled by the hill-climbing algorithm. With hill-climbing scheme, appropriate number of TSA transistors in each loop is selected automatically by the digital controller for required V_{OUT}. At a time, one of the coarse, medium or fine loop is active and single transistor is turned-on/off in each clock cycle. The transient reaction time and the output voltage variations is determined by the number of turned-on/off switches on every clock cycle depending upon the voltage difference between the V_{OUT} and the V_{REF}.

The conventional D-LDO uses long shift register (SR), which results in a slow transient response and large quiescent current. At maximum load condition, all the switches are turned-on which increase the leakage current through the LDO body. To solve this problem, in the proposed ADLDO, the TSA is divided into three sub-parts namely coarse TSA, medium TSA and fine TSA as shown in Fig. 2. The power switch unit size is 0.5 μm, for all the fine loop (1 $\times$ LSB), medium loop (M $\times$ LSB) and coarse loop ((C $\times$ M) $\times$ LSB).The coarse loop has higher voltage step resolution than that of medium loop. Similarly, medium loop exhibits higher voltage step than fine loop. The various load conditions are sensed and different loops are activated automatically to achieve fast transient response. At heavy load condition, coarse loop is activated first to take higher steps, then medium loop, and finally fine loop comes into action to reach to the desired output value. This mechanism is shown in Fig. 3(a). At light load condition, the fine loop remains active and finds the new target. This mechanism is shown in Fig. 3(b). The proposed multi-loop architecture reduces the bi-directional shift register length and consequently reduces the power loss, quiescent current and achieve fast transient response.

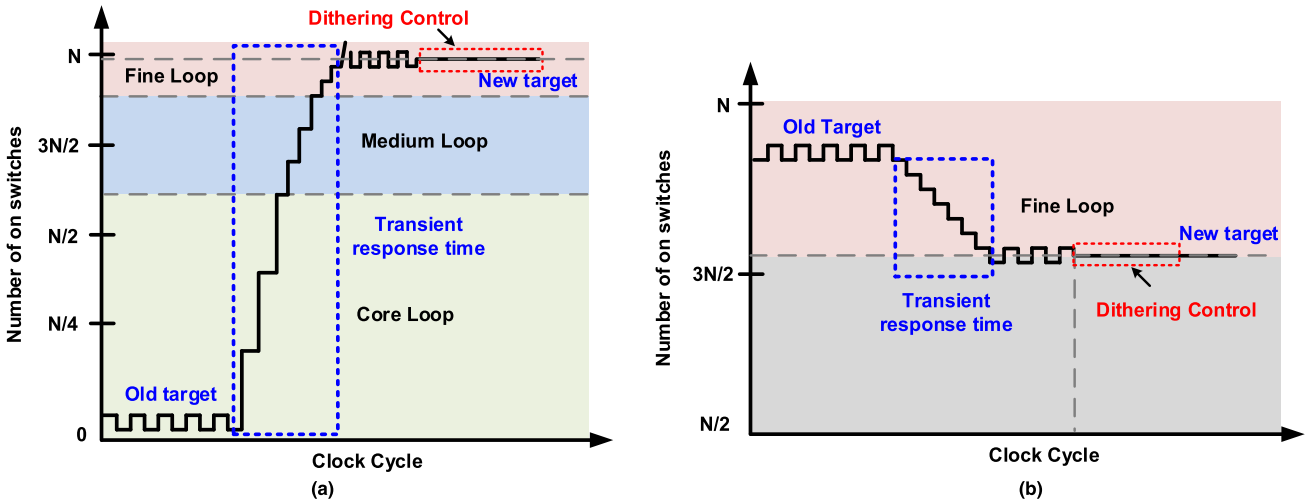

FIGURE 3. Timing diagram for hill climbing algorithm (a) for drastic change (b) for small load change.

III. IMPLEMENTATION OF SUB-BUILDING BLOCK

A. ADAPTIVE DIGITAL LDO CONTROLLER

The adaptive digital LDO controller is the brain of the proposed digital LDO. It senses load variations, selects reference voltages, controls TSA, manages loops, and directs dithering and DFS for fast settling with minimized ripples and low IQ. The architecture of ADLC is shown in Fig. 4(a). It is composed of adaptive FSM controller, dithering control unit (DCU) and loop control logic blocks, namely coarse control, medium control and fine control.

The identical architecture for loop control logic blocks is adapted and it is elaborated in Fig. 4(b). The loop control logic directly controls TSA in corresponding loop and is derived from FSM by INC and DEC signals. It is composed of hill climbing shift register, a counter and related control circuit. The shift register is a parallel in, parallel out left right shift register. On reset or power up, it is loaded with default value of all one's which means all PMOS transistors in TSA are in off state. When load increases, shift register, shifts left and its LSB is filled with zero on each clock cycle. This will turn on the PMOS transistors one by one in TSA until the required output voltage is achieved. Similarly, in case of light load, sensed by FSM, the shift register, shifts right and its MSB is filled with one, turning off transistors. The counter tracks shift register minimum and maximum boundaries during loop operation. When the Adaptive digital LDO regulator (ADLDO) powers up and there is no load or minimum current at the output, according to the proposed architecture the feed-back voltage is compared with a low reference (LR) voltage and only one PMOS is active in each of coarse, medium and fine loop transistor array. For reducing V_{OUT} ripples, the DCU is designed with digital first order sigma-delta modulator (DSDM) as shown in Fig. 4(c). The DSDM internally generates 8-bit random pattern and uses two LSB <1:0> bits for turn-on/off of two PMOS switches in the dithering mode while third transistor is always in on state. The flowchart of FSM is depicted in Fig. 5. On power up, it loads default TSA control values, disables dithering control and DFS and selects low reference (LR) voltage. Since, the output voltage is zero on power up, therefore, it turns on coarse loop by controlling coarse control and coarse TSA and continuously monitors the comparator output CMPO signal. When V_{OUT} reaches to required coarse range, the CMPO becomes high. The FSM, then turn off coarse control and freeze its value, selects medium reference (MR) voltage, and triggers medium control for medium loop voltage tuning. Similarly, fine loop operation is completed after achieving medium output voltage range. When fine tuning finishes, the output voltage is monitored for few clock cycles to get steady state and for verifying stability. The FSM turns on dithering control to minimize and suppress output ripples and keeps sensing load variation in steady state. It also enables DFS to lower the CLK frequency and save power consumption. In steady state, in case of load variation, FSM disables dithering, identifies the new loop region by selecting LR, MR and high reference (HR) voltages one by one in this order and monitoring CMPO. When the CMPO is detected low for a reference voltage, then the corresponding and subsequent loops including dithering and DFS are activated one by one to get steady state as shown in Fig. 5.

B. VOLTAGE SELECTION

In the previous literature, if multiple references are used, the same number of comparators and band-gap references (BGR) are mandatory. It occupies large area, increases power consumption and also results in circuit complexity. In this proposed work, multiple internal references (LR, MR and HR) are derived from single external reference V_{REF}. The voltage selection selects required reference according to load. The voltage selection block diagram and circuit implementation show in Fig. 6.

The voltage selection circuit is implemented using transmission gate (TG) and an inverter (INV). In the voltage selection circuit, one main reference V_{REF} is divided into

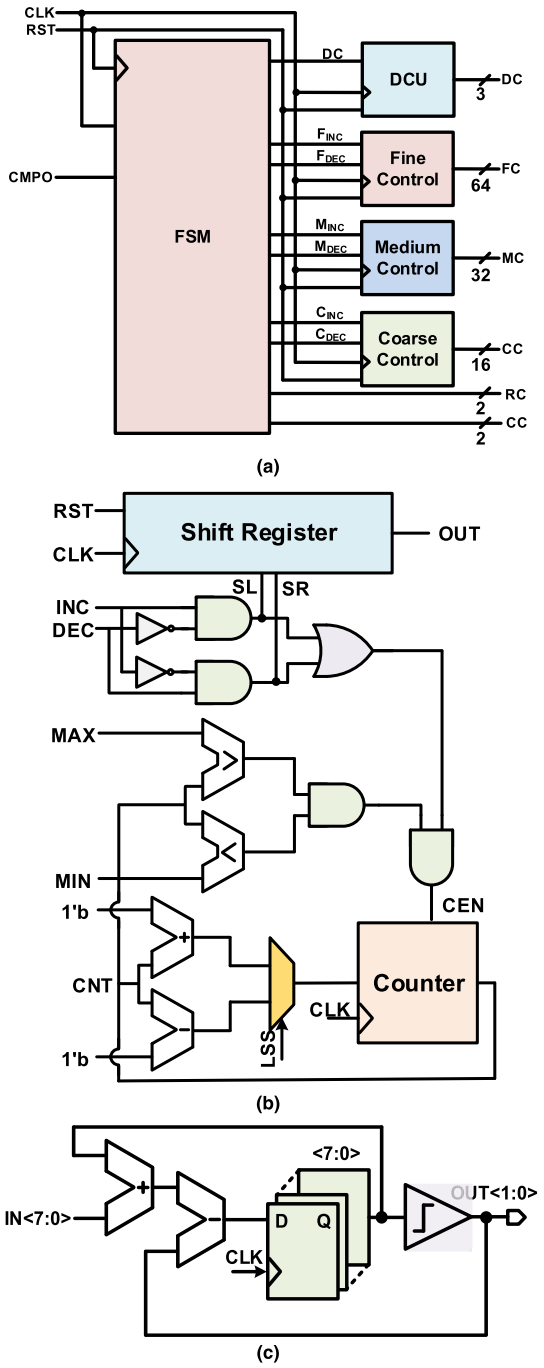

FIGURE 4. ADLC controller architecture (a) FSM (b) LCL (c) DCU.

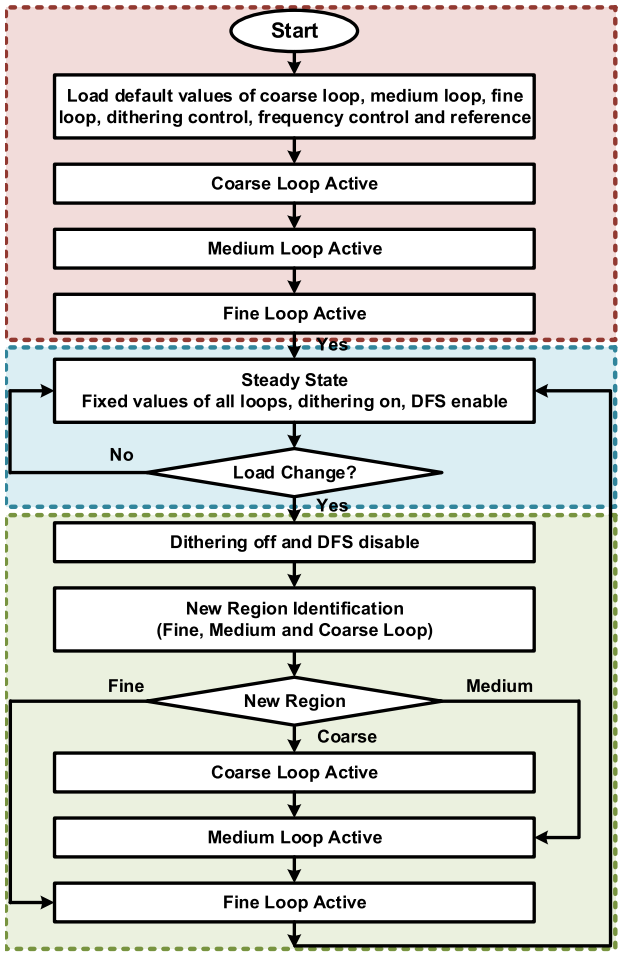

FIGURE 5. Digital controller flow chart diagram.

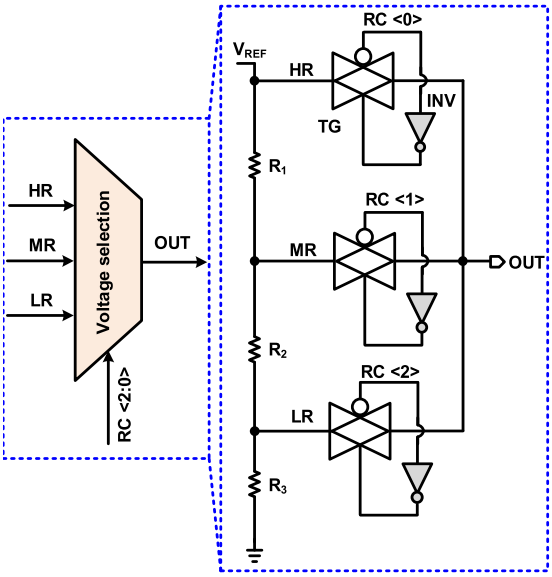

FIGURE 6. Proposed voltage selection symbol and circuit implementation.

two more reference voltages by using voltage divider and these voltages are given to the comparator. The main reference, called HR, is selected when the fine loop is activated. Similarly, MR and LR are selected, when medium loop and coarse loop are active, respectively. The different voltage references are selected during loop operations form FSM with voltage selection select signal.

C. DYNAMIC COMPARATOR

The use of conventional comparator at ultra-low supply voltage results in two main problems; 1) insufficient voltage headroom, and 2) longer comparison time [24]. In order to overcome these problems and improve overall speed and intrinsic gain, a regenerative latch dynamic comparator with

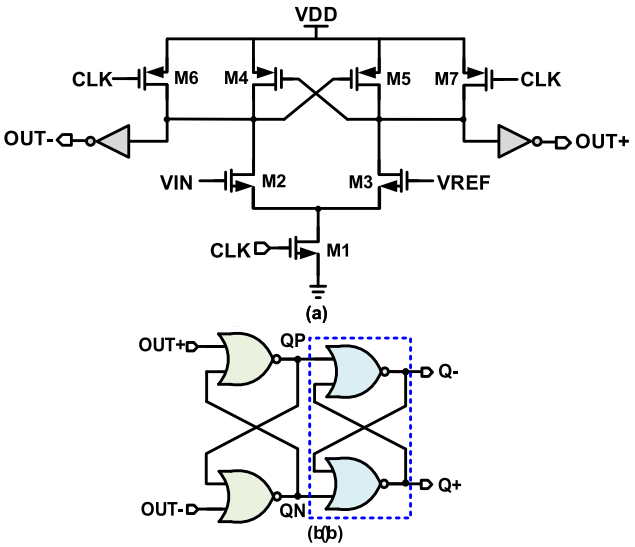

FIGURE 7. Schematic of proposed (a) dynamic comparator (b) S-R latch.

strong arm is similar to proposed in [24]. The circuit diagram of the comparator is shown in Fig. 7.

The working principle of the regenerative latch is explained as follows. The M2 and M3 are N-type MOS input transistors. During the comparison phase, the M1 is turned on, when the CLK changes to VDD. For the duration of the reset phase, OUT+ and OUT- of the regenerative latch are reset to supply voltage (VDD) when the CLK is set to low (VSS). The cross coupled P-type transistors (M4 and M5) are turned on which create positive latch comparator, a pair of inverters are added at the output node (OUT+ and OUT-) for the next stage. These inverters also play important role as an isolation stage between the output and input, decreasing the kick back effect compared to the conventional comparators. However, at low supply voltage condition, the common-mode output nodes, OUT+ and OUT−, of the regenerative latch reach as close as VDD during the sampling and regeneration phases. This causes a race condition to occur in the S-R latch, where the inputs QP and QN transits into a forbidden state and both outputs Q- and Q+ are pulled down momentarily before comparison phase is completed. The subsequent logic outcome is affected by the incorrect output caused by the glitches. To maintain the COM output constant and eliminating the glitches, NOR based latch is used with two stage in this work. The proposed comparator compares the feedback voltage (FBV) and the output voltage of the RVSM block and translates this voltage difference to digital control signal '0' or '1'. The number of turn-on PMOS transistors is decided by these signal.

D. ULTRA-LOW POWER RC OSCILLATOR

Fig. 8 shows the circuit diagram of ultra-low power RC oscillator that is composed of start-up, charge/discharge sensing, clock generation, and current reference. The current source/sink operates in sub-threshold region or weak inversion for low power operation. The output resistance of a current source or sink is increased by cascaded the

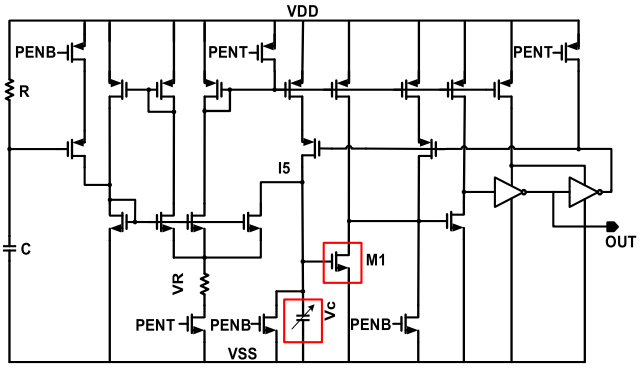

FIGURE 8. Schematic of ultra-low power RC oscillator.

current mirrors. For clock generation, generated current is mirrored by the current mirror to feed hysteresis controller M1, capacitor and current-starved invertors. The capacitor is charged by the drain current I5 and when Vc becomes equal to Vth of M1, the hysteresis controller M1 will turn on.

E. DITHERING CONTROL

In the previous D-LDO structures, different techniques such as freeze mode [18] and dead zone [22] are used to control output voltage ripples. After fine loop, the freeze mode is enabled by an external signal in the steady state [18]. The main drawback of this manual approach is that it stops the controller clock and halts the system in the freeze mode resulting relatively either higher or lower voltage compared to target value as shown in Fig. 9(a). Also, in freeze mode, since he controller is disabled, therefore, the load variation cannot be identified and rectified. In another dead zone approach, output ripples are eliminated to some extent to achieve smooth output at the cost of additional circuitry [22]. Two additional comparators are incorporated for this purpose which require more area and additional power. To overcome the issues in previous structures, an automatic digital dithering technique is proposed in the ADLDO regulator for suppressing LCO in the output. A DCU, depicted in Fig. 4(c) is designed for dithering operation. The digital controller automatically enables DCU after completing fine loop operation in the steady state condition. The DCU controls three transistors which are very small in size as compared to that of fine loop. It turns on one transistors permanently and toggles two others transistors by a random pattern generated by SDM. The output ripples are reduced almost 70% as compared to that in fine loop as elaborated in Fig. 9(b). In dithering state, if there is load variation, it is detected automatically and LDO achieves steady state again for new target output. In the dithering state, controller reduces LCO and enhance the overall system performance.

F. DYNAMIC FREQUENCY SCALING

The average power consumption PAV in CMOS circuit is sum of dynamic PDYN, short circuit PSHORT, leakage PLEAKAGE and static PSTATIC power consumptions [27] as explained in (2) as follows:

$$P_{AV} = P_{DYN} + P_{SHORT} + P_{LEAKAGE} + P_{STATIC} \quad (2)$$

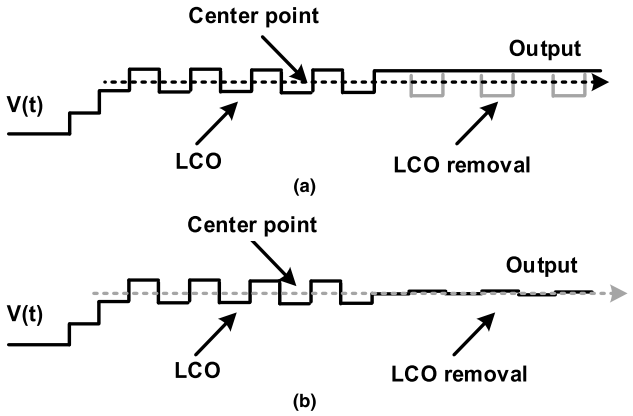

FIGURE 9. Conceptual waveform with (a) freeze mode (b) dithering control.

In CMOS circuits, P_{DYN} is the dominant power consumption component. It is linear function of operating frequency f of the circuit as given in (3) as follows:

$$P_{DYN} = KCfV_{DD}^2 \tag{3}$$

Where, K is switching activity factor, C is loading capacitance and VDD is supply voltage [28]. From (3) it is obvious, if the switching frequency reduces, the power consumption of the CMOS circuit is reduced.

In the proposed ADLDO, dynamic frequency scaling is designed for reducing power consumption of ADLC and ULPO in steady state. The ULPO clock frequency is configurable from ADLC. Two frequency modes, namely transient frequency mode (TFM) and power frequency mode (PFM) are designed in frequency scaling technique. In TFM, the ULPO generates faster clock and it is enabled during loop operations for fast transient response. The PFM is relatively very slow clock mode and it is selected in steady state after fine loop for monitoring the load variations and reducing power consumption. On power up and reset, ADLC selects TFM for attaining desired output voltage in transient phase. Once, the steady state is identified, the PFM is enabled for monitoring load variations and lowering the power consumption. When output load changes, ADLC identifies it and switches ULPO from PFM to TFM for fast transient.

IV. EXPERIMENTAL RESULTS

A. CHIP PHOTOGRAPH AND MEASUREMENT SETUP

Fig. 10(a) shows the chip photograph of the proposed ADLDO regulator. The proposed circuit is implemented in a 28 nm CMOS technology with an active chip area of 0.016 mm^2. The Fig. 10(b) shows measurement setup to test the chip. On-chip resistor (RINT) is used to control the load current. A waveform generator feeds a test signal (LOAD_Test) to the MN transistor in order to sharpen the edge of the signal. The voltage across source and drain is reduced by using large size MN transistor. The separate supply voltage (VDD_CONT) is used to find the current consumption of the proposed controller. The VDD supply

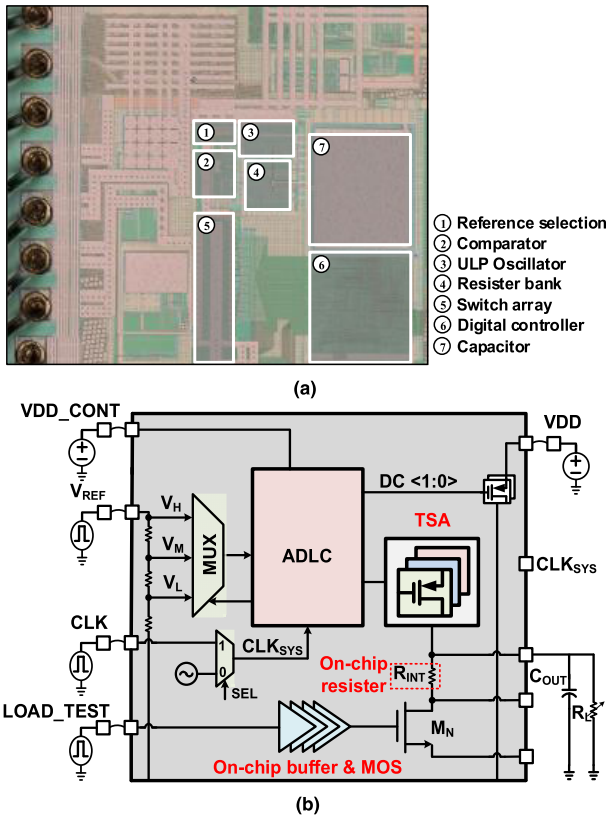

FIGURE 10. (a) Chip microphotograph of the proposed circuit, and (b) measurement setup to test the performance of the proposed ADLDO.

voltage is used to provide power to MOS switches and to measure the load current. During measurement, the ULPO frequencies are configured to 10 MHz and 1 MHz in TFM and PFM respectively. An external clock is also added for reliable operation of the proposed circuit. The value of the off-chip load capacitor (C_{OUT}) used in the proposed circuit is 100 pF. This optimum off-chip capacitor value helps in fast recovery of counters during load transients. In addition, the off-chip load capacitor improves the under-shoot and over-shoot of the output voltage when load current changes.

B. LOAD TRANSIENT RESPONSE

Fig. 11 shows the measured load transient response waveforms of the proposed ADLDO. The performance of the circuit is checked from 0.5 mA to 10 mA load current. Fig. 11(a) shows measured load response of the ADLDO circuit when load current is changed from 2 mA to 10 mA at $V_{IN} = 0.95$ V, and fs = 10 MHz. The resulting measured undershoot and overshoot voltages of the proposed circuit are 45 mV and 20 mV, respectively. Fig. 11(b) shows measured load response when load current is changed from 0.5 mA to 2 mA at $V_{IN} = 0.5$ V while $V_{OUT} = 0.45$V, and fs = 10 MHz. The measured undershoot and overshoot voltages are 48 mV and 24 mV, respectively. Fig. 12(a) shows the measured load response from minimum to maximum load variations while Fig. 12(b) shows the real-time simulation results of dithering mode. The load transient edge time is < 1 ns.

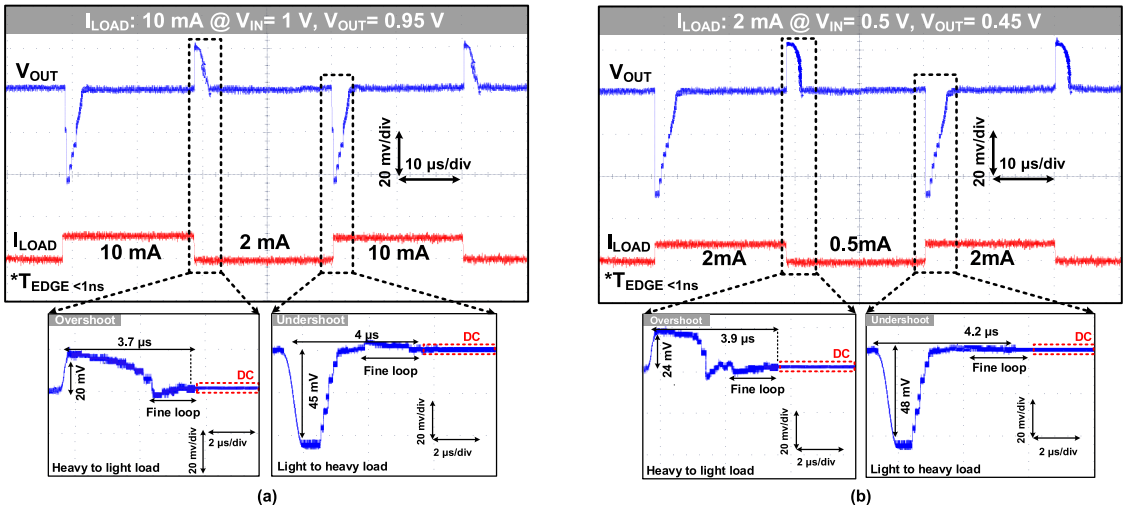

FIGURE 11. Measured load transient response with (a) V_{IN} = 1V, f_s = 10MHz, and (b) V_{IN} = 0.5V, f_s = 10MHz.

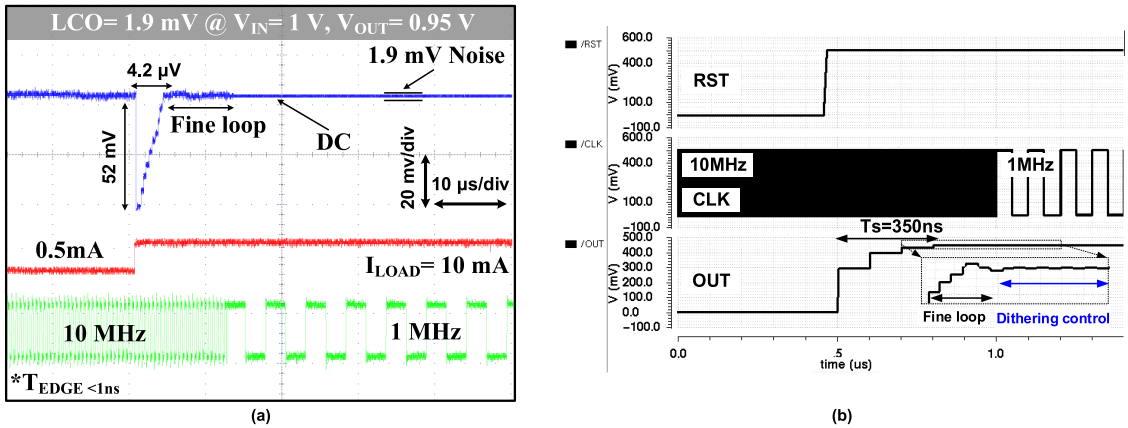

FIGURE 12. Measured load transient response from minimum to maximum load with (a) V_{IN} = 1V, f_s = 10MHz, and (b) Simulation results of Dithering mode in real-time.

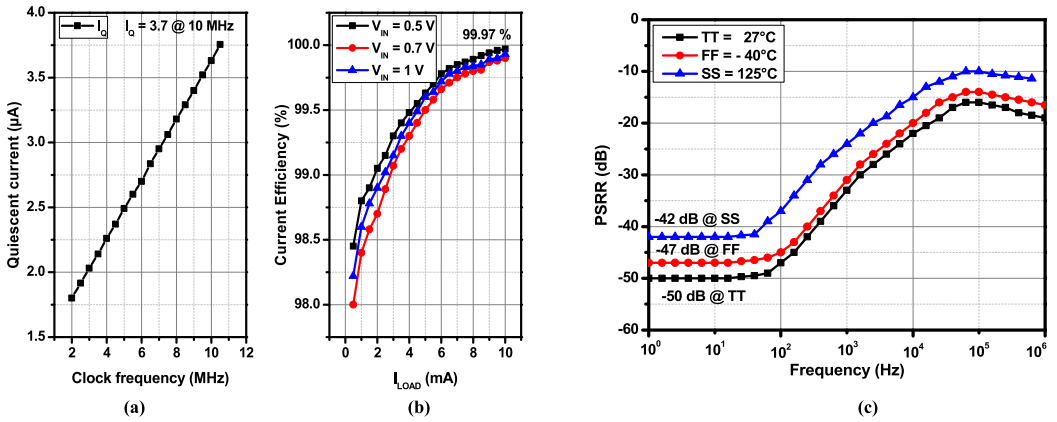

FIGURE 13. Measured (a) quiescent current with respect to frequency (b) current efficiency, and (b) PSRR with corner simulation.

C. QUESENT CURRENT AND PSRR

The quiescent current (I_Q), PSRR and current efficiency measurement results are shown in Fig. 13. The I_Q increases linearly with the increase of the frequency as plotted in Fig. 13(a). The I_Q and PSRR is defined in (4) and (5). The measured minimum value of I_Q is 1 μA at 1 MHz while maximum I_Q is 3.7 μA at 10 MHz. The LDO current efficiency as a function of load current is measured for three different input voltages of 0.5 V (min), 0.7 V and 1 V (max) shown in Fig. 13(b). The proposed ADLDO shows superior

TABLE 1. Performance comparison.

Parameter	This Work	[19]	[17]	[18]	[20]
Architecture	Digital	Digital	Digital	Digital	Digital
Process (nm)	28	28	65	65	130
Chip Area (mm^2)	0.016	0.019	0.012	0.034	0.114
INPUT (V)	0.5-1	0.6-0.65	0.5-1	0.5-1	0.5-1.2
OUTPUT (V)	0.45-0.95	0.55-0.6	0.35-0.95	0.45-0.95	0.45-1.14
ILOAD (mA)	0.5-10	5-25	2.8	10	3
I_Q (µA)	3.7 @ 10 MHz 1 @ 1 MHz	28	45.2	4.2	24
Vdrop_Out (mV)	50	50	60	50	750
Operating Frequency (MHz)	10	10	12	10	10
Transient Time (µs)	0.350	10	0.37	1	3
Load Regulation (mV/mA)	2.2	20	46	2.3	10
Line Regulation (mV/V)	9.5	-	-	30	3.5
Current Efficiency (%)	99.97	99.6	98.4	95.5	> 90
Power Efficiency (%)	89.7 @ 10 MHz 93.4@ 1 MHz	-	88.6	88	-
Output ripple (mV)	1.9	-	10	3	-

current efficiency at 0.5 V input voltage. The peak current efficiencies of the proposed circuit are 99.97%, 99.93%, 99.88%, at input voltages of 0.5 V, 0.7 V, and 1 V, respectively, for 10 mA load current. Fig. 13(c) shows the measurement results of power supply

$$PSRR = \frac{V_{OUT\_VARI}}{V_{IN\_VARI}}, at\ all\ frequency \tag{4}$$

$$I_Q = I_{IN} - I_{OUT} \tag{5}$$

ratio (PSRR) at three different temperature ranges −40 °C, 27 °C and 125 °C. The measured PSRR of the proposed circuit is −50 dB (at 27 °C), −47 dB (at −40 °C), and −42 dB (at 125 °C), respectively.

D. LINE AND LOAD REGULATION RESULTS

Fig. 14 shows the load and line regulation measurement results of the proposed ADLDO regulator to check the stability. The load regulation is measured at three different reference voltages by varying the load. As shown in Fig. 14(a), the minimum measured load regulation is 2.2 mV/mA at 450 mV reference voltage while the maximum measured load regulation value is 6 mV/mA at 650 mV. The line regulation is also measured by using three different reference voltages by changing the supply voltage. For 10 mA load, the minimum and the maximum measured line regulation is 9.5 mV/V at 450 mV and 12.7 mV/V at 650 mV, respectively as depicted in Fig. 14(b). The load and line regulation is defined in (6) and (7).

$$Load_{REG} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{6}$$

$$Line_{REG} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{7}$$

E. COMPARISON WITH PUBLISHDED WORK

Table 1 shows the performance of the proposed ADLDO regulator and compares with the prior works. The proposed ADLDO regulator achieves fast transient response, courtesy multi-loop architecture. The power and current efficiencies of the proposed circuit are better than the published works.

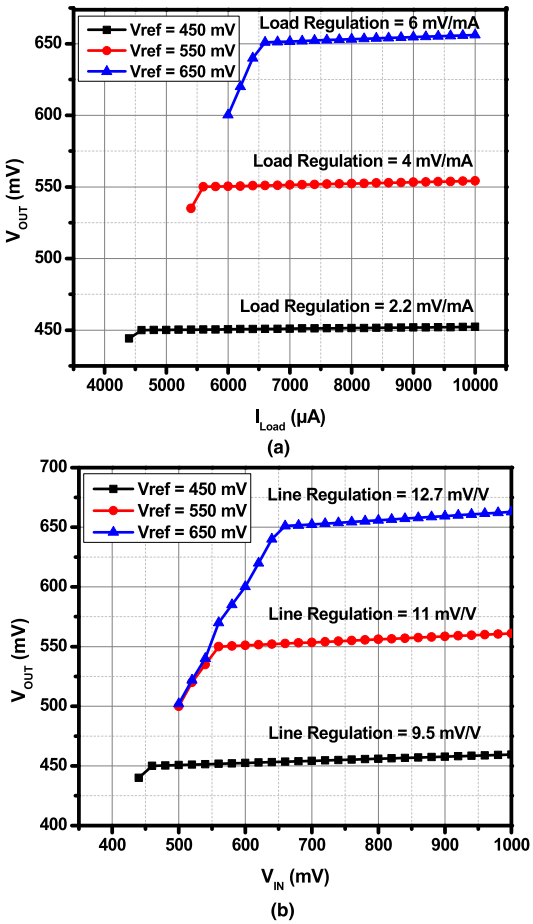

FIGURE 14. Measured (a) Load regulation, and (b) Line regulation with respect output voltage.

Moreover, the proposed circuit obtains better line and load regulation than most of the reported works.

V. CONCLUSION

A high performance adaptive digital LDO is presented in this paper for IoT applications. For achieving high current and power efficiencies, suppressing output voltage ripples and attaining fast transient response, fully synthesizable adaptive

digital controller automatically senses load variations and adaptively controls multi-loop architecture. The hill climbing technique minimizes transient response, reduces leakage current in TSA and improves output DC voltage accuracy. In steady state, dithering minimizes LCO and DFS reduces controller power consumption. Dynamic latch comparator reduces offset and output voltage error. The measured output voltage is from 0.45 V to 0.95 V with 50 mV dropout voltage when the input supply voltage is varied from 0.5 V to 1 V. The operating frequency is 10 MHz in TFM for fast transient response and quiescent current of 350 ns and 3.7 μA, respectively. The load current value ranges from 0.5 mA to 10 mA. Measured load and line regulations are 2.2 mV/mA and 9.5 mV/V respectively. The maximum measured power and current efficiencies are 89.7 % and 99.97 %, respectively, with 1.9 mV output voltage ripples. The proposed circuit is fabricated with 28 nm CMOS process with 0.016 mm^2 chip area.

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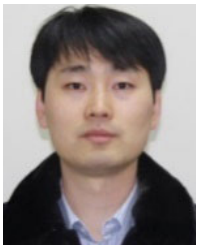

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