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An Investigation of Gate Voltage Oscillation and Its Suppression for SiC MOSFET

WEICHI ZHANG[1], (Member, IEEE), XIANG WANG[1], MOHAMED S. A. DAHIDAH[1], (Senior Member, IEEE), GRAEME N. THOMPSON[2], VOLKER PICKERT[1], (Member, IEEE), AND MOHAMMED A. ELGENDY[1]

[1]School of Engineering, Newcastle University, Newcastle upon Tyne NE1 7RU, U.K.
[2]New Product Department, Turbo Power Systems Ltd., Gateshead NE11 0QD, U.K.

Corresponding author: Weichi Zhang (weichi.zhang@ncl.ac.uk)

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ABSTRACT Silicon Carbide (SiC) MOSFET has undergone a rapid development and commercialization in recent years due to its superior features. However, the mainstream commercial SiC MOFESTs are often fitted to packages that are previously designed for silicon-based devices, which brings oscillation issues at faster switching speed. This paper investigates the gate oscillation based on the parasitic parameter analysis of equivalent SiC MOSFET circuit, where the influences of di/dt and dv/dt are discussed and compared. Moreover, the paper recommends a guideline for the acceptable gate oscillation for SiC MOSFET based on the data from manufacturers and carries out detailed comparisons of the conventional gate driver tuning methods. It is found that the external gate-source capacitor provides better switching performance and gate oscillation suppression than the tuning of gate resistor. The analysis and the switching performance are verified from the experimental results based on Cree CAS300M12BM2 SiC MOSFET Module.

INDEX TERMS SiC MOSFET, equivalent circuit model, gate oscillation, di/dt and dv/dt feedback, double-pulse-test.

NOMENCLATURE

ABBREVIATIONS

DPT	Double pulse test
EMI	Electromagnetic interference
IGBT	Insulated-gate bipolar transistor
KVL	Kirchhoff's voltage law
MOSFET	Metal-oxide-semiconductor field-effect transistor
Si	Silicon
SiC	Silicon Carbide
WBG	Wide bandgap

I. INTRODUCTION

Wide bandgap (WBG) semiconductors show superior material properties over conventional silicon (Si) devices, featuring higher voltage and temperature operation, low on-resistance and faster switching speed. These characteristics facilitate higher efficiency, power density and arguably better reliability, which promise to revolutionize the next generation of power electronics converters [1]–[3]. Among the WBG semiconductors, SiC MOSFET are under rapid development and commercialization, mainly targeting the high-voltage and high-power applications as a substitution of conventional Si IGBT. The applications that adopt SiC technology can utilize higher switching frequency, together with lower losses and high-temperature capability, showing evident advantages over conventional Si-based applications in terms of performance and volume [4]–[6].

However, the fast switching characteristics of SiC MOSFET also poses challenges as their benefits are limited by the packaging technology, specifically the parasitic parameters [7]–[10]. Due to large dv/dt slew rate, the parasitic capacitance in the SiC MOSFET brings crosstalk and false turn-on issues, which have been discussed in previous studies [11]–[14]. On the other hand, the issues of gate voltage spikes and oscillations from the stray parameters remains under consideration [15], [16]. Owing to the bonding wires and interconnections in the package, the parasitic inductance can lead to undesirable voltage spikes across the device during turn-off as documented in [17], [18]. In addition,

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TABLE 1. Supply voltage from manufactures.

Manufacturers		$-Vg$	$+Vg$
Infineon CoolSiC™	Limit	$-10\,V$	$+20\,V$
	Recommended	$-5\,V$	$+15\,V$
Cree 2nd gen SiC BM2	Limit	$-10\,V$	$+25\,V$
	Recommended	$-5\,V$	$+20\,V$
Semikron SEITRANS® 3	Limit	$-6\,V$	$+22\,V$
	Recommended	$-3\,V$	$+18\,V$
Rohm SiC MOSFET BSM	Limit	$-4\,V$	$+26\,V$
	Recommended	$0\,V$	$+18\,V$
Infineon IGBT Modules	Limit	$-20\,V$	$+20\,V$
	Recommended	$-15\,V$	$+15\,V$
Rohm IGBT W-Series	Limit	$-30\,V$	$+30\,V$
	Recommended	$-15\,V$	$+15\,V$

the source inductance in the gate loop can induce a voltage feedback that works against the supplied gate voltage during turn-on and turn-off due to the di/dt. For SiC devices, this voltage feedback is particularly large due to the fast switching speed, and it could potentially pose a positive voltage spike during turn-off that is above the threshold voltage, thus having the risk of turning the device back on. Furthermore, the parasitic inductance also forms a resonant tank with the gate-source capacitance, leading to high frequency voltage oscillations across the gate loop, where the negative undershoot could exceed the maximum allowable negative voltage [19]. All in all, the high gate oscillation could lead to spurious turn-on, extra losses and EMI that pose reliability issues on the power converter, as well as potential degradation of device lifetime.

For IGBT devices this feedback voltage is not an issue as its switching speed is slower, and the supply turn-off voltage is typically low ($\leq -8V$). Whereas for SiC devices, the faster switching speed leads to a much large di/dt and dv/dt [20]. Meanwhile, as the maximum allowable negative voltage remains a challenge in the SiC technology, it also needs a higher turn-off voltage compared to Si-based power device [21], [22]. Moreover, as there is no regulation and standard on the supply voltage, and it varies with evolving development and new chip generations from different manufacturers. Table 1 lists some gate supply voltages for SiC MOSFET and Si IGBT from different suppliers, where the typical turn-off voltage is above -5V, or even zero for some devices.

For some applications, the feedback voltage can be reduced by carefully selecting the devices in low parasitic housing, or the ones that adopt Kelvin source [17]. These methods could in turn minimize the gate voltage spikes and oscillations. However, Kelvin source is not enough for oscillation reduction when driving some high current SiC power modules at their rated current. With the feedback, the positive voltage spike could still reach the threshold voltage during turn-off. Consequently, mitigating the feedback voltage from the device itself is not effective for all applications, and more importantly, gate drivers need to be designed and tuned specifically to tackle these issues.

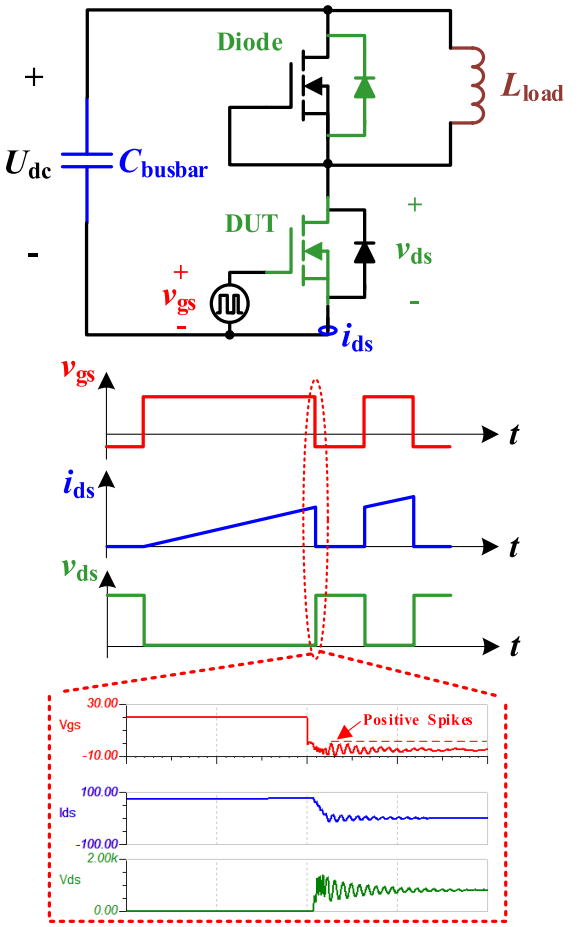

FIGURE 1. DPT simulation with ideal supply voltage.

In this paper, the gate oscillation from di/dt and dv/dt feedback is analyzed in detail, along with validation using experimental tests. Furthermore, a guideline for gate voltage oscillation is proposed, in which it should be limited between the minimum threshold voltage and allowable negative voltage of the device to avoid any false turn-on and overstress issue. In addition, different gate driver tuning methods are investigated based on the experimental results. By comparing the switching performance and the suppression of gate oscillation, an optimal gate driver tuning for SiC devices is carried out to ensure the gate voltage oscillation is within the recommended guideline. The remainder of the paper is structured as follows: Section II depicts the gate voltage oscillation from simulation and analysis of the dv/dt and di/dt feedback using equivalent circuit model. Section III reports the experimental testing of the gate voltage oscillations at different voltage and current levels. In Section IV, the effectiveness of oscillation suppression for different gate driving tuning methods are studied with respect to their switching performance. Finally, some conclusions are drawn in Section V.

II. ANALYSIS OF FEEDBACK FROM PARASITIC MODEL

The voltage spike and oscillations that normally appear across the gate and source/emitter are due to the housing parasitic inductance and the change of di/dt and dv/dt during

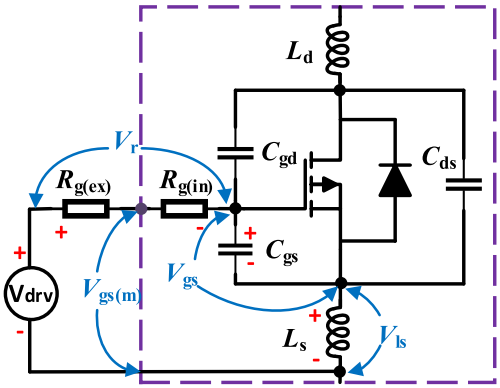

FIGURE 2. di/dt feedback via stray inductance.

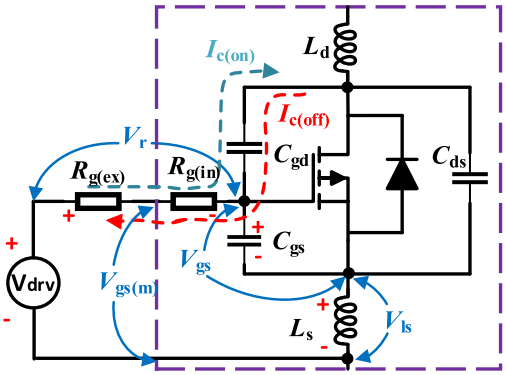

FIGURE 3. dv/dt feedback via miller capacitor.

switching transient. As highlighted in the previous section, these are particularly dangerous in SiC applications as the much faster switching speed leads to a larger di/dt and dv/dt slew rate. Fig. 1 shows the double pulse test (DPT) simulations that are designed to investigate the gate-source oscillations during switching transient. The simulations are carried out based on Cree MOSFET model C3M0016120K, in which a Kelvin Source is included. In this case, an external stray source inductance is manually introduced to help identify its implication with the di/dt.

Given a drive voltage at +20V/−5V and an external source inductance of $8nH$ in the gate loop, Fig. 1 shows the results during turn-off for 800 V and 80 A. It can be observed that the gate-source voltage V_{gs}, after the miller plateau, has positive voltage spikes that are higher than the threshold voltage, which could pose spurious turn-on issues. Meanwhile, its negative peaks also oscillate below the maximum negative voltage (−10V) of the device, which leads to device degradation over long-term operation. As a result, these oscillations must be mitigated. The following sub-sections present the analysis of the di/dt and dv/dt feedback from parasitic model.

A. di/dt FEEDBACK FROM SOURCE STRAY INDUCTANCE

Fig.2 shows a generic circuit model of the MOSFET, where the gate is connected to an external ideal drive voltage source V_{drv}. To note that only the di/dt is considered in this model thus there is no current flowing through the miller capacitor. Applying KVL to the gate loop, yields:

$$V_{drv} = V_r + V_{gs} + V_{ls} \tag{1}$$

where, V_{gs} is the gate-source voltage, V_{ls} is the voltage induced from the stray inductance and V_r is the voltage across both internal $R_{g(in)}$ and external $R_{g(ex)}$ gate resistors. Assuming gate resistors are zero, $R_{g(ex)} = R_{g(in)} = 0$, then with considering di/dt on the source stray inductance L_s, the gate-source voltage can be simplified to:

$$V_{gs} = V_{drv} - L_s \frac{di}{dt} \tag{2}$$

Equation (2) indicates that gate-source voltage will be smaller than the supply voltage V_{drv} due to the positive di/dt feedback during the turn-on transient. Whilst during turn-off, the gate-source voltage will be larger than supply voltage due to the negative di/dt feedback. Compared with the turn-on transient, the negative feedback during turn-off poses a risk as it can lead to a spurious voltage spike above the threshold voltage and turns the device back on.

B. dv/dt FEEDBACK FROM MILLER CAPACITOR

The equivalent circuit of the MOSFET with only dv/dt feedback is portrayed in Fig 3. The expression of gate loop voltage remains same as in (1). However, without di/dt, the voltage across the stray inductance L_s is neglected and therefore, the gate-source voltage V_{gs} can be represented as:

$$V_{gs} = V_{drv} - V_r \tag{3}$$

The dv/dt across the drain-source induces currents that flow through the miller capacitor C_{gd}, yielding:

$$I_c = C_{gd} \frac{dv}{dt} \tag{4}$$

To note that the direction of Miller current I_c is opposite to the change of voltage. Specifically, when the dv/dt is negative during turn-on, the Miller current is sourcing from V_{drv}. Whereas during turn-off where the dv/dt is positive, the Miller current is sinking to the V_{drv}. Therefore, the resistor voltage V_r resulted from this current feedback and the corresponding gate-source voltage V_{gs} can be expressed as:

$$V_r = -C_{gd} \frac{dv}{dt} \left(R_{g(in)} + R_{g(ex)}\right) \tag{5}$$

$$V_{gs} = V_{drv} + C_{gd} \frac{dv}{dt} \left(R_{g(in)} + R_{g(ex)}\right) \tag{6}$$

Similar to the impact of di/dt feedback, it can also be observed from (6) that the V_{gs} is smaller than the supply voltage during turn-on due to the negative dv/dt but it becomes higher during turn-off due to the positive dv/dt.

Consequently, the voltage feedback from both, di/dt and dv/dt works against the gate supply voltage. Taking into consideration the MOSFET switching behaviors, the dv/dt happens after the di/dt during turn-on, and the plateau voltage dominates the turn-on feedback. On the other hand, as the di/dt occurs after the dv/dt during turn-off, the voltage spikes and oscillation across the gate and source are dominated by the di/dt. As the turn-off voltage normally has less margin between the threshold and maximum negative rated value,

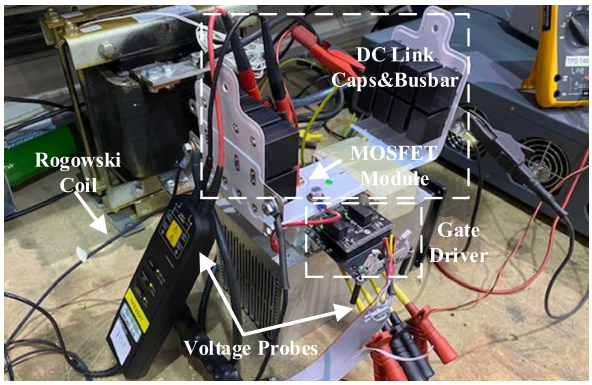

FIGURE 4. Experimental test setup.

the voltage induced from the source inductance could be more of an issue.

To investigate the switching behavior of the MOSFET, the gate-source voltage is normally monitored. However, the measurement is taken between the gate and source terminals, which is the operating driver voltage. As shown in Fig. 3 and Fig. 4, the static measurement is same as the gate-source voltage inside the module. However, owing to the di/dt and dv/dt feedback in the switching transient, the real gate-source voltage could be worse than the observed oscillations in the measurement. Therefore, to avoid any potential long-term reliability issues, the guideline for gate voltage is recommended to be between the threshold voltage and the lowest negative excursion specified in datasheet.

III. EXPERIMENTAL INVESTIGATION AND VALIDATION

Experimental tests have been conducted to further investigate the gate-source voltage oscillations. The test setup is shown in Fig. 4, which is connected to a $50uH$ inductive load. All tests are carried out based on Cree SiC half-bridge module CAS300M12BM2. The tests are first carried out at different voltage and current levels to observe the impact of di/dt and dv/dt feedback. Then, different gate driver configurations are examined and compared to help minimizing the oscillations and achieving optimal switching performance.

A. GATE-SOURCE OSCILLATIONS AT DIFFERENT CURRENT AND VOLTAGE LEVELS

In order to verify the analysis of di/dt and dv/dt feedback during turn-off, the tests are repeated with different dc-link voltages of 400V, 600V and 800V, building a drain-source current up to 350A. Fig. 5 illustrates the measured gate-source voltage and drain-source current with turn on/off voltage of 17.5V/-2.5V.

Specifically, Fig. 5(a) shows a double pulse test with a dc-link voltage of 800V. The turn-off current is shown separately at 220A and 350A, where the gate-source spike increases from 1.2 V to 2.2 V respectively, and an increase of oscillations can be observed. This is same in Fig. 5(b) and Fig. 5(c), where triple-pulse at 600V and four-pulse at 400V are triggered to build up the drain current. Noticeable increases in gate-source spikes and oscillations are observed with the increase of current; i.e. from 0V at 100 A up to 2V at 350A, as shown in Fig. 5(c). On the other hand, when comparing three dc-link voltages at 350 A in parallel, there are subtle changes in the voltage spikes, from 2V at 400V to 2.2V at 600V and 800V. Hence, the experimental results verified the previous analysis, where the di/dt feedback dominates gate-source voltage oscillation and spikes during turn-off.

B. INVESTIGATION OF GATE DRIVER CONFIGURATIONS

Similarly, the voltage across gate-source capacitor could be worse than its measurements with the parasitic taken into account. The gate-source voltage should be strictly limited between the minimum threshold voltage and the datasheet lowest specified negative voltage. According to the datasheet for CAS300M12BM2, the measured gate-source voltage oscillations should be limited between -10 V and 1.8 V when applying a turn-off voltage at -5V. These can be realized by tuning the gate driver parameters, among which, changing gate resistors and adding additional gate-source capacitance are normally the easiest and most cost-effective methods that can be adopted in most industrial applications. The following results analyze the effectiveness of suppression for the voltage spike and oscillations, as well as their implication on the switching performance. Consequently, tuning guidelines are recommended to tackle this issue.

Fig. 6 shows the gate-source voltage measurement at 800V and 300A with using three sets of gate resistors, i.e. 1.1 Ω, 2.6 Ω and 5.2 Ω. It can be seen that the amplitude of the oscillation is reduced with higher resistors. In particular, the negative undershoot greatly decreases from over −10V at 1.1 Ω to −7 V at 5.2 Ω. However, the positive voltage spikes have not changed with using different resistors. All results show a similar measurement of above 5V, which are much higher than the threshold voltage. The reason could be found in (6), in which the increase of resistor counters the decrease of the dv/dt and di/dt.

Fig. 7 shows the results for drain-source voltage and current. Larger gate resistors result in smaller voltage and current oscillations. The turn-off voltage overshoot decreases from 976V at 1.1 Ω to 920V at 5.6 Ω. Note that this is not an issue for the 1200V device, in this case, the low-inductance busbar allows to use even a lower gate resistor. Fig. 7 also shows a longer delay and turn-off transient with larger gate resistors. This impact can be clearly observed in Fig. 8 where the resultant switching powers using three different gate resistors are demonstrated. The turn-off energy, which is calculated from the integration of the switching power at 6.6mJ, 8.9mJ, 13.5mJ. In order to validate the measurement accuracy, the loss calculation is also bench-marked with the datasheet, where an inductive turn-off energy of 8mJ is given for $V_{ds} = 800$V, $I_{ds} = 300$A with $R_g = 2.5\Omega$. This is very close to the tested condition of $V_{ds} = 800$V, $I_{ds} = 306$A with $R_g = 2.6\Omega$, for which the turn-off energy calculated is 8.9mJ.

Consequently, from the previous results, although the peak-to-peak amplitude of gate-source oscillation can be reduced with larger gate resistors, there is a huge increase in

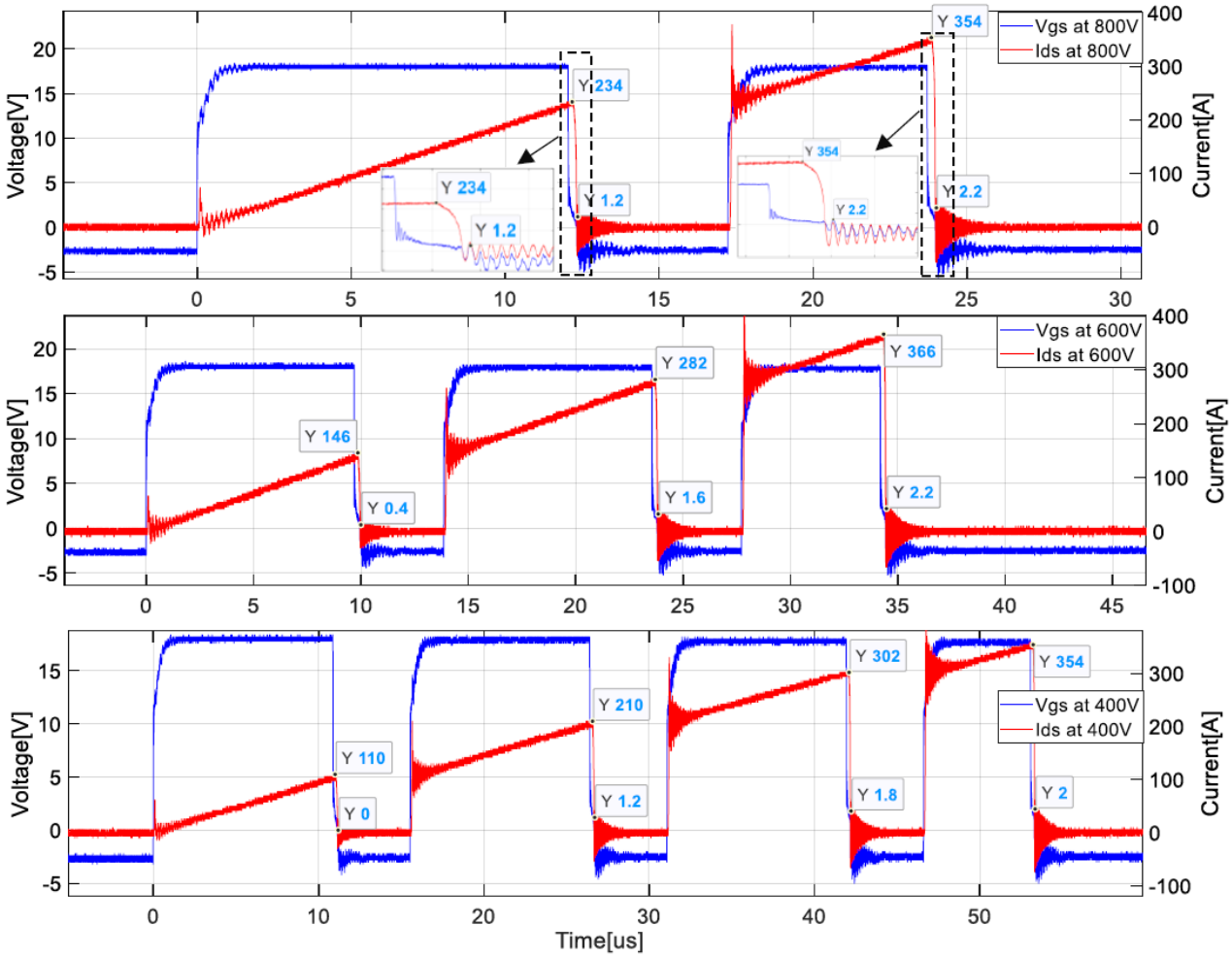

FIGURE 5. (a). Gate-source voltage and drain current measurements at 800V; (b). Gate-souce voltage and drain current at 600V; (c). Gate-source voltage and drain current measurements at 400V.

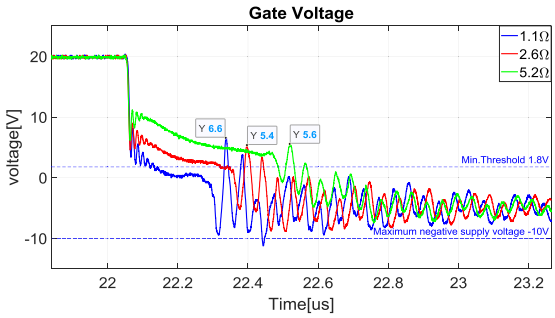

FIGURE 6. Gate-source voltage measurements with different gate resistors.

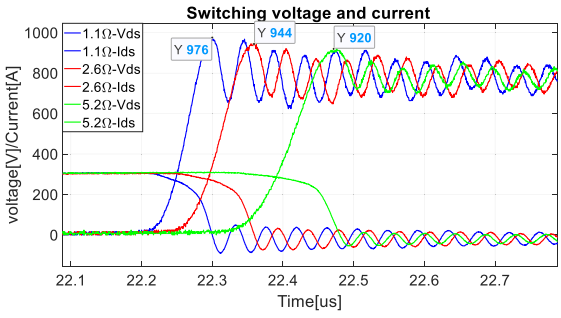

FIGURE 7. Drain-source voltage and current with different gate resistors.

switching power. More specifically, a doubled turn-off energy is calculated by increasing the gate resistor, from 6.6 mJ at 1.1 Ω to 13.5 mJ at 5.2 Ω. Besides this, high positive voltage spikes are still observed in the gate measurement. Therefore, the gate resistor does not offer a good tradeoff for this issue, and its selection should be dominated by other switching characteristics, e.g. voltage overshoot and switching energy.

Adding extra capacitance between the gate and source terminals is used in the crosstalk issue which takes up additional charge from Miller capacitance. In addition, this external gate-source capacitor could also be used as a snubber to reduce the gate voltage oscillation. As the tested module has a typical internal gate-source capacitance of 19.18nF, an additional capacitance of 10nF, 33nF and 47nF is added to the external gate-source terminals for investigation.

Fig. 9 shows the gate-source voltage measurements, where the results without any external capacitor is also captured for comparison. It can be seen that both the positive spikes and

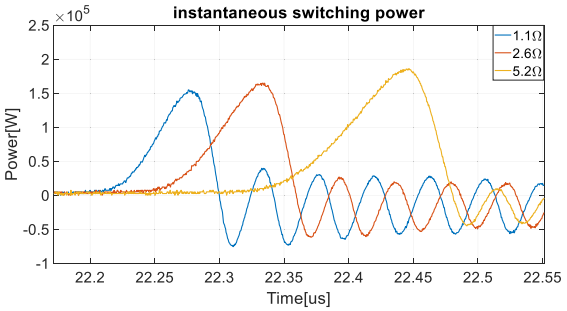

FIGURE 8. Switching power with different gate resistors.

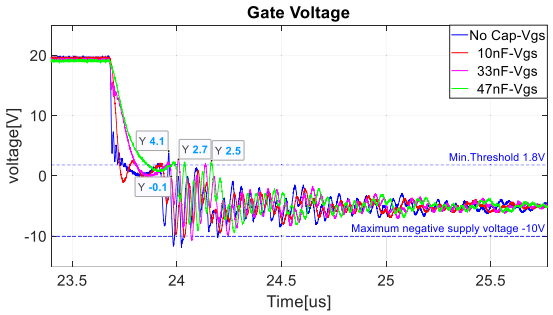

FIGURE 9. Gate-source measurements with gate-source capacitance.

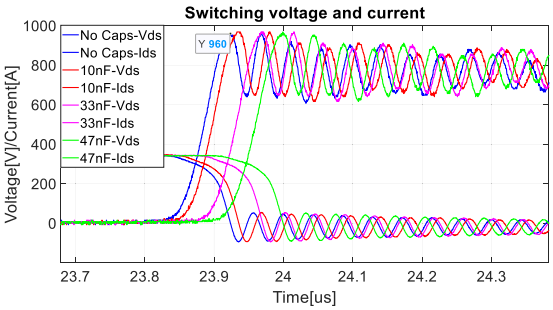

FIGURE 10. Drain-source voltage and current with gate-source capacitance.

negative undershoots are reduced with the use of external gate-source capacitance. However, the external capacitor introduces a resonant frequency with the loop inductance in the gate driver, resulting in a low-frequency oscillation that is superimposed onto the gate voltage. This can be seen in the case of 47nF, where the low frequency oscillation brings the gate voltage back to 2.5V at 24.17us. From the results, 10nF shows the best overall performance where both positive spikes and negative undershoot are within the specified range.

Fig. 10 shows the drain-source voltage and current where a 100ns delay is observed with an extra 47nF capacitor. The overshoot and oscillations are quite similar in all voltage and current waveforms. This has also been proven in the switching power presented in Fig. 11, and their corresponding switching energies are calculated at 7.6mJ (without caps), 7.7mJ (10nF), 7.7mJ (33nF) and 8.2mJ (47nF). From the results, it can be concluded that the addition gate-source capacitance could help reduce the gate voltage oscillation. While larger external capacitance does not greatly increase the switching losses compared to using larger gate resistors (13.5mJ at 5.2 Ω). It could however, introduce a larger

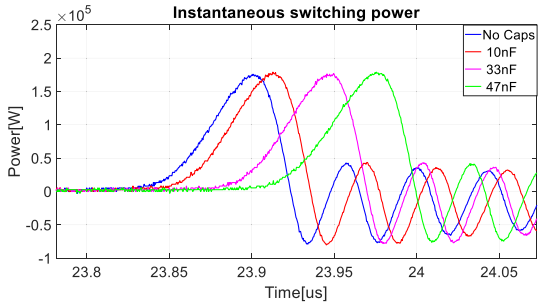

FIGURE 11. Switching power with gate-source capacitance.

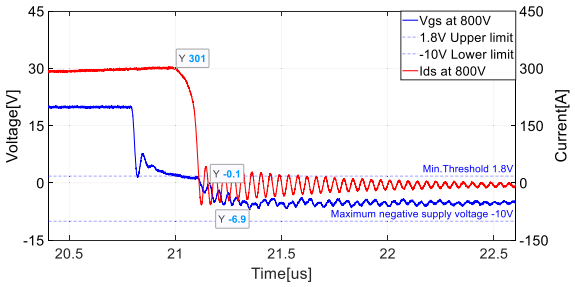

FIGURE 12. Optimized gate voltage oscillaiton at rated voltage and current (800V, 300A).

low-frequency oscillation as well as a longer switching delay. For the tested cases, 10nF is the best option that gives minimum delay and least gate voltage oscillation.

The gate oscillations can be optimized by further reducing the additional gate-source capacitance, bringing down the positive voltage spike. For the tested MOSFET module, 2nF capacitance achieved the lowest gate oscillation, and any further reduction would cause an increase of the voltage spike again. In addition, the low frequency oscillations can be further reduced by putting larger decoupling capacitors on the supply side. Fig. 12 shows the optimal gate-source voltage with an external gate-source capacitance of 2.2nF, for $V_{ds} = 800$V and $I_{ds} = 300$A.

Consequently, using both additional gate-source capacitor and larger gate resistors are cost-effective ways of tuning the switching performance. Compared with larger gate resistors, adding additional gate-source capacitance shows advantages in suppressing the gate voltage oscillation. Meanwhile, it has minimal impact on the switching performance whereas the use of larger gate resistors greatly increases the switching losses. Thus, the selection of gate resistors should be determined by other criteria, such as voltage overshoot. Note that, in order to achieve the best performance, the additional capacitor needs to be as close to the gate as possible, which should be considered in the design of the gate driver.

IV. CONCLUSION

Due to the fast switching speed and the lower maximum allowable negative gate voltage, the gate oscillation in the SiC MOSFET, particularly during turn-off, is posing health and reliability threats on the device itself and the power converter. This paper extensively analyses the gate oscillation using the equivalent circuit and simulation tools, which is then further

experimentally validated. In addition, the paper has recommended a guideline for safe turn-off gate voltage operational conditions, and at the same time investigated cost-effective gate driver tuning methods, namely larger gate resistors and additional gate-source capacitance, to suppress the oscillations. The results of switching performance as well as the techno-economic have been analyzed and compared, which could be used for any future SiC applications.

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WEICHI ZHANG (Member, IEEE) received the B.E. degree from the Xi'an University of Technology, Xi'an, China, in 2012, and the M.Sc. and Ph.D. degrees from Newcastle University, Newcastle upon Tyne, U.K., in 2014 and 2019, respectively. His Ph.D. degree research was on the power quality improvement of grid-connected PV inverter systems. He is currently a Knowledge Transfer Partnership (KTP) Associate with Newcastle University, working in collaboration with Turbo Power System (TPS) Ltd., on the utilization of Silicon Carbide technology and the development of new generation power converters. His research interests include the control of power converters, electromagnetic interferences (EMIs) and compatibility issues (EMC), and wide bandgap (WBG) devices.

XIANG WANG received the B.Sc. degree from the School of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2014, and the M.Sc. degree from the School of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2017. He is currently pursuing the Ph.D. degree with the School of Engineering, Newcastle University, Newcastle upon Tyne, U.K. His research interests include the gate driver design and health monitoring for wide bandgap (WGB) devices, and wireless power transfer techniques.

MOHAMED S. A. DAHIDAH (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Multimedia University, Malaysia, in 2008. He was an Assistant Professor with the Department of Electrical and Electronics Engineering, The University of Nottingham at Malaysia Campus, until November 2012. He is currently a Senior Lecturer with the School of Engineering, Newcastle University, Newcastle upon Tyne, U.K. He has authored or coauthored a number of refereed journal articles and conference papers. His research interests include modular multilevel converters, SHE-PWM modulation techniques for power electronics converters, battery chargers for EVs, solid-state transformers, and renewable energy integration. He is the Deputy Editor-in-Chief of *IET Power Electronics* and has been a regular Reviewer of both IEEE and IET journals.

GRAEME N. THOMPSON received the B.Sc. degree in electrical and electronics engineering from Newcastle University, Newcastle Upon Tyne, in 1984. He was previously employed as a Senior/Lead Engineer by the NEI/Rolls-Royce, specializing in power electronics and controls for rail and industrial systems. He is currently employed by Turbo Power Systems Ltd., as a Chief Engineer for Power Electronics and the Engineering Manager (for product development). He is also a member of the Institution of Engineering and Technology and registered with the U.K. Engineering Council as a Chartered Engineer.

VOLKER PICKERT (Member, IEEE) received the Dipl.Ing. degree in electrical and electronics engineering from RWTH Aachen University, Germany, in 1994, and the Ph.D. degree in power electronics from Newcastle University, Newcastle upon Tyne, U.K., in 1997. He studied at RWTH Aachen University and Cambridge University, U.K. From 1998 to 1999, he was an Application Engineer with Semikron GmbH, Nuremberg, Germany. From 1999 to 2003, he was a Group Leader at Volkswagen AG, Wolfsburg, Germany, responsible for the development of electric drives for electric vehicles. In 2003, he was appointed as a Senior Lecturer with the Electrical Power Group, Newcastle University, and he became a Full Professor of power electronics, in 2011. In 2012, he became the Head of the Electrical Power Group. He has published more than 150 book chapters, journal articles, and conference papers in the areas of power electronics and electric drives. His current research interests include power electronics for transport applications, thermal management, health monitoring techniques, and advanced nonlinear control. He received the IMarEST Denny Medal for the Best Article in the *Journal of Marine Engineering and Technology*, in 2011, and the Best Paper Award from the IEEE International Conference on Computing Electronics and Communications Engineering (iCCECE), Essex, U.K., in 2018. He is regularly invited as a Keynote Speaker and advises various governments on energy and transport-related issues. In 2019, he also became the Director of the U.K. EPSRC Doctoral Training Centre in Power Electronics for Sustainable Electric Propulsion. He is the active Editor-in-Chief of *IET Power Electronics* journal.

MOHAMMED A. ELGENDY received the B.Sc. degree from Menoufia University, Menoufia, Egypt, in 1997, the M.Sc. degree from Ain Shams University, Cairo, Egypt, in 2003, and the Ph.D. degree from Newcastle University, Newcastle upon Tyne, U.K., in 2010, all in electrical engineering. From 1998 to 2006, he was a Research Assistant with the New and Renewable Energy Department, Desert Research Centre, Cairo. From 2011 to 2014, he was a Research Associate with the Electrical Power Research Group, Newcastle University, where he currently holds the position of a Lecturer. His research focus is on the design and control of power electronic converters for drives and renewable generation schemes.