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A Health Indicator for Interconnect structure of QFP Package Under Vibration and Steady Temperature

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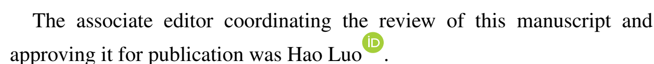
ABSTRACT Interconnect structure, as the weak point of reliability, is often the critical part in electronic devices during their service. In order to monitor the health state and degradation of interconnect structure, the charging time is used as the health indicator for interconnect structure of QFP package in this paper. Firstly, a monitoring circuit, based on the proposed electrical model of interconnect structure, is designed to measure the charging time in real time. Secondly, the equivalent circuit of the monitoring circuit is derived and the effect of the parameters of the monitoring circuit on the charging time is analyzed. Then, experiments under vibration and steady temperature are conducted to analyze the failure of interconnect structure and derive the damage model. Finally, the effect of charging time as the health indicator to monitor the damage of interconnection structures is analyzed and the uncertainty is discussed. Results show that the charging time is directly related to the interconnect damage and can well characterize the interconnect failure, which can be used as a health indicator to assess the damage and predict the failure of interconnect structure.

INDEX TERMS Health indicator, interconnect structure, damage, vibration, charging time.

I. INTRODUCTION

With the development of technology, electronic equipment has been widely used in the complex system, like aircraft or ships, which may assume important functions and tasks [1]. It has been a hot and difficult topic to evaluate the health and reliability of electronic equipment in service, especially for electronic equipment in critical system. Health refers to the extent of degradation or deviation from normal conditions [2], based on which the Remaining Useful Life (RUL) can be estimated. Prognostics, as the main content of prognostics and health management (PHM), involves real-time monitoring of health indicators such as current, voltage and strain of electronic devices, based on which the damage of those devices can be estimated and their RULs can be calculated.

Prognostics has been used in electronics in three formats. The first are fuses and canaries. Chauhan et al used canaries to predict the solder interconnect failure of resistance by adjusting the printed circuit board pad dimensions and the solder interconnect area [3]. It can be a feasible method for some small devices like resistance or capacitance, to indicate failures by designing canaries. However, it may be difficult and impractical to predict failures of bigger devices like CPU. The second is monitoring and reasoning the failure precursors. Chauhan et al have used temperature rise to assess the degradation in varistor solder interconnects due to thermal fatigue damage [4]. Whereas Cai et al used the junction temperature of LEDs to predict the lifetime of luminaires [5]. Ji et al used the on-state voltage drop as an indicator to monitoring the wire-bond-related failure in the insulated-gate bipolar transistor (IGBT) [6]. It is a difficulty for this method to find the failure precursors of devices. The last one is monitoring environmental and usage profiles for damage modeling. Some researchers have used environment loadings such as temperature, humidity, and vibration to assess the reliability of products [7]–[10]. However, there could be a great uncertainty to assess reliability by monitoring environmental loadings and usage profiles, and its result may be very inaccurate due to the difference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between the monitoring environmental loadings and the actual environmental loadings suffered by devices.

Surface mount devices like chips and resistance, as the important electronic components, have received much focus to research its reliability. For some complex devices like integrated circuits and FPGA, it is impractical to design canaries due to its relatively large size and high cost, and there may be large prediction error by monitoring environmental and usage profiles due to their complex structure. Therefore, it has been increased interest in finding health indicators of complex devices [11]–[14].

The failure of interconnect between electronic device and the printed circuit board, which provides the mechanical fixing and electrical interconnection, has a significant impact on the reliability of electronic equipment. Many researches have focus on the failure and failure characterization of interconnect structure. There are two main ways to investigate failure indicators for the interconnect. One way is to extract physical signals like strain and stress. Yang et al have used the strain and stress of solder joints for electronic packaging to predict RUL under vibration and temperature cycling [15]. This method needs to monitor the strain and stress of solder joints, which is difficult during the operation of electronic package. Tang *et al.* [16] have attached the strain gauges on the PCB near or rear to the key solder joints of the chip to measure the strain of PCB in order to predict the fatigue life of BGA solder joints. There are too many interference factors in this method, resulting in the prediction results are not stable. Full field strain on the PCB has been extracted by Lall et al using high speed cameras, to evaluate the solder joints reliability [17]. However, the requirements for strain measurement are high, and the characterization results are closely related to the strain position and sensor accuracy. The other methods are using electrical signals such as current and voltage. Liu *et al.* [18] have measured the voltage change of solder joints to predict failure, by connecting solder joints of special BGA package in series to form two daisy-chain loops. But this method is not practical when electronic devices work. Additionally, some researchers have used FPGA's function to monitor the health of solder joints in real-time [19], [20], by designed specific monitoring circuit.

However, there are few researches on the health monitoring of Plastic Quad Flat Package (QFP) interconnect, which is widely used in electronic equipment. As the main component of electronic equipment, QFP package device's health states has great influence on the function and reliability of electronic equipment. Studies show that interconnect failure is one of the most causes of QFP package failure in electronic equipment, which is mainly induced by temperature and vibration loading [21]–[23]. In this paper, a study is conducted to find the indicator that can represent the health state and degradation of the interconnect structure in QFP package under vibration and steady temperature.

In the previous study [21], the electrical model of QFP interconnect structure has been modeled. But the failure characterization and damage derivation have not been investigated thoroughly, which will be studied depth in this article. The interconnect structure of QFP package in this paper includes lead, solder and pad, as defined in the literature [21]. In order to investigate the failure characterization and damage derivation of QFP package interconnect, a systematic study is conducted in this paper, by designing the monitoring circuit, conducting the degradation test under random vibration and steady temperature, analyzing the results and deriving the damage of interconnect structure.

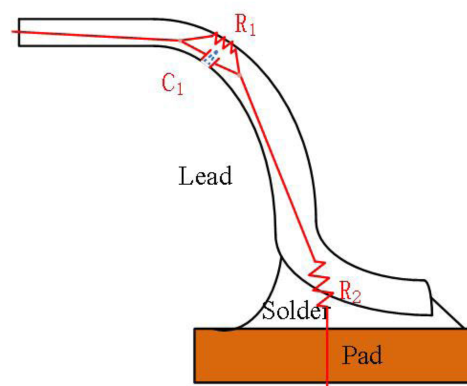


FIGURE 1. Single crack electrical model of interconnect structure.

The remainder of this paper is organized as follows. Section II introduces the electrical model and the monitoring circuit of interconnect structure. Section III is the analysis of failure characterization by analyzing test results and the monitoring indicator. Section IV is damage derivation and verification. Section V concludes this paper.

II. MONITORING SCHEME OF INTERCONNECT STRUCTURE

A. ELECTRICAL MODEL OF INTERCONNECT STRUCTURE

The Electrical model of QFP interconnect structure has been established in an earlier work [21], in which the crack is equivalent to the parallel connection of capacitance and resistance, as shown in Fig. 1 is the electrical model of a single crack. In the process of crack propagation, there are three stages. In the first stage, there is no crack initiation, and an interconnect structure is equivalent to a resistance. At the stage of crack initiation and propagation, the interconnect structure is equivalent to the parallel of a capacitance and resistance. When a penetrative crack is formed, the interconnect structure is equivalent to a capacitance.

B. MONITORING CIRCUIT OF INTERCONNECT STRUCTURE

In order to monitor the health status of interconnect structure at work, a monitoring capacitor is added at the back end, as shown in Fig. 2. Each monitoring unit is composed of two interconnect structures, one is monitored interconnect structure (interconnect structure 1) and the other is feedback interconnect structure (interconnect structure 2). Fig. 3 shows the equivalent monitoring circuit of interconnect structures.

Where R_3 is the equivalent resistance of the wire between the lead and the monitoring capacitor. Based on the equivalent

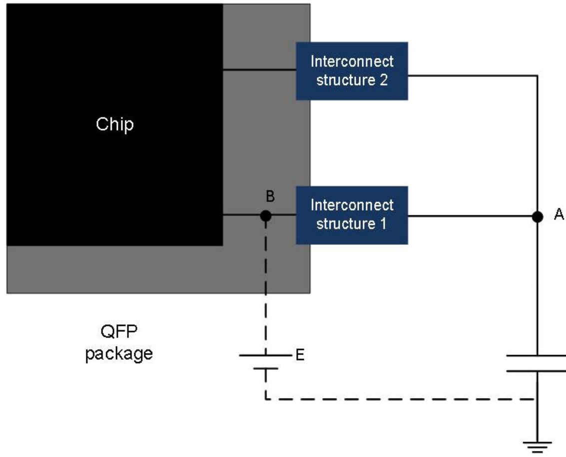


FIGURE 2. Monitoring circuit.

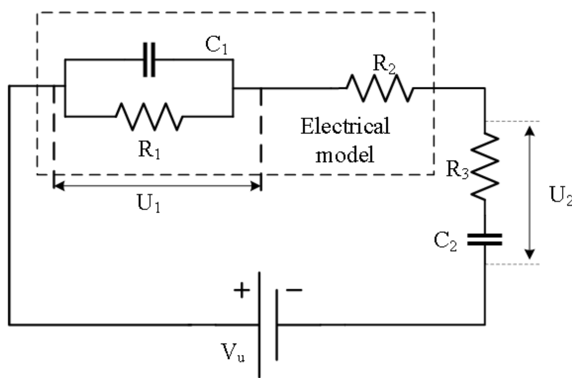


FIGURE 3. The equivalent monitoring circuit.

monitoring circuit, voltage U_2 at the back end of the lead (point A in Fig. 3) is deduced to be:

$$U_2 = \frac{R_1R_3C_1C_2s^2+(R_1C_1+R_3C_2)s+1}{R_1(R_2+R_3)C_1C_2s^2+[R_1C_2+R_1C_1+(R_2+R_3)C_2]s+1} \cdot V_u = \frac{c_2s^2+c_1s+c_0}{s^2+a_1s+a_0} \cdot V_u \quad (1)$$

Here

$$\begin{aligned} c_2 &= R_3/(R_2+R_3) \\ c_1 &= (R_1C_1+R_3C_2)/R_1(R_2+R_3)C_1C_2 \\ a_0 &= c_0 = 1/R_1(R_2+R_3)C_1C_2 \\ a_1 &= [R_1C_2+R_1C_1+(R_2+R_3)C_2]/R_1(R_2+R_3)C_1C_2 \quad (2) \end{aligned}$$

Then, the charging time could be measured by controlling the voltage at the front of the monitored interconnect structure periodicity (point B in Fig. 2). The procedure of measuring the charging time is showed in Table 1. Where, the initialization of the chip mainly includes pins setting, clock setting and serial port setting. The monitored interconnect structure is set to output, whereas the feedback interconnect structure is set to input. During the measurement of charging time, the monitored interconnect structure first outputs high potential and starts the timer. Due to the presence of the monitoring capacitor, the potential at point A will increase gradually.

TABLE 1. The procedure of measuring the charging time.

Procedure: Measurement of the charging time
Step 1: Initialization of the chip
Step 2: Monitored interconnect structure (interconnect structure 1) output high potential and start timer
Step 3: Feedback interconnect structure (interconnect structure 2) receives high potential trigger, and stop timer
Step 4: Monitored interconnect structure output low potential
Step 5: Get the time recorded by timer and send it through the serial port
Step 6: Repeat from step 2 to step 5

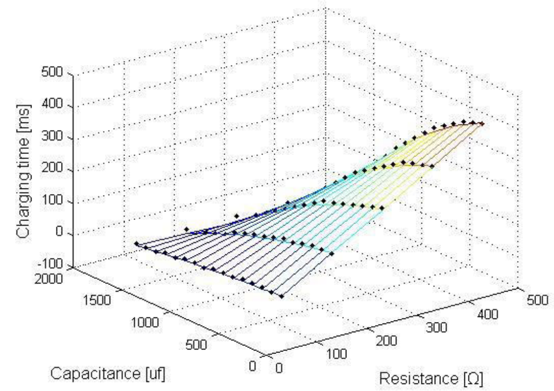


FIGURE 4. Charging time curve with R1 and C1.

The timer stops when the potential at point A reaches the high trigger potential of the feedback interconnect structure. Then, the monitored interconnect structure outputs low potential. The time recorded by timer is defined as the charging time, which is used as the health indicator for the monitored interconnect structure. The equivalent impedance of monitored interconnect structure will change with the crack propagation, resulting in the charging time change.

C. SIMULATION AND VERIFICATION OF MONITORING CIRCUIT

Since STM32F103VBT6 is used in the verification test, and its high potential trigger potential is $2V$, the charging time defined in this paper is the time required from $0V$ to $2V$. V_u is the working voltage of the chip, so $V_u = 3.3V$. Base on the Eq. (1) and (2), we get the change curve of charging time with the equivalent resistance R_1 and the equivalent capacitance C_1, when $C_2 = 1000uf$, which is shown in Fig. 4. It can be found that the charging time increases with the increase of the equivalent resistance R_1 and decreases with the increase of the equivalent capacitance C_1. Due to the different initial values of resistance R_1, R_2 and capacitance C_1, different initial values of charging time will appear. Fig. 5 shows that the charging time decreases with the increase of equivalent resistance R_3 under different initial charging time, and the charging time is zero when the equivalent resistance R_3 exceeds a certain value.

A verification test is conducted by connecting a variable resistor in series at the back of the monitored interconnect structure, which simulates the resistance change caused by

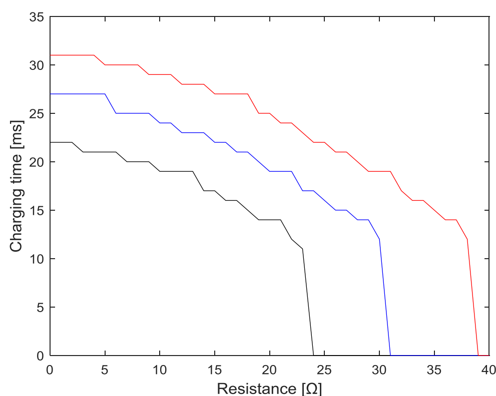


FIGURE 5. Charging time curve with R3.

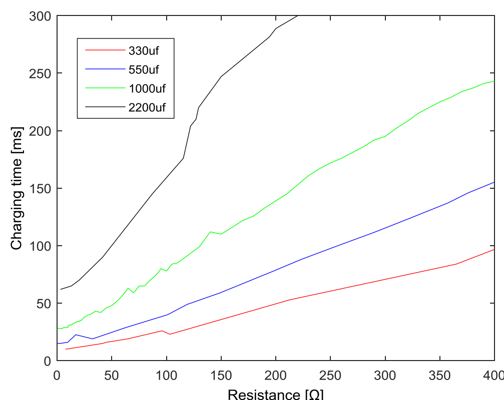


FIGURE 6. Relationship between the charging time and the equivalent resistance.

the crack propagation of the monitored interconnect structure. The evolution relationship between charging time and equivalent resistance of the monitored interconnect structure, with different monitoring capacitance ($330uf$, $550uf$, $1000uf$, and $2200uf$), is shown in the Fig. 6. The results show that there is a linear relationship between the charging time and the equivalent resistance, which is consistent with the simulation results. There is a blind area in the initial stage of resistance change, that is, the change of equivalent resistance of interconnection structure cannot be reflected by the change of charging time, and the smaller the monitoring capacitance is, the larger the blind area is, the smaller the initial charging time is, as shown in table 2 in detail. This phenomenon is mainly caused by two aspects. One is that the interconnect structure and conductor have initial resistance. According to the formula $\tau = RC$, the time constant increases with the increase of capacitance, so the initial charging time exists, and increases with the increase of the monitoring capacitance. The other one is that different monitoring capacitance results in different charging time change rates, i.e. different measurement accuracy. The larger the monitoring capacitance is, the higher the measurement accuracy will be, and the chip clock is fixed, so different blind resistance appears. In the next study, capacitor with capacitance of $1000uf$ is selected as the monitoring capacitor, because of its moderate initial resistance, small blind area, high measurement accuracy and proper volume.

TABLE 2. Blind resistance and charging time under different capacitance.

Capacitance (uf)	Initial charging time (ms)	Blind area (Ω)
330	10	25
550	15	15
1000	29	10
2200	62	8

FIGURE 7. The combined vibration-temperature tester.

FIGURE 8. The test specimen.

III. FAILURE ANALYSIS OF INTERCONNECT STRUCTURE

In this section, the experiment that specimens subjected to random vibration and steady temperature is conducted, with the charging time monitored, to study the charging time manifestation under different failure modes and analyze the failure characterization of interconnect structure.

A. EXPERIMENT SCHEME

The combined vibration-temperature tester is composed of DONGLING ES-6-230 shaker and temperature and humidity box THV402-5, which can provide the maximum acceleration of 1000 m/s^2 and temperature of − 65 to 150 °, as show in Fig. 7.

Fig. 8 shows the test specimen consisting of surface mounted QFP100 chip STM32F103VBT6 and other components like resistance and capacitance. Components on the test specimen are assembled with Sn-Pb solders on the printed circuit board (PCB). The test specimens are constructed of flame retardant (FR4) material with the size 180 × 90 × 1.6 mm. For each test specimen, the charging time of 16 pairs of interconnect structures is monitored

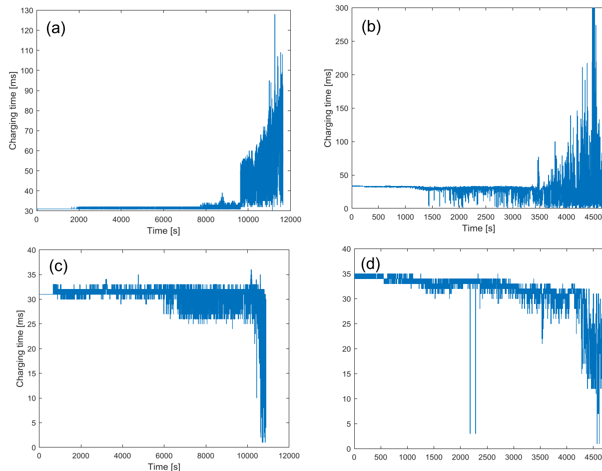


FIGURE 9. Four manifestation of charging time.

automatically in real-time, and its distribution was consistent with that in the literature [21].

Test specimens are subjected to a random vibration with bandwidth 280~320 Hz and power spectral density 0.8 g^2/Hz under temperature −25, 25 and 75°C, respectively. The test stopped when the test specimen fails to automatically transmit data to monitoring software.

B. FAILURE MODE CHARACTERIZATION ANALYSIS

After cutting, mounting, polishing and sectioning the failure test specimens, surfaces of specimens are observed under the scanning electron microscope. The observation results show that there are four failure modes and three places easy to crack for the interconnection structure [21]. Through the analysis of the charging time data under each failure mode, it is obvious that the manifestation of charging time shows certain rules, which can be explained by the electrical model established before.

In the experiment, there are four manifestations of charging time, as shown in Figure 9, while Figure 10 is the corresponding SEM. The first manifestation is shown in Fig. 9 (a). During the experiment, the charging time increases gradually with fluctuation, and its value is not less than the initial value. The second manifestation shows that the charging time increases gradually with fluctuation, but occasionally it is less than the initial value, as shown in the Fig. 9 (b). At the same time, Fig. 9 (c) is the third manifestation of charging time. Compared with the first two manifestations, the charging time mainly decreases gradually and occasionally exceeds the initial value. Whereas the fourth manifestation is similar to the third manifestation, except that it will not exceed the initial value, as shown in Fig. 9 (d).

For the first three manifestations, the results show cracks are found in interconnect structure, which may be any failure mode of interconnect structure. However, for the fourth manifestation, there is no crack in interconnect structure, which results from the fracture of the wire connecting the monitoring capacitor. This phenomenon also occurs in other specimens.

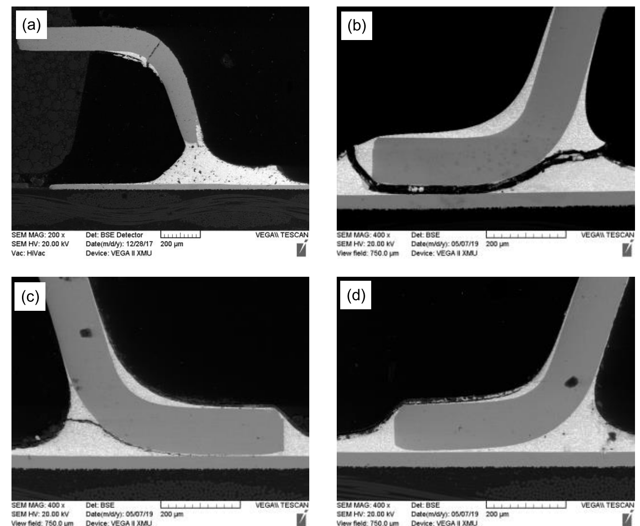


FIGURE 10. SEMs corresponding to Fig. 12.

The charging time may increase or decrease, how to explain this phenomenon is the focus of the next part. Based on the electrical model above, there are two reasons for the charging time decreasing, one is the equivalent capacitance C_1 increased, the other is the equivalent resistance R_3 increased. During the vibration process, when the crack closes, the gap between the two sides of the crack decreases, resulting in an increase in the equivalent capacitance and a decrease in the charging time. The fracture of the wire connecting the monitoring capacitor is equivalent to the increase of R_3 resistance, which would result in the decrease of the charging time. Whereas for the charging time increasing, only result from the equivalent resistance R_1 increase.

During the experiment, the charging time increase is the result of crack propagation, whereas the fluctuation is due to the change of effective length of crack in the vibration. For the first manifestation, the change of charging time is only related to the change of equivalent resistance R_1. The equivalent resistance R_1 increases with crack propagation, result in the charging time increasing. Whereas the effective length of crack changes randomly due to vibration, which makes the charging time to fluctuate. For the other three manifestations, the charging time is affected by the equivalent capacitance C_1 and the equivalent resistance R_3. C_1 or R_3 increases during test, resulting in the decrease of charging time. However, how the value C_1 or R_3 affects the change of charging time, and which is the main factor, will be analyzed in the next part.

IV. DAMAGE DERIVATION AND VERIFICATION

From the analysis above, we find that the increase of charging time is only related to crack propagation of interconnect structure. However, the decrease of charging time is related to the increase of equivalent capacitance C_1 or equivalent resistance R_3 referring to crack in the wire connecting the monitoring capacitor. In this part, we firstly deduce the relationship between cracks in interconnect structure and the charging time. Then, we discuss the effect of uncertainty

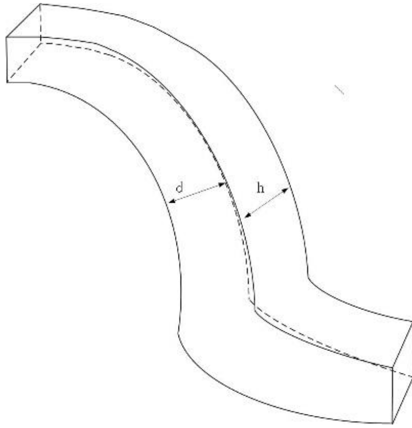


FIGURE 11. Lead size diagram.

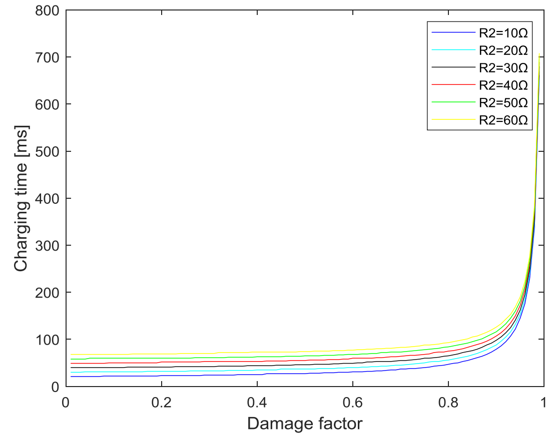


FIGURE 12. The curve of damage factor and charging time.

due to random vibration, and analyze the effect of equivalent capacitance C_1 and equivalent resistance R_3 on charging time.

A. MODELING AND FITTING

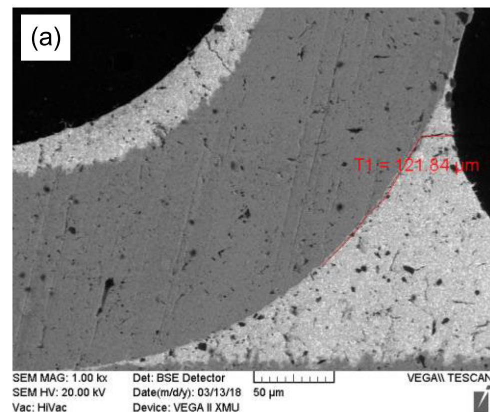
The general formula of resistance is $R = \rho L/A_R$. Where L is the length of the conductor, A_R is the cross-sectional area of the current passing through the conductor, and ρ is the conductivity of the conductive material. For the interconnection structure of QFP package, the cross-sectional area of current passing through can be equivalent to $A_R = h \cdot d \cdot (1 - D)$. Where d is the width of lead. h is the thickness of lead, and D is the ratio of crack length to crack propagation length, named damage factor. When the interconnection structure does no crack $D = 0$, the resistance value is small. When a penetrating crack occurs $D = 1$, the resistance value is infinite.

The expression of flat capacitor is:

$$C = \frac{\varepsilon A_c}{d_c} = \frac{\varepsilon_0 \varepsilon_r A_C}{d_c} \tag{3}$$

Among them, ε_0 is the vacuum dielectric constant $\varepsilon_0 = 8.85 \times 10^{-12} \, (F/m)$, ε_r is the relative dielectric constant of the material, and the air relative dielectric constant $\varepsilon_r = 1.000585$. $A_C = d \cdot h \cdot D$ is the area of the capacitor plate, and d_c is the distance between capacitor plates, equivalent to the average opening width of the cracks in the interconnection structure.

By measuring the size of interconnect structure and combining with the electrical model of interconnect structure, the curve between damage factor and charging time is fitted with different R_2 initial resistance values, as shown in Fig. 12, which shows a nonlinear relationship between the damage factor and the charging time. During the test, only the initial value and the real-time monitoring value of the charging time can be measured, so the fitting model between the damage and the initial value and the real-time monitoring value is established according to the simulation results. Fig. 12 shows that the non-linearity between the damage and charging time is obvious. In order to better deduce the relationship between damage and charging time, the curve is divided into two stages. And an optimization algorithm, the sequential quadratic programming (SQP) method, is used to determine the split point, with the minimum value of the R-square of two-stage fitting as the objective function. Result shows the split point is 0.8, so the first stage is $D \sim (0, 0.8]$ and the second stage is $D \sim (0.8, 1)$.



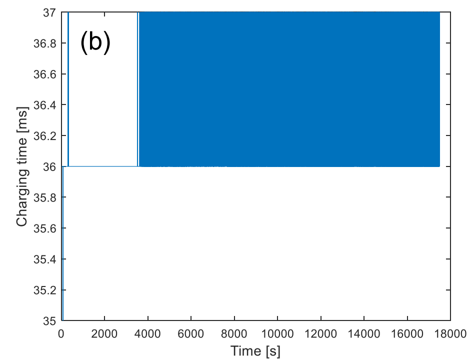


FIGURE 13. Failure mode 1 of interconnect structure.

When $D \sim (0, 0.8]$, by fitting with formula $T = \mathrm{a}^* \exp(-\mathrm{b}^* \mathrm{D}) + \mathrm{c}^* \mathrm{T}_0$, we can get,

$$\begin{aligned} \mathrm{a} &= 0.6746(0.6278, 0.7215) \\ \mathrm{b} &= -4.497(-4.586, -4.408) \\ \mathrm{c} &= 0.9983(0.9957, 1.001) \end{aligned} \tag{4}$$

The fitting R-square is 0.9986, which shows a good fitting effect. The values in parentheses indicate the 95% confidence interval for the estimated parameter.

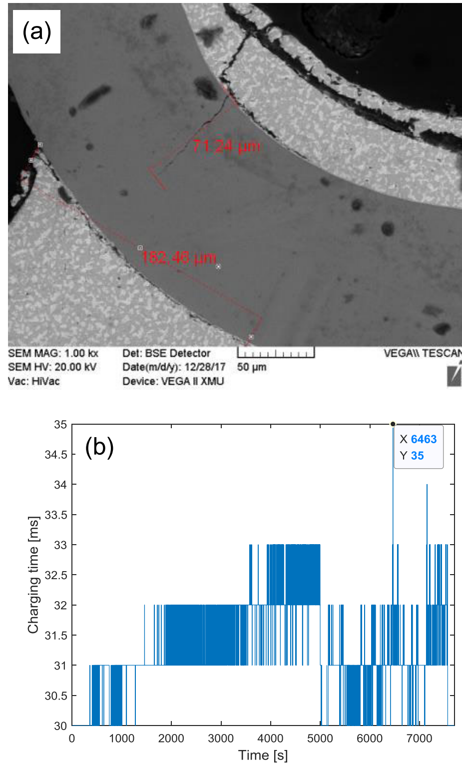


FIGURE 14. Mixed failure modes of interconnect structure.

When $D \sim (0.8, 1)$, it can also be obtained by fitting formula $T = \mathrm{a}^*\mathrm{D}^{\mathrm{b}} + \mathrm{c}^*\mathrm{T}_0$,

$$\begin{aligned} a &= 1013(952.2, 1073) \\ b &= 56.13(52.28, 59.99) \\ c &= 1.9(1.78, 2.02) \end{aligned} \tag{5}$$

The fitting R-square is 0.9706, which shows a good fitting effect.

Combining formula (4) and (5), the relationship between damage factor D and initial charging time T_0 and real-time monitoring charging value T is established, which is defined as *Dfun*:

$$Dfun = \begin{cases} Dfun1(T, T_0) & D \sim (0, 0.8] \\ Dfun2(T, T_0) & D \sim (0.8, 1) \end{cases} \tag{6}$$

*Dfun*1 and *Dfun*2 are defined in (0, 0.8] and (0.8, 1) for charging time T and T_0 to induce damage factor D, respectively.

B. DAMAGE MODEL VERIFICATION

In this part, SEM results and charging data of interconnect structure are analyzed to verify the damage model. It is known from measurement under SEM that the average width of three leads is 117um, while the average length of the interface between the solder and the lead is 669um.

Fig. 13-Fig. 16 show SEM results and their charging time of interconnect structure under random vibration in three stages of crack growth (short crack, long crack and penetrative crack). Fig. 13 shows short crack, Fig. 14 shows long crack, whereas Fig. 15 and Fig. 16 show penetrative cracks. Mixed failure modes appear in Fig. 14, where the length of crack for failure mode 1 and failure mode 3 are 182,46um and 71.24um respectively, whose corresponding damage factors are 0.27 and 0.6. Therefore, failure mode 3 is the main failure for this interconnect structure, and the damage factor is 0.6, according to the principle of competitive failure. Fig. 13, Fig. 15 and Fig. 16 present only one failure mode, namely mode 1, mode 4 and mode 3, with corresponding damage factors of 0.18, 1 and 1 respectively.

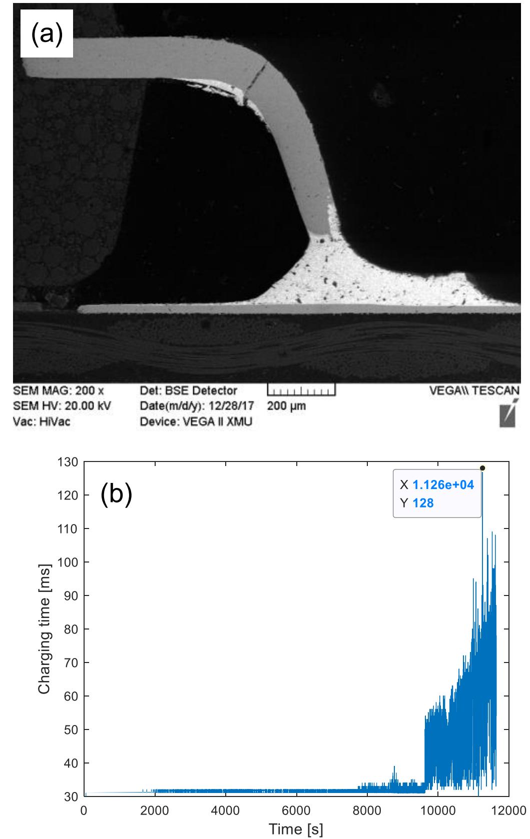


FIGURE 15. Failure mode 4 of interconnect structure.

According to the damage derivation formula (6), the damage can be calculated form initial charging time T_0 and real-time monitoring charging time T. In the process of crack propagation, the length of crack is monotonically increasing. However, the charging time does not always increase monotonously, due to the existence of vibration. So, the maximum of charging time is used to calculate the damage factor. Table 3 shows the comparison between the actual damage and the calculated damage under three temperatures. The error estimates for each specimen are listed, with a negative error for underestimation and a positive error for overestimation, all of which are below 0.15, and most below 0.05, indicating that charging time can be used as health indicator of interconnect structure in QFP electronic packaging. Additionally, it can be seen that the estimation error decreases with the crack growth.

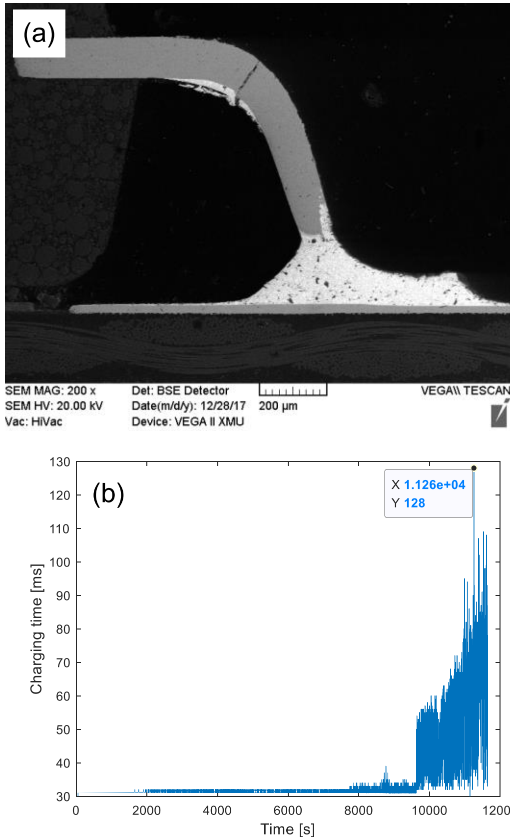


FIGURE 16. Failure mode 3 of interconnect structure.

TABLE 3. The calculated damage factors.

Temperature	Specimens	Calculated damage	Actual damage	Error
25℃	1	0.25	0.37	-0.12
	2	0.97	1	-0.03
	3	0.95	1	-0.05
	4	0.45	0.6	-0.15
-25℃	5	0.97	1	-0.03
	6	0.97	1	-0.03
	7	0.33	0.24	0.09
	8	0.25	0.18	0.07
75℃	9	0.94	0.9	0.04
	10	0.97	1	-0.03
	11	0.97	1	-0.03
	12	0.97	1	-0.03

C. UNCERTAINTY ANALYSIS AND DISCUSSION

The equivalent capacitance C_1 is decided by the distance between capacitor plates d_c, which changes in the vibration, resulting in the charging time change. Another factor affects the charging time is the damage factor. The effective crack length L_e (corresponding to effective damage factor D_e) may less than the actual crack length L_a (corresponding to actual damage factor D_a), due to the vibration. Assume $d_{ce} \sim U(0, d_{c0})$ and $L_e \sim U(0, L_a)$, then use Monte Carlo method to analyze the influence of vibration on charging time, where d_{c0} is the distance between equivalent capacitor plates without vibration, whereas d_{ce} is the effective distance under vibration.

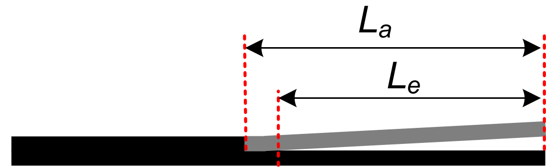


FIGURE 17. A crack length under random vibration.

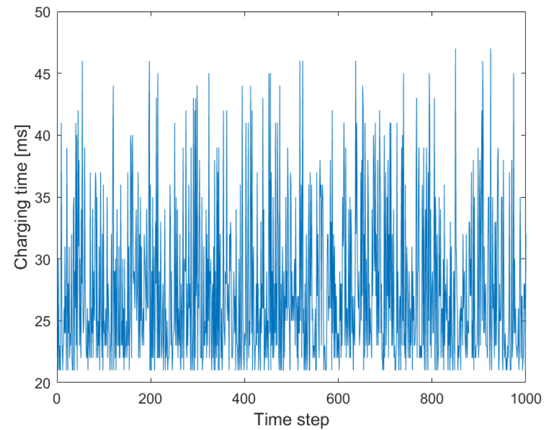


FIGURE 18. Simulation of charging time under random vibration when $D_e = 0.8$ without considering R_3 changes.

When $D_e = 0.8$, the change of charging time under random vibration is simulated without considering the effect of equivalent resistance R_3, shown in Fig. 18. If without vibration, the charging time would be 47 *us* when $D_e = 0.8$, with the initial value of charging time being 21 *us*. The simulation shows that the charging time would change randomly between 21 *us* and 47 *us*, due to the vibration. Fig. 19 shows the changes of equivalent capacitance C_1 under random vibration when $D_e = 0.8$, which shows the value of is only a few *pF* or *nF*. When considering the effect of equivalent resistance R_3, the charging time may less than the initial value due to random vibration, as shown in Fig. 20. Therefore, it is assumed that the equivalent capacitance C_1 is too small to affect the charging time, and the decrease of charging time is mainly result from the increase of R_3, which is due to the crack propagation in the wire connecting the monitoring capacitor.

Charging time is linearly related to equivalent resistance R_1, and effective crack length D_e is uniformly distributed, so charging time is uniformly distributed under random vibration, $T \sim U(T_l, T_u)$. Upper limit T_u of uniform distribution reflects the maximum equivalent resistance R_1, which corresponds to the actual damage factor D_a of interconnect structure. If there is no crack in the wire connecting the monitoring capacitor, T_l is the initial charging time, otherwise, T_l. corresponds to the effect of the actual damage in the wire connecting on charging time. Therefore, we could estimate T_u to calculate the actual damage factor of interconnect structure. Table 4 lists the estimate of T_u for twelve specimens under different temperatures at 95% confidence level. It is shown that the confidence interval of the method is very narrow

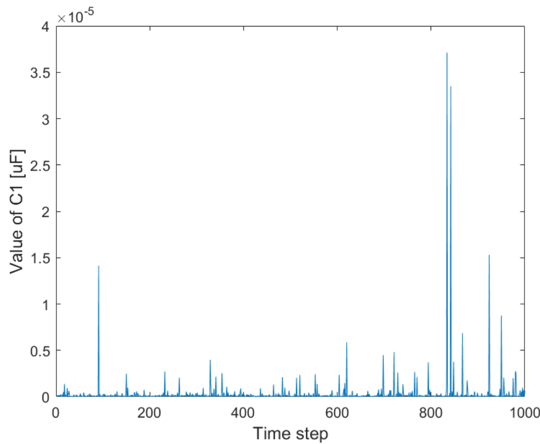


FIGURE 19. Simulation of equivalent capacitance C_1 under random vibration when $D_e = 0.8$.

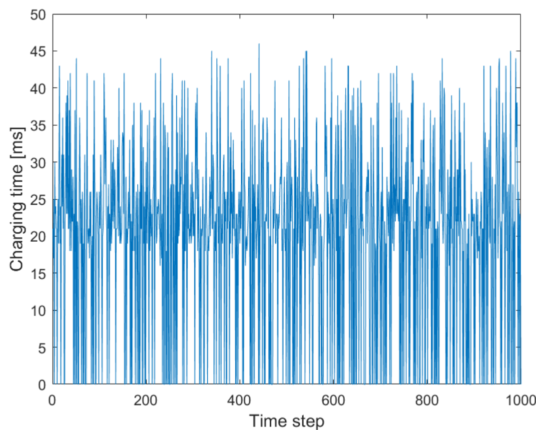


FIGURE 20. Simulation of charging time under random vibration when $D_e = 0.8$ considering R_3 changes.

TABLE 4. Estimate at 95% confidence level.

Tempe rature	Specimens	Estimated T_u (us)	Confidence interval (us)	Calculated damage
25℃	1	36	[36,36]	[0.25,0.25]
	2	296	[296, 297.11]	[0.97,0.97]
	3	128	[128,128.42]	[0.95,0.95]
	4	35	[35,35.01]	[0.45,0.45]
-25℃	5	300	[300,301.15]	[0.97,0.97]
	6	300	[300,301.23]	[0.97,0.97]
	7	40	[10,40.11]	[0.33,0.34]
	8	37	[37,37]	[0.25,0.25]
75℃	9	86	[86,86.27]	[0.94,0.94]
	10	300	[300,301.2]	[0.97,0.97]
	11	300	[300,301.28]	[0.97,0.97]
	12	300	[300,301.28]	[0.97,0.97]

and the damage interval is almost constant, which shows that the confidence of predicting damage by estimating the upper limit value T_u is high.

V. CONCLUSION

In this paper, the electrical model of QFP interconnect structure has been proposed for crack propagation, base on which, the monitoring circuit is designed, and the charging time is monitored as the health indicator of interconnect structure during the experiment. Moreover, combined with the SEM and the charging time, the failure characterization has been analyzed, and damage derivation of QFP interconnect structure has been studied under random vibration and steady temperature.

Results show that the charging time can be a health indicator for interconnect structure of QFP package in three aspects. Firstly, the charging time can indicate the failure of the interconnection structure. Secondly, the failure position, interconnect structure or the wire connecting the monitoring capacitor, can be inferred by the manifestation of charging time. Thirdly, the damage of interconnect structure can be estimated by the initial charging time and the upper limit value of current charging time, combined with the damage derivation model established in this paper. In addition, the charging time is monitored by the function of the QFP package chip itself, by adding an external capacitor for the monitored interconnect structure. Therefore, this method is feasible because of its low cost and easy implementation, which can be applied to engineering practice by monitoring the spare pins in the QFP package.

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REFERENCES

[1] K. Ni, Y. Liu, Z. Mei, T. Wu, Y. Hu, H. Wen, and Y. Wang, "Electrical and electronic technologies in more-electric aircraft: A review," *IEEE Access*, vol. 7, pp. 76145–76166, 2019.
[2] G. P. Pandian, D. Das, C. Li, E. Zio, and M. Pecht, "A critique of reliability prediction techniques for avionics applications," *Chin. J. Aeronaut.*, vol. 31, no. 1, pp. 10–20, Jan. 2018.
[3] P. Chauhan, S. Mathew, M. Osterman, and M. Pecht, "*In situ* interconnect failure prediction using canaries," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 3, pp. 826–832, Sep. 2014.
[4] P. Chauhan, M. Osterman, M. Pecht, and Q. Yu, "Use of temperature as a health monitoring tool for solder interconnect degradation in electronics," in *Proc. IEEE Prognostics Syst. Health Manage. Conf. (PHM- Beijing)*, Beijing, China, May 2012, pp. 1–4.
[5] M. Cai, Z. Liang, K.-M. Tian, M.-H. Yun, P. Zhang, D.-G. Yang, and G.-Q. Zhang, "Junction temperature prediction for LED luminaires based on a subsystem-separated thermal modeling method," *IEEE Access*, vol. 7, pp. 119755–119764, 2019.
[6] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "*In situ* diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.
[7] E. M. Benavides, "Reliability model for step-stress and variable-stress situations," *IEEE Trans. Rel.*, vol. 60, no. 1, pp. 219–233, Mar. 2011.
[8] H. Qingchuan, C. Wenhua, P. Jun, and Q. Ping, "Improved step stress accelerated life testing method for electronic product," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2773–2780, Nov. 2012.
[9] J. Lan, M. Yuan, H.-J. Yuan, and P. Lv, "Reliability assessment under real world environmental stress," in *Proc. 2nd Int. Conf. Rel. Syst. Eng. (ICRSE)*, Jul. 2017, pp. 1–5.
[10] Y. Chen, N. Tang, and Z. Yuan, "Prognostic and remaining life prediction of electronic device under vibration condition based on CPSD of MPI," *Shock Vibrat.*, vol. 2016, Nov. 2016, Art. no. 2650569.
[11] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 235–247, Jan. 2012.

[12] W. Lai, Y. Zhao, M. Chen, Y. Wang, X. Ding, S. Xu, and L. Pan, "Condition monitoring in a power module using on-state resistance and case temperature," *IEEE Access*, vol. 6, pp. 67108–67117, 2018.
[13] K. Wei, W. Wang, Z. Hu, and M. Du, "Condition monitoring of IGBT modules based on changes of thermal characteristics," *IEEE Access*, vol. 7, pp. 47525–47534, 2019.
[14] A. Bhatia, J. Hofmeister, J. Judkins, and D. Goodman, "Advanced testing and prognostics of ball grid array components with a stand-alone monitor IC," *IEEE Instrum. Meas. Mag.*, vol. 13, no. 4, pp. 42–47, Aug. 2010.
[15] P. Yang, D. Liu, Y. Zhao, Y. Tang, and H. Wang, "Approach on the life-prediction of solder joint for electronic packaging under combined loading," *IEEE Trans. Rel.*, vol. 62, no. 4, pp. 870–875, Dec. 2013.
[16] W. Tang, B. Jing, Y. Huang, and Z. Sheng, "Feature extraction for latent fault detection and failure modes classification of board-level package under vibration loadings," *Sci. China Technological Sci.*, vol. 58, no. 11, pp. 1905–1914, Nov. 2015.
[17] P. Lall, G. Limaye, J. Suhling, M. Murtuza, B. Palmer, and W. Cooper, "Reliability of lead-free SAC electronics under simultaneous exposure to high temperature and vibration," in *Proc. 13th Intersoc. Conf. Thermal Thermomech. Phenomena Electron. Syst.*, May 2012, pp. 753–761.
[18] C. Liu, J. Wang, A. Zhang, and H. Ding, "Research on the fault diagnosis technology of intermittent connection failure belonging to FPGA solder-joints in BGA package," *Optik*, vol. 125, no. 2, pp. 737–740, Jan. 2014.
[19] N. Wang, Y. Li, Z. Yu, and Z. Ren, "Online test method of FPGA solder joint resistance with low power consumption," *Microelectron. Rel.*, vol. 55, nos. 9–10, pp. 1867–1871, Aug. 2015.
[20] N. Wang, X. Ma, X. Xu, and Z. Rui, "A low power online test method for FPGA single solder joint resistance," *J. Electron. Test.*, vol. 33, no. 6, pp. 775–780, Dec. 2017.
[21] H. Jiaxing, J. Bo, S. Zengjin, L. Fang, C. Yaojun, and Z. Yulin, "Failure and failure characterization of QFP package interconnect structure under random vibration condition," *Microelectron. Rel.*, vol. 91, pp. 120–127, Dec. 2018.
[22] R. Tian, C. Hang, Y. Tian, and L. Zhao, "Growth behavior of intermetallic compounds and early formation of cracks in Sn-3Ag-0.5Cu solder joints under extreme temperature thermal shock," *Mater. Sci. Eng., A*, vol. 709, pp. 125–133, Jan. 2018.
[23] D. A. Shnawah, M. F. M. Sabri, and I. A. Badruddin, "A review on thermal cycling and drop impact reliability of SAC solder joint in portable electronic products," *Microelectron. Rel.*, vol. 52, no. 1, pp. 90–99, Jan. 2012.

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