IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received May 20, 2020, accepted June 29, 2020, date of publication July 3, 2020, date of current version July 16, 2020.
Digital Object Identifier 10.1109/ACCESS.2020.3006904

Real-Time Hardware-in-the-Loop Emulation of High-Speed Rail Power System With SiC-Based Energy Conversion

TIAN LIANG[1], (Graduate Student Member, IEEE), QIN LIU[1,2], (Graduate Student Member, IEEE), AND VENKATA R. DINAVAHI[1], (Fellow, IEEE)
[1]Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Alberta T6G 2V4, Canada
[2]School of Mechanical, Electronic and Control Engineering, Beijing Jiaotong University, Beijing 100044, China

Corresponding author: Qin Liu (qin9@ualberta.ca)

This work was supported by the Natural Science and Engineering Research Council of Canada (NSERC). The work of Qin Liu was supported by the China Scholarship Council (CSC).

ABSTRACT Real-time *device-level* hardware-in-the-loop (HIL) emulation of a complete high-speed rail system is challenging due to its complex modeling and high computing demand. With higher energy-efficient and switching frequency semiconductor material being found and adopted in the power electronic electrified traction application, there is a need to develop such new material based real-time device-level power electronic models in the modern and future traction system to estimate and verify the device switching transients, energy efficiency, and power quality improvement capability. This paper proposes a real-time SiC IGBT model based on the Wiener-Hammerstein configuration. A complete Beijing-Shanghai AC traction application is utilized as the study case, implemented on the hybrid multiprocessor system-on-chip (MPSoC) and field-programmable gate array (FPGA) platform, to verify both the system-level and device-level performance of the proposed model with comparisons to commercial software PSCAD/EMTDC and SaberRD. The dedicated hardware implementation enabled model execution at 10 *ns* for device-level transients and 10 μs for system-level transients.

INDEX TERMS Behavioral model, device-level, electro-thermal, field-programmable gate array (FPGA), hardware-in-the-loop (HIL), high-speed rail (HSR), insulated-gate bipolar transistor (IGBT), modular multi-level converter (MMC), real-time systems, silicon carbon (SiC), system-on-chip (SoC), wideband gap (WBG).

I. INTRODUCTION

High-speed rail (HSR) delivers fast, efficient, and reliable transportation in all weather conditions, fosters economic development in second-tier cities along train routes, links cities together into integrated regions that can then function as a single stronger economy, broadens labour markets and offers populace a wider network of employers to choose from [1], and has been specifically researched for stability and compensation [2]–[4], control [5], design optimization [6], and hardware-in-the-loop (HIL) application [7]. In the twentieth and the twenty-first century, HSR has achieved some noticeable achievements regarding test speed and operation scale. In 1903, Marienfelde–Zossen HSR line reached 200km/h for the first time and demonstrated the feasibility of the modern electrified HSR [8]. With tremendous advances of HSR field speed tests, research and development pushes the world's fastest train to the limit with a speed record of 603km/h on Japanese SCMaglev in 2015. Meanwhile, China has extended the HSR network to the operation scale of 25,000 km which is still growing rapidly today.

The future HSR system relies on high efficiency, operating temperature and switching frequency next-generation power semiconductor. The invention of the silicon (Si) power device inexorably paved the way for the modern HSR era. Silicon carbide (SiC) and gallium nitride (GaN), both wide

The associate editor coordinating the review of this manuscript and approving it for publication was Jenny Mahoney.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

bandgap (WBG) semiconductors, have emerged as the front-running solutions to make inroads into high power, high-temperature segments [9]. The SiC characteristic enables dramatic reductions in conduction loss by the improvement of low-impedance packaging technology and switching loss by the significant reduction of reverse recovery phenomenons, and prevents the flow of leakage current at high temperature by the higher breakdown voltage in nature [10]. Innovative SiC power module may lead the way of advanced HSR transportation for a low-carbon sustainable future. With the advantages mentioned above, there is a growing need to model the SiC power device in the existing HSR AC traction scenarios to test and evaluate the performance of the control and protection algorithm and circuits, and controller in a device-level non-destructive environment repeatedly. For this purpose, real-time HIL emulation of the HSR power system can be a promising answer in this application. To maximize the HIL emulator performance, both high sequential clocking and massive parallel compute devices have been utilized in previous works.

HIL application requires real-time capable models to fulfill the timing constraint. System-level power switch models, which neglect device-level transients, are applied in the commercial HIL application. In this work, a real-time device-level SiC model is developed with proper consideration and order-reduction to meet the real-time application requirement. Currently, SiC device-level models are available in three categories, starting from the simplest behavioural model to the most compute resource demanding numerical model: 1) Behavioral models [11]–[14], which simulate the device transients without considering the physical mechanism and require the least compute resource to conduct the modeling calculation; 2) Physics-based models [15]–[17]. These models solve the detailed nonlinear physics equations related to thermal and electrical issues; 3) Numerical models [18]–[20], which provide accurate device-level details using finite element simulation but become extremely computationally intensive; also, detailed device geometry information and material properties are necessary for this type of model. The nonlinear physics-based model requires multiple Newton iterations for convergence and it extends the execution time in the compute hardware, which makes this type of model difficult to be applied in the real-time device-level emulation. For material properties and geometry based numerical model, it is unrealistic to get access to the detailed manufacturer fabrication information for every power electronic device, not even mentioning the enormous complex calculation for its real-time application. Therefore, the behavioural model seems to be the only option to realize the real-time device-level SiC power electronic emulation. The electro-thermal behaviors usually change very slow compared to the electrical characteristics. Thus, in the implementation of electro-thermal model, the thermal counterpart can exchange its information with the electrical counterpart at the system-level time-step. In the literature, a wide range of methods devoted to thermal modelling can be found: 1) Lumped model, which links up the high-order nonlinear behavioral and analytical electrical model or utilizes transfer function to represent the physical heat flow transmit by measurement [21]–[28]; 2) Numerical modeling: finite difference [29], finite element [30], boundary element approaches [31], etc. were employed. In the proposed model, the electrothermal model based on the device datasheet (Foster model) is developed.

For simplification of the device-level behavioural model, Wiener-Hammerstein configuration, consists of two linear dynamic blocks in the front and the back with a sandwiched linear static block in the middle, is employed as the behavioural modeling tool for separating the static and dynamic characteristics in this work [32]. After generations of development in nonlinear system identification theory, the Wiener-Hammerstein-based models have been applied in various areas, such as system identification [33]–[35], hysteresis phenomena [36], [37], power electronics [38]–[39], and electrical drives [40]. Different from the Wiener-Hammerstein model, the configuration extends the linear time-invariant (LTI) nonlinear static block to linear or nonlinear time-variant static one, which is considered to have little impact on the model accuracy and execution efficiency.

This paper proposes real-time electrothermal behavioural models for the SiC hybrid IGBT module via the Wiener-Hammerstein configuration with the equivalent electrical component representation in the study case of Beijing-Shanghai HSR AC traction system based on the hybrid multiprocessor system-on-chip (MPSoC) and field-programmable gate array (FPGA) platform. The parameters of the Wiener-Hammerstein configuration model is extracted from the dedicated device datasheet from the manufacturer. The performance of the proposed real-time model is tested and validated with commercial software at both system-level and device-level. This paper is organized as follows. Section II describes the construction of the Wiener-Hammerstein configurations for SiC IGBT module. Section III explains the details of the Beijing-Shanghai HSR. Section IV shows the detailed hardware implementation on hybrid MPSoC-FPGA platform. Section V gives the real-time emulation results and validation. Section VI concludes the contribution of this paper.

II. OSCILLATION MECHANISM AND WIENER-HAMMERSTEIN CONFIGURATION MODELING OF SiC IGBT MODULE

This section introduces the oscillation mechanism of the SiC IGBT module and the detailed modeling method based on the Wiener-Hammerstein configuration which includes the carrier charge dynamic characteristics, operating static characteristics, and operating dynamic characteristics. The voltage reconstruction is explained in the last subsection. The device datasheet utilization is listed in Table 1 for the Wiener-Hammerstein configuration modeling procedure.

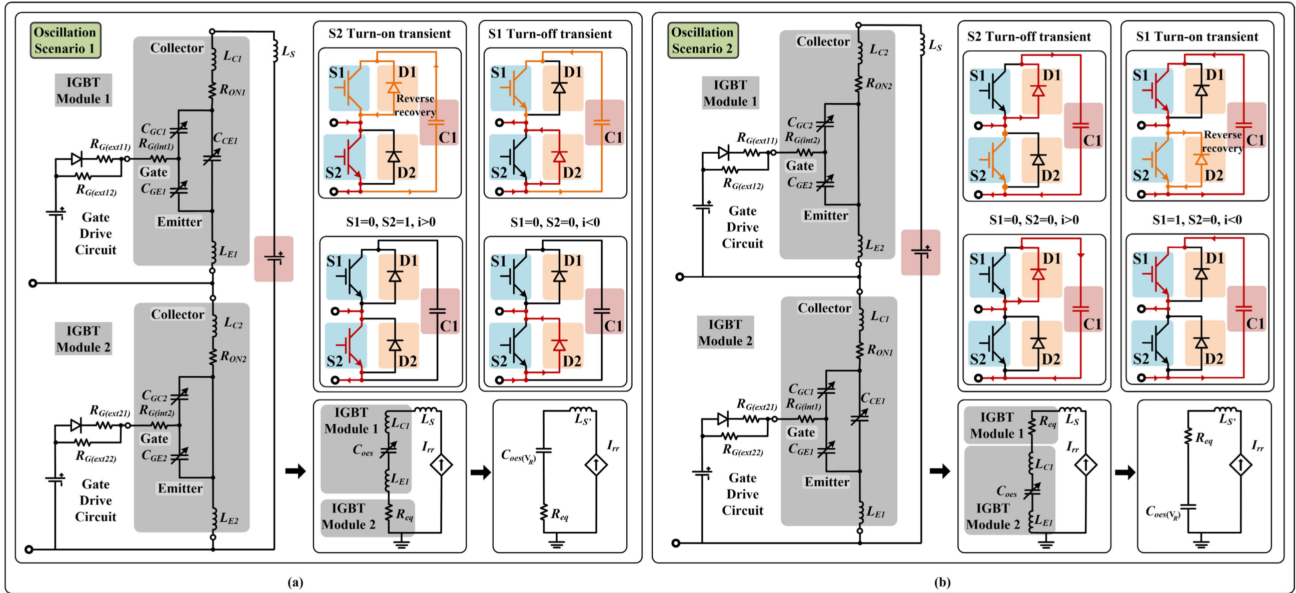

FIGURE 1. Oscillation mechanism of hybrid SiC IGBT module: (a) Oscillation Scenario 1. (b) Oscillation Scenario 2.

TABLE 1. Wiener-Hammerstein Configuration Modeling Procedure.

Dynamic carrier charge	Static electrical characteristic	Dynamic electrical characteristic	Power loss and thermal calculation
$t_{d,ON}$- I_C, $t_{d,OFF}$- I_C	I_C-V_{CE}, I_F-V_F	t_r- I_C, t_f- I_C, Q_c, R_{Gon}, R_{Goff}, L_s, L_{pCE}, C_{oes} - V_{CE}, C_{ies} - V_{CE}	E_{on}-I_C, E_{off}-I_C, E_{on}-R_G, E_{off}-R_G, Z_{thjc}^{IGBT}-t, Z_{thjc}^{Diode}-t

A. OSCILLATION MECHANISM OF SiC IGBT MODULE

Due to the advantage of the SiC material, it enables the lower resistance and capacitance in high power switching device, which introduces the oscillation problem during both turn-on and turn-off. The low resistance worsen the damping effect while the low capacitance increases the oscillation frequency compared to the Si-based switching device.

In Fig. 1 (a) (b), the scenario of positive and negative current inside the MMC submodule for the turn-on and turn-off can be observed. During the turn-on transient, the IGBT receives a current injection from both MMC submodule terminal and SiC diode reverse recovery current which creates an oscillation loop inside the submodule. The detailed oscillation loop of the MMC submodule can be seen in Fig. 1 (a) (b) with parasitic components where the diode symbol is considered as the ideal diode. The equivalent oscillation circuit is given in the subplot of each oscillation scenario and the parasitic parameters of the circuit in the oscillation Scenario 1 are given as:

$$\omega \approx \frac{1}{\sqrt{Ls' C_{oes}(V_R))}}, \quad Ls' = L_{C1} + L_{E1} + L_S + L_{C2}, \tag{1}$$

$$R_{Gon} = R_{Int} + R_{Ext(ON)} = 1.3\Omega, \tag{2}$$

$$C_{ies} = C_{GC2} + C_{GE2}, \quad X_G = R_{Gon} + \frac{1}{j\omega C_{ies}}, \tag{3}$$

$$R_{eq} = \left| \frac{X_G \cdot j\omega L_{E1}}{X_G + j\omega L_{E1}} + R_{ON2} \right| \approx 1.5\Omega. \tag{4}$$

where L_{C1}, L_{E1}, L_S are the IGBT module 1 collector and emitter parasitic inductance and circuit stray inductance, respectively. ω is the oscillation frequency. R_G, R_{Int}, $R_{Ext(ON)}$ and R_{ON2} are the total gate resistance, internal gate resistance, external turn-on gate resistance and turn-on static resistance, respectively. C_{GC2}, C_{GE2} are the IGBT module 2 gate-collector and gate-emitter capacitance, respectively. R_{eq} is the equivalent RLC oscillation circuit resistance. For oscillation Scenario 2, the calculations of the equivalent RLC components are similar.

B. CARRIER CHARGE STAGE

The carrier charge stage, shown in Fig. 2, is the prerequisite condition before the IGBT's turn-on and turn-off. The IGBT consists of three nonlinear capacitors C_{GC}, C_{GE}, and C_{CE}, between the three nodes: collector, gate, and emitter. When the gate signal of IGBT is on, C_{GE} and C_{GC} start charging with the nonlinear characteristic, which can be simplified to the equivalent first-order RC circuit. The resistance of the charge state is referred to as the internal and external gate resistor while the capacitor is the nonlinear node capacitor inside the IGBT module. The equivalent charging capacitor value is calculated by the turn-on and turn-off delay time T_d which equals to 2.2τ=$2.2R_{Geq}C_{eq}$. Thus, the C_{eq} value is obtained by the relation given as:

$$Ceq = \frac{T_d}{2.2R_{Geq}}, \tag{5}$$

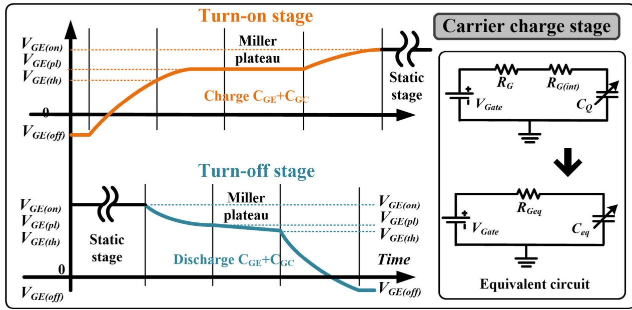

FIGURE 2. Carrier charge stage of SiC-IGBT.

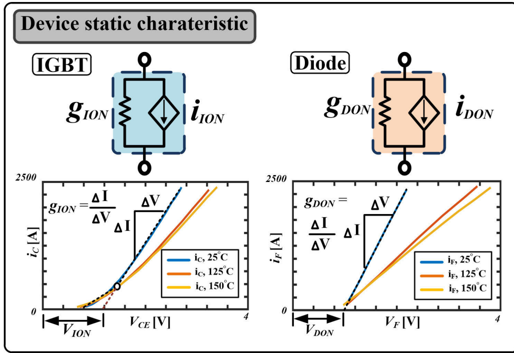

FIGURE 3. Static characteristic of SiC-IGBT.

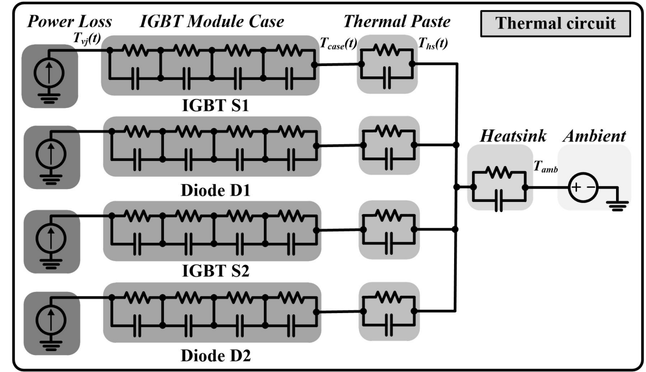

FIGURE 4. Thermal circuit of SiC-IGBT module.

TABLE 2. Thermal Impedances for CMH1200DC-34S Thermal Network.

Thermal impe.	Z_{thjc}				Z_{thch}	Z_{thha}
	i=1	i=2	i=3	i=4	i=5	i=6
$R^i_{th}[K/kw]$	0.0096	0.1893	0.4044	0.3967	16	10
$\tau^i_{th}[ms]$	0.1	5.8	60.2	351.2	3000	45000

C. STATIC CHARACTERISTIC

In Fig. 3, the static characteristics of IGBT and diode are shown with detailed component representation. IGBT and diode can be represented by a conductance g_{ION} and g_{DON} in parallel with a voltage controlled current source (VCCS). Both the conductance and the VCCS are temperature sensitive and change over time with the dedicated dynamic thermal circuit, shown in Fig. 4 and Table 2. v_{ION} and v_{DON} is the collector-emitter saturation voltage and diode forward voltage, respectively. i_{ION} and i_{DON} are the Nodal representation of v_{ION} and v_{DON} in the static characteristics. In static operating condition, the capacitive characteristic inside the SiC-based diode is negligible with the reduction of the corresponding component representation. The temperature sensitive relation of the nodal representations are given as:

$$g_{ON}(T_{vj}) = \frac{T_{vj}-T_{low}}{T_{low}-T_{high}}(g_{ON}^{T_{low}} - g_{ON}^{T_{high}}) + g_{ON}^{T_{low}}, \quad (6)$$

$$v_{ON}(T_{vj}) = \frac{T_{vj}-T_{low}}{T_{low}-T_{high}}(v_{ON}^{T_{low}} - v_{ON}^{T_{high}}) + v_{ON}^{T_{low}}, \quad (7)$$

$$i_{ON}(T_{vj}) = v_{ON}(T_{vj}) \cdot g_{ON}(T_{vj}). \quad (8)$$

where T_{vj}, T_{low} and T_{high} are the junction temperature, datasheet low experimental temperature, and the datasheet high experimental temperature, respectively.

D. DYNAMIC CHARACTERISTIC

In Fig. 5, the dynamic characteristics of the hybrid IGBT module are shown with three stages in turn-on transients in Fig. 5 (a) and two stages in turn-off transients in Fig. 5 (b).

In the turn-on Stage 1, the IGBT module employs a first-order approximation in the calculation. The VCCS of IGBT is set to zero while its conductance utilized the first-order approximation which is calculated by the turn-on rise time. Stage 2 of turn-on uses the triangle shape to calculate the peak value of the reverse recovery current where the period time is obtained from the oscillation frequency and the capacitor charge value is from the device datasheet. The transient current of Stage 3 is calculated by the equivalent RLC circuit.

In the turn-off Stage 1, the IGBT module employs both a first-order approximation and the linearly decrease calculation. The conductance of IGBT is set to zero while its VCCS utilized the first-order approximation which is calculated by the turn-off rise time. But the stage 1 is approximated by the two cross points of linearly decrease curve and first-order approximation curve. After the cross point of linearly decrease curve and the first-order approximation curve, the transient current waveform utilized the combination of first-order approximation curve and oscillation circuit result in stage 2 of turn-off. The oscillation initial current is set to the previous cross point value. In the static state, the dynamic characteristics are neglected and blocked. And the whole IGBT module is set to the form of Fig. 5 (c).

During the turn-on or turn off transient, it is assumed that the RLC sub-circuit loop introduces the oscillation waveform. The RLC circuits equations are given as:

$$u_C + u_R + u_L = 0, \quad (9)$$

$$u_R = Ri_L, \quad u_L = L\frac{di_L}{dt}, \ u_C = \frac{Q}{C}, \ i_L = \frac{dQ}{dt}, \quad (10)$$

$$LCp^2+RCp+1 = 0, \quad p = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}. \quad (11)$$

where u_R, u_L, and u_C are the transient voltage of the RLC components. R, L, and C are the resistive, inductive, and capacitive component of RLC circuit, respectively. The accurate representation of RLC transient current with the initial

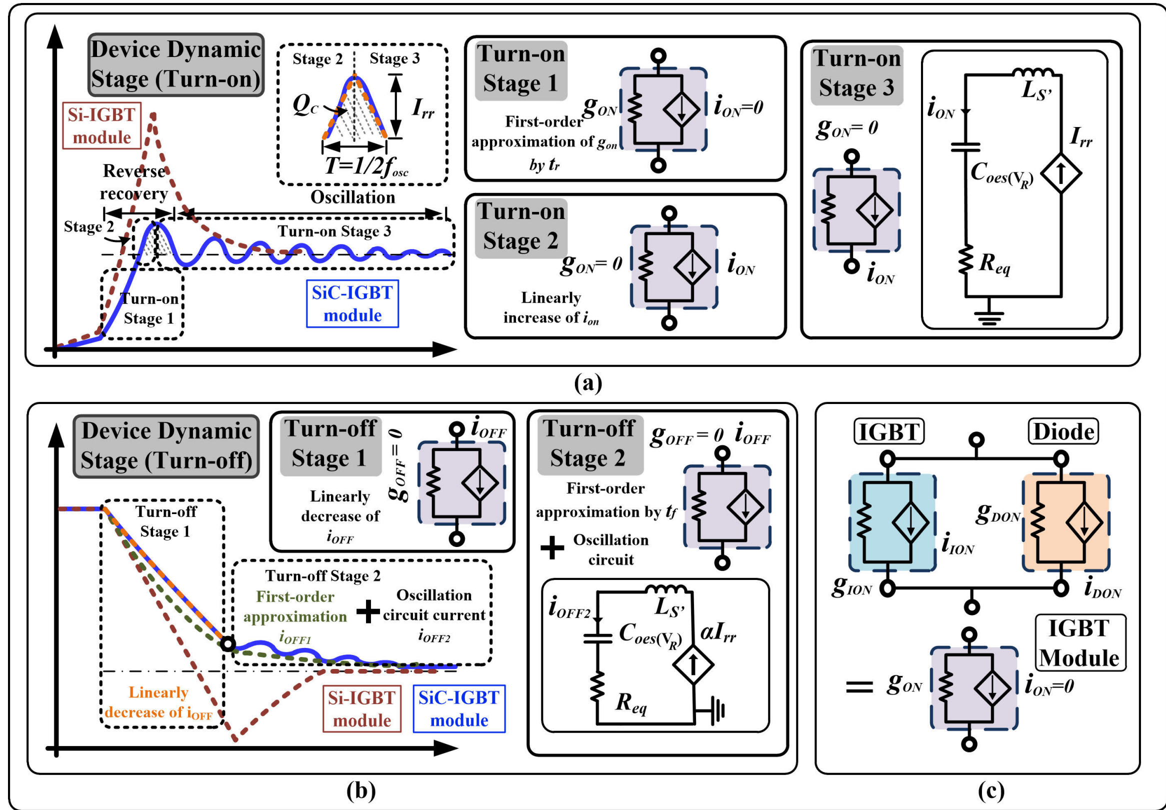

FIGURE 5. Dynamic characteristics of Si and SiC IGBT modules for: (a) turn-on, (b) turn-off, (c) hybrid IGBT module Norton circuit representation.

current injection at the peak is given as:

$$i = I_0 e^{-\delta t} cos\left(\omega t\right), \quad I_0 = I_{rr} = 4Q_{rr}f_{osc}, \ \delta = \frac{R}{2L} \tag{12}$$

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \approx \sqrt{\frac{1}{LC}}, \quad R \ll 2\sqrt{\frac{L}{C}}. \tag{13}$$

where i is the transient current of the RLC circuit; I_0 is the initial current for the inductor current which is actually the reverse recovery current peak value I_{rr}; Q_{rr} is the reverse recovery charge of the IGBT module; f_{osc} is the oscillation frequency of the RLC circuit. The change of the conductance and accompanied current value of first-order approximation in the switching transient can be estimated, given as:

$$H(s) = \frac{1}{\tau S + 1}, \quad S = \frac{2}{\Delta t} \cdot \frac{1 - z^{-1}}{1 + z^{-1}}, \tag{14}$$

$$h(t) = \frac{\Delta t + \Delta t z^{-1}}{\Delta t + 2\tau + (\Delta t - 2\tau)\, z^{-1}}. \tag{15}$$

where the $H(s)$ is the transfer function of the first-order approximation. Bilinear transformation is utilized with the simulation timestep Δt. $h(t)$ is the time domain transfer function. τ can be calculated by utilized of the value of 90.03% for 0.105τ and 10.01% for 2.302τ, which is the definition value of the rise and fall time in the datasheet.

E. VOLTAGE RECONSTRUCTION

The transients turn-on and turn-off power loss of hybrid SiC IGBT module are shown in Fig. 6 under specific circumstance from the datasheet. From which, the transient voltage waveform can be obtained via the relationship of $V = P/I$. The current, voltage and the power loss waveform has been normalized to percentage level based on their maximum value. Both the turn-on and turn-off waveform consist of a linear or polynomial region and a mixed region of the first-order approximation and the oscillation. The turn-on and turn-off power loss are given as

$$\begin{aligned} P_{ON} &= \int_{t_1}^{t_2} (A_1 x + D_1) + \int_{t_2}^{t_3} (B_1 x^2 + E_1 x + F_1) \\ &\quad + \int_{t_3}^{\infty} ((C_1 x + G_1) e^{-\frac{x}{\tau_1}} cos(\omega x)), \end{aligned} \tag{16}$$

$$\begin{aligned} P_{OFF} &= \int_{0}^{t_4} (A_2 x + E_2) + \int_{t_4}^{t_5} (B_2 x + F_2) \\ &\quad + \int_{t_5}^{t_6} (C_2 e^{-\frac{x}{\tau_2}} + D_2 e^{-\frac{x}{\tau_3}} cos(\omega x) + G_2), \end{aligned} \tag{17}$$

where P_{ON} and P_{OFF} are the total power loss during the turn-on and turn-off transient, respectively. t_1 - t_6 indicate the start time of specific region; A_1, A_2, B_1, B_2, C_1, C_2, D_1, D_2, E_1, E_2, F_1, F_2, G_1, G_2 are the parameters for fitting; τ_1 - τ_3 are the parameters for the first-order approximation.

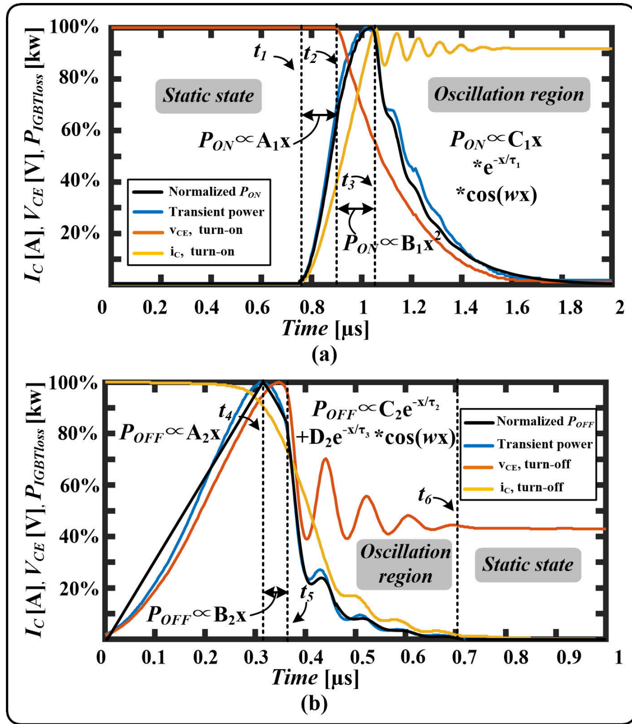

FIGURE 6. Voltage reconstruction of SiC-IGBT module for: (a) turn-on, (b) turn-off.

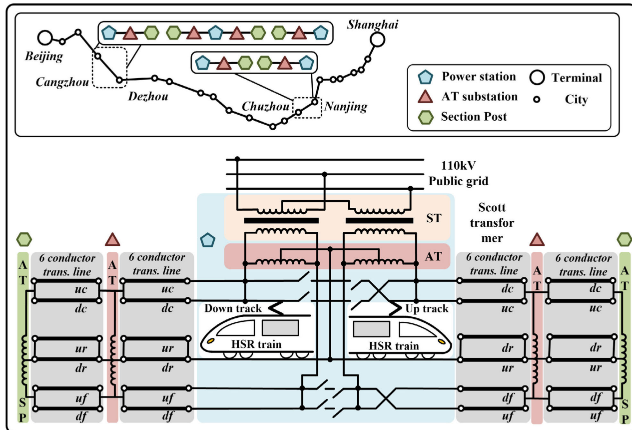

FIGURE 7. Complete topology of Beijing-Shanghai HSR network.

III. CASE STUDY: BEIJING-SHANGHAI HSR NETWORK

A. HSR PROTOTYPE

The 1318 km length Beijing-Shanghai HSR, which includes 27 power stations and 26 section posts, is selected as the study case in this work. A complete topology of the power station, AT substation, and section post is shown in Fig. 7 with up and down track. The connection among the section post, AT substation, and the power station employs the distributed travelling wave transmission line model.

B. DETAILED HSR TRAIN POWER SYSTEM

MMC-based motor drive system has been increasingly adopted in recent years [41], [42]. A complete SiC-based MMC train system is illustrated in Fig. 8. The train receives

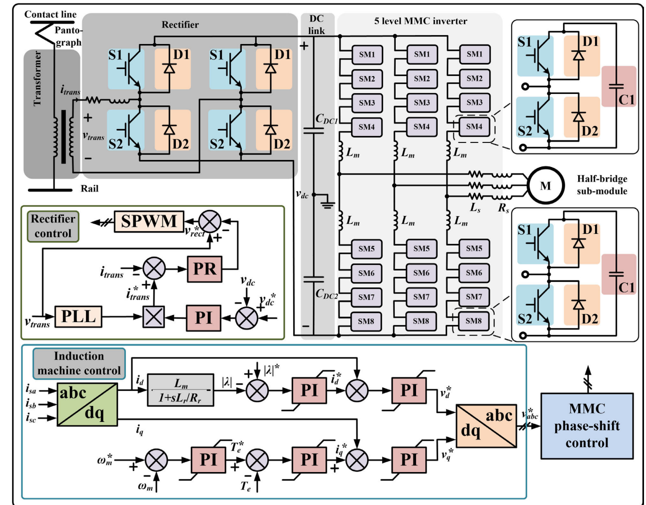

FIGURE 8. Detailed HSR traction system configuration.

the energy from the contact wire with the help of the pantograph system, and scales down the voltage from 27.5kV to 3kV by the single-phase transformer. Then, the rectifier converts the AC power to the DC connection of MMC-based induction machine drive system. The rectifier employs the proportional-resonant controller while the MMC-based induction machine is controlled by the outer induction machine drive control system.

IV. HARDWARE IMPLEMENTATION OF HSR SYSTEM

A. MPSoC-FPGA PLATFORM

Two VCU118 boards and one ZCU102 MPSoC board are utilized for HIL platform (Fig. 9) for the complete HSR system emulation. The Xilinx® ZCU102 development board features a Zynq UltraScale+ MPSoC device with a quad-core ARM® Cortex-A53, dual-core real-time Cortex-R5 on 16nm FinFET+ programmable logic fabric while the Xilinx® VCU118 board provides the highest performance and integration capabilities in a FinFET node with four times larger hardware programmable logic resource capacity of ZCU102. The ZCU102 utilizes the QSFP connectors with Aurora communication protocol to exchange data from board to board, which can achieve with 650*ns* latency in the implementation.

B. DETAILED SYSTEM DECOMPOSITION

A comprehensive HSR topology is implemented in the MPSoC-FPGA platform with both device-level and system-level model. The detailed device-level SiC MMC-based drive train model, with nanosecond-level transient waveform, is emulated in the ZCU102 MPSoC system along one complete section including a power station, AT substation, and section post (SP). The other two VCU118 FPGA boards emulate the system-level AC traction system. The MPSoC communicates with the two VCU118 FPGA boards for train distance information.

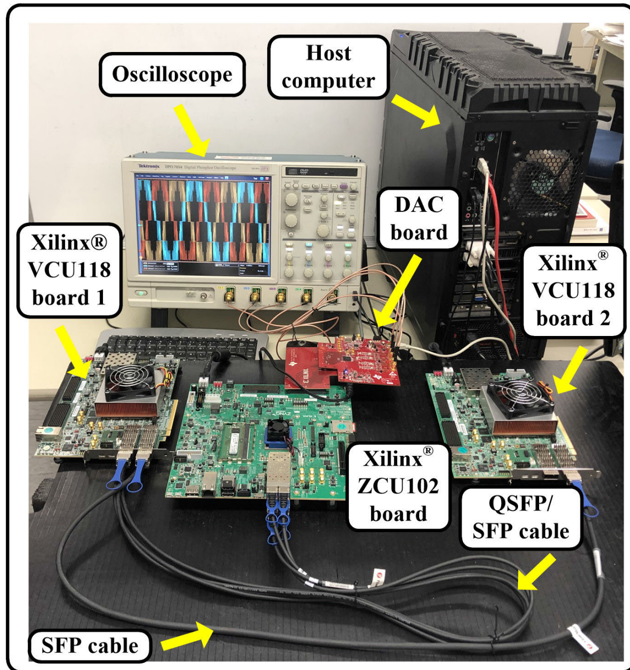

FIGURE 9. Hybrid hardware platform configuration of HSR system.

V. RESULTS AND DISCUSSIONS

Fig. 10 gives the SaberRD® offline (fixed line) and the real-time experimental results (black point) comparison under datasheet standard. Fig. 10 (a) shows the turn-on current waveform. In the static state, the submodule is operated at 100ns. After which, the first-order approximation is employed to execute the circuit emulation also at 100ns time-step wise. In the oscillation region, the equivalent RLC circuit utilized the pre-restored historical current in the circuit emulation which results in much faster emulation speed for the single-node circuit for 6ns per time-step. The prerequisite of applying the fixed pre-restored historical current is that I_C has little influence on the reverse recovery charge Q_{rr}. All device-level results are executed in the processing system's 1.3Ghz capable ARM® cores for real-time emulation in this case. In the case of I_C equals to 168*A*, only one first-order approximation circuit calculation (100*ns* per time-step) is needed while it requires the most RLC circuit emulation results of 62 points (6*ns* per time-step) in the emulation. Thus the total emulation time delay is 100*ns*+62*6*ns* =472*ns* while the its turn-on delay time is 500*ns*, which means the emulation is real-time capable. The time-delay for the case of I_C equals to 1206*A* is 2*100*ns*+43*6*ns* = 458*ns*. In Fig. 10 (b), the turn-off current waveform is divided into two parts: linearly decreasing region and mixed oscillation region. In the linearly decreasing region, the first-order approximation calculations are also emulated simultaneously. After the cross point of linearly decrease and the first-order approximation, the tail current waveform is combined by the oscillation circuit result and the first-order approximation. But in Fig. 10 (b), the α is fixed for all the current ratings which introduces higher error rate for the oscillation region under low current rating. In the final device tail current implementation, α has been adjusted to the cross point percentage value for better fitting result. Fig. 10 (c) (d) are the turn-off current and the reconstructed V_{CE} based on the previous normalized transient power loss waveform by utilizing the relationship of $V=P/I$.

Fig. 11 compares the proposed normalized power loss and the datasheet standard power loss. The errors are acceptable which shows the accuracy of the reconstructed switching voltage transient waveform. The device thermal calculation is not utilizing the normalized power loss value but the datasheet standard power loss value to ensure the accuracy of the device thermal behaviors.

Another thermal performance comparison is shown in Fig. 12 with Si-based IGBT module FD1000R171E4. The submodule is considered to be mounted on one heat sink and shares the same setup and gate signal from the SiC-based device. From the result, the temperature variation of the Si-based device shows higher fluctuation during the ten seconds, and ranges between 40 and 43°C which is nearly three times that of the range for the SiC-based device.

Fig. 13 (a) (b) give the IGBT S2 turn-on and turn-off transients, respectively. The front carrier charge linear dynamic block in the Wiener-Hammerstein configuration starts to operate when gate signal generated. Once charged to the threshold voltage, the front carrier charge linear dynamic block triggers the linearized static characteristic block and the back linear dynamic characteristic block. The linear static characteristic block computes its device conductance and VCCS value. The back linear dynamic characteristic block emulates the first-order delay transient. At the turn-on stage, the collector current shoots up with the oscillation phenomenon which is mainly introduced by the low capacitance and resistance by the diode D1. The lower capacitance introduces higher oscillation frequency while the lower resistance results for worse damping in the oscillation process. The ARM® core is only able to perform a 10*ns* time-step real-time device-level emulation and 6*ns* time-step for a 10*ns* time-step wise in the RLC oscillation waveform because the high-frequency oscillation requires smaller time-step to show the detailed transients. During the carrier charge stage, the IGBT module is not activated to be turned on, which can be utilized for calculating the turn-on transient. Thus, the real-time turn-on transients borrow time for 500*ns* time-step in the emulation process. In this case, the ARM® core executes the transient calculation under the 100*ns* time-step for static state or first-order approximation to emulate ten 100*ns* time-step points and RLC oscillation waveform for 10*ns* time-step wise. When the turn-off gate signal is generated, the front linear dynamic block calculates the capacitor discharge status. Once the gate-emitter capacitor discharge voltage drop to the turn-off threshold voltage, the linear static block and the back linear block are triggered and the static state and the tail current shape can be determined by first-order approximation and its RLC oscillation waveform. Fig. 13 (c) shows the device junction temperature within ten seconds. Temperature

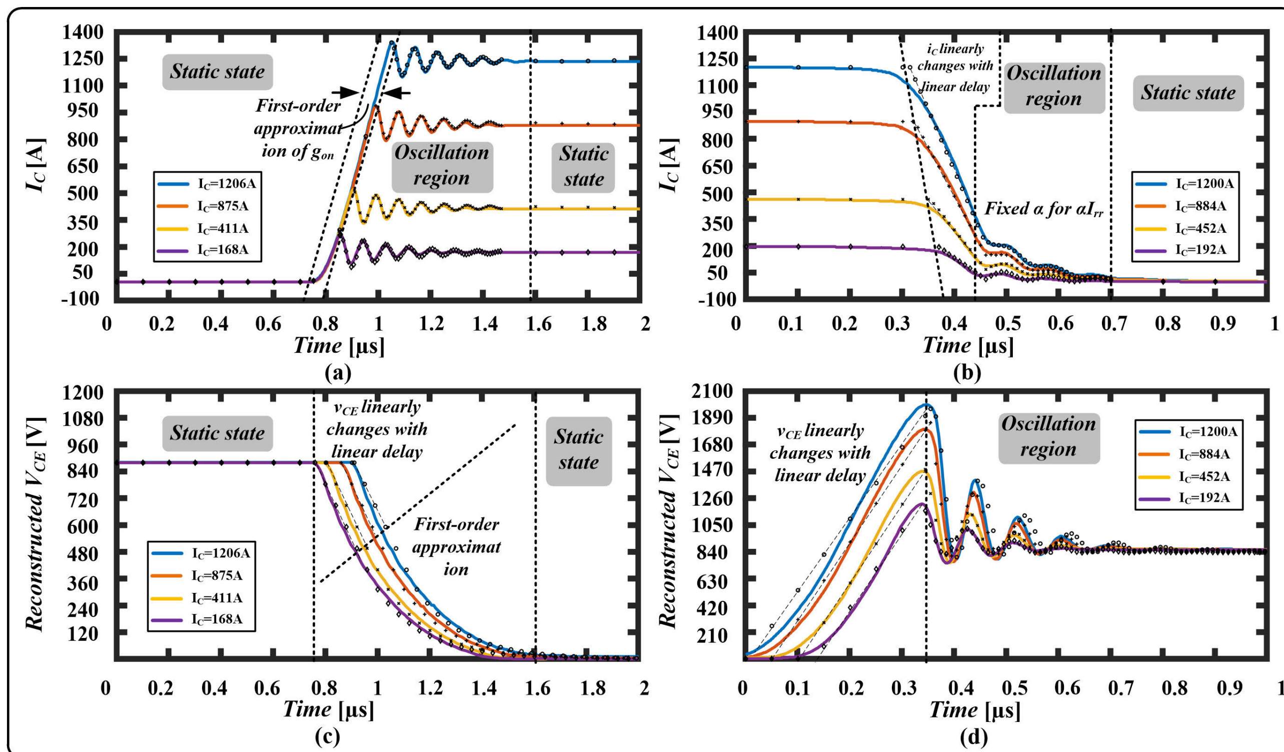

FIGURE 10. Device-level offline (SaberRD®) and real-time emulation results comparison under datasheet standard for: (a) turn-on current, (b) turn-off current, (c) reconstructed turn-on voltage, (d) reconstructed turn-off voltage.

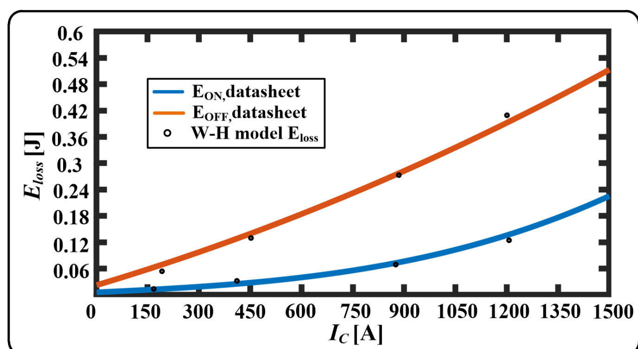

FIGURE 11. Comparison of normalized power loss and datasheet power loss.

cooldown can be observed during the time period with less power loss for each dedicated device. Due to SiC device advanced thermal feature, all the devices do not go beyond 41°C during stable operation.

Fig. 14 (a) (b) show the line voltage and line current, respectively. They are captured at the time when the train is cruising between the AT substation and power station. The voltage results include feeder-rail (FR) voltage on train and section post (SP) side, catenary-rail (CR) voltage on train and SP side. The voltage of the SP is slightly smaller than the one on the train side. The locomotive connects to the traction network by its catenary-pantograph system. The connected lines include catenary and its rail from both AT substation and power station or the source (S) side. From Fig. 14 (b), i_{R-S}, the current on the rail to the source, shares the equal

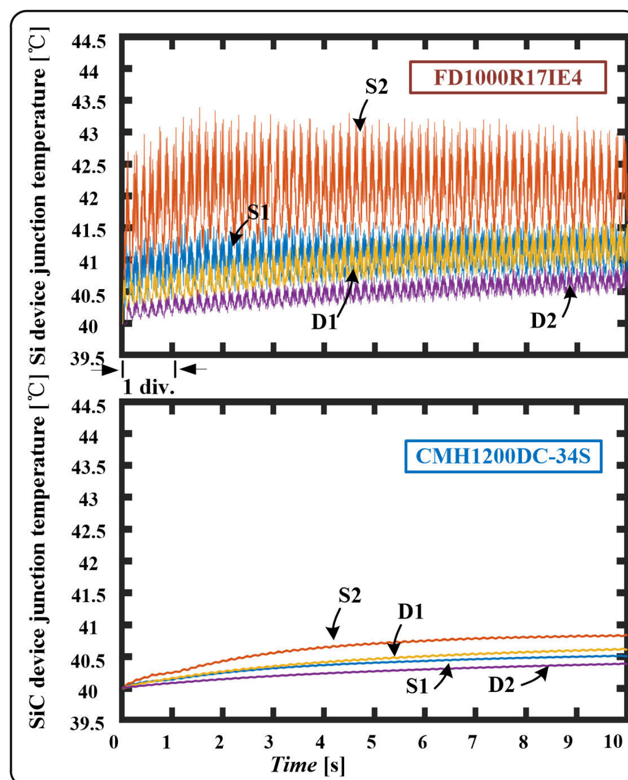

FIGURE 12. Thermal performance comparison between Si and SiC IGBT module.

quantity with the i_{R-AT} which is the current on the rail to the AT substation. The rectifier inside the locomotive converts

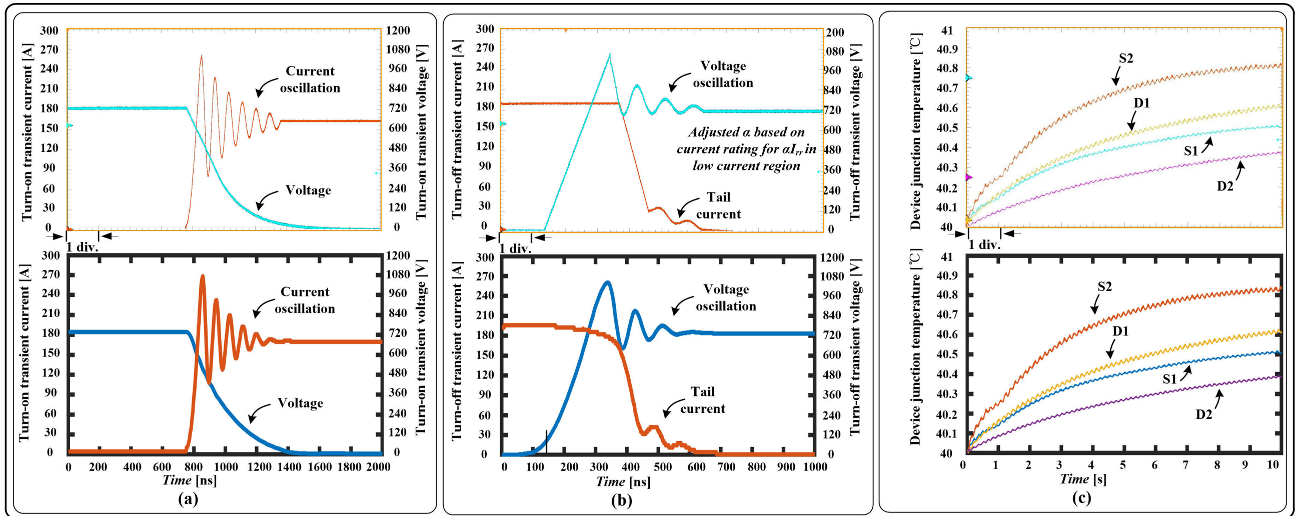

FIGURE 13. Device-level results for MMC submodule from real-time simulation (top oscilloscope sub-figure) and off-line simulation by SaberRD® software (bottom sub-figure) for: (a) turn-on transient current, (b) turn-off transient current, (c) device junction temperature. Scale: (a) x-axis: 200ns/div. (b) x-axis: 100ns/div. (c) x-axis: 1s/div.

TABLE 3. Traction network line voltage in dedicated position and its error (per 1000) comparison.

Train loc.	Position 1 Line vol. (error ‰)	Position 2 Line vol.	Position 3 Line vol. (error ‰)	Position 4 Line vol.	Position 5 Line vol. (error ‰)	Position 6 Line vol.	Position 7 Line vol. (error ‰)	Position 8 Line vol.	Position 9 Line vol. (error ‰)
1	27.4969 (0.37)	27.5001	27.5024 (0.28)	27.5038	27.5043 (0.07)	27.5051	27.5049 (0.14)	27.5037	27.5015 (0.12)
3	27.496 (0.39)	27.4369	27.3825 (3.29)	27.4145	27.4473 (1.67)	27.4491	27.4499 (1.59)	27.4498	27.4486 (1.43)
5	27.5 (0.12)	27.4734	27.4475 (1.68)	27.4223	27.3978 (2.97)	27.3999	27.4011 (2.83)	27.4013	27.4006 (2.57)
7	27.4992 (0.20)	27.4687	27.4385 (1.84)	27.4088	27.3795 (3.26)	27.3195	27.2642 (6.12)	27.2949	27.3264 (4.46)
9	27.4987 (0.20)	27.4697	27.4407 (1.69)	27.412	27.3835 (2.99)	27.3557	27.3286 (4.53)	27.3024	27.2769 (5.79)

the AC power from the traction network to DC link and gives the result in Fig. 14 (c). As seen in Fig. 14 (d) (e), MMC capacitance forming voltage and motor voltage are given with their FFT analysis in Fig. 14 (g) (h) which analyzes the high-frequency harmonic impact on the grid. Due to the large inductance inside the motor, the difference of MMC terminal and source voltage are not obvious for comparison. The most observable high-harmonic frequency is about 4000Hz and 8000Hz with the negligible amplitude to the 50Hz one. The high-frequency harmonic is introduced by the 2000Hz carrier wave in the control system. The capacitance voltages of the upper arm and lower arm of the MMC sub-module are shown in Fig. 14 (f) (i), respectively. $V_{cap,a}$ of the upper arm varies from 727 V and 742 V while $V_{cap,a}$ of the lower arm varies from 726 V and 741 V. The variation percentage of capacitance in the upper arm is 2.022% while the one in the lower arm is 2.024%.

As seen in Table 3, the location of the train results in the different voltage changes along the line which energized the train power system. Position 1, Position 5, Position 9 indicate the power station, AT substation, and SP, respectively. Position 3 and Position 7 are the middle point between the power station and the AT substation, and the middle point between the AT substation and the SP substation. Voltage drop can be observed at the location of the train and its voltage become the lowest along the line. The comparison of error (per thousand) with respect to PSCAD/EMTDC® simulation is also given in Table 3. The FPGA resource consumption for study case is illustrated in Table 4 and the highest percentage usage of resource is the LUT, with 90.92%, 67.47%, 88.55% on ZCU102, VCU118-1, and VCU118-2, respectively. In this work, it is considered that only one uptrack and one downtrack train are cursing inside the traction network that is energized by one power station. The device-level high-speed train communicates with first VCU118 to get the corresponding voltage and current information from the traction network.

The average errors are shown in Table 5 where the voltage average error rates are higher than the current ones. Because the front part of the normalized transient power waveform utilized linear approximation which is easier to be interpreted in terms of the linear delay. If higher order of polynomial approximation is employed, the error rate can be reduced to certain percentage but the delay part might be hard to implement and interpret. The average error of the device-level transient is less than 4.32% while the one at system-level is 0.217%.

The latencies of hardware implementation is shown in Table 6. The device-level transient takes 100 ns for the first-order approximation and 10ns for the mixed oscillation

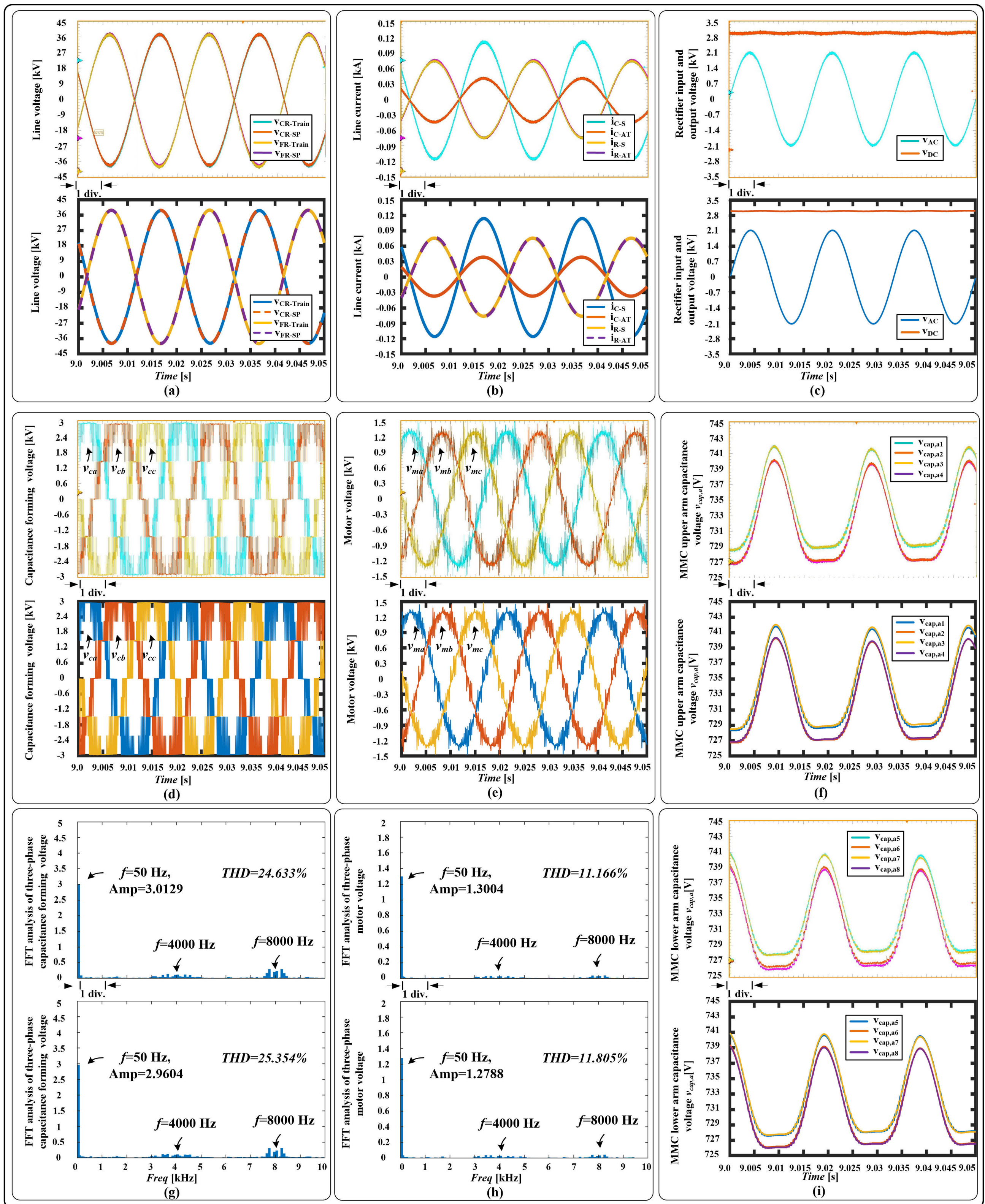

FIGURE 14. System-level results for complete HSR traction system from real-time simulation (top oscilloscope sub-figure) and off-line simulation by PSCAD/EMTDC® software (bottom sub-figure) for: (a) line voltage, (b) line current, (c) rectifier input and output voltage, (d) capacitance forming voltage, (e) motor voltage, (f) MMC upper arm capacitance voltage, (g) FFT analysis of capacitance forming voltage, (h) FFT analysis of motor voltage, (i) MMC lower arm capacitance voltage. Scale: (a) (b) (c) (d) (e) (f) (i) x-axis: 5*ms*/div. (g) (h) x-axis: 1*kHz*/div. .

TABLE 4. FPGA hardware resource consumption for device-Level and system-Level model on dedicated platform.

Model	BRAM	DSP	FF	LUT
Device-level Train 1 on ZCU102				
Train 1	21.81%	45.83%	26.17%	90.92%
System-level HSR System 1 on VCU118-1				
Train 2	0.07%	16.89%	6.07%	21.08%
Station 1	0%	29.78%	22.94%	46.39%
Total	0.07%	46.67%	29.01%	67.47%
System-level HSR System 2 on VCU118-2				
Train 3	0.07%	16.89%	6.07%	21.08%
Train 4	0.07%	16.89%	6.07%	21.08%
Station 2	0%	29.78%	22.94%	46.39%
Total	0.14%	63.56%	35.08%	88.55%

TABLE 5. Average error rate of W-H model with SaberRD®.

i_{on}	v_{on}	i_{off}	v_{off}
0.17%	4.32%	1.02%	3.72%

TABLE 6. Latencies of hardware implementation.

Device-level first-order appro.	Device-level mixed osc.	System-level
100ns	10ns	10μs

waveform in real-time with proper precalculation assignment while the system-level transients need 10 μs to conduct the emulation.

VI. CONCLUSIONS

The technology of high-speed rail network is constantly evolving with the introduction of newer power semiconductor device, and an accurate and efficient hardware-in-the-loop simulation is necessary. Real-time device-level modeling of ultrafast power switch is demanding due to high amount of computation execution and time-sensitive condition. With proper allocation of the high-sequential clocking ARM® core and massively parallel FPGA execution resource, real-time ultra small time-step modeling of detailed power converter system can be realized for both device-level and system-level transients. This paper proposed a Wiener-Hammerstein based real-time modelling method for SiC IGBT module emulation in the energy conversion system of the Beijing-Shanghai HSR application. Oscillation mechanism for SiC device has been explained in detail with three dedicated stages: carrier charge stage, static characteristic, and dynamic characteristic. The complete HSR prototype and the detailed HSR train power system have been implemented in MPSoC-FPGA hardware platform with optimized communication protocol, where the device-level transients, verified by SaberRD®, are executed at 10ns time-step and system-level transients, verified by PSCAD/EMTDC®, are emulated at 10μs time-step. This work can be utilized as the HIL tool to estimate the SiC material based power switch performance for the increasing demand of energy-efficient application of the future generations of HSR.

TABLE 7. Parameters of Hybrid SiC IGBT module.

Parameter	Value
L_{E1},L_{E2}	10 nH
L_{C1},L_{C2}	20 nH
L_S	100 nH
$C_{oes(V_R)}$	1.17 nF
R_{eq}	1.5 Ω
$Q_c(1/2module)$	2.5 μC
I_{rr}	100 A

TABLE 8. Parameters of traction power system.

Parameter	Value
DC bus voltage	3 kV
DC bus capacitor	10 mF
Carrier frequency	2000 Hz
Z_C	0.119+j0.752 Ω/km
Z_F	0.204+j0.885 Ω/km
Z_R	0.162+j0.671 Ω/km
Z_{CR}	0.057+j0.388 Ω/km
Z_{CF}	0.057+j0.395 Ω/km
Z_{RF}	0.057+j0.341 Ω/km
C_{CF}	0.000504 $\mu F/km$
C_{CR}	0.002057 $\mu F/km$
C_{FR}	0.003262 $\mu F/km$
$K_{P(PR)}$	0.7
$K_{R(PR)}$	0.4

APPENDIX

Tables 7 and 8.

REFERENCES

[1] T. Uzuka, "Faster than a speeding bullet: An overview of japanese high-speed rail technology and electrification," *IEEE Electrific. Mag.*, vol. 1, no. 1, pp. 11–20, Sep. 2013.
[2] B. Xie, Y. Li, Z. Zhang, S. Hu, Z. Zhang, L. Luo, Y. Cao, F. Zhou, R. Luo, and L. Long, "A compensation system for cophase high-speed electric railways by reactive power generation of SHC&SAC," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 2956–2966, Apr. 2018.
[3] Z. Liu, G. Zhang, and Y. Liao, "Stability research of high-speed railway EMUs and traction network cascade system considering impedance matching," *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4315–4326, Sep. 2016.
[4] F. Ma, A. Luo, X. Xu, H. Xiao, C. Wu, and W. Wang, "A simplified power conditioner based on half-bridge converter for high-speed railway system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 728–738, Feb. 2013.
[5] F. Ma, Z. He, Q. Xu, A. Luo, L. Zhou, and M. Li, "Multilevel power conditioner and its model predictive control for railway traction system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7275–7285, Nov. 2016.
[6] J. H. Kim, B.-S. Lee, J.-H. Lee, S.-H. Lee, C.-B. Park, S.-M. Jung, S.-G. Lee, K.-P. Yi, and J. Baek, "Development of 1-MW inductive power transfer system for a high-speed train," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6242–6250, Oct. 2015.
[7] A. Facchinetti and M. Mauri, "Hardware-in-the-Loop overhead line emulator for active pantograph testing," *IEEE Trans. Ind. Electron.*, vol. 56, no. 10, pp. 4071–4078, Oct. 2009.
[8] A. Siemens, "High-speed electric railway experiments on the marienfelde-zossen line," *J. Inst. Electr. Eng.*, vol. 33, no. 168, pp. 894–923, Aug. 1904.
[9] J. C. Dries, "SiC research and development at united silicon carbide Inc.-looking beyond 650-1,200 v diodes and transistors [happenings]," *IEEE Power Electron. Mag.*, vol. 2, no. 1, pp. 12–15, Mar. 2015.
[10] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.
[11] B. Ozpineci and L. M. Tolbert, "Characterization of SiC Schottky diodes at different temperatures," *IEEE Power Electron Lett.*, vol. 1, no. 2, pp. 54–57, Jun. 2003.
[12] M. Zubert, M. Napierlska, G. Jablonski, L. Starzak, M. Janicki, and A. Napieraski, "Static electro-thermal model of SiC merged p-i-n Schottky diodes," in *Proc. 10th Int. Seminar Power Semiconductors*, Sep. 2002, pp. 227–232.

[13] T. Liang and V. Dinavahi, "Real-time device-level simulation of MMC-based MVDC traction power system on MPSoC," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 626–641, Jun. 2018.
[14] Z. Shen and V. Dinavahi, "Real-time device-level transient electrothermal model for modular multilevel converter on FPGA," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6155–6168, Sep. 2016.
[15] H. A. Mantooth and J. L. Duliere, "A unified diode model for circuit simulation," *IEEE Trans. Power Electron.*, vol. 12, no. 5, pp. 816–823, Sep. 1997.
[16] T. R. McNutt, A. R. Hefner, H. A. Mantooth, J. Duliere, D. W. Berning, and R. Singh, "Silicon carbide PiN and merged PiN Schottky power diode models implemented in the saber circuit simulator," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 573–581, May 2004.
[17] T. R. McNutt, A. R. Hefner, H. A. Mantooth, J. L. Duliere, D. W. Berning, and R. Singh, "Physics-based modeling and characterization for silicon carbide power diodes," *Solid-State Electron.*, vol. 50, no. 3, pp. 388–398, Mar. 2006.
[18] R. L. Thomas, M. Morgenstern, and S. B. Bayne, "Silvaco modeling of a 10 kV SiC p-i-n diode," in *Proc. 26th Int. Conf. Power Modular Symp.*, May 2004, pp. 567–570.
[19] R. Chibante, A. AraÚjo, and A. Carvalho, "Finite-element modeling and optimization-based parameter extraction algorithm for NPT-IGBTs," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1417–1427, May 2009.
[20] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, "A 3-D-lumped thermal network model for long-term load profiles analysis in high-power IGBT modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050–1063, Sep. 2016.
[21] P. Liu, N. Lin, and V. Dinavahi, "Integrated massively parallel simulation of thermo-electromagnetic fields and transients of converter transformer interacting with MMC in multi-terminal DC grid," *IEEE Trans. Electromagn. Compat.*, vol. 62, no. 3, pp. 725–735, Jun. 2020, doi: 10.1109/TEMC.2019.2915340.
[22] N. Lin and V. Dinavahi, "Electrothermal transient behavioral modeling of thyristor-based ultrafast mechatronic circuit breaker for real-time DC grid emulation," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1660–1670, Mar. 2020.
[23] N. Lin and V. Dinavahi, "Exact nonlinear micromodeling for fine-grained parallel EMT simulation of MTDC grid interaction with wind farm," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6427–6436, Aug. 2019.
[24] N. Lin and V. Dinavahi, "Dynamic electro-magnetic-thermal modeling of MMC-based DC–DC converter for real-time simulation of MTDC grid," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1337–1347, Jun. 2018.
[25] N. Lin and V. Dinavahi, "Detailed device-level electrothermal modeling of the proactive hybrid HVDC breaker for real-time Hardware-in-the-Loop simulation of DC grids," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1118–1134, Feb. 2018.
[26] F. Bertoluzza, G. Sozzi, N. Delmonte and R. Menozzi, "Hybrid large-signal/lumped-element electro-thermal modeling of GaN-HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3163–3170, Dec. 2009.
[27] A. R. Hefner, "A dynamic electro-thermal model for the IGBT," *IEEE Trans. Ind. Appl.*, vol. 30, no. 2, pp. 394–405, Mar./Apr. 1994.
[28] H. Bai, C. Liu, S. Zhuo, R. Ma, D. Paire and F. Gao, "FPGA-based device-level electro-thermal modeling of floating interleaved boost converter for fuel cell hardware-in-the-loop applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5300–5310, Sep./Oct. 2019.
[29] K. Fukahori and P. R. Gray, "Computer simulation of integrated circuits in the presence of electrothermal interaction," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 6, pp. 834–846, Dec. 1976.
[30] M. K. Lee, C.-K. Kim, J. W. Park, E. Kim, M.-L. Seol, J.-Y. Park, Y.-K. Choi, S.-H.-K. Park, and K. C. Choi, "Electro-thermal annealing method for recovery of cyclic bending stress in flexible a-IGZO TFTs," *IEEE Trans. Electron Devices*, vol. 64, no. 8, pp. 3189–3192, Aug. 2017.
[31] C. C. Lee, A. L. Palisoc, and J. M. W. Baynham, "Thermal analysis of solid-state devices using the boundary element method," *IEEE Trans. Electron Devices*, vol. ED-35, no. 7, pp. 1151–1153, Jul. 1988.
[32] K. Narendra and P. Gallman, "An iterative method for the identification of nonlinear systems using a Hammerstein model," *IEEE Trans. Autom. Control*, vol. 11, no. 3, pp. 546–550, Jul. 1966.
[33] F. Chang and R. Luus, "A noniterative method for identification using Hammerstein model," *IEEE Trans. Autom. Control*, vol. AC-16, no. 5, pp. 464–468, Oct. 1971.
[34] E.-W. Bai and M. Fu, "A blind approach to Hammerstein model identification," *IEEE Trans. Signal Process.*, vol. 50, no. 7, pp. 1610–1619, Jul. 2002.
[35] Y. Bao, L. Y. Wang, C. Wang, and Y. Wang, "Hammerstein models and real-time system identification of load dynamics for voltage management," *IEEE Access*, vol. 6, pp. 34598–34607, 2018.
[36] J.-T. Hsu and K. D. T. Ngo, "A Hammerstein-based dynamic model for hysteresis phenomenon," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 406–413, May 1997.
[37] X. Gao, C. Zhang, C. Zhu, and X. Ren, "Identification and control for Hammerstein systems with hysteresis non-linearity," *IET Control Theory Appl.*, vol. 9, no. 13, pp. 1935–1947, Aug. 2015.
[38] F. Alonge, R. Rabbeni, M. Pucci, and G. Vitale, "Identification and robust control of a quadratic DC/DC boost converter by Hammerstein model," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 3975–3985, Sep. 2015.
[39] B. D. S. Pes, E. Oroski, J. G. Guimaraes, and M. J. C. Bonfim, "A Hammerstein–Wiener model for single-electron transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 1092–1099, Feb. 2019.
[40] A. Balestrino, A. Landi, M. Ould-Zmirli, and L. Sani, "Automatic nonlinear auto-tuning method for Hammerstein modeling of electrical drives," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 645–655, Jun. 2001.
[41] B. Li, S. Zhou, D. Xu, S. J. Finney, and B. W. Williams, "A hybrid modular multilevel converter for medium-voltage variable-speed motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4619–4630, Jun. 2017.
[42] S. Du, B. Wu, and N. Zargari, "A control strategy for star-channel modular multilevel converter in variable-speed motor drive application," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5094–5101, Jul. 2019.

TIAN LIANG (Graduate Student Member, IEEE) received the B.Eng. degree in electrical engineering from Nanjing Normal University, Nanjing, Jiangsu, China, in 2011, and the M.Eng. degree from Tsinghua University, Beijing, China, in 2014. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of Alberta, Edmonton, AB, Canada. His research interests include real-time simulation of power systems, power electronics, field-programmable gate arrays, and system-on-chip.

QIN LIU (Graduate Student Member, IEEE) received the B.Eng. degree in measurement and control technology and instrument from Beijing Jiaotong University, Beijing, China, in 2013, where she is currently pursuing the Ph.D. degree with the School of Mechanical, Electronic, and Control Engineering. She is also a Visiting Ph.D. Student in electrical and computer engineering with the University of Alberta, Edmonton, Alberta, Canada. Her research interests include real-time simulation and control of power systems, hardware acceleration, and system-on-chip.

VENKATA R. DINAVAHI (Fellow, IEEE) received the B.Eng. degree in electrical engineering from the Visveswaraya National Institute of Technology (VNIT), Nagpur, India, in 1993, the M.Tech. degree in electrical engineering from IIT Kanpur, India, in 1996, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, ON, Canada, in 2000. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His research interests include modeling and simulation of electromagnetic transients, real-time simulation, device-level modeling, large-scale systems, and parallel and distributed computing.