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An Improved Hysteresis Voltage Mode of Synchronous Rectifier Buck Circuit

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ABSTRACT To achieve high power and high efficiency over a wide load range, an improved hybrid hysteresis voltage mode for Buck circuit is proposed in this paper. The strategy and workflow of the proposed improved hybrid hysteresis voltage mode are demonstrated step by step. The output voltage performance of the Buck circuit with proposed hysteresis voltage mode is compared with the same circuit with typical hysteresis voltage mode. Numerical simulation results show that with the introduction of the PD link, the overshoot can be completely controlled or eliminated; with the introduction of the dynamic voltage reference, the static difference can be completely negligible; relatively stable input voltage improves its steady-state working frequency and the electromagnetic interference significantly. Thus, the proposed control strategy can not only achieve satisfied performance, but also provide a basis for further design and optimization.

INDEX TERMS Buck circuit, hysteresis voltage mode, ripple elimination, static difference.

I. INTRODUCTION

High-power Class-D amplifiers (CDAs) have been studied for the applications that require high switching frequency and high-power handling capability, such as industrial vibration test systems, electromagnetic interference test systems, and current control systems for magnetic resonance imaging scanners [1], [2]. As one of research hot-spots, Class-D amplifiers are widely investigated. Wang *et al.* [3] proposed a general analytical method to characterize the steady-state phase and the total current ripple in the multi-leg CDAs with full-bridge configuration under inductance mismatches. Monte Carlo simulation was used to study the impact of inductance mismatches on the harmonic contents of the total current ripple, and the distribution law of the inductance at the worst case was revealed. A design guideline was given to optimize the filter design based on the analytical method. Zhou*et al.* [4] proposed a soft switching symmetric bipolar outputs DC transformer (DCX) for eliminating power supply pumping of half-bridge Class-D audio amplifiers. Compared with the traditional unidirectional front-end DC–DC converter in the half-bridge Class-D audio amplifier, output capacitance of the proposed DCX and voltage stress of the half-bridge Class-D audio amplifier were significantly reduced. High-power Class-D power amplifiers generally use Buck circuits as the basis for design. With the consideration of the good dynamical performance, as well as to meet the accuracy requirements of the applications, Buck circuits usually work with various feedback control schemes. Meanwhile, the combination of variable and fixed frequency hybrid modulation is a popular technique for improving the efficiency over a wide load range [5]. For instance, at heavy loads, pulse-width modulation (PWM) with low on-resistance power switches at the input stage can reduce conduction losses. And also with the help of the multiple control techniques, Buck circuits can be used as high-power low-voltage converter.

Taking switching-mode power supplies (SMPSs) in the most commonly application field of Buck circuits as an example, most of the currently adopted control methods are linear or digital control methods which are both based on PWM technology. Fu *et al.* [6] developed a 200 W two-stage rail grade DC–DC module based on gallium-nitride devices. It converted a wide input voltage (64–160V) to a constant output voltage (24V). The voltage regulation was discussed for the Buck converter when the inductors are negatively coupled, and then the zero-voltage switching (ZVS) extension

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was explored. However, the overshoot and undershoot voltage was too high to be accepted, and the recovery time was too long. What's more, due to the limitation of the digital controller, a trade-off had to be made between the dynamic response and the footprint. The compromise solution was got by using a small and slow micro-controller for high frequency control (including voltage regulation, critical mode operation and phase interleaving) and various demands (including soft start-up, external communication, and various protections). Inanlou *et al.* [7] presented a buck type DC-DC converter based on an asynchronous pulse width modulator (APWM). The proposed APWM is a self-oscillating circuitry which is composed of a binary comparator (BAPWM) and a distinctive digitally controlled delay cell. The oscillating frequency of the BAPWM can be tuned by the delay of the modulator loop. Hsu *et al.* [8] presented a dual operating modes (DOMs) control technique to achieve fast-transient response for DC–DC Buck converter. The proposed operational trans-conductance amplifier with DOM control circuit was used as an error amplifier in the PWM control circuit. The operating frequency was set at 1MHz, while the load current range was from 100 to 500 mA. Li *et al.* [9] presented design and analysis of the switching rule based on affine switched systems, and simulation and experimental verification were carried out for the Buck converter. A switching rule based on affine switched systems was introduced. The experimental results showed that the switching rule makes the system asymptotically stable. Their research showed that a huge inductor with 4.5 mH should be used to build the circuit, which means that the dynamic performance of the output voltage is unacceptable, or the load step must be small enough. Moreno-Valenzuela *et al.* [10] gave a novel design matching the proposed class of controllers. The results of real-time experimental tests were presented, including the implementation of the linear proportional-integral (PI) control and a known anti-windup (AW) approach. According to the result of the paper, the recovery time seemed to be shorter, but the power-on overshoot remained at a high value. Meurer*et al.* [11] proposed a new grid current controller for a photovoltaic (PV) module integrated Buck converter using a single pulse-width modulation switch and an unfolding H-bridge, which significantly reduced switching losses. Wang *et al.* [12]presented a reconfigurable transient optimizer (RTO) applied to a four-phase Buck converter for optimizing both dynamic-voltage-scaling (DVS) and load transient responses to approach the theoretically minimum output-voltage undershoot (VUS), overshoot (VOS), and settling time (tS). The response time remained more than several period, which means that the controller needs more information to ensure the load or the settings to be changed. Yuan*et al.* [13] presented a monolithic voltage-mode DC–DC Buck converter with advanced burst mode (ABM) and pulse-width modulation (PWM) to achieve high frequency and high efficiency over a wide load range. Suh *et al.* [14] proposed a pulse-width modulation buck converter with an active ramp tracking control to achieve a fast load transient response. When the difference between the output voltage and reference voltage increased to a certain level in the load transient situation, the ramp bias voltages would tracked the error voltage and provide a full duty to power switches. This helped restore the output voltage to the reference voltage, and improved the load transient response speed and decreased the overshoot/undershoot and their recovery times at the output voltage. The above research results show that although the linear control methods can achieve a reasonable control effect, they can not be separated from the digital control design, which leads to high cost. When the digital control method is unused, the performance of the linear control method based on PWM technology is not ideal. And if we look back on the PWM-based controller, it is obvious that we don't need the part of the feedback signal which remains the same frequency with the PWM pulse generated by the controller. But when we try to move it away from the feedback signal, we will lost some useful signal, which will cause controllers work without enough information of the circuit.

The basic nonlinear control methods of Buck Circuits belong to Bang-Bang control theory. The basic nonlinear control strategy is that when the feedback voltage is lower than the reference voltage, the input voltage is adjusted to the maximum value; when the feedback voltage is higher than the reference voltage, the input is adjusted to the minimum value. Obviously, this kind of strategy is with all parts of the feedback signal, so the robustness of this strategy is strong enough, but its steady-state frequency would be unlimited, which is unable to be realized in engineering fields. Thus, the hysteresis voltage mode is developed from the basic nonlinear control strategy. By setting a target voltage hysteresis band, hysteresis voltage mode overcomes the frequency problem of the basic nonlinear control strategy. The controller of hysteresis voltage mode is mainly composed of a hysteresis comparator, which is simple in designation and low in cost. And this type of method has been fully researched during recent years. Veligorskyi*et al.* [15] proposed a new photovoltaic panel maximum-power-point optimizer based on a Buck converter. Three different realizations of proposed hysteresis optimizers had been analyzed in his work, including operation principle and adjustment of hysteresis intervals. Park*et al.* [16] presented a new technique that could adjust the hysteresis window depending on the variations in load current caused by a voltage-mode circuit to reduce the voltage and current ripples. In addition, a zero-current detection circuit was also proposed to eliminate the reverse current at light loads. This paper showed that the hysteresis mode had reasonable performance, but the load should be light. Kapat [17] thought that the inductor current ripple under hysteresis current control was sensitive to system as well as controller parameters, which often deviated from the desired band. Thus, a phase-locked-loop (PLL) was employed to regulate the switching frequency over the operating range. The result from the work showed that there was an unexpected gradual slope on the curve of the output voltage, which was probably caused by the current mode. Lu [18]

thought that by using electrolytic capacitors as the output capacitor, the traditional capacitor current hysteresis (CCH) controller was in over-damping state due to the equivalent series resistance of the capacitor (*ESR*), and had a poor dynamic performance. To solve those problems, an improved constant frequency CCH (CF-CCH) control scheme using the reconstructed ideal-capacitor voltage was proposed. The ideal capacitor voltage was reconstructed through a low-pass filter and an integrator, and introduced into the control loop to replace the actual output voltage. It can be found that the dynamic performance met the expectation, but the *ESR* was still a bit large, and the unexpected overshoot remained.

In these studies, the researchers used classical control theories to design the hysteresis voltage mode. That leads to a result that the application of the hysteresis voltage mode depends on the large *ESR* of filter capacitance, which means this kind of control strategy has better dynamical performance, but poorer steady-state performance, compared with traditional strategies. When using capacitors with low *ESR*, special ripple compensation measures are needed to remain acceptable steady-state performance. That means, although this compensation method is feasible, it affects both the dynamic performance and robustness of the system, which leads difficulties to calculate and match parameters in the system. So there are few applications of hysteresis voltage mode in engineering. And the reasons can be concluded that, (1) When the load is constant, the system is a typical constant-coefficient second-order piece-wise linear damped system, as the upper and lower transistors are alternately turn on and off. When *ESR* in the Buck Circuit is smaller than the value it should be matched with the inductance value L, the second-order property of the system is stronger, and the hysteresis phenomenon is more obvious. In the same case, the steady-state operating frequency of the circuit is low, and the dynamic performance is poor. When *ESR* is larger than the value it should be matched with L, the first-order property of the system is stronger, and the hysteresis is less obvious. Meanwhile, the peak-to-peak voltage of steady state is larger when operating in the hysteresis voltage mode; (2) The Buck circuit has significant hysteresis characteristics. The lack of predictability of the control strategies will cause overshoot and make the system diverge; (3) The Buck circuit in the hysteresis voltage mode may not necessarily work at a fixed frequency. During high-power electrical energy converting, the hysteresis voltage mode will generate electromagnetic waves with the change of the operating frequency, which will affect the operation of other equipment.

To overcome these problems and get the advances of the hysteresis voltage mode, this work focuses on designing an improved hybrid hysteresis voltage mode. The organization of this paper is as follows. A nonlinear second order differential equation of the Buck circuit model will be established in Section 2. The hybrid hysteresis voltage mode design will be described in Section 3. To eliminate the static difference, an improved strategy will be proposed in Section 4.

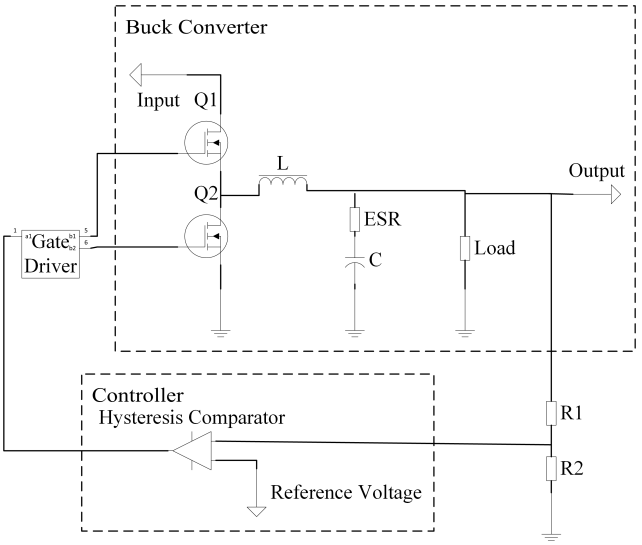

FIGURE 1. Buck circuit.

And some further discussions about the operating frequency will be made in Section 5. Finally, Section 6 concludes this paper.

II. MODELING OF THE BUCK CIRCUIT WITH HYSTERESIS VOLTAGE MODE

When controlling the synchronous rectifier Buck circuit, the hysteresis voltage mode has the constant-frequency characteristics. A piece-wise linear second-order damped system will be chosen as the theoretical model to analyze the working process of the controller. Thus, a typical Buck Circuit, shown in Figure 1, will be selected. And the governing equation of the circuit will be established. All the definitions of the variables and parameters in this paper are listed in Table 1.

The basic form of chosen synchronous rectifier Buck circuit is shown in Figure 1. It is easy to simplify it into a simple structure which is shown in Figure 2. It can be seen from Figure 2 that this circuit is obviously a second-order circuit. For a ideal Buck circuit, one has

$$U_{out} = U_R \tag{1}$$

For the inductance, we have

$$\begin{aligned} U_L &= L\frac{dI_L}{dt} \\ U_L &= U_{in} - I_L R_{DS(on)} - U_R \\ I_L &= I_C + I_R \end{aligned} \tag{2}$$

For the capacitance, we have

$$\begin{aligned} I_C &= C\frac{dU_C}{dt} \\ U_R &= U_{ESR} + U_C \\ U_{ESR} &= I_C r_{ESR} \end{aligned} \tag{3}$$

For the resistance, we have

$$I_R = \frac{U_R}{R_{load}} \tag{4}$$

TABLE 1. The definitions of the parameters.

Parameters	Definitions	Default values	Parameters	Definitions	Default values
$U_{in,\max}$	Maximum input voltage	90.0 V	U_{in}	Input voltage	N/A
$U_{in,\min}$	Minimum input voltage	70.0 V	$R_{DS(on)}$	On-resistance of the transistor	N/A
f_{in}	Variation frequency of input voltage	100 Hz	U_{out}	Output voltage	N/A
U_{GND}	Ground voltage	0 V	R_{Load}	Load resistance	N/A
$R_{DS(on),upper}$	On-resistance of the upper transistor	10.0 mΩ	V_{FB}	Feedback voltage	N/A
$R_{DS(on),lower}$	On-resistance of the lower transistor	10.0 mΩ	V_{HB}	The half of hysteresis width	N/A
L	Inductor	20.0 μH	t_{delay}	Total delay of the controller	N/A
C	Capacitance	5.00×10^3 μF	P	Proportional coefficient	N/A
r_{ESR}	Equivalent series resistance of the Capacitance	2.40 mΩ	D	Differential coefficient	N/A
$U_{out,set}$	The set value of output voltage	12 V	dV_{ref}	Adjustment value of dynamic reference voltage	N/A
$I_{out,\max}$	Maximum value of I_{out}	60.0 A	U_L	Voltage of the inductor	N/A
$I_{out,\min}$	Minimum value of I_{out}	0.10 A	U_C	Voltage of the capacitance	N/A
f_{out}	Variation frequency of load resistance	100 Hz	U_R	Voltage of the load resistance	N/A
V_{ref}	Reference voltage	2.5 V	U_{ESR}	Voltage of the ESR	N/A
$V_{OPA,\max}$	Maximum output voltage of operational amplifier	4.00 V	I_L	Current of the inductor	N/A
$V_{OPA,\min}$	Minimum output voltage of operational amplifier	1.00 V	I_C	Current of the capacitance	N/A
I_{out}	Expected current output	$U_{out,set}/R_{Load}$	I_R	Current of the load resistance	N/A

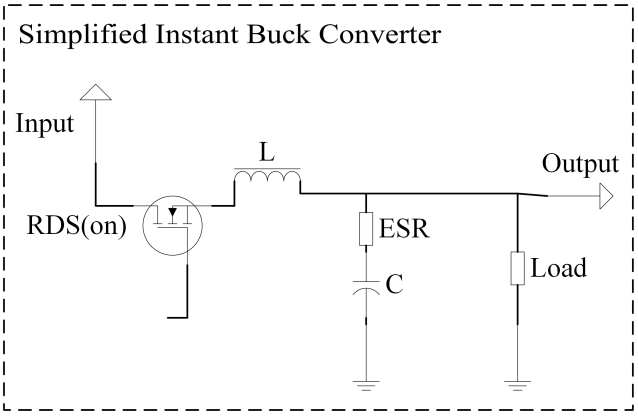

FIGURE 2. Simplified Buck circuit.

Combining all the ideal relationship expressions gives

$$I_L = C\frac{dU_C}{dt} + \frac{C\frac{dU_C}{dt}r_{ESR} + U_C}{R_{load}} = C\frac{dU_C}{dt}(1 + \frac{r_{ESR}}{R_{load}}) + \frac{U_C}{R_{load}} \quad (5)$$

Deriving Eq. 5, we can get

$$\frac{dI_L}{dt} = C\frac{d^2U_C}{dt^2}(1 + \frac{r_{ESR}}{R_{load}}) + \frac{1}{R_{load}}\frac{dU_C}{dt} \quad (6)$$

Then, it is obviously to describe the circuit into a second-order differential equation as

$$C(1 + \frac{r_{ESR}}{R_{load}})\frac{d^2U_C}{dt^2} + (\frac{1}{R_{load}} + CR_{DS(on)}\frac{1 + \frac{r_{ESR}}{R_{load}}}{L} + C\frac{r_{ESR}}{L})\frac{dU_C}{dt} + \frac{1 + \frac{R_{DS(on)}}{R_{load}}}{L}U_C = \frac{U_{in}}{L} \quad (7)$$

where the output voltage is

$$U_{out} = U_R = Cr_{ESR}\frac{dU_C}{dt} + U_C \quad (8)$$

and the definitions and the default values of the parameters are given in Table 1.

It is noting that when you design a control system, the optimal parameters should be determined by the working condition, like in this work, U_{in} and R_{load} and the expected performance, like U_{out}. But U_{in} and R_{load} can change with time, once the hardware parameters have been fixed, the change of the working condition should be tackled by the robustness of the control. Thus, when using the analysis method of second-order linear system, we should pay attention to the impact of the sudden and large change of load resistance R_{load} and input voltage U_{in} in the system and make sure the control strategy has robustness.

The basic work flow of hysteresis voltage mode is like

```
Flow 1 Hysteresis voltage mode
-----------------------------------------
1: upper_transistor = 0;
2: lower_transistor = 1;
3: // initialization of the controller,//
4: // while~0~means off and~1~means on //
5: while~1 {
6: // begin the loop //
7:  If V_FB < V_ref - V_HB
8:  // V_FB is the feedback voltage,   //
9:  // V_ref is the reference voltage, //
10:  // V_HB is the half of hysteresis  //
11:  // width.                          //
12:  { upper_transistor = 1;
13:    lower_transistor = 0;}
14:  Else if V_FB > V_ref + V_HB
15:  { upper_transistor = 0;
16:    lower_transistor = 1;}
17: }
-----------------------------------------
```

Take the Buck circuit controlled by the hysteresis voltage mode with parameters given in Table 1 as an example. The output voltage is shown in the Figure 3.

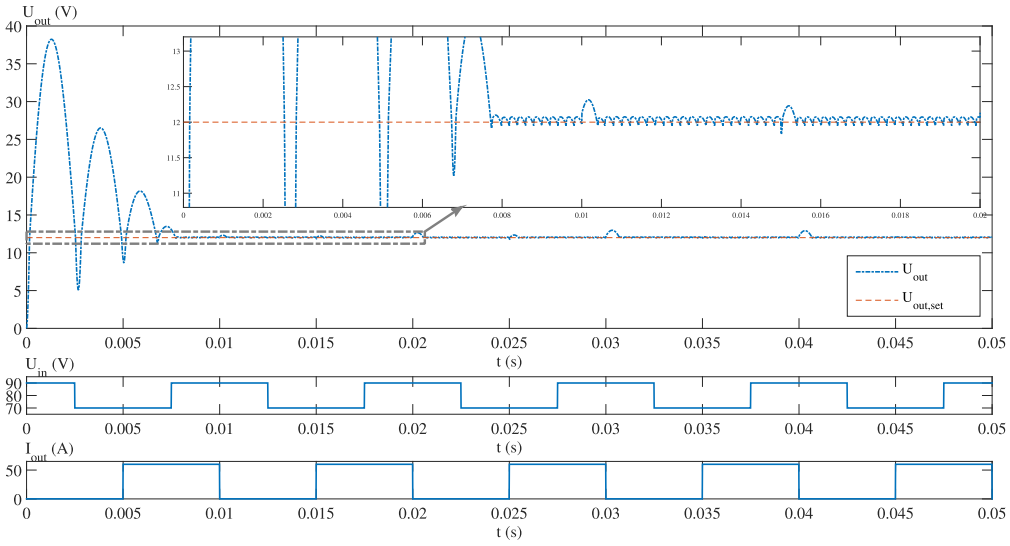

FIGURE 3. The output voltage in hysteresis voltage mode.

Figure 3 shows that the output voltage is insensitive to the changes of input voltage and load, and has fast enough dynamic response(less than 0.01s). And for further simulation, it can be found that when $0.1 \leqq U_{out}/U_{in} \leqq 0.8$, and $U_{out}/R_{load} \leqq 50$ A, the system will not lose its stability. Thus the hysteresis voltage mode has strong robustness. But, during the start-up process, its large overshoot amplitude, long overshoot time, and extremely low operating frequency, as well as extremely high peak-to-peak voltage after entering steady-state process are all unacceptable.

III. PROPOSAL OF THE ALGORITHM

A. PROPORTIONAL DIFFERENTIAL HYBRID HYSTERESIS VOLTAGE MODE

In order to improve the steady-state control performance, we should try to improve and stabilize the steady-state control frequency, and support the use of capacitors with smaller *ESR*. The method in previous literature usually used passive device to design feedback signal processing circuit to simulate large steady-state output voltage ripple caused by *ESR*. But this method is not only difficult to debug, but also hard to analyze in time domain.

From the point of improving the dynamical control performance, we should try to make the output of the system deviate barely from the steady state or return to the steady state at the fastest speed, and make the maximum overshoot as small as possible when the circuit remains without the unnecessary physical damping. The proportional-integral-derivative (PID) controller is one of the oldest control strategy used in process industries. Performance of the PID controller depends upon its three tuning parameters, i.e., proportional, integral, and derivative gains [19]. In the field of linear control, both proportional integral (PI) feedback control and proportional differential (PD) feedback control can improve the steady and dynamical performance. The traditional PID control needs fine tuning of the parameters to meet the robustness and performance requirements. So in the real practise, hybrid strategies are usually proposed and adopted. Fathy *et al.* [20] presented a novel optimal fuzzy proportional-integral-derivative controller for load frequency control (LFC), which was designed by a proposed approach of mine blast algorithm (MBA) for multi-interconnected areas. Zeng *et al.* [21] drew on the merits of fuzzy controller and PID controller, and a fuzzy-PID composite controller is designed. The composite controller can control a system by automatically switching between fuzzy control and PID control according to the range of error.

Based on the same idea, we combined the PID feedback control with the digital PWM. The proportional term controls the current state. The integral term stores every past state. The differential term calculates the next state. However, as a kind of low-pass filter, the integral term absorbs transient feedback signal. When the transient feedback signal appears with long enough time, the integral term takes effect, which means lag. The differential term focuses on transient and real-time signal, and controls the system immediately against sudden changes. Thus, the PD feedback control strategy is chosen here to make the control system predictive, make the system in any damping state conveniently, and adjust parameters relatively easily, so it has high reference value.

Meanwhile, the resistance change process when power transistors are on and off with short time occupation is ignored, that is to say, power transistors are only with on or off state; the parameters such as inductance and capacitance are constant; the load current only changes back and forth between minimum value and maximum value; the time of delay from the output feedback to the switch action is fixed on a undersigned value.

The implementation of the control strategy is that the output voltage is processed in a proportional differential circuit with an operational amplifier, the output results and the reference voltage are processed in the hysteresis voltage mode controller, and the rest of the hysteresis voltage mode control method remains unchanged. Above all, a proportional-differential link (PD link) is implemented before the hysteresis comparator.

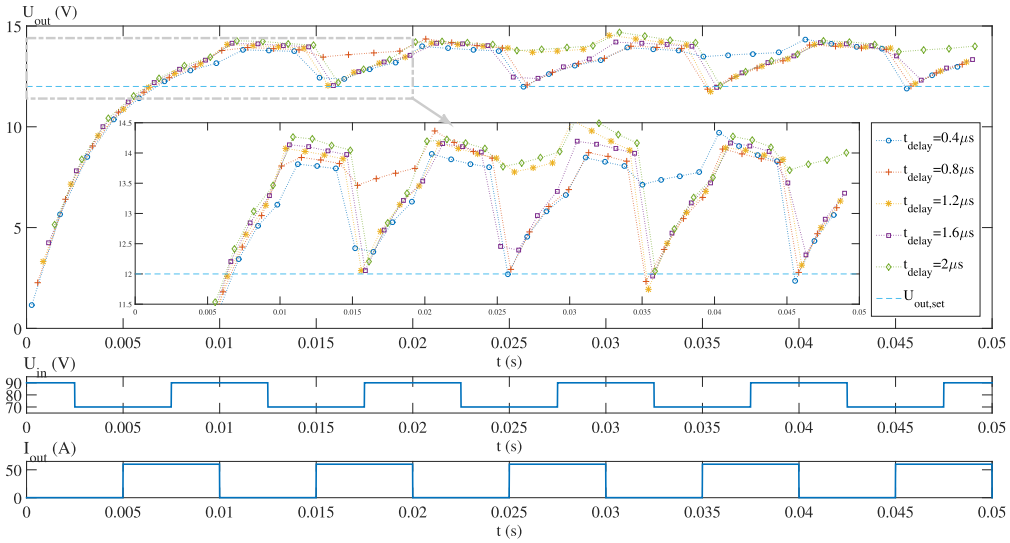

FIGURE 4. The output voltage in PD hybrid hysteresis voltage mode with any possible total delay of the controller.

And the work flow is like

```
Flow 2 Hybrid mode
----------------------------------------
1: upper_transistor = 0;
2: lower_transistor = 1;
3: while~1 {
4:  diff_V_FB = (V_FB(t)-V_FB(t - 1))/dt;
5:  // Calculate the differential of the//
6:  // feedback voltage, and the forward//
7:  // difference is used here.         //
8:  If P * (V_FB - V_ref) + D * diff_V_FB
9:     < V_HB
10:  // PD controller, which can be built//
11:  // with an operational amplifier.   //
12:  // P is the coefficient of the      //
13:  // proportional term, D~is the      //
14:  // coefficient of the differential  //
15:  // term.                            //
16:  { upper_transistor = 1;
17:    lower_transistor = 0;}
18:  Else if P * (V_FB - V_ref) + D *
19:            diff_V_FB > - V_HB
20:   { upper_transistor = 0;
21:     lower_transistor = 1;}
22: }
----------------------------------------
```

With $V_{HB}/P = 5.00 \times 10^{-3}$ V, $D/P = 1.00 \times 10^{-3}$, $t_{delay} = 0.40\,\mu$s, $0.80\,\mu$s, $1.20\,\mu$s, $1.60\,\mu$s and $2.00\,\mu$s, respectively, the output voltage of the circuit is simulated in Figure 4.

Through Figure 4, we could see that, from the perspective of steady-state performance, with any possible total delay of the controller, the effective value of the output voltage can converge to a certain value when the input voltage and load are stable, the steady-state output is sufficiently uniform and stable, and the dynamic response speed is fast enough, but different input voltages, loads and output voltages obviously correspond. There are different output voltages, and there is obvious static difference phenomenon.

Further, Figure 5 gives a comparison of the control performance of the output voltage of the hysteresis voltage mode after introducing the PD link and the hysteresis voltage mode without the PD link.

The curves in Figure 5 show that the PD link (the yellow curve) eliminates the overshoot of the hysteresis voltage mode completely (the blue curve). The output voltage always access to the set value from only one direction when the input voltage and the load are stable, which differs from the situation without the PD link. On the other hand, the operation frequency of the controller is much higher than the situation without PD link, which is too low to be an acceptable control mode. However, the static difference is unacceptable compared with the situation without the PD link which remains with negligible static difference.

B. IMPROVEMENT OF THE METHOD TO DISMISS THE STATIC DIFFERENCE

The above simulation process shows that the hybrid hysteresis voltage mode has a steady-state static difference similar to the PD control system, which is affected by the change of system parameters. The simulation in the previous section shows that when the input voltage and the load change, the effective value of output voltage changes.

It can be seen that the change of input voltage and load in the circuit has great influence on the static difference between the effective value of output voltage and the set value, so special design is needed to eliminate the static difference.

Under the condition that the input voltage and load are changing greatly, the effective value of the output voltage varies widely due to the influence of other intrinsic parameters in the system, and the relationship between the effective value and the set value is uncertain. The reasons for this are that, on one hand, although the integral controller may eliminate the static difference, it is unused in the controller for its damage to immediacy of the controller, which will make the system under-damped and the

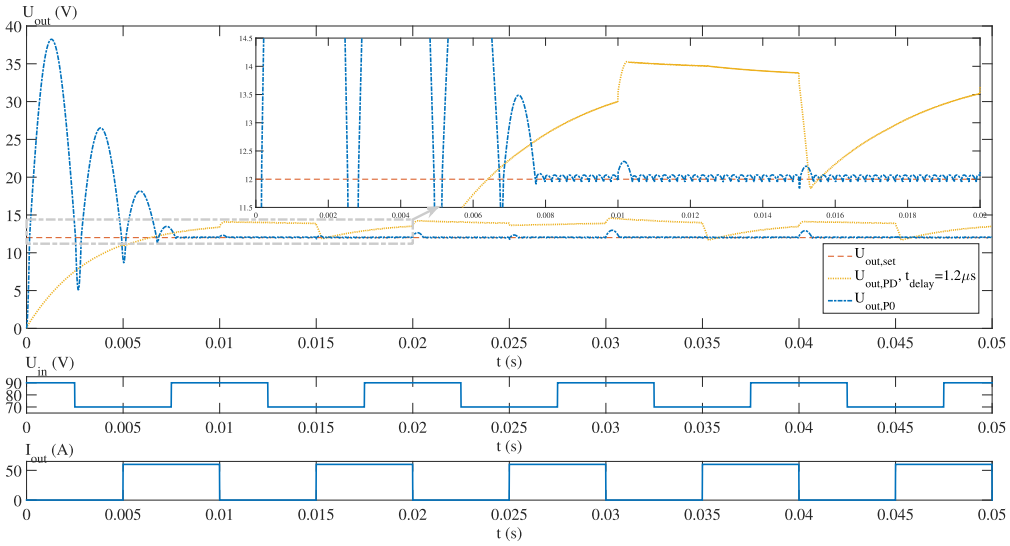

FIGURE 5. Comparison of the voltage outputs of hysteresis voltage modes with and without PD link.

parameter setting difficult. On the other hand, the traditional PID controllers always generate analog or continuous output (even the PWM output is based continuous signal). However, the hysteresis voltage mode controller generates discrete output: it just inputs onto the Buck circuit with input voltage or ground voltage but not a certain kind of intermediate analog output. This is the most remarkable advantage of the controller, for the reason that the lack of the certain kind of intermediate analog output will barely bring interference signal to the output of the circuit or the feedback signal compared with traditional PID-PWM controller which always makes researchers and engineers struggle dealing with the signal in PWM frequency in the feedback. That is, the ripple frequency generated by the PD link of the controller should be similar to the PWM frequency. But the integral term will decrease the ripple frequency and enhance the ripple voltage, which is unexpected.

A natural way to eliminate the static difference is to adjust the set value of the output voltage. When the effective value of steady-state output voltage is higher than the set value, the effective value of output voltage can be returned to the set value by properly lowering the set value. Otherwise, the set value can be properly increased. Although the expected static difference may increase in one of the two directions, as long as the output value and the feedback signal changes between the two sides of the setting or the reference value, the static difference can be eliminated. The idea is also relatively simple in hardware implementation. It can be achieved just with operational amplifiers and simple peripheral circuits.

The work flow is like

```
Flow 3 Improved hybrid mode
-----------------------------------------
1: upper_transistor = 0;
2: lower_transistor = 1;
3: while~1 {
4:  If V_FB < V_ref
5:  { V_ref_d = dV_ref;}
6:  Else if V_FB > V_ref
7:  { V_ref_d = - dV_ref;}
8:  // Adjust the direction of the    //
9:  // dynamic reference voltage to   //
10:  // the opposite one of the static //
11:  // difference, which can be       //
12:  // realized with a comparator     //
13:  // and an operational amplifier.  //
14:  // V_ref_d is the dynamic         //
15:  // reference voltage, dV_ref is   //
16:  // the adjustment value of        //
17:  // dynamic reference voltage.     //
18:  diff_V_FB = (V_FB(t) -
19:                V_FB(t - 1))/dt;
20:   If P * (V_FB - V_ref) + D *
21:      diff_V_FB < V_ref_d + V_HB
22:    { upper_transistor = 1;
23:      lower_transistor = 0;}
24:   Else if P * (V_FB - V_ref) + D *
25:           diff_V_FB > V_ref_d - V_HB
26:    { upper_transistor = 0;
27:      lower_transistor = 1;}
28: }
-----------------------------------------
```

With $V_{HB}/P = 5.00 \times 10^{-3}$ V, $D/P = 1.00 \times 10^{-3}$, $dV_{ref}/P = 0.5$, $t_{delay} = 0.40\,\mu$s, $0.80\,\mu$s, $1.20\,\mu$s, $1.60\,\mu$s and $2.00\,\mu$s, respectively. The output voltages of the hysteresis voltage mode Buck circuit with variable reference voltages are shown in Figure 6.

It can be seen from Figure 6 that the static difference between the effective value of steady-state output voltage and the set value is basically eliminated, the steady-state performance is good enough, the dynamic response is fast enough, and the control of overshoot is also within the allowable range under the sudden change of the load within the designed range.

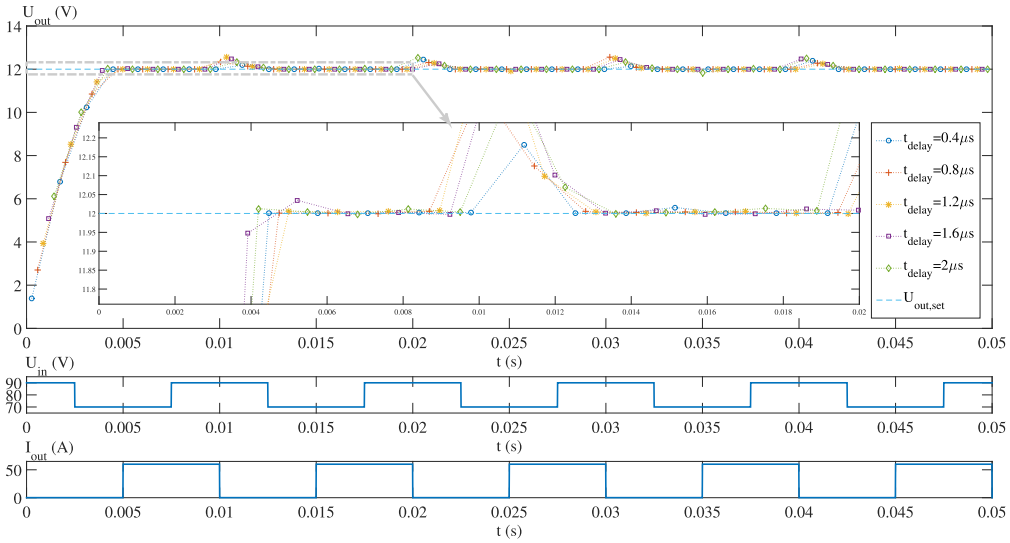

FIGURE 6. The output voltage in PD hybrid hysteresis voltage mode with dynamic voltage reference, with any possible total delay of the controller.

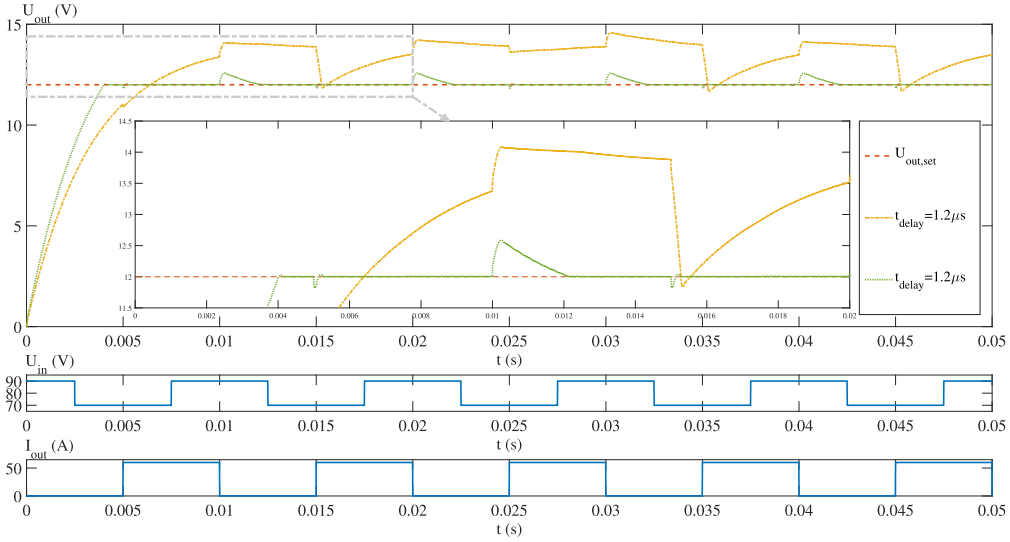

FIGURE 7. Differences of the output voltage between PD hybrid hysteresis voltage modes with and without dynamic voltage reference.

To demonstrate the improvement of the method, Figure 7 gives a comparison of the control performances of the output voltage of the circuit under PD hybrid hysteresis voltage mode with and without the dynamic reference voltage.

Figure 7 shows that, the dynamic reference voltage method (the green curve) can effectively make the static difference negligible which is highly increased due to the introduction of the PD link (the yellow curve), and maintain the anti-overshoot capability and excellent steady-state output effect as good as the situation without the dynamic reference voltage. Because the final control method uses the easy-to-stabilize PD link, and the controller has only two core parameters, the parameters of the controller are easy to adjust manually, which is beneficial to rapid development and debugging by engineering developers.

C. OPERATING FREQUENCY IN HYSTERESIS VOLTAGE MODE

Because the operating frequency of the hysteresis voltage mode is obviously affected by the hysteresis band width of the hysteresis comparator, which is difficult to obtain by theoretical calculations, this paper also pays attention to the change of the operating frequency of the controller during the numerical simulation. Under different total delays of feedback and control, the operating frequency of the controller changes as shown in Figure 8.

Obviously, in a certain steady state, the operating frequency of the circuit is constant, but with the change of the input voltage and output voltage ratio, the operating frequency of the circuit still changes. At the same time, the total delay of the feedback

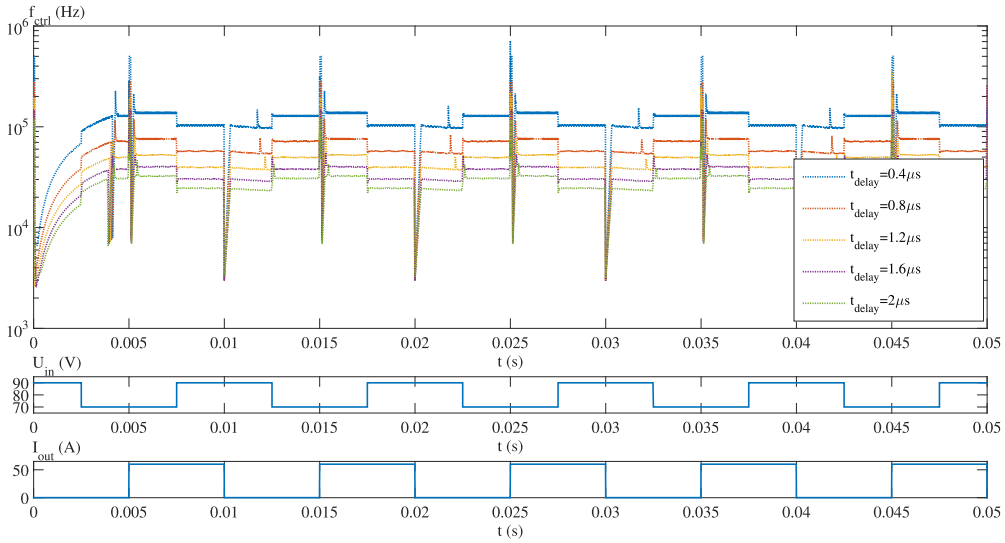

FIGURE 8. The operating frequency of the PD hybrid hysteresis voltage mode with dynamic voltage reference, with any possible total delay of the controller.

and control links affect the operating frequency. In short, when the amplitude of the input voltage does not change much, the operating frequency bandwidth of the controller is narrow enough.

The instantaneous frequency spikes appearing in the graph are due to step impacts of the input voltage and the load. Because the impact strength of input voltage and load in reality is limited, and there are more auxiliary means to deal with the impact, these transient spikes can be basically ignored. Because the total delay of the feedback and control links is not a design amount, the hysteresis band width needs to be carefully adjusted to obtain the optimal operating frequency.

IV. COMPARISON AND APPLICATION ANALYSIS

In this section, four groups of comparison will be made to further prove that the hybrid control mode proposed in this work is valid and physically realizable.

(1) In the Inalou's work [7], by increasing the delay of the modulator loop, the switching frequency decreases and the BAPWM can be reconfigured as a low frequency APWM (LFAPWM) modulator to meet the efficiency requirement at light loads. Also, to save the switching power consumption, the high-side power switch size is scaled according to the load conditions. Since the carrier signal is internally generated by the APWM itself, there is no major concern about the ramp signal discontinuity which is make duty cycle disturbance. In addition, from the point of view of the output spectrum, the proposed converter provides a better performance compared to the conventional PWM (CPWM) and PFM due to its noise shaping property.

Choosing similar external inductor and capacitor configurations, the performances of the work are compared with the results from Inanlou's work. The results are shown in Table 2 and indicate that the control mode proposed in this paper has a response speed that is significantly better than that of Reference [7]. The ripple voltage is smaller at the frequency of 300 kHz. When the load transient amplitude is large, the faster response speed is obviously conducive to the stability of the load.

TABLE 2. Comparison with Inanlou's work.

	Inanlou[7]	This work
Input voltage	5.0 V	5.0 V
Output voltage	2.5 V	2.5 V
Maximum current	1.0 A	1.0 A
Minimum current	0.1 A	0.1 A
Off-chip capacitance	10 μF	10 μF
Off-chip inductance	10 μH	10 μH
switching frequency	0.3 Mhz & 3 Mhz	0.313 Mhz (stable)
Transient response settling	65 μs @ 0.3Mhz	14 μs
Overshoot / Undershoot voltage	212 mV	209 mV
Ripple voltage	63 mV @ 0.3 MHz	16 mV

(2) In the Yuan's work [13], to achieve high frequency and high efficiency over a wide load range, a monolithic voltage-mode dc-dc buck converter with advanced burst mode (ABM) and pulse-width modulation (PWM) is presented. The load current is detected by estimating the currents flowing through the high-side and low-side switches, which maintains a near constant mode changing point. A counter-based scheme is used to achieve seamless and smooth transition between PWM and ABM. Both operating modes share the same control blocks, and no additional zero current detecting circuit is needed.

Choosing similar external inductor and capacitor configurations, the performances of the work are compared with the results from Yuan's work. The results are shown in Table 3 and indicate that the control mode proposed in this paper has significantly lower overshoot / undershoot voltage and ripple voltage. When the amplitude of the load transient is large, the smaller overshoot / undershoot voltage is obviously beneficial to the stability of the load.

Comparison 1 and 2 indicate that the control mode proposed in this paper is more suitable for the case of large load and high load change rate.

(3) In the Hsu's work [8], to achieve fast- transient response for DC-DC Buck converter, a proposed operational transconductance amplifier with DOM control circuit was used as an error amplifier in the pulse-width modulation (PWM)

TABLE 3. Comparison with Yuan's work.

	Yuan[13]	This work
Input voltage	5.0 V	5.0 V
Output voltage	1.15 V	2.5 V
Maximum current	1.0 A	1.0 A
Minimum current	0.1 A	0.1 A
Off-chip capacitance	47 μF	47 μF
Off-chip inductance	0.47 μH	0.47 μH
switching frequency	3 Mhz	1.36 Mhz (stable)
Recovery time	12 μs	12 μs
Overshoot / Undershoot voltage	35 mV	5 mV
Ripple voltage	30 mV	6 mV

TABLE 4. Comparison with Hsu's work.

	Hsu[8]	This work
Input voltage	5.0 V	5.0 V
Output voltage	3.3 V	3.3 V
Maximum current	0.5 A	0.5 A
Minimum current	0.1 A	0.1 A
Off-chip capacitance	8 μF	8 μF
Off-chip inductance	4.7 μH	4.7 μH
switching frequency	1 Mhz	1.225 Mhz (stable)
Recovery time	2 μs	5 μs
Overshoot/ Undershoot voltage	30 mV	47 mV
Ripple voltage	20 mV	4 mV

control circuit. This approach conduces to transient response by accelerating the output level shifting of the error amplifier. Thus, PWM control circuit generates the proper signal to drive the power transistors. Finally, the output voltage of the dc-dc buck converter is rapidly recovered when the load transient occurs.

Choosing similar external inductor and capacitor configurations, the performances of the work are compared with the results from Hsu's work. The results are shown in Table 4 and indicate that the recover time is longer and the overshoot voltage is larger but the ripple voltage is much smaller than Hsu's work. The reason for this is that the control parameters chosen in this work focus on the steady-state performance.

(4) In the Suh's work [14], to achieve a fast load transient response, the ramp bias voltages are introduced to track the error voltage and provide a full duty to power switches. This helps restore the output voltage to the reference voltage, improve the load transient response speed and decreas the overshoot/undershoot and their recovery times at the output voltage.

Choosing similar external inductor and capacitor configurations, the performances of the work are compared with the results from Suh's work. The rusults are shown in Table 5 and indicate that the recover time is longer but the overshoot voltage is smaller. The reason for this is same as the comparsion 3.

Through 4 groups of comparison, it could be found that the control mode proposed in this work is valid (as the performance is reasonable) and achievable (as the electronic components needed are common). In addition, the improved proportional differential hybrid hysteresis voltage mode proposed in this paper has a very low load regulation rate. The load adjustment rate is less than 0.1%, compared with the load adjustment rate of 2.5% from Inalou's work.

It is worth noting that one of the parameters related to the specific implementation is the delay time of the control link, which is determined by the delay of the device signal transmission. The total delay time of the control link in comparison is

TABLE 5. Comparison with Suh's work.

	Suh[14]	This work
Input voltage	3.3 V	3.3 V
Output voltage	2.5 V	2.5 V
Maximum current	0.9 A	0.9 A
Minimum current	0.45 A	0.45 A
Off-chip capacitance	4.7 μF	4.7 μF
Off-chip inductance	4.7 μH	4.7 μH
switching frequency	1 Mhz	1.25 Mhz (stable)
Recovery time	4 μs	6.4 μs
Overshoot/ Undershoot voltage	85 mV	75 mV
Ripple voltage	N/A	12 mV

set to 100 ns, which is easy to realize for engineering practice, because the response speed of discrete devices currently on the market is much lower than this level. In summary, if the control method proposed in this work is used to design a DC-DC converter, it is not necessary to design a new and highly integrated IC separately, which greatly speeds up the engineering implementation speed.

V. CONCLUSION REMARKS

When controlling the synchronous rectifier Buck circuit, the hysteresis voltage mode improved by the above schemes can provide a lower voltage drop ratio U_{out}/U_{in} with the case of proper *LC* parameter design, a high dynamic response speed with high frequency and low ripple rate of steady-state output and large load current change, as well as an acceptable range of steady-state operating frequency change. Hysteresis voltage mode can greatly improve the single-phase current output capacity and effect of Buck circuit, which is conducive to improve the power supply performance in the occasions where the dynamic capacity of single-phase power supply is highly required, such as high-level operation equipment power supply, class-D power amplifier, precision experimental instrument and precision inverter welding machine.

When the Buck circuit is designed with a smaller *ESR* capacitor, the improved PD hybrid hysteresis voltage mode is used to control the Buck circuit, which can simultaneously provide the same steady-state performance as the constant frequency control technology and the dynamic performance beyond the constant frequency control technology. With the introduction of the PD link, the improved hysteresis voltage mode has a certain predictive function, so the hysteresis of the circuit has been significantly improved, and the overshoot can be completely controlled. When the front-end circuit can provide relatively stable input voltage, the improved hysteresis voltage mode will produce frequency mutation only when the load impact changes, its steady-state working frequency is effectively limited in a narrow range, and the electromagnetic interference generated is also within the acceptable range.

However, like most of the defects of pulse frequency modulation control, the hysteresis voltage mode controller works in the quasi-constant frequency state, but the frequency spectrum of Electro-Magnetic Interference is still slightly wider than that of the constant frequency PWM controller. Therefore, the improved PD hybrid hysteresis voltage mode should be used to supply power to low-voltage equipment after a pre-stage module (such

as a power faction correction module) that can provide relatively stable input voltage.

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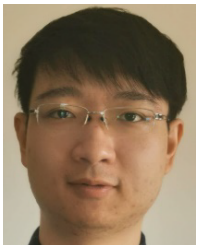

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