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# Minimum Loss Discontinuous Pulse-Width Modulation Per Phase Method for Three-Phase Four-Leg Inverter

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**ABSTRACT** The three-phase four-leg inverter (TPFLI) provides unbalanced voltage to a load or injects unbalanced current to a grid to compensate unbalanced current. However, it has a high switching loss because of the fourth leg. This paper presents a discontinuous pulse-width modulation (DPWM) method that minimizes the per-phase switching loss of the TPFLI. The discontinuous three-dimensional space-vector pulse-width modulation (3D SVPWM) can be implemented in the TPFLI by injecting the same offset voltage as the conventional DPWM of three-phase three-leg inverter (TPTLI). However, the conventional DPWM is unsuitable for TPFLI because of its unbalanced current. We demonstrate that the discontinuous phase can be chosen according to the offset direction when a voltage reference vector is specified. Based on this result, a new per-phase minimum-loss discontinuous PWM strategy is developed and compared with the conventional DPWM. This method can also be applied to the TPTLI and implemented by injecting an offset voltage generated using the inverter phase voltage reference and phase current. Furthermore, the lifespan of a TPFLI can be extended by preventing deterioration of a specific leg. The validity of the proposed method is verified through simulation and experiments.

**INDEX TERMS** Discontinuous pulse width modulation (DPWM), three-dimensional space vector pulse width modulation (3D SVPWM), three-phase four-leg inverter, switching loss.

## I. INTRODUCTION

The three-phase three-leg inverter (TPTLI) is a power converter that connects dispersed generations (DGs), such as photovoltaic (PV) and energy storage system (ESS), to the grid. However, DGs using TPTLI as a grid-tied power converter cannot supply unbalanced current when there is a current imbalance in the three-phase distribution network due to single-phase load or a network accident. Subsequently, the unbalanced current, which is also called zero-sequence current of the distribution line, will increase the losses and reduce the stability of the system [1]–[5]. To supply zero-sequence current, a transformer is installed on the output side of the inverter such that its neutral point is connected with that of the three-phase load. However, additional transformers increase the overall costs and volume of the power converter. In general, there are two ways to provide zero-sequence current without transformers: a three-phase four-wire inverter with split DC-link capacitors, and a three-phase four-leg inverter (TPFLI) [6]–[11]. On the one hand, the topology of three-phase four-wire inverter with split DC-link capacitors divides the DC-link capacitors in series and connects a neutral line to the midpoint of the capacitors. The structure is the simplest and has the least number of switches. However, the capacity of the DC-link capacitor is quite large for alleviating the capacitor voltage ripple caused by the current flowing in the midpoint of the capacitors [6], [7].

On the other hand, TPFLI has the advantage of a high DC-link voltage utilization approximately 15% higher than the three-phase four-wire inverter with split DC-link capacitors. However, TPFLI has a high switching loss due to the additional switches as shown in Fig. 1 [8]–[11]. Since TPFLI

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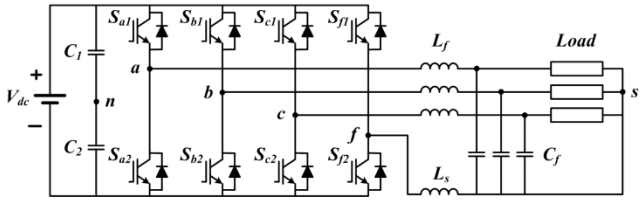



**FIGURE 1.** Three-phase four-leg inverter (TPFLI) topology.

has 16 switching states due to the addition of a fourth leg, various modulation methods have been proposed to generate the unbalanced phase voltage of the inverter [12]–[19]. The three-dimensional space vector modulation (3D SVPWM), which is the extension of the well-known two-dimensional space vector modulation(2D SVPWM) has been proposed, and 3D SVPWM has been extensively researched [12]–[16]. Reference [12] proposed a 3D SVPWM, and divided them into two classes: class I is a modulation scheme that reduces total harmonic distortion (THD) by continuous modulation (CPWM), whereas class II reduces the switching loss by DPWM. Additionally, [15] showed that several conventional DPWMs can be applied to the TPFLI by fixing the switching state of a specific area. However, the 3D SVPWM scheme involves a complex procedure and is difficult to implement.

To solve this problem, [17] proposed a carrier-based PWM method (CBPWM) that involves generating an unbalanced voltage by injecting the offset voltage ($V_{fn}$) to the three-phase voltage reference, and then using it as the voltage reference of the fourth leg. This method has the same performance as a 3D SVPWM and is easy to implement, and therefore commonly used [17], [18]. However, the study only focused on the CPWM scheme corresponding to class I of the 3D SVPWM. In addition, the power loss of each legs is different because of the unbalanced current. The power conversion system(PCS)'s lifespan depends on the leg that is most deteriorated by the unbalanced current. Therefore, the PCS has a short service life. The implementation of the conventional DPWM to a TPFLI using CBPWM was discussed in [19]–[22]. Reference [19] applied the conventional $\pm 120°$ DPWM to a TPFLI and [20], [21] demonstrated the implementation of various DPWMs can be implemented by adjusting the gating time. However, the conventional DPWM of a TPTLI is unsuitable for the TPFLI, because the inverter operates with an unbalanced current and across the entire ranges of the phase angle.

Reference [22] proposed a DPWM for the TPFLI that fixes a switching state when the absolute value of phase current becomes maximum. However, since the offset voltage is selected by considering only the maximum current value, if a switching state of the phase voltage having the maximum current cannot be fixed, the switching state of the unspecified phase voltage is fixed. Therefore, the reduction in switching loss is insufficient. In recent years, research has been carried out to improve the electromagnetic interference (EMI) characteristics of a DPWM by reducing the DC-link current ripple or common mode voltage(CMV) [23], [24]. However, the results of studies on selecting an offset voltage for minimizing the loss of a TPFLI when the output current is unbalanced inadequate.

In this paper, first, we summarize the conventional 3D SVPWM and a CBPWM. We then show that the discontinuous 3D SVPWM can be easily implemented to the TPFLI by injecting the same offset voltage as that of the conventional DPWM of the TPTLI. Second, we demonstrate how to select a discontinuous phase according to the offset direction when a voltage reference vector is specified. To this end, we propose a carrier-based discontinuous PWM method suitable for a TPFLI, which minimizes the switching loss. The proposed PWM method has an optimal switching state according to the inverter output current and the same effect as the MLDPWM proposed in [25], when the current is balanced among three phases. In addition, it is simple to implement, and the lifespan of a PCS can be extended by preventing deterioration of a specific leg. The performance and validity of the proposed method is confirmed by simulation and experimental results.

## II. THREE-DIMENSIONAL SVPWM AND A CARRIER-BASED PWM METHOD

### A. THREE-DIMENSIONAL SVPWM (3D SVPWM)

The voltage reference for the 3D SVPWM is expressed in a 3D orthogonal $\alpha$-$\beta$-$\gamma$ coordinate. Therefore, the orthogonal coordinate transform from the $a$-$b$-$c$ coordinate system to the orthogonal $\alpha$-$\beta$-$\gamma$ coordinate system is expressed as

$$\begin{bmatrix} V_\alpha^* & V_\beta^* & V_\gamma^* \end{bmatrix}^T = C \begin{bmatrix} V_{af}^* & V_{bf}^* & V_{cf}^* \end{bmatrix}^T \tag{1}$$

where $V_\alpha$, $V_\beta$, and $V_\gamma$ are the $\alpha\beta\gamma$-axis voltage vectors, $V_{af}$, $V_{bf}$, and $V_{cf}$ are the $abc$-axis phase voltages respectively, and $^*$ denotes the reference value. The transformation matrix, $C$, is expressed as

$$C = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2}$$

The reference vector calculated from (1) and (2) is synthesized in the following steps:

1. Identification of the corresponding prism of the voltage reference vector
2. Identification of the corresponding tetrahedron of the voltage reference vector
3. On-time calculation of each switch using three active voltage vectors and two zero voltage vectors.

Sixteen switching vectors can be displayed on the hexagonal column as shown in Fig. 2(a). The $\gamma$-axis voltage vectors represent a zero-sequence voltage. The hexagonal column is divided into six prisms; each prism consists of six active voltage and two zero voltage vectors. For example, prism I consists of $V_1$, $V_{14}$, $V_8$, $V_9$, $V_{12}$, $V_{13}$, $V_0$, and $V_{15}$.

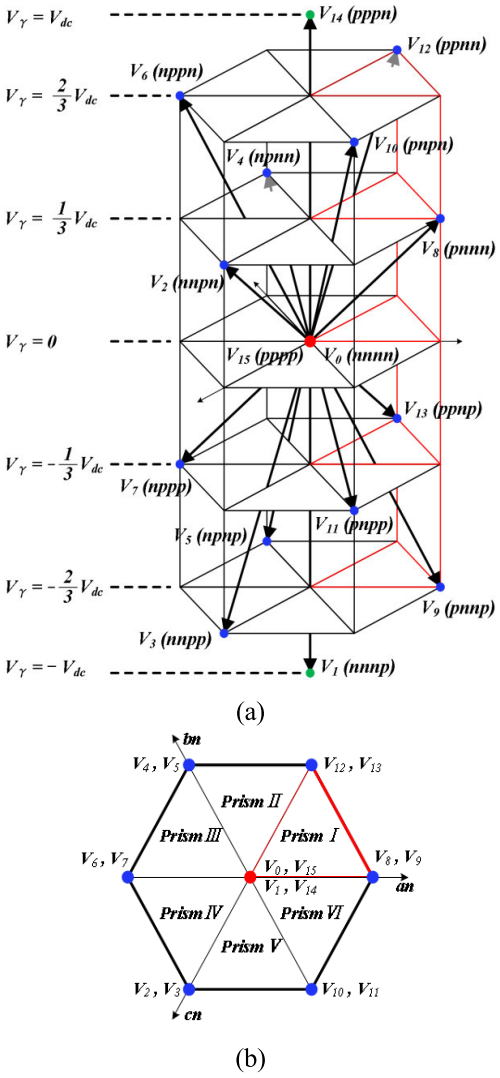



**FIGURE 2.** Sixteen switching vectors of a 3D SVPWM. (a) $\alpha$-$\beta$-$\gamma$ coordinate system. (b) vertical projection.

The corresponding prisms are identified by comparing the magnitudes of $V_{af}$, $V_{bf}$, and $V_{cf}$ in Table 1.

**TABLE 1.** Voltage condition according to prism.

| *Prism I* | *Prism II* | *Prism III* | *Prism IV* | *Prism V* | *Prism VI* |
|---|---|---|---|---|---|
| $V_{af} \geq V_{bf} \geq V_{cf}$ | $V_{bf} \geq V_{af} \geq V_{cf}$ | $V_{bf} \geq V_{cf} \geq V_{af}$ | $V_{cf} \geq V_{bf} \geq V_{af}$ | $V_{cf} \geq V_{af} \geq V_{bf}$ | $V_{af} \geq V_{cf} \geq V_{bf}$ |

The prism identification is the same with the sector identification of a 2D SVPWM. Figure 2(b) shows the vertical projection of the prism, which has the same shape as the 2D SVPWM, However, unlike in the 2D SVPWM, there are two active voltage vectors generating the same voltage reference. After the prism is identified, a tetrahedron with three active voltage vectors adjacent to the voltage reference vector should be identified among the four tetrahedrons. The tetrahedron can be identified by the polarities of $V_{af}$, $V_{bf}$, and $V_{cf}$ in Table 2. The four tetrahedrons of the prism can be seen in Fig. 3 as an example. Lastly, in order to calculate the gating time of the three active voltage vectors and two zero voltage vectors for the synthesis of the voltage reference vector, the voltage reference vector must be orthogonally projected on to each active voltage vector. The voltage reference vector is expressed as

$$V^* = d_{a1}V_{a1} + d_{a2}V_{a2} + d_{a3}V_{a3} \tag{3}$$

**TABLE 2.** Voltage polarity according to tetrahedron.

| | *Tetrahedron 1* | *Tetrahedron 2* | *Tetrahedron 3* | *Tetrahedron 4* |
|---|---|---|---|---|
| *Prism I* | $V_{af} \geq 0$<br>$V_{bf} \leq 0$<br>$V_{cf} \leq 0$ | $V_{af} \geq 0$<br>$V_{bf} \geq 0$<br>$V_{cf} \leq 0$ | $V_{af} \geq 0$<br>$V_{bf} \geq 0$<br>$V_{cf} \geq 0$ | $V_{af} \leq 0$<br>$V_{bf} \leq 0$<br>$V_{cf} \leq 0$ |
| *Prism II* | $V_{bf} \geq 0$<br>$V_{af} \leq 0$<br>$V_{cf} \leq 0$ | $V_{bf} \geq 0$<br>$V_{af} \geq 0$<br>$V_{cf} \leq 0$ | $V_{bf} \geq 0$<br>$V_{af} \geq 0$<br>$V_{cf} \geq 0$ | $V_{bf} \leq 0$<br>$V_{af} \leq 0$<br>$V_{cf} \leq 0$ |
| *Prism III* | $V_{bf} \geq 0$<br>$V_{cf} \leq 0$<br>$V_{af} \leq 0$ | $V_{bf} \geq 0$<br>$V_{cf} \geq 0$<br>$V_{af} \leq 0$ | $V_{bf} \geq 0$<br>$V_{cf} \geq 0$<br>$V_{af} \geq 0$ | $V_{bf} \leq 0$<br>$V_{cf} \leq 0$<br>$V_{af} \leq 0$ |
| *Prism IV* | $V_{cf} \geq 0$<br>$V_{bf} \leq 0$<br>$V_{af} \leq 0$ | $V_{cf} \geq 0$<br>$V_{bf} \leq 0$<br>$V_{af} \geq 0$ | $V_{cf} \geq 0$<br>$V_{bf} \leq 0$<br>$V_{af} \geq 0$ | $V_{cf} \leq 0$<br>$V_{bf} \leq 0$<br>$V_{af} \leq 0$ |
| *Prism V* | $V_{cf} \geq 0$<br>$V_{af} \leq 0$<br>$V_{bf} \leq 0$ | $V_{cf} \geq 0$<br>$V_{af} \geq 0$<br>$V_{bf} \leq 0$ | $V_{cf} \geq 0$<br>$V_{af} \geq 0$<br>$V_{bf} \geq 0$ | $V_{cf} \leq 0$<br>$V_{af} \leq 0$<br>$V_{bf} \leq 0$ |
| *Prism VI* | $V_{af} \geq 0$<br>$V_{cf} \leq 0$<br>$V_{bf} \leq 0$ | $V_{af} \geq 0$<br>$V_{cf} \geq 0$<br>$V_{bf} \leq 0$ | $V_{af} \geq 0$<br>$V_{cf} \geq 0$<br>$V_{bf} \geq 0$ | $V_{af} \leq 0$<br>$V_{cf} \leq 0$<br>$V_{bf} \leq 0$ |

where $V_{a1}$, $V_{a2}$, and $V_{a3}$ are adjacent active voltage vectors, and $d_{a1}$, $d_{a2}$, and $d_{a3}$ are the corresponding duty ratios of the active voltage vectors. The duty ratios are given by

$$\begin{bmatrix} d_{a1} \\ d_{a2} \\ d_{a3} \end{bmatrix} = \frac{1}{V_{dc}} P \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_\gamma^* \end{bmatrix} \tag{4}$$

$$d_z = 1 - (d_{a1} + d_{a2} + d_{a3}) \tag{5}$$

where $P$ is the projection matrix for projecting the voltage reference vector of the orthogonal coordinate system on to the active voltage vectors $V_{a1}$, $V_{a2}$, and $V_{a3}$. Since the projection matrix has different values for each prism and tetrahedron, it has a total of 24($6 \times 4$) matrix tables. Therefore, 3D SVPWM needs a lot of memory and is time consuming. The projection matrix P is described in Appendix B of [12].

### B. A CARRIER-BASED PWM METHOD (CBPWM)

The CBPWM generates an offset voltage based on the phase voltage reference, as shown in Fig. 4. The offset voltage, which is a zero-sequence voltage, is added to the phase voltage reference to generate the pole voltage reference defined

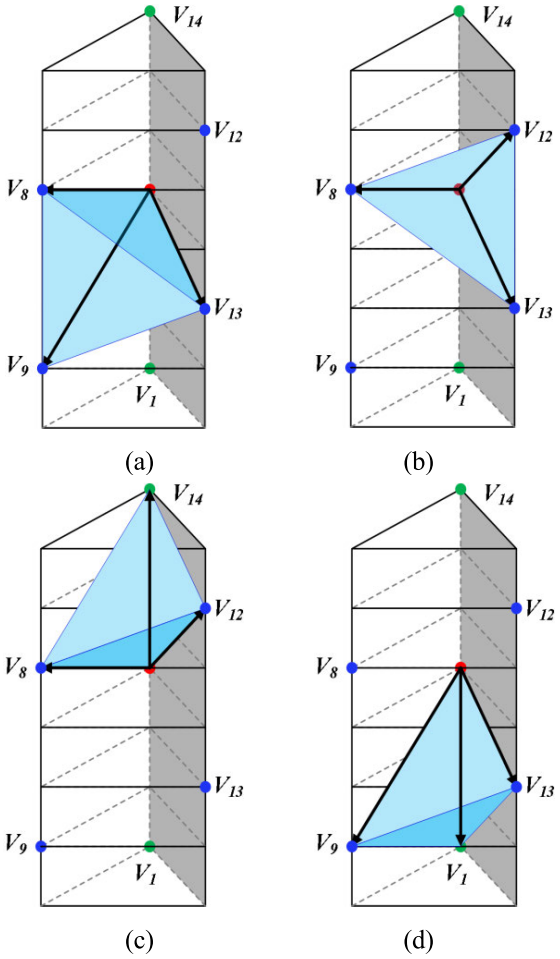



**FIGURE 3.** Identification of adjacent switching vectors. (a) Tetrahedron 1. (b) Tetrahedron 2. (c) Tetrahedron 3. (d) Tetrahedron 4.

by $V_{an}$, $V_{bn}$, $V_{cn}$ as

$$\begin{aligned} V_{an}^* &= V_{af}^* + V_{fn}^* \\ V_{bn}^* &= V_{bf}^* + V_{fn}^* \\ V_{cn}^* &= V_{cf}^* + V_{fn}^* \end{aligned} \tag{6}$$

In order to implement the symmetrically aligned-class **I** 3D SVPWM of [12], according to [17], the offset voltage is given by

$$V_{fn}^* = \begin{cases} -\dfrac{V_{max}}{2}, & V_{min} > 0 \\ -\dfrac{V_{min}}{2}, & V_{max} < 0 \\ -\dfrac{V_{max} + V_{min}}{2}, & Otherwise \end{cases} \tag{7}$$

$-V_{max}/2$ and $-V_{min}/2$ are the upper and lower limits, respectively. The actual offset voltage equation is the third term that is same with the offset voltage of 2D SVPWM. The PWM signals are then generated by comparing them with the triangular-carrier waveform. At this time, the maximum, medium, and minimum values are expressed as

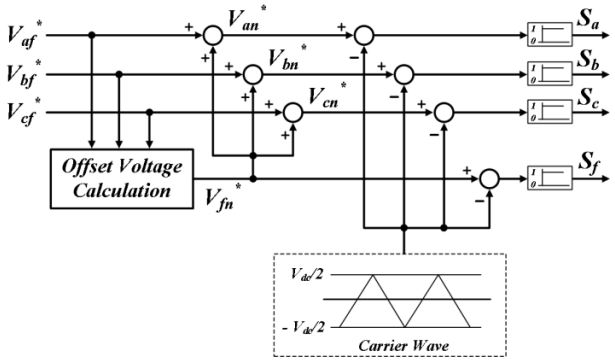



**FIGURE 4.** A carrier-based PWM for TPFLI.

$$V_{max} = max(V_{af}^*, V_{bf}^*, V_{cf}^*) \tag{8}$$

$$V_{mid} = mid(V_{af}^*, V_{bf}^*, V_{cf}^*) \tag{9}$$

$$V_{min} = min(V_{af}^*, V_{bf}^*, V_{cf}^*) \tag{10}$$

Therefore, unlike 3D SVPWM, CBPWM is easy to implement because of the simplicity of the offset voltage computation procedure.

As shown in (7), CBPWM generates the offset voltage by changing the phase voltage reference to its maximum, medium, and minimum values. This process is the same as finding the adjacent active voltage vector by identifying the prism and tetrahedron of the 3D SVPWM. Figure 5 shows the waveform of the phase voltage and the maximum, medium, and minimum values of the phase voltage. It can be seen that the prism and tetrahedron regions of 3D SVPWM can be identified according to the maximum, medium, and minimum values. Since Fig. 5 is a balanced three-phase circuit, tetrahedrons 4 and 5, which have a large zero-sequence voltage, are not shown.

The symmetrically aligned-class I 3D SVPWM of [12] has the advantage of low output voltage distortion and small current ripple since the switching state of each pole is located

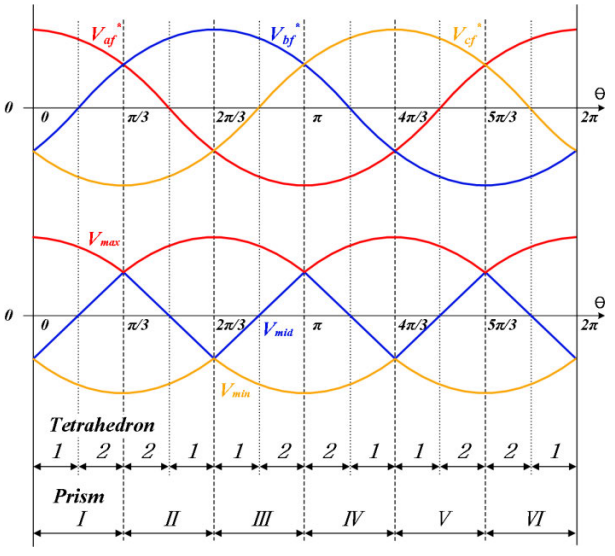



**FIGURE 5.** Prism and tetrahedron according to phase voltage reference.

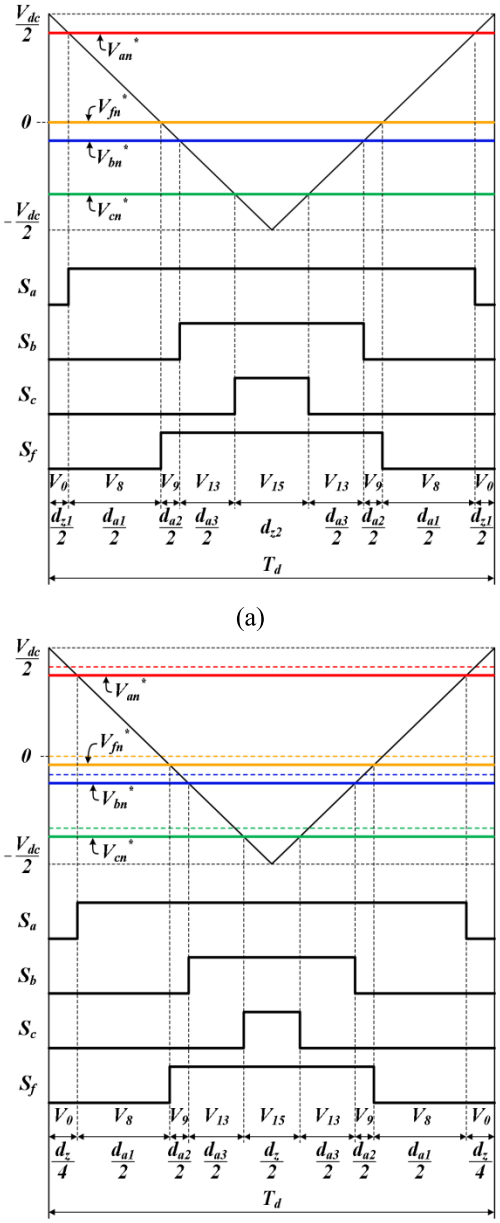



**FIGURE 6.** Switching state of CBPWM. (a) SPWM. (b) SVPWM.

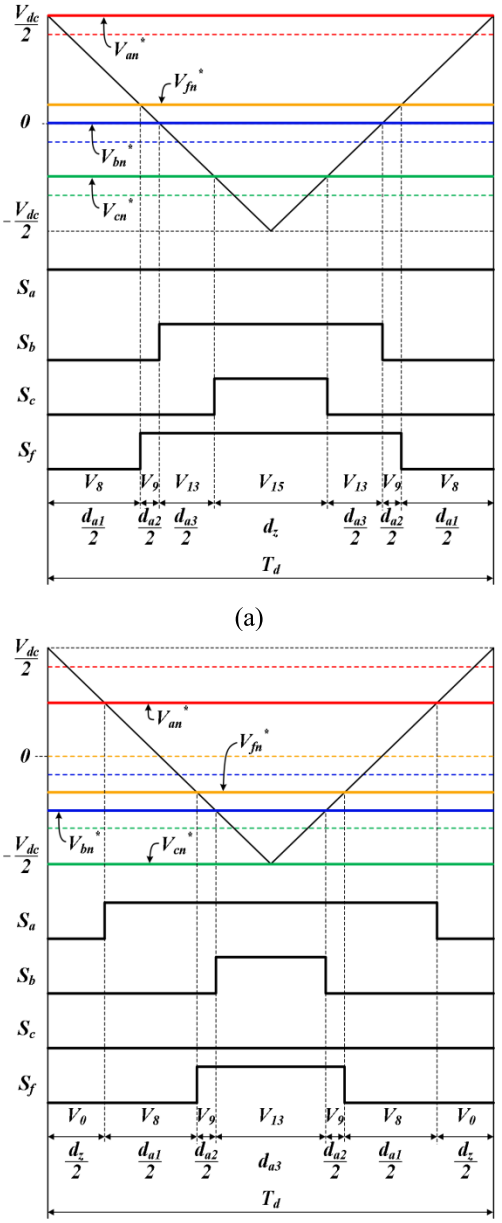



**FIGURE 7.** Switching state of CBPWM. (a) Upper-side offset. (b) Low-side offset.

at the center of the switching cycle. The principle of implementing the symmetrically aligned-class I 3D SVPWM using CBPWM can be seen in Fig. 6. The voltage reference vector in Fig. 6 is located in tetrahedron 1 in prism I. Figure 6(a) shows the switching state of sinusoidal PWM (SPWM) that is traditionally used in TPTLI. The gating times of zero voltage vectors $V_0$ and $V_{15}$ are $d_{Z1}$ and $d_{Z2}$, respectively. In order to implement the symmetrically aligned-class **I** 3D SVPWM using CBPWM, the gating time must be equalized by injecting the offset voltage

$$V_{max} + V_{fn}^* = -(V_{min} + V_{fn}{}^*) \tag{11}$$

This equation can also be written as (7), and the switching state is shown in Fig 6(b) [26], [27]. From the equation and the figure, the effect of offset voltage is the same for TPTLI and TPFLI. As a result, various modulation methods of TPTLI can be used for the TPFLI by using the same offset voltage. However, the conventional DPWM of a TPTLI is unsuitable for the TPFLI, because DPWM is a modulation method that assumes a balanced three-phase state.

## III. PROPOSED PER-PHASE MINIMUM-LOSS DPWM

The previous sections showed how various DPWMs can be implemented through the same offset voltage in a TPFLI. Figure 7 represents the DPWM switching state that can be implemented by the offset voltage. It has the same voltage reference vector as Fig. 6. Figure 7(a) shows that the switching state of phase $a$ is fixed to $p$ by an upper-side offset, and

Fig. 7(b) shows that the switching state of phase $c$ is fixed to $n$ by low-side offset. It means that there are two phases that can fix the switching state when a voltage reference vector is specified, and the phase with the higher current must be fixed to minimize the switching loss. Figure 7(a) has the same switching state as the symmetrically aligned class II 3D SVPWM in [12]. The state is implemented as follows

$$\begin{aligned} &if, \quad V_{max}+V_{min} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{max} \\ &if, \quad V_{max}+V_{min} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{min} \end{aligned} \tag{12}$$

The offset voltage in (12) is the same offset voltage as the conventional 60° DPWM [27]. Equation (12) fixes the switching state's upper side on tetrahedron 1 of each prism and the switching state's lower side on tetrahedron 2 of each prism. However, the effect of the 60° DPWM is high only when the power factor (PF) is 1.0. The other traditional DPWMs like the 60°(+30°) DPWM, 60°(−30°) DPWM, and 30° DPWM exhibit the effect only at a fixed PF. The offset voltages corresponding to the 60°(+30°) DPWM, 60°(−30°) DPWM, and 30° DPWM are calculated as follows:

$$\begin{aligned} &if, \quad V_{af}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{cf}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{cf}^{*} \\ if, \quad V_{cf}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{cf}^{*} \end{cases} \\ &if, \quad V_{bf}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{af}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{af}^{*} \\ if, \quad V_{af}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{af}^{*} \end{cases} \\ &if, \quad V_{cf}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{bf}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{bf}^{*} \\ if, \quad V_{bf}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{bf}^{*} \end{cases} \end{aligned} \tag{13}$$

$$\begin{aligned} &if, \quad V_{af}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{bf}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{bf}^{*} \\ if, \quad V_{bf}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{bf}^{*} \end{cases} \\ &if, \quad V_{bf}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{cf}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{cf}^{*} \\ if, \quad V_{cf}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{cf}^{*} \end{cases} \\ &if, \quad V_{cf}^{*} = V_{mid} \\ &\Rightarrow \begin{cases} if, \quad V_{af}^{*} \geq 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{af}^{*} \\ if, \quad V_{af}^{*} < 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{af}^{*} \end{cases} \\ &if, \quad V_{max}+V_{min} \geq 0 \Rightarrow V_{fn}^{*} = -\frac{V_{dc}}{2} - V_{min} \\ &if, \quad V_{max}+V_{min} < 0 \Rightarrow V_{fn}^{*} = \frac{V_{dc}}{2} - V_{max} \end{aligned} \tag{14, 15}$$

Equation (13) that is the offset voltage of 60°(+30°) DPWM fixes the switching state upper side on the odd prism and the switching state low side on the even prism. The others are the same principle. Fig. 8 shows the proposed minimum loss PWM method per phase (MLDPWM-PP). Since the magnitude of the instantaneous current is required to minimize the switching loss, it is necessary to detect the maximum, medium, and minimum values of phase current as

$$I_{max} = max(i_a, i_b, i_c) \tag{16}$$

$$I_{mid} = mid(i_a, i_b, i_c) \tag{17}$$

$$I_{min} = min(i_a, i_b, i_c) \tag{18}$$

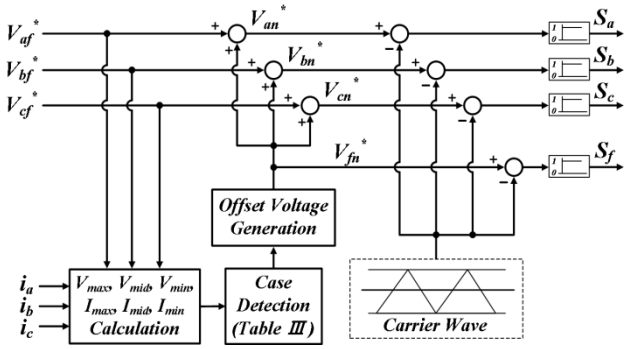



**FIGURE 8.** Proposed minimum-loss DPWM per phase (MLDPWM-PP).

where $i_a$, $i_b$, and $i_c$ are the instantaneous phase currents, and $I_{max}$, $I_{mid}$, and $I_{min}$ are the maximum, medium, and minimum values of phase current, respectively. The offset voltage is selected under the conditions shown in Table 3.

Table 3 comprises of three conditions. The voltage condition detects Vmid whereby the switching state is impossible to fix. Therefore, the phase voltage of Vmid is excluded from discontinuous switching. The current condition detects Imid for determining the higher phase current. The phase voltage concernings Imid is excluded from discontinuous switching. One phase voltage reference remains for minimizing the switching loss because Imid has the lowest absolute value. If the voltage and current conditions have the same phase, two phase voltage references remain. This implies that PF is near unity. In this case, the offset voltage equal to 60° DPWM of the equation (12) is selected. The polarity condition determines the offset direction.

The proposed method can be summarized as a process of selecting the optimal DPWM that can minimize for each switching cycle switching loss among the conventional 60°(+30°) DPWM, 60°(−30°) DPWM, and 30° DPWM.

The offset voltage generated in Table 3 produces an optimized and discontinuous switching state irrespective of the PF and, in the case of balanced three-phase, is the same as that produced by the MLDPWM proposed in [23]. Therefore, it is also applicable to TPTLI. The MLDPWM proposed in [23] follows a complex procedures; it detects the phase difference ($\phi$) between pole voltage and phase current in order to set the optimal discontinuous area, converts it into a phase angle ($\phi'$) for offset generation, and rotates the voltage

**TABLE 3.** Offset voltage calculation for proposed MLDPWM-PP.

| Case | Voltage | Current | Polarity | Offset Voltage |
|---|---|---|---|---|
| I | $V_{af} = V_{mid}$ | $I_a = I_{mid}$ | $I_{max} + I_{min} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{max}$ |
| | | | $I_{max} + I_{min} < 0$ | $V_{fn} = -V_{dc}/2 - V_{min}$ |
| II | $V_{af} = V_{mid}$ | $I_b = I_{mid}$ | $V_{cf} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{cf}$ |
| | | | $V_{cf} < 0$ | $V_{fn} = -V_{dc}/2 - V_{cf}$ |
| III | $V_{af} = V_{mid}$ | $I_c = I_{mid}$ | $V_{bf} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{bf}$ |
| | | | $V_{bf} < 0$ | $V_{fn} = -V_{dc}/2 - V_{bf}$ |
| IV | $V_{bf} = V_{mid}$ | $I_a = I_{mid}$ | $V_{cf} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{cf}$ |
| | | | $V_{cf} < 0$ | $V_{fn} = -V_{dc}/2 - V_{cf}$ |
| V | $V_{bf} = V_{mid}$ | $I_b = I_{mid}$ | $I_{max} + I_{min} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{max}$ |
| | | | $I_{max} + I_{min} < 0$ | $V_{fn} = -V_{dc}/2 - V_{min}$ |
| VI | $V_{bf} = V_{mid}$ | $I_c = I_{mid}$ | $V_{af} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{af}$ |
| | | | $V_{af} < 0$ | $V_{fn} = -V_{dc}/2 - V_{af}$ |
| VII | $V_{cf} = V_{mid}$ | $I_a = I_{mid}$ | $V_{bf} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{bf}$ |
| | | | $V_{bf} < 0$ | $V_{fn} = -V_{dc}/2 - V_{bf}$ |
| VIII | $V_{cf} = V_{mid}$ | $I_b = I_{mid}$ | $V_{af} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{af}$ |
| | | | $V_{af} < 0$ | $V_{fn} = -V_{dc}/2 - V_{af}$ |
| IX | $V_{cf} = V_{mid}$ | $I_c = I_{mid}$ | $I_{max} + I_{min} \geq 0$ | $V_{fn} = V_{dc}/2 - V_{max}$ |
| | | | $I_{max} + I_{min} < 0$ | $V_{fn} = -V_{dc}/2 - V_{min}$ |
| X | $V_{min} > 0$ | | | $V_{fn} = -V_{max}/2$ |
| | $V_{max} < 0$ | | | $V_{fn} = -V_{min}/2$ |

reference to generate the offset voltage. In addition, since it is a modulation method that assumes a balanced three-phase state, it cannot be applied to TPFLI. Furthermore, in the unbalanced condition, the conventional modulation method has a different deterioration rate because the phase current between the legs is different. The MLDPWM-PP proposed in this paper is simple to implement and has a short calculation time, and the deterioration between the legs can be matched similarly by reducing the switching loss of the leg with the largest current under the unbalanced condition.

## IV. CALCULATION OF INVERTER LOSS

### A. SWITCHING LOSSES OF SWITCH AND DIODE

In order to compare the effects of the conventional DPWM and the proposed MLDPWM-PP, it is necessary to calculate the switching and conduction losses. Figure 9 shows the switching state according to the current polarity of each leg and the loss due to the switching state change. The switching state and the current polarity help determine which one is conductive, the IGBT or the diode. However, regardless of the current polarity, one diode is turned on/off based on one leg in the switching cycle, and one IGBT is turned on/off as shown in Fig. 9(a). For example, when the current polarity is positive, the bottom diode ($D_L$) turns on/off and the top IGBT ($S_U$) turns on/off. Therefore, when calculating the switching loss of one leg, only the on/off loss of the IGBT and the on/off loss of the diode must be considered. At this point, the on loss of the diode is negligible

$$\Delta P_{SW} = \Delta P_{IGBT(on/off)} + \Delta P_{Diode(off)} \tag{19}$$

where $\Delta P_{SW}$ is the switching loss, $\Delta P_{IGBT(on/off)}$ is the switching loss of the IGBT, and $\Delta P_{Diode(off)}$ is the turn off loss of the diode in the switching cycle. Figure 9(b) shows the characteristics of the switch. If the rise time of current $i_{ce}$ flowing through the switch is $t_{ri}$ and the fall time of the gate-emitter voltage, $v_{ce}$, is $t_{fv}$ when turning on the switch, the slopes are expressed as

$$a_{ri} = \frac{I_{ce(datasheet)}}{t_{ri}}, \quad a_{fv} = \frac{V_{CC(datasheet)}}{t_{fv}} \tag{20}$$

$$a_{fi} = \frac{I_{ce(datasheet)}}{t_{fi}}, \quad a_{rv} = \frac{V_{CC(datasheet)}}{t_{rv}} \tag{21}$$

It can be calculated from IGBT's datasheet. Using (20) and (21), dissipation energy during on/off, $E_{s(on/off)}$, can be obtained as

$$\begin{aligned} E_{S(on/off)} &= E_{s(on)} + E_{s(off)} \\ &= k_i \cdot V_{dc} \cdot i_{ce}^2 + k_v \cdot V_{dc}^2 \cdot i_{ce} \end{aligned} \tag{22}$$

where

$$k_i = \frac{1}{a_{ri}} + \frac{1}{a_{fi}}, \quad k_v = \frac{1}{a_{rv}} + \frac{1}{a_{fv}} \tag{23}$$

The average switching loss for a period of the fundamental wave of the phase $a$ current can be obtained by integrating the half period as

$$\begin{aligned} P_{SW(IGBT)} = \frac{1}{\pi} \Bigg\{ &\int_0^{\frac{\pi}{2} - \frac{\delta a}{2}} \Delta P_{on/off(IGBT)} d\theta \\ &+ \int_{\frac{\pi}{2} + \frac{\delta a}{2}}^{\pi} \Delta P_{on/off(IGBT)} d\theta \Bigg\} \end{aligned} \tag{24}$$

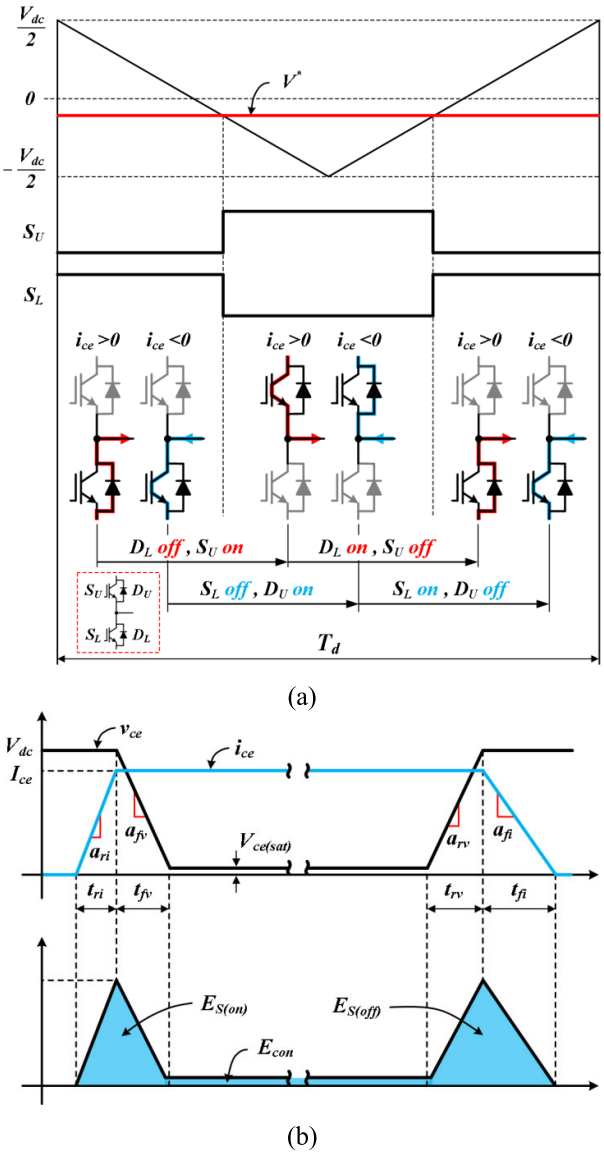



**FIGURE 9.** Switching loss calculation of each leg. (a) switching state according to current polarity. (b) switching characteristic.

where

$$\Delta P_{on/off(IGBT)} = f_{SW} \cdot E_{s(on/off)} \tag{25}$$

$$i_{ce} = I_a \cdot \sin\theta \tag{26}$$

$\delta_a$ is the discontinuous area of phase $a$. The diode's switching loss is calculated in the same way

$$\Delta P_{SW(Diode)} = f_{SW} \cdot E_{rr} \tag{27}$$

$$P_{SW(Diode)} = \frac{1}{\pi}\left\{\int_0^{\frac{\pi}{2}-\frac{\delta_a}{2}} \Delta P_{SW(Diode)} d\theta + \int_{\frac{\pi}{2}+\frac{\delta_a}{2}}^{\pi} \Delta P_{SW(diode)} d\theta\right\} \tag{28}$$

Other phases can be calculated in the same way. However, it is difficult to express discontinuous area of the proposed method since it is determined nonlinearly according to the current unbalance factor(CUF). Therefore, the validity of the proposed method is verified through experimental result and numerical analysis based on (24) and (28).

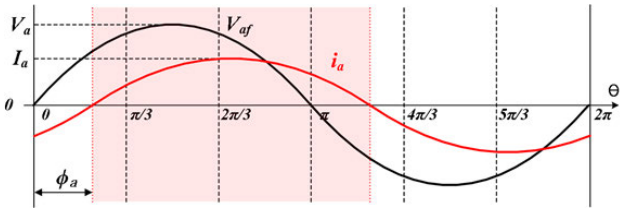



**FIGURE 10.** Conduction loss calculation area in phase a.

### B. CONDUCTION LOSSES OF SWITCH AND DIODE

When current polarity is positive, current flows through $S_U$ during the ON state and flows through $D_L$ during OFF state as shown in Fig. 9(a). Therefore, the conduction loss in the switching cycle can be expressed as

$$\Delta P_{CON(S)} = M \cdot V_{CE(sat)} \cdot i_a \tag{29}$$

$$\Delta P_{CON(D)} = (1 - M) \cdot V_{EC} \cdot i_a \tag{30}$$

$M$ is the modulation index, $V_{CE(sat)}$ is the collector emitter saturation voltage, $V_{EC}$ is the emitter collector voltage across the diode, and $\Delta P_{CON(S)}$ and $\Delta P_{CON(D)}$ are the conduction losses of the IGBT and the diode, respectively. $V_{CE(sat)}$, and $V_{EC}$ can be expressed as

$$V_{CE(sat)} = V_{TH(S)} + K_{CE} \cdot i_a \tag{31}$$

$$V_{EC} = V_{TH(D)} + K_{EC} \cdot i_a \tag{32}$$

The forward voltage drops across the IGBT and the diode are approximated by linear equations in (31) and (32). $M$ and $i_c$ can be expressed as

$$M = \frac{1}{2} + \frac{V_a}{V_{dc}} \cdot \sin\theta \tag{33}$$

$$i_a = I_a \cdot \sin(\theta - \emptyset_a) \tag{34}$$

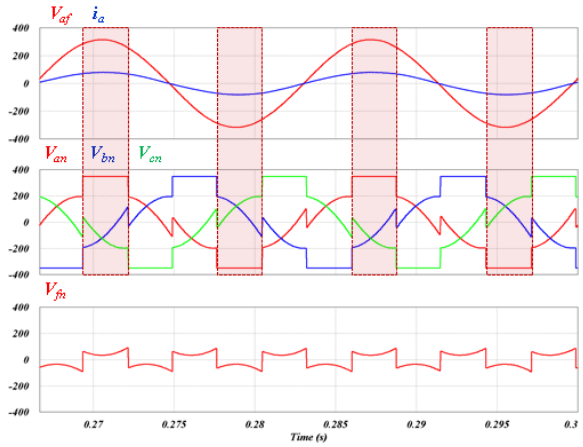
Because voltage and current waveforms have half-wave symmetry as shown in Fig. 10, the average conduction loss for a period of the fundamental wave of the phase $a$ current can be obtained by integrating the half period. The average conduction loss can be expressed as

$$P_{CON(S)} = \frac{1}{\pi}\int_{\emptyset_a}^{\pi+\emptyset_a} \Delta P_{CON(S)} d\theta \tag{35}$$

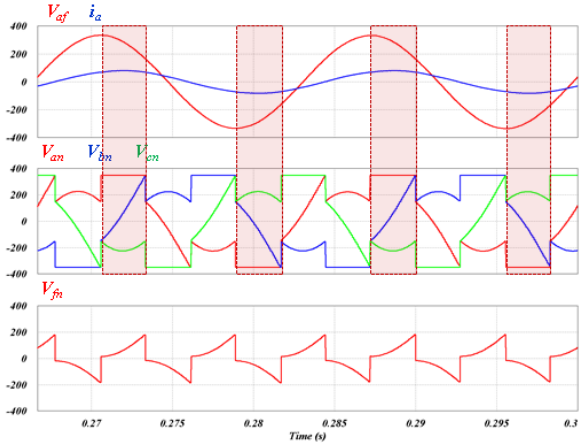
$$P_{CON(D)} = \frac{1}{\pi}\int_{\emptyset_a}^{\pi+\emptyset_a} \Delta P_{CON(D)} d\theta \tag{36}$$

By substituting (29) to (34) into (35) and (36), the average conduction loss of one leg is obtained as

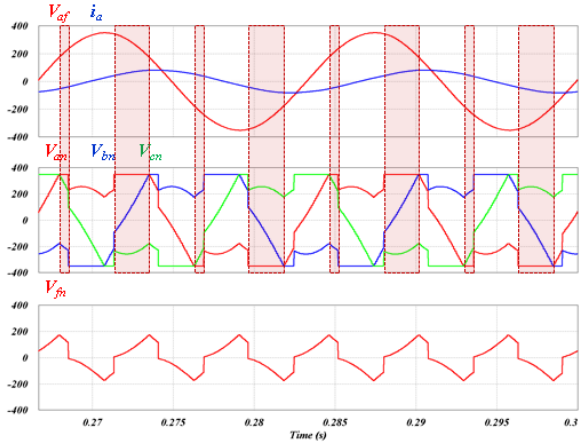
$$\begin{aligned} P_{CON} &= P_{CON(S)} + P_{CON(D)} \\ &= \frac{I_a}{\pi}\left(V_{TH(S)} + V_{TH(D)}\right) + \frac{1}{4}\left(K_{CE} + K_{EC}\right) \cdot I_a^2 \\ &\quad + \frac{V_a}{V_{dc}}\left(V_{TH(S)} - V_{TH(D)}\right) \cdot I_a \cdot \frac{1}{2}\cos\emptyset_a \\ &\quad + \frac{V_a}{V_{dc}}\left(K_{CE} + K_{EC}\right) \cdot I_a^2 \cdot \frac{4}{3\pi}\cos\emptyset_a \end{aligned} \tag{37}$$




(a)




(b)




(c)

**FIGURE 11.** Steady-state characteristics of MLDPWM-PP when balanced load. (a) $\phi = 0°$. (b) $\phi = 30°$. (c) $\phi = 70°$.

Other phases can be calculated in the same way. This calculation procedure was referenced from [25]. The loss calculation result will be discussed later with experimental results.

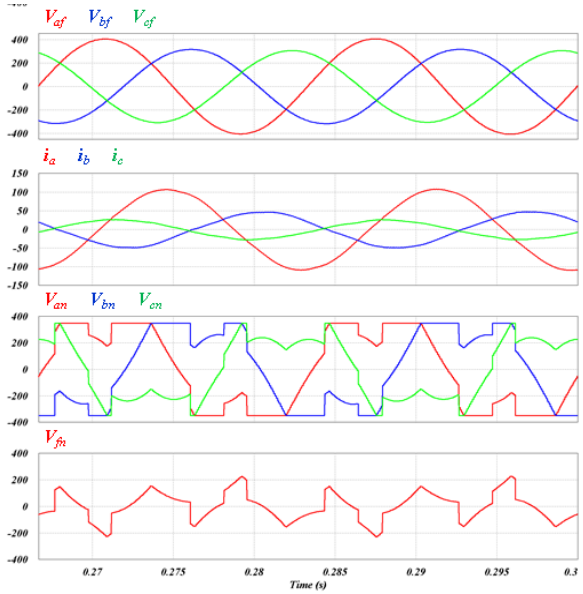



**FIGURE 12.** Steady-state characteristics of MLDPWM-PP when unbalanced load.

## V. SIMULATION RESULTS

To verify the proposed PWM method, the TPFLI of Fig. 1 was implemented using a PSIM simulation tool. The DC-link voltage was 700 V and the switching frequency ($f_{sw}$) was set to 6 kHz. The parameters of LC filter, $L_f$ and $C_f$, are 1.2 mH and 70 $\mu$F, respectively. The inductance of natural inductor, $L_s$, is the same as $L_f$. Figure 11 shows the pole voltage, phase current, and offset voltage waveforms using the proposed MLDPWM-PP when the balanced phase current. Figure 11(a) represents the situation where the phase difference is 0°. The switching state is fixed at the 60° area around the peak value of the current by generating the same offset voltage as the 60° DPWM. Figure 11(b) represents the situation where the phase difference is 30° and the offset voltage is the same as that of the 60°(+30°) DPWM. Figure 11(c) presents the situation where the phase difference is 70°. The discontinuous area is divided because the pole voltage could not be clamped around the peak value of the current. In this case, the generated offset voltage is the same as the conventional MLDPWM, so the MLDPWM-PP can be applied to the TPTLI. MLDPWM-PP is also much simpler to implement than the conventional method.

Figure 12 shows the voltage and current waveforms when the phase current is unbalanced. The phase voltage has unbalanced values due to the phase current. The simulation conditions are as follows: $i_a = 76.3\ \mathrm{A_{rms}}$, $i_b = 33.6\ \mathrm{A_{rms}}$, and $i_c = 18.6\ \mathrm{A_{rms}}$, and the phase differences in the order of a-b-c are 83°, 95°, 128°, respectively. Therefore, phase $a$ has the largest magnitude, whereas phase $c$ has the smallest.

Figure 13 shows the discontinuous area for each phase to analyze the pole voltage in Fig. 12. The discontinuous area of phase $a$ with the largest current magnitude is the widest.

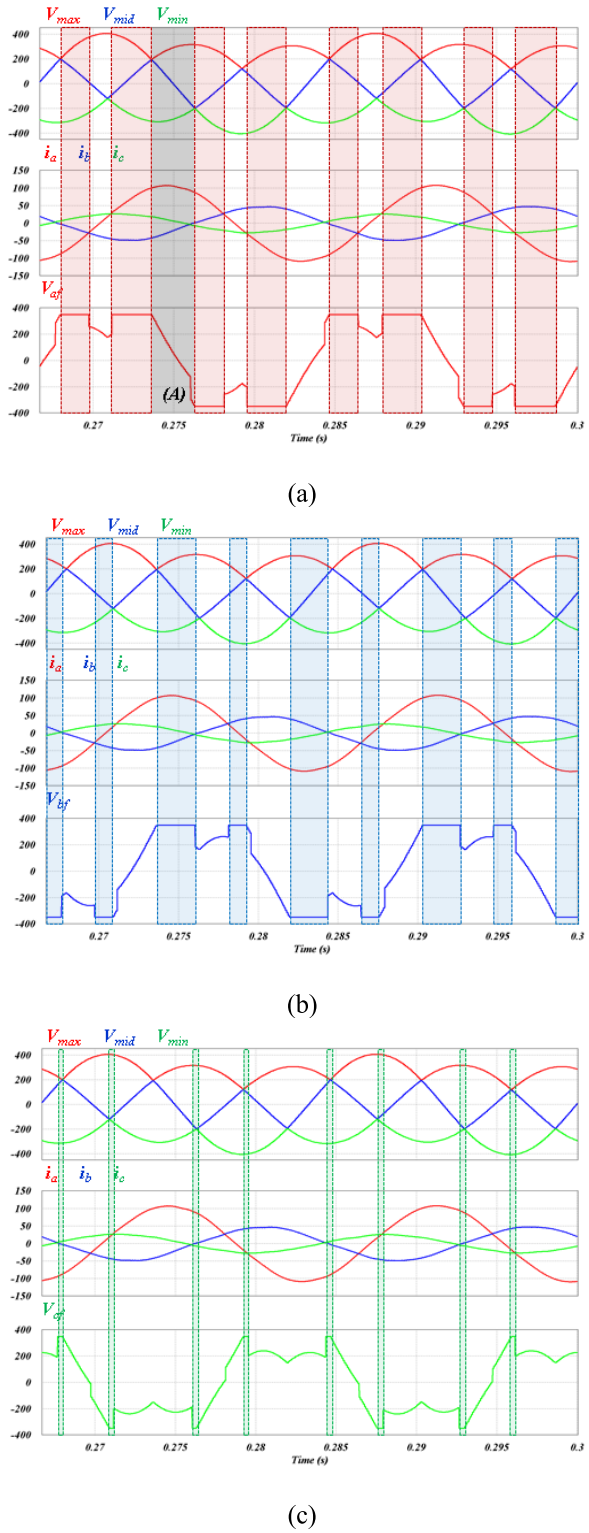



**FIGURE 13.** Discontinuous area according to phase when unbalanced load. (a) phase a. (b) phase b. (c) phase c.

However, even though the area (A) in Fig. 13(a) is the peak area of $i_a$, it is impossible to fix the switching state because $V_{an}$ has a medium value. So, in the area (A), $i_b$ and $i_c$ are compared to fix the switching state of the phase $b$ when $i_b$ is

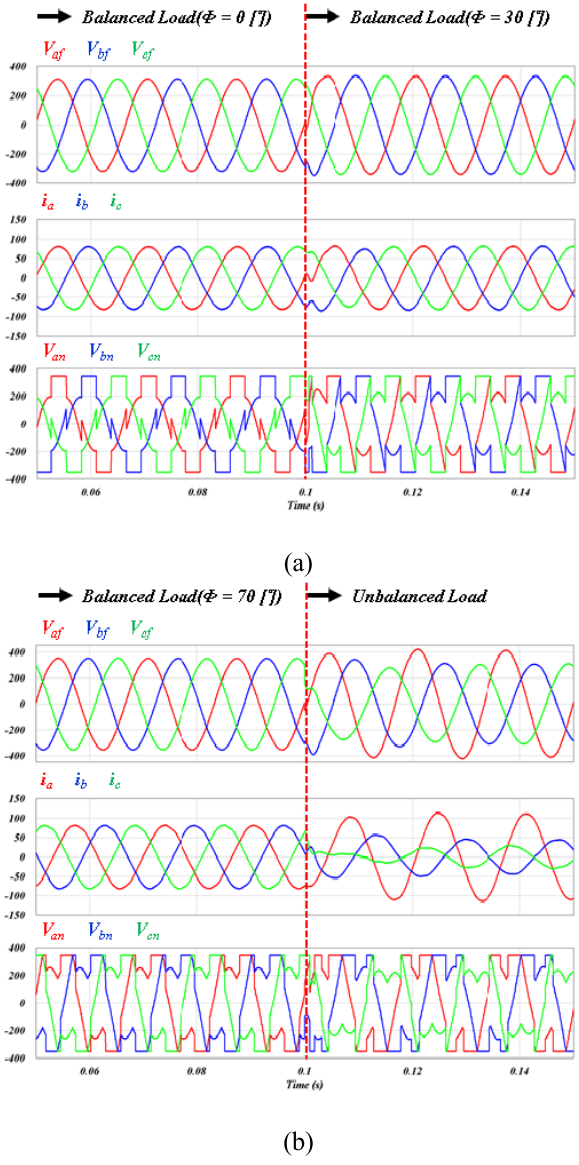



**FIGURE 14.** Transient characteristics of MLDPWM-PP. (a) balanced load($\phi = 0°$ to $\phi = 30°$). (b) balanced load($\phi = 70°$) to unbalanced load.

larger than $i_c$ or vice versa. Therefore, it can be confirmed that the proposed MLDPWM-PP selects an optimal offset voltage that minimizes switching loss under the corresponding conditions. Figure 14 represents the dynamic characteristics of the proposed MLDPWM-PP. In the figure, the fixed position of the switching state is changed seamlessly according to the current changes.

## VI. EXPERIMENTAL VALIDATION

Figure 15 shows the experimental setup of a TPFLI with a DSP(TMS320C28335) for the modulation method. Except for the DC-link voltage, i.e., 500 V, the parameters of the experimental stack were set to be the same as the simulation.

Figure 16 shows the phase a voltage and the three-phase current. The phase difference is close to 10° and the magni-

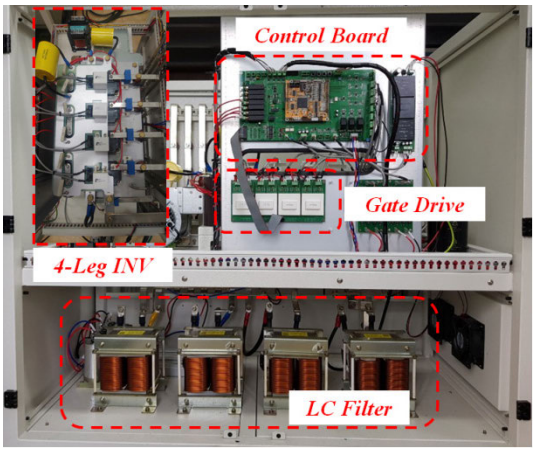



**FIGURE 15.** Experiment stack.

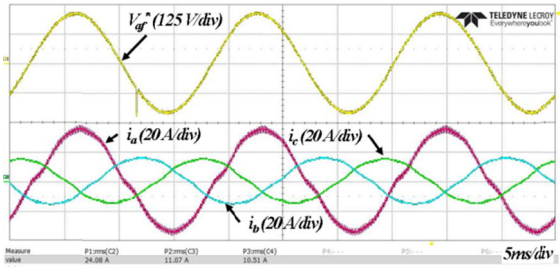


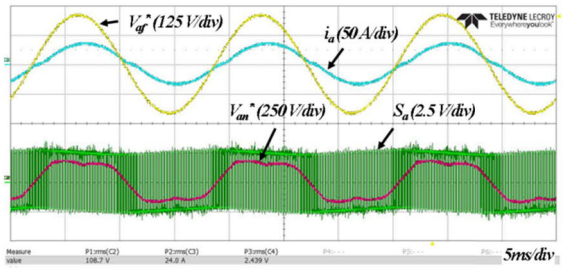

**FIGURE 16.** Unbalanced voltage and current.

tudes of $i_a$, $i_b$, and $i_c$ are 24.2 $A_{rms}$, 11.0 $A_{rms}$, and 10.5 $A_{rms}$, respectively. Further, load resistances of phases a, b, and c are 5.3 Ω, 12 Ω, and 12 Ω, respectively. The current unbalance factor (CUF) is calculated as

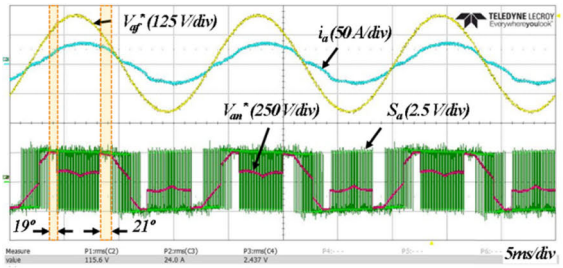
$$CUF = \frac{I_{max.abc} - I_{min.abc}}{I_{avg}} \tag{38}$$

where $I_{avg}$ is the average value of the phase currents, and $I_{max.abc}$ and $I_{min.abc}$ are the maximum and minimum values of the phase currents, respectively. The RMS values are used for calculating of CUF, not instantaneous values. The CUF is 0.9 in Fig. 16. Figure 17 shows the phase and pole voltages, current, and PWM signal of phase a. The conventional 3D SVPWM in Fig. 17(a) performs continuous switching every switching cycle, whereas the 60° DPWM in Fig. 17(b) and the 30° DPWM in Fig. 17(c) perform discontinuous switching. However, due to the unbalanced phase voltage, the discontinuous area is changed from 30° to 19° and 21° in the 30° DPWM and from 60° to 81° in the 60° DPWM. The 30° DPWM has a narrower discontinuous area with the largest phase current. Therefore, the 30° DPWM is not suitable for TPFLI. In the case of the 60° DPWM, the discontinuous area is wider with the largest phase current, but the effect will decrease if the phase difference is changed.

Figure 17(d) illustrates the waveforms of the proposed MLDPWM-PP. The MLDPWM-PP has the widest discontinuous area. A more detailed discontinuous area can be observed in Fig. 18. Figure 18(a), (b), and (c) depict the




(a)

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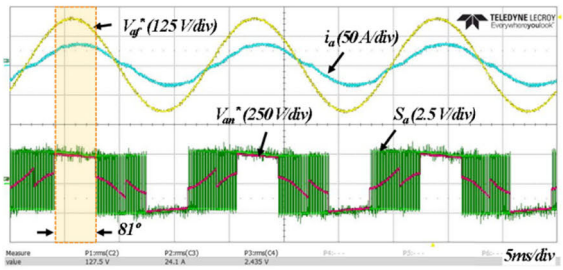
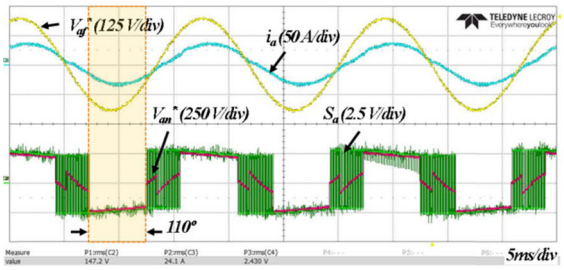



(c)




(d)

**FIGURE 17.** Voltage, current, and PWM signal of phase a. (a) SVPWM. (b) 30° DPWM. (c) 60° DPWM. (d) proposed MLDPWM-PP.

discontinuous areas of phases a, b, and c of MLDPWM-PP, respectively. In the figures, the discontinuous phase is decided where the absolute value of the phase current becomes the maximum value. Figure 19 represents the loss improvement ratio (LIR) according to CUF. The loss improvement ratio is expressed as

$$LIR = \frac{P_{Loss(SV)} - P_{Loss(D)}}{P_{Loss(SV)}} \tag{39}$$

where $P_{Loss(SV)}$ and $P_{Loss(D)}$ are the inverter losses when using the 3D SVPWM and the DPWM, respectively.

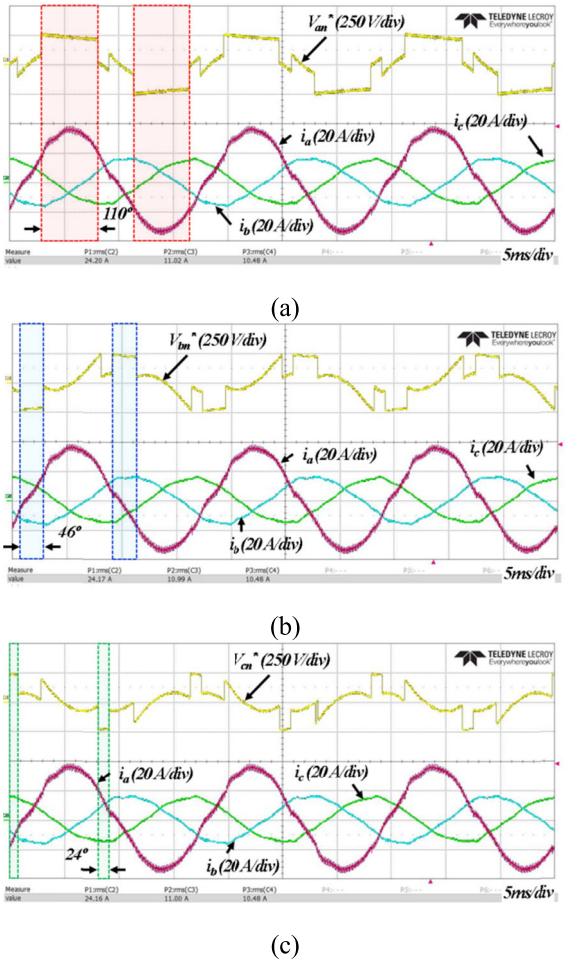



**FIGURE 18.** Discontinuous area of each phase in proposed MLDPWM-PP. (a) phase a. (b) phase b. (c) phase c.

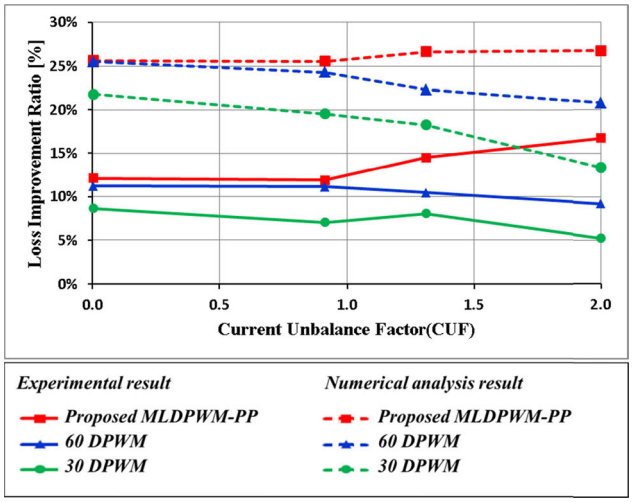



**FIGURE 19.** Experiment stack.

To change the CUF, phase a was fixed to 24 $A_{rms}$, whereas the other phase was reduced. The experimental results are indicated by solid lines, and the numerical analysis results by

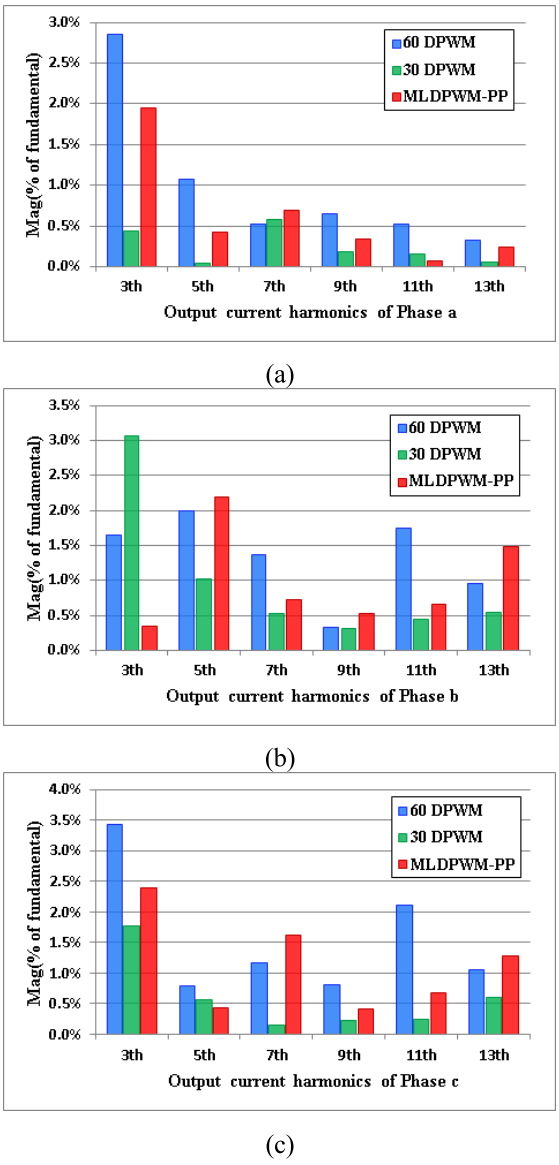



**FIGURE 20.** Output current harmonics in the unbalance situation. (a) phase a. (b) phase b. (c) phase c.

dashed lines. The numerical analysis results are better than the experimental results, because the former only considered the switching loss and conduction loss. However, the trend between the two is similar. As a result, in Fig. 19, the 30° and 60° DPWMs decrease the LIR as the CUF increases. However, the MLDPWM-PP increases the LIR as the CUF increases.

Figure 20 illustrate output current harmonics under the same current condition as in Fig. 16. The harmonics of each phase output current are different owing to the voltage unbalance. For phase a, 30° DPWM has the lowest harmonics while 60° DPWM has the highest harmonics except for $7^{th}$ and $11^{th}$ order harmonics. However, 30° DPWM has the most $3^{rd}$ order harmonics in phase b. Generally, the harmonics of

MLDPWM-PP are higher than those of 30° DPWM, whereas they are lower than those of 60° DPWM. From the result, MLDPWM-PP does not have a significant adverse effect on the THD of the output current when compared with the conventional DPWM.

From a simulation and an experimental result, the MLDPWM-PP is suitable for TPFLI more than the conventional DPWMs.

## VII. CONCLUSION

In this study, the conventional 3D SVPWM and CBPWM were summarized. We demonstrated the applicability of the DPWM offset voltage of the conventional TPTLI to the TPFLI. Through this, we proposed a DPWM to minimize the switching loss for a TPFLI. Furthermore, to compare the effects of the conventional DPWM and the proposed MLDPWM-PP, the switching and conduction losses were calculated. The MLDPWM-PP increased the inverter efficiency by selecting the offset voltage that minimized the switching loss, considering the magnitude and phase difference of phase current in the TPFLI. In addition, it can be applied to TPTLI as well, MLDPWM-PP is simple to implement. It can extend the service life of a switch. To verify the validity of the MLDPWM-PP, a simulation and an experiment were carried out. We confirmed that the effectiveness of the proposed method (in the form of LIR) increased by 6 – 7 % when compared with the 60° DPWM and by approximately 11 – 13 % when compared with the 30° DPWM under the experimental conditions wherein the CUF as 2.0. If the CUF or output current increased further, the effectiveness of the MLDPWM-PP will increase.

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