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FPGA-Based Digital Lock-in Amplifier With High-Precision Automatic Frequency Tracking

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ABSTRACT Aiming to overcome the problem of the frequency error between the reference signal and the measured signal in an analog lock-in amplifier, this paper presented a digital lock-in amplifier (DLIA) with accurate frequency automatic tracking to improve its performance. In this paper, a modular design approach based on DSP Builder was employed to develop a quadrature vector type lock-in amplifier with automatic frequency tracking. A reference signal generator with high-frequency resolution and a digital filter with good performance were implemented. The performance of the design was tested by determining the linearity, the Q value, and the noise immunity of the DLIA. The experimental results showed that the proposed DLIA has good linearity and the Q value can reach up to 82. The relative errors of the signals with amplitudes greater than 10 mV were less than 1% when the equivalent input was a sine wave signal with a frequency of 1 kHz and an amplitude of 500 mV. When the superimposed noise was less than or equal to 400 mV, the relative error was less than 2% in the same condition. The proposed DLIA has higher precision and efficient noise immunity.

INDEX TERMS Automatic frequency tracking, digital lock-in amplifier, weak signal detection, DSP builder.

I. INTRODUCTION

The detection of weak signals under complex background noise is a cutting-edge technology in scientific research, geological exploration, biomedical science, military, aerospace, and other fields [1]–[3]. Relevant scholars have done a lot of fruitful research in this key field and proposed a variety of detection methods, from the detection methods of linear theory such as the conventional time domain, frequency domain, and time-frequency domain, to the detection methods of nonlinear theory such as chaos and stochastic resonance [4]–[6]. Lock-in amplifier is a mature solution with strong detection ability and high reliability in many weak signal detection schemes [7], [8].

After years of development, general-purpose lock-in amplifiers have matured, and many companies have excellent performance related products [9], [10]. At present, a large amount of relevant research is mainly focused on a dedicated lock-in amplifier, which is applied as a module in a specific research field [11], [12]. One of the key factors affecting the measurement accuracy of the lock-in amplifier is the frequency error between the measured signal and the reference signal. An automatic frequency tracking digital lock-in amplifier (DLIA) was designed based on LabVIEW [13]. The design uses FFT to realize automatic frequency tracking, which effectively reduces the frequency mismatch of the measured signal and the reference signal. However, there are some problems with the FFT frequency tracking method. Due to the fence effect of the FFT, this method can only capture some discrete frequencies, and the accuracy of frequency tracking is limited. Increasing the number of sampling points can improve the accuracy of frequency tracking, but it greatly increases the amount of computation.

Aiming at the problem of the frequency error between the reference signal and the measured signal, scholars have proposed a number of methods for automatic frequency tracking.

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However, some problems have still existed, such as how to maintain high precision, how to measure continuously in real time, etc. These are the keys to improve the performance of DLIAs and have an extensive application space and significance prospect.

Aiming to solve the aforementioned problems, this paper proposes a DLIA with high-precision frequency automatic tracking capability, and applies it as a module to the electromagnetic exploration devices. The highlights of this study consist of the following points:

1) A DLIA with automatic frequency tracking ability is designed based on the DSP Builder, which synchronize the frequency of the reference signal and the measured signal;

2) A high-frequency resolution reference signal generator and a high-order digital low-pass filter are designed to improve the measurement accuracy and the noise immunity of the DLIA;

3) The proposed DLIA shows superiority than the analog lock-in amplifier (ALIA) in a noisy environment.

II. METHODOLOGY

A. PRINCIPLE OF LOCK-IN AMPLIFIER

The lock-in amplifier is based on the fact that measured signal is not correlated with noise [14], [15]. First, the measured and the reference signal are multiplied to achieve spectrum shifting. Then, the noise is filtered by low pass filter to obtain a DC signal proportional to the amplitude of the measured signal. Fig. 1 shows the structure of the most common single channel lock-in amplifier.

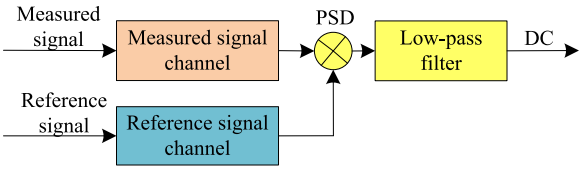

FIGURE 1. Single channel lock-in amplifier.

As one of the most basic structural forms, the single channel lock-in amplifier mainly includes a measured signal channel, a reference signal channel, and a phase sensitive detector (PSD). Among them, the phase sensitive detector is the core of the lock-in amplifier, which mainly includes a multiplier and a low-pass filter.

Let the measured signal be $x(t) = A\sin(2\pi f_1 t + \theta_1) + n(t)$ and the reference signal be $r(t) = B\sin(2\pi f_2 t + \theta_2)$, where A is the amplitude of the measured signal, B is the amplitude of the reference signal, f_1 and f_2 are the frequency of the measured signal and the reference signal respectively, θ_1 and θ_2 are the initial phase of the measured signal and the reference signal respectively, and $n(t)$ is noise. The result of multiplication of the measured signal and the reference signal is:

$$\begin{aligned} x(t) \bullet r(t) &= [A\sin(2\pi f_1 t + \theta_1) + n(t)] \bullet [B\sin(2\pi f_2 t + \theta_2)] \\ &= n(t) \bullet r(t) + \frac{AB}{2}\cos[2\pi(f_1 - f_2)t + (\theta_1 - \theta_2)] \\ &\quad + \frac{AB}{2}\cos[2\pi(f_1 + f_2)t + (\theta_1 + \theta_2)] \end{aligned} \tag{1}$$

The above multiplication result is filtered by the low-pass filter of the phase sensitive detector to filter out the high frequency signal. The result is:

$$V(t) = \frac{AB}{2}\cos[2\pi(f_1 - f_2)t + (\theta_1 - \theta_2)] + n'(t) \tag{2}$$

Obviously, the smaller the frequency difference $f_1 - f_2$ and the residual noise $n'(t)$, the more accurate the signal. When the frequency error between the measured signal and the reference signal can be ignored, that is $f_1 - f_2 = 0$, and $V(t)$ becomes a DC signal mixed with some residual noise. When the phase difference between the two signals is a specific value, the value of cos (θ_1- θ_2) is also constant. When the bandwidth of the low-pass filter is very narrow, the residual noise is also very weak.

According to the above analysis, it can be known that the lock-in amplifier needs three conditions to obtain a more accurate value: 1) The phase difference θ_1- θ_2 between the measured signal and the reference signal is a specific value; 2) The reference signal is at the same frequency as the measured signal, that is $f_1 - f_2 = 0$; 3) The bandwidth of the low pass filter is narrow enough to ensure that the residual noise approaches zero.

B. QUADRATURE VECTOR TYPE LOCK-IN AMPLIFIER

The digital lock-in amplifier works similarly to the analog lock-in amplifier, except that its multiplier and low-pass filter are implemented digitally, overcoming the nonlinearity and drift of the analog device [16], [17]. The quadrature vector type lock-in amplifier overcomes the influence of phase difference from the structure, avoiding the cumbersome and inefficient shifting process. Fig. 2 shows the schematic of the quadrature vector type digital lock-in amplifier used in the design.

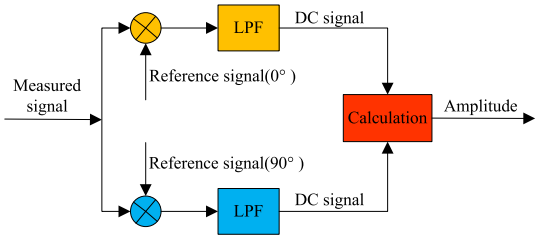

FIGURE 2. Quadrature vector type digital lock-in amplifier.

Let the measured signal be: $x(t) = A\sin(2\pi f t + \theta) + n(t)$, where A is the amplitude of the signal, f is the frequency of the signal, θ is the initial phase of the signal, and $n(t)$ is noise. The signal is discretized at the sampling frequency f_s, and the measured signal sequence is $x(k) = A\sin(2\pi k/N + \theta) + n(kt_s)$. Among them, the sampling frequency is $f_s = Nf$, and the sampling interval is $t_s = 1/(Nf)$. The two quadrature reference signal sequences generated by the internal digital signal generator are $r_1(k) = B\sin(2\pi k/N)$ and $r_2(k) = B\cos(2\pi k/N)$ respectively, where B is the amplitude of the reference signal.

The measured signal and the reference signal are multiplied in the multiplier to complete the frequency spectrum

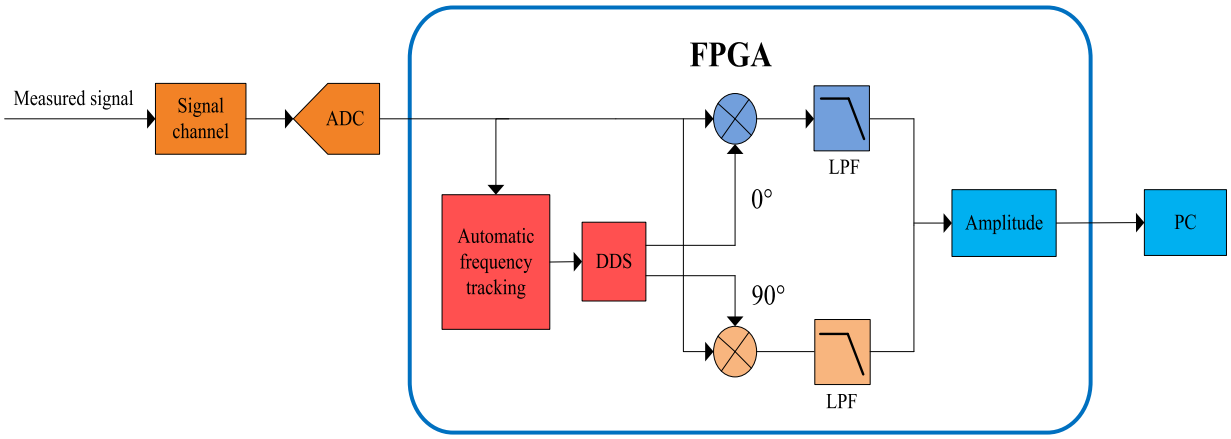

FIGURE 3. Structure of automatic frequency tracking digital lock-in amplifier.

shift, and the output result is a difference frequency term (DC signal) and a sum frequency term (double frequency signal). The outputs of the two multipliers are:

$$\begin{aligned} R_1(k) &= [A\sin(\frac{2\pi k}{N}+\theta)+n(kt_s)]\bullet[B\sin(\frac{2\pi k}{N})] \\ &= AB\sin(\frac{2\pi k}{N}+\theta)\bullet\sin(\frac{2\pi k}{N})+B\sin(\frac{2\pi k}{N})\bullet n(kt_s) \\ &= \frac{AB}{2}[\cos\theta-\cos(\frac{4\pi k}{N}+\theta)]+B\sin(\frac{2\pi k}{N})\bullet n(kt_s) \end{aligned} \tag{3}$$

$$\begin{aligned} R_2(k) &= [A\sin(\frac{2\pi k}{N}+\theta)+n(kt_s)]\bullet[B\cos(\frac{2\pi k}{N})] \\ &= AB\sin(\frac{2\pi k}{N}+\theta)\bullet\cos(\frac{2\pi k}{N})+B\cos(\frac{2\pi k}{N})\bullet n(kt_s) \\ &= \frac{AB}{2}[\sin\theta+\sin(\frac{4\pi k}{N}+\theta)]+B\cos(\frac{2\pi k}{N})\bullet n(kt_s) \end{aligned} \tag{4}$$

In the two multipliers, the noise is also multiplied by the reference signal, and the result is almost always an alternating signal. In digital lock-in amplifiers, the passband of the low-pass filter can be very narrow to ensure that almost the double frequency signal and noise are completely filtered out, leaving only the DC signal. The two DC signals are:

$$U_1 = \frac{AB}{2}\cos\theta \tag{5}$$

$$U_2 = \frac{AB}{2}\sin\theta \tag{6}$$

Under ideal conditions, after passing through the digital low-pass filter, the noise is completely filtered out, leaving only two DC signals related to the initial phase. The amplitude of the signal can be obtained by the following operation.

$$A = \frac{2}{B}\sqrt{U_1^2+U_2^2} \tag{7}$$

It can be seen from the above analysis that the quadrature vector type digital lock-in amplifier not only eliminates the influence of phase difference from the structure, but also improves the system's ability to suppress uncorrelated noise, and improves the accuracy and anti-interference of the lock-in amplifier.

III. DESIGN OF AUTOMATIC FREQUENCY TRACKING DIGITAL LOCK-IN AMPLIFIER

In order to improve the accuracy and anti-interference of the digital lock-in amplifier and overcome the influence of the frequency error between the measured signal and the reference signal, the quadrature vector type digital lock-in amplifier designed in this paper combines the automatic frequency tracking technology to reduce the frequency error. The system adopts FFT phase-locked loop module with automatic frequency tracking to overcome the barrier effect limitation of simple FFT tracking and achieve more accurate frequency tracking. A high frequency resolution reference signal generator and a high performance digital filter are designed to improve the accuracy and anti-interference ability of the digital lock-in amplifier. Its system structure is shown in Fig. 3.

The signal to be measured is directly digitally sampled after passing through the conditioning circuit of the signal channel, and the automatic frequency tracking module accurately tracks the frequency of the measured signal to generate a quadrature reference signal without frequency error. Then, the measured signal and the reference signal are multiplied to complete the frequency mixing, and the AC signal is filtered by the digital low-pass filter. Finally, calculating the amplitude of the measured signal makes high-precision weak signal detection in the noise a reality. In this design, the core module of the digital lock-in amplifier is designed with Altera's DSP Builder development tools, which greatly reduces the difficulty of program development, making the design intuitive and simplified.

A. DESIGN OF AUTOMAIC FREQUENCY TRACKING MODULE

One of the important factors determining the performance of a lock-in amplifier is the frequency error between the measured signal and the reference signal [18], [19]. Regardless of the internal or external excitation mode, there is error and jitter in

the frequency of the modulator output usually, which causes the frequency of the measured signal and the reference signal to be inconsistent. At present, the automatic frequency tracking method applied in the digital lock-in amplifier mostly adopts the FFT transform [20], and after performing fast Fourier transform on the discrete data, the frequency of the measured signal is obtained according to the frequency amplitude feature. However, due to the fence effect of the FFT, this method can only capture the frequency roughly, and the frequency between the FFT frequency lines cannot be tracked. This method has certain defects.

For the FFT, the interval between adjacent frequency lines is $df = f_s/N = 1/(N^*T_s)$, where f_s is the sampling frequency, and $T_s = 1/f_s$. The spacing of the frequency lines determines the frequency resolution of FFT. When the spacing is large, useful information is lost due to the fence effect. When the sampling rate is constant, the spacing can be reduced by increasing the number of sampling points. However, this method increases the number of sampling points, resulting in a large increase in the amount of calculation.

Therefore, this paper designs an FFT phase-locked loop module with frequency adaptive tracking to achieve high-precision frequency tracking. When the FFT roughly calculates the frequency of the measured signal, the phase-locked loop searches for the true frequency with the rough frequency as the center frequency. The structure of automatic frequency tracking module is shown in Fig. 4.

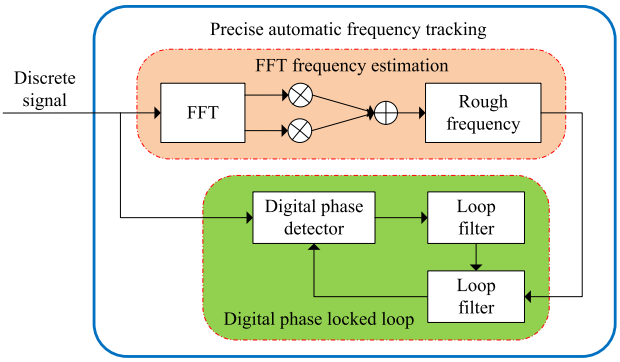

FIGURE 4. Structure of high precision automatic frequency tracking module.

First, the measured signal enters the FFT frequency estimation module, which performs fast Fourier transform on the measured signal, and the highest amplitude among the transformed frequency lines is the frequency position. Then, the frequency position is converted into a rough frequency by constant multiplication. The phase-locked loop scans the measured signal with the rough frequency as the center frequency, that is, searches the actual frequency near the estimated frequency until the local reference signal and the external measured signal complete the frequency synchronization.

For the above frequency tracking module, the subject of frequency tracking is the digital phase-locked loop. After the signal is synchronized, a high quality sine and cosine reference signal is provided to the system by the internal DDS (Direct Digital Synthesizer) signal generator. The FFT frequency estimation module continuously modifies the center frequency of the phase-locked loop as the frequency of the external measured signal changes, so that the frequency of the external measured signal is always within the capture bandwidth of the phase-locked loop.

B. DESIGN OF QUADRATURE REFERENCE SIGNAL GENERATOR

In the analog lock-in amplifier, in order to prevent the amplitude drift of the reference signal from reducing the output precision of the lock-in amplifier, the square wave is used as the reference signal to realize the switching phase sensitive detection. In the digital lock-in amplifier, there is no problem of amplitude drift. The advantage of using square wave as the reference signal is not obvious, but the output noise is increased due to the influence of its harmonics. If square wave is used as the reference signal in the digital lock-in amplifier, the subtracted frequency signal of the harmonic will appear in the output. The noise appears not only at $\omega_n = \omega_0$, but also near $\omega_n = (2n-1)\omega_0$, $(n = 1, 2, 3, \ldots)$, and the amplitude drops by $1/(2n-1)$, which is called the harmonic response of PSD. Therefore, the sine wave is selected as the reference signal in the digital lock-in amplifier.

The local quadrature reference signal is generated by DDS. According to the Fourier transform theorem, any periodic signal that satisfies the Dirichlet condition can be decomposed into a series of sine or cosine signals. Based on this feature, DDS generates the reference signals required by the system. In the design, DDS model is designed by Altera's development tool DSP Builder. The quadrature signal generator model is shown in Fig. 5.

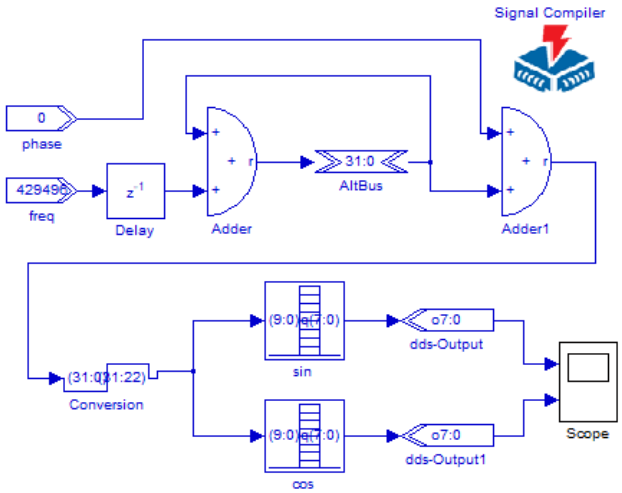

FIGURE 5. Quadrature signal generator model.

The local reference generator model has two constant inputs and two waveform outputs. The two constant inputs are frequency control word (*freq*) and phase control word (*phase*); two waveform outputs are sine wave and cosine wave output respectively, and the two waveforms have a

phase difference of 90°. In the model, *Adder* and *Adder1* form a phase accumulator and a phase modulator. Sin and cos are two ROM tables whose parameter settings are 127*sin([0:2*π/(2^10):2*π]) and 127*cos([0:2*π/(2 ^10):2*π]). To achieve higher frequency resolution, the *freq* of the DDS module is set to 32 bits, that is, the phase accumulator word length is 32 bits. The frequency resolution of the DDS output waveform is f_{clk}/2^32, where f_{clk} is the operating frequency of the signal generator. It can be seen that the local quadrature reference signal generator has a higher frequency resolution and meets the design requirements of the system.

In order to verify the feasibility of the local quadrature reference signal model, the system-level functional simulation is directly performed after the DDS model is established in Simulink. Here, the output waveform is set to a quadrature reference signal of 1 kHz, and the simulation result is shown in Fig. 6. It can be seen from the simulation results that under the control of the frequency word, a standard quadrature reference signal can be obtained.

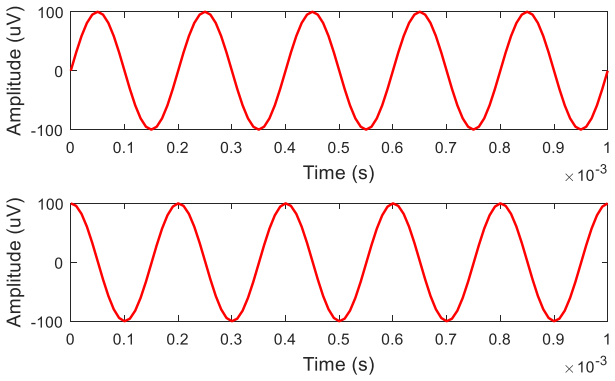

FIGURE 6. Simulation results of the quadrature reference signal.

C. DIGITAL LOW-PASS FILTER

The digital low-pass filter is very important in the entire lock-in amplifier algorithm, and its performance directly affects the signal-noise improvement ratio of the lock-in amplifier. The equivalent noise bandwidth of the lock-in amplifier depends on the bandwidth of the low-pass filter. Narrowband low-pass filter with large attenuation and short transition band makes the performance of digital lock-in amplifiers better. FIR filter (Finite Impulse Response Filter) has the advantages of precise linear phase, easy hardware implementation and stable system, etc. It has been widely used in engineering practice.

The difference equation expression of the FIR filter is:

$$y(n) = \sum_{k=0}^{N-1} h(k) \cdot x(n-k) \tag{8}$$

where N is the order of the FIR filter, $h(n)$ is the FIR filter coefficient, $x(n)$ is the digital sample sequence after A/D conversion, and $y(n)$ is the filtered digital sequence. According to the above formula, the essence of the FIR filter algorithm is a multiply and accumulate operation.

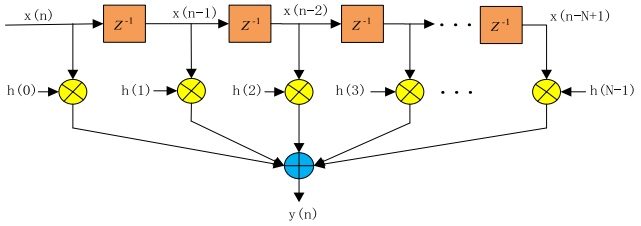

FIGURE 7. Block diagram of FIR low-pass filter.

As shown in Fig. 7, the input signal $x(n)$ is processed to a different number of delay factors and then multiplied by an appropriate coefficient $h(n)$. Finally, add all the products to get the output sequence $y(n)$. The designed FIR filter uses a direct type structure, which is mainly composed of a number of delay units, multipliers and accumulators. In the FIR filter of this structure, the key to its implementation is the determination of the coefficient $h(n)$.

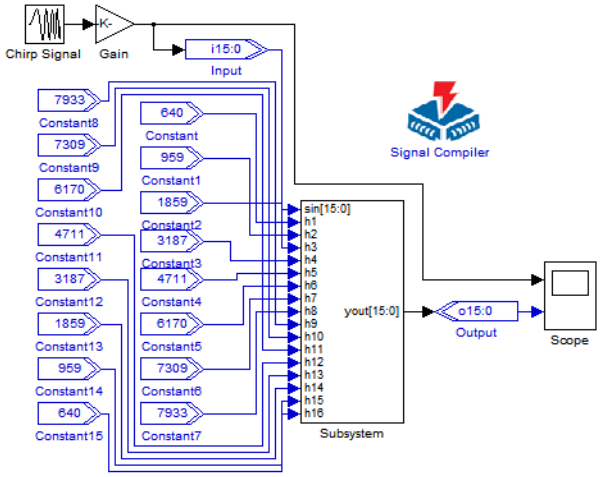

FIGURE 8. 16-stage FIR low-pass filter model.

Considering the requirements of the system for filtering and data processing speed, a 16-order FIR low-pass filter with a cutoff frequency of 10Hz is designed. The design of the FIR filter is relatively simple. It is to design a digital filter to approximate an ideal low-pass filter. First, a 16-stage FIR low-pass filter was designed by using the development tool DSP Builder. The FIR low-pass filter model is shown in Fig. 8. The Filter Design and Analysis (FDA) tool is adopted to determine the filter coefficients. In the FDA Tool, the filter type is selected as low-pass, the filter order is set to 15 (N order filter, specify order $= N - 1$), and the window function type is selected as the Hamming window.

Since the filter coefficient is floating-point data, it is difficult to implement its operation in FPGA, which results in great resource consumption. Therefore, the coefficients are quantized and converted into integers. First, export the coefficients *Num* to the workspace. Enter command *round*(*Num**(2^16)) in MATLAB's command window to get the optimized coefficients. Fig. 9 shows the comparison of the response curves before and after the quantization of the filter

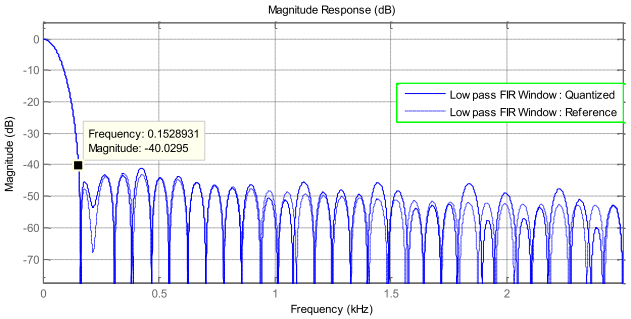

FIGURE 9. Comparison of amplitude-frequency response curves of FIR filter.

coefficients. It can be seen that the quantized response curve does not change significantly, and the FIR filter maintains the performance of the design. After the signal frequency is greater than 153 Hz, the attenuation reaches −40 dB or more.

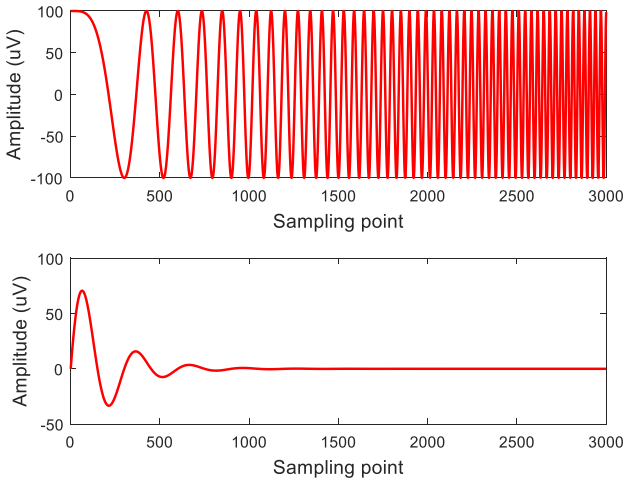

FIGURE 10. Simulation result of FIR filter.

To verify the feasibility of the FIR low-pass filter, a verification simulation was performed. A sweep signal source is added to the input port of the model, and the input and output signals of the FIR filter is shown in Fig. 10. From the result, it can be seen that as the frequency increases, the attenuation increases. The high-frequency signal is effectively suppressed. The low-pass filtering performance of the model meets the design requirements of digital lock-in amplifiers.

IV. IMPLEMENTATION AND TESTING OF DIGITAL LOCK-IN AMPLIFIER IN FPGA

A. EXPERIMENTAL PLATFORM SETUP

The digital core of the realized DLIA is a cyclone IV FPGA from Altera (mounted on a commercial module ALTERA AX301 including also PLLs, external memory and USB interface). The implemented digital architecture comprises:

- a Direct Digital Synthesizer (DDS) for phase and quadrature sinusoidal signal generation;
- an ADC control interface module;
- a signal reconstruction module;
- multipliers for quadrature demodulation;
- a filter module;
- a PC interface module

Through the above verification simulation, the feasibility of the digital lock-in amplifier developed using the DSP builder is verified. In this section, we transfer the designed model to hardware implementation, after the simulation. The Signal Compiler in the model is employed to generate the Quartus II project.

FIGURE 11. Picture of the realized DLIA instrument prototype.

This design uses the cyclone IV series EP4CE6F17C8 device as shown in Fig. 11, compiled with Quartus II 12.0 synthesis. Engineering hardware consumption statistics report Flow Summary shows that 1317 logic elements are used, and the consumption rate is only 21% (1317/6272). The resource usage of FPGA devices is effectively reduced in the design.

B. EXPERIMENTAL RESULTS AND ANALYSIS

A series of tests were performed to test the performance of the digital lock-in amplifier, including linearity test, Q value test and noise test. The schematic of the test is shown in Fig. 12.

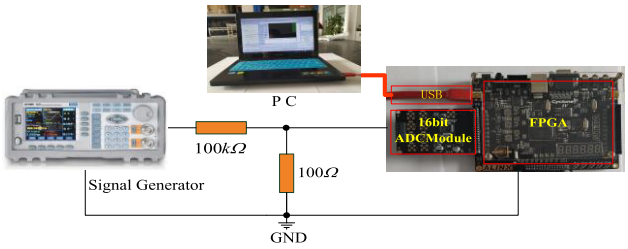

FIGURE 12. Schematic of the test.

1) LINEARITY

The generator exported a sine wave signal with a frequency of 1 kHz and an amplitude range of 10-500 mV to test the linearity of the DLIA. The sinusoidal signal had a fixed frequency of 1 kHz throughout the experiment. Fig. 13 shows the linearity of relationships between the DLIA input and output.

Further, the experimental data and relative errors for the amplitudes of 10 mV, 50 mV, 100 mV, and 500 mV are listed in Table 1.

It can be seen from Table 1 that the relative error of signals above 10 mV is less than 1%. The larger the signal,

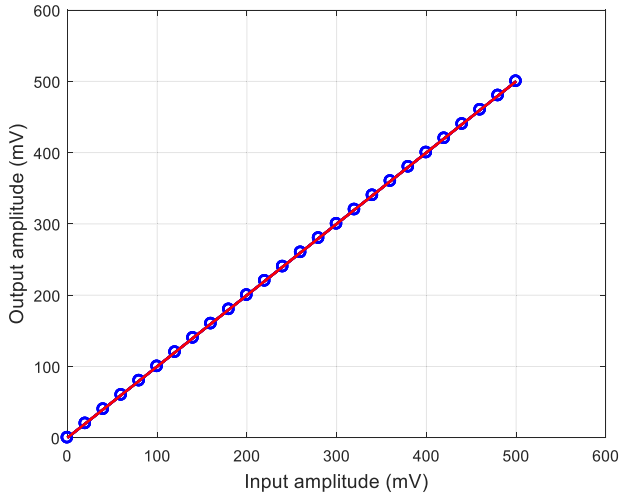

FIGURE 13. The linearity of relationships between the DLIA input and output.

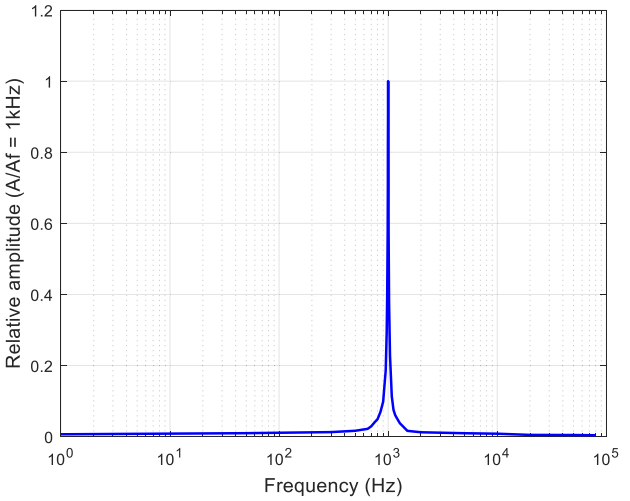

FIGURE 14. The amplitude-frequency response of the DLIA.

TABLE 1. Experimental data and relative errors.

Theoretical value/mV	Measured value/mV	Relative error
10	9.936	0.64%
50	49.830	0.34%
100	100.156	0.156%
500	500.246	0.049%

the smaller the measurement error. Relative errors for the amplitudes of 500 mV is only 0.049%. The experimental results show that the performance of the system meets the design requirements.

2) Q VALUE

The Q value of DLIA can be described using the following equation as:

$$Q = \frac{f_0}{\Delta_f} \tag{9}$$

where f_0 is the center frequency and Δf is the DLIA bandwidth. In this case, when performing Q value experiments, the generator exported a sine wave signal with a frequency range of 600 to 1400 Hz and an amplitude of 500 mV. The reference signal was set to a fixed frequency of 1 kHz throughout the experiment. Fig. 14 shows the amplitude-frequency response of the proposed DLIA. In this case, when the frequency of the input signal is about 994 Hz, the amplitude attenuates from 500 mV to 354 mV, which is about 0.707 times, and thus the corresponding 3 dB bandwidth is 12 Hz. According to Equation (9), we can obtain the Q value of the DLIA which is approximately 82.

3) ANTI-NOISE EXPERIMENT

To control the singularity of the variable, the generator exported a sine wave signal with a frequency of 1 kHz and an amplitude of 500 mV. The experiments were carried out under random noise of amplitudes of 100, 200, 300, 400, and 500 mV, with 10 data per group. In addition, to further verify the superiority of the proposed DLIA, we compare it with a commonly used and accepted ALIA in the same experimental condition.

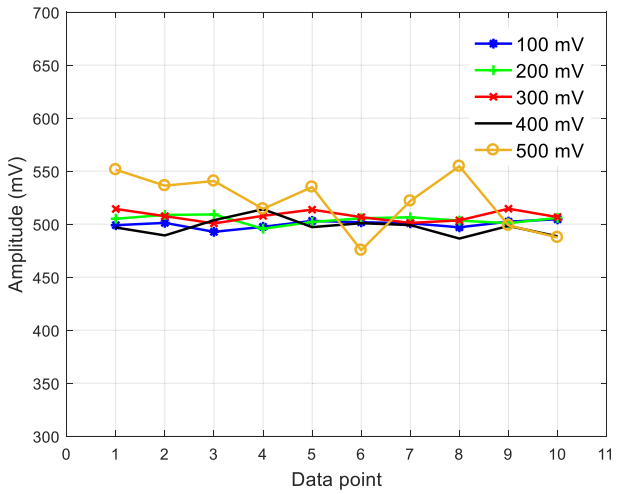

FIGURE 15. Experimental data under different noises using the proposed DLIA.

The experimental data is shown in Fig. 15 and Fig. 16 respectively. It can be seen that as the amplitude of the noise increases, the relative error of the measured data gradually becomes larger no matter using the DLIA and the ALIA, which is consistent with the real situations. The measured amplitudes under different noises using the proposed DLIA are relatively smoother than those of the ALIA, and the obtained amplitudes are closer to 500 mV.

Fig. 17 and Fig. 18 shows the relative error of the measured relative error under different noises using the proposed DLIA and the ALIA, respectively. It can be seen that when the amplitude of the noise is less than or equal to 400 mV, the relative error using the DLIA is less than 2%, while that of the ALIA appropriately reaches up to 5%. Likewise, when the

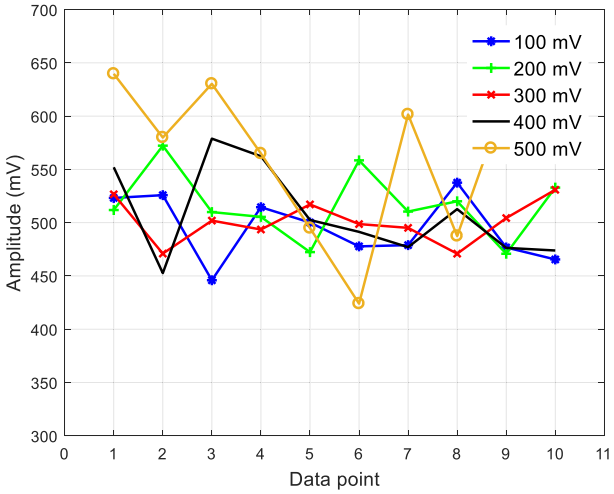

FIGURE 16. Experimental data under different noises using the ALIA.

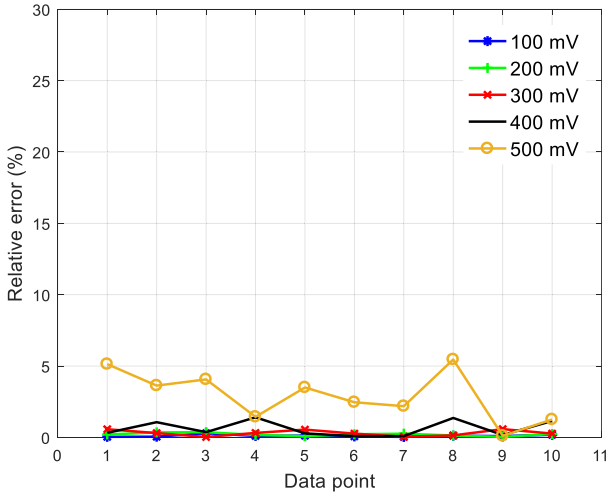

FIGURE 17. Relative error of measured amplitude under different noise using the proposed DLIA.

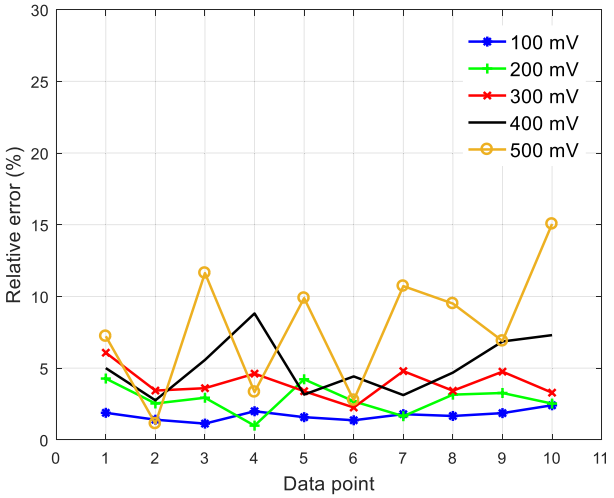

FIGURE 18. Relative error of measured amplitude under different noise using the ALIA.

amplitude of the noise is equal to 500 mV, the relative error using the DLIA is still less than 5%, while that of the ALIA appropriately reaches up to 15%. The experimental results further demonstrate that the digital lock-in amplifier has a relatively better noise immunity.

V. CONCLUSION

For the problem of the frequency error between the measured signal and the reference signal in an analog lock-in amplifier, an FFT phase-locked loop module with automatic frequency tracking is developed in this study, which realizes the true frequency synchronization. The designed high-frequency resolution signal generator ensures that the reference signal has a sufficient frequency resolution to achieve frequency synchronization. The designed high-performance filter makes the DLIA with a high Q value of 82. In the laboratory environment, the relative error of signals above 10 mV is less than 1%. When the noise is less than or equal to 400 mV, the relative error is less than 2%. The proposed digital lock-in amplifier has a relative higher precision and an efficient noise immunity.

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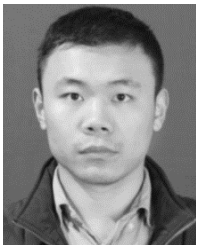

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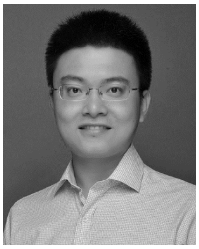

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