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0.3-V Nanopower Biopotential Low-Pass Filter

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ABSTRACT This paper presents a compact power-efficient CMOS fourth-order low-pass filter suitable for electrocardiogram (ECG) acquisition systems. The CMOS structure of the proposed filter utilize the bulk-driven technique and operates in subthreshold region to achieve extremely low-voltage supply (0.3V) and nanopower consumption (0.676 nW) for cut-off frequency of 100 Hz. The filter was designed and simulated using 0.18 μm CMOS TSMC technology. The total input referred noise of the filter is 87 μVrms and the dynamic range is 58.1 dB. The filter offers the best figure of merit of 2.91 $\times$ 10^{-14} J, the lowest power consumption and voltage supply, compared with the previous state-of-the-art nanowatt filter designs.

INDEX TERMS Biopotential filter, bulk-driven, low voltage, low power.

I. INTRODUCTION

In recent years, an increased interest in the design of ultra-low-voltage (ULV) and ultra-low-power (ULP) electronic systems, devoted to biomedical applications, is observed. This new trend is associated with the development of different kind of implantable and wearable biomedical systems, where low dissipation power is of crucial importance [1], [2].

One of the most important blocks in such systems is the low-pass filter (LPF). As an example let us consider a typical electrocardiogram (ECG) acquisition system shown in Fig.1. The weak ECG signal, whose amplitude is in the range of 100 μV- 4 mV is first amplified by a low-noise preamplifier with variable gain, typically in the range of 10-100 V/V [1]. Next it is filtered with a LPF with adjustable cutoff frequency f_c (100-250 Hz), to decrease out-of-band noise. Finally, the signal is converted into digital form by an analog-to-digital converter (ADC) [1], [2].

Active filters devoted to such applications usually have very simple structures and exploit MOS transistors operating in sub-threshold region. This allows decreasing both, the dissipation power, as well as the occupied area. Simple structure allows decreasing the input referred noise as well.

In recent years a number of ULV and ULP solutions for biopotential filters has been proposed [3]–[7]. In order to simplify their structures, usually the authors use a single transistor as a transconductor, to realize a g_m-C integrator. Their linearity and dynamic range (DR) is usually improved thanks to the local or global negative feedback loops. In order to further decrease their structures and current consumption, some of the proposed solutions of biquadratic sections contain only one branch of current, consisting of several stacked transistors [4]–[6]. However, the stacked transistors between the supply rails limit the minimum supply voltage (V_{DD}) and entail different dc levels between input and output.

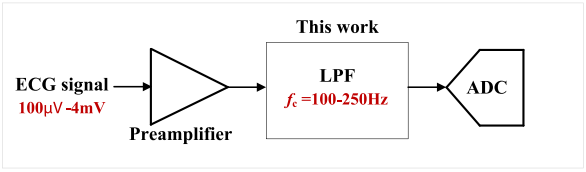

FIGURE 1. ECG acquisition system.

In order to overcome the above mentioned constraints and further decrease both, the supply voltage, as well as the dissipation power (P_{diss}) of an ECG filter, a bulk-driven (BD) technique can be considered. The BD circuits proved their capability to operate from extremely low V_{DD}, even much below the threshold voltage (V_{TH}) of MOS transistors, while maintaining the input common mode range (ICMR) almost rail-to-rail [7]–[13]. It is also worth noting, that in some cases the BD approach can extend the DR of analog circuit under ULV supply, since it can extend the input range for which

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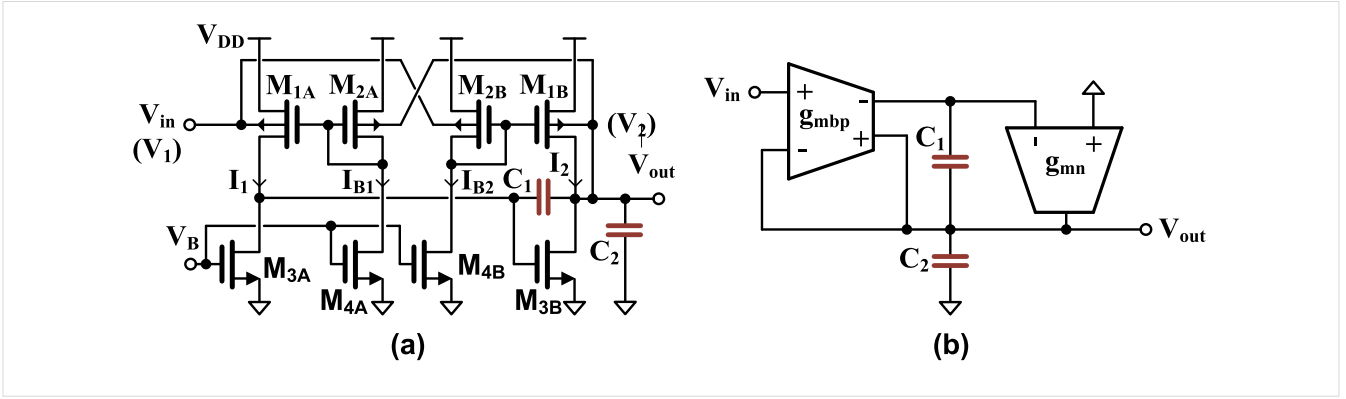

FIGURE 2. CMOS schematic of the biquad filter (a) and its block diagram (b).

the circuit performance is not limited by hard non-linearities. Therefore, the BD technique can be a promising approach to design ULV ECG filters.

In this paper we propose a new solution for an ULV ECG filter based on the BD approach. The filter is a cascade connection of two newly-proposed ULV BD biquad filters. Similarly as in [4], the biquad was developed from a low-voltage current re-use CMOS buffer [14]. Nevertheless, since the traditional long-tailed gate-driven (GD) differential pair was replaced with a non-tailed BD differential pair, a much lower minimum supply voltage was achieved. The lower V_{DD} entails lower P_{diss} of the overall structure. Moreover, the DR of the proposed biquad is better than reported for other designs in literature, even though its supply voltage is much lower (0.3 V). Due to the low dissipation power and good DR, the proposed filter outperforms other ECG filters in terms of standard Figures of Merit (FOMs).

The rest of the paper is organized as follows. In Section II the newly-proposed BD biquad filter is discussed in detail. Section III describes the overall structure of the ECG filter. The simulation results and comparison with other similar designs are presented in Section IV. Finally, the paper is concluded in Section V.

II. PROPOSED BIQUAD CELL

A. CIRCUIT DESCRIPTION

The schematic of the proposed ULV biquad filter is shown in Fig. 2. Its principle of operation is based on the idea of a simple CMOS unity-gain buffer [14]. This idea has been next adopted to signal filtering purposes, in a similar way as described in [4]. The circuit shown in Fig. 2. exploits similar operation principle, however, in this structure a traditional long-tail GD differential amplifier has been replaced by a non-tailed BD differential amplifier composed of the transistors $M_{1A,B}$-$M_{2A,B}$. Due to the non-tailed architecture combined with the BD approach, a rail-to-rail input swing can be achieved for very low supply voltage.

The input differential amplifier, composed of the transistors $M_{1A,B}$-$M_{2A,B}$, exploits the idea first proposed in [15]. Let us assume that V_1 and V_2 represent the input voltages of the amplifier and the connection between the biquad output node and V_2 is broken. The transistors M_{1A}-M_{2A} and M_{1B}-M_{2B} form two current mirrors, biased with the current sinks $I_{B1} = I_{B2} = I_B$. The input signals are applied to the bulk terminals of the transistors $M_{1A,B}$-$M_{2A,B}$, as shown in Fig. 2. Assuming $V_1 = V_2$, the V_{BS} voltages of all transistors are equal to each other, which entails that their threshold voltages are equal as well. Therefore, neglecting the impact of g_{ds} conductances, the currents I_1 and I_2 are also equal to each other and equal to I_B. Consequently, for $V_1 = V_2$, the differential output current of the first stage (I_1-I_2) is equal to zero, i.e. with the above assumptions, the input amplifier is insensitive to the common-mode voltage.

For input differential signals, when $V_1 \neq V_2$, the threshold voltages of M_{1A} and M_{2A} (M_{1B} and M_{2B}) are different, because of the dependence of the threshold voltages of MOS transistors on their bulk potentials. This affects the current transfer ratio of the current mirrors and produces a difference of the output currents I_1 and I_2.

Assuming that the p-channel transistor operates in saturated weak inversion region, its transfer characteristics can be approximated as:

$$I_D = I_O \left(\frac{W}{L}\right) exp\left(\frac{V_{SG} + V_{TH}}{n_p U_T}\right) \tag{1}$$

where I_o is the technology current, n_p is the subthreshold slope factor for p-channel MOS and U_T is the thermal potential. The threshold voltage V_{TH}, can be expressed as a function of V_{BS} voltage as follows:

$$V_{TH} = V_{THO} - \gamma_p \left(\sqrt{2\,|\phi_F| + V_{BS}} - \sqrt{2\,|\phi_F|}\right) \tag{2}$$

where V_{THO} is the threshold voltage for $V_{BS} = 0$, $2|\Phi_F|$ is twice the Fermi potential and γ_p is the bulk threshold parameter.

Straightforward analysis shows that with the above model the differential output current of the first stage I_1-I_2 can be expressed as:

$$I_1 - I_2 = -2I_B \sinh\left(\eta \frac{V_1 - V_2}{n_p U_T}\right) \tag{3}$$

where η is the ratio of the bulk (g_{mbp}) to gate (g_{mp}) transconductance of the transistors $M_{1A,B}$-$M_{2A,B}$ at the operating point, given by:

$$\eta = \frac{g_{mbp}}{g_{mp}} = \frac{\gamma_p}{2\sqrt{2\,|\phi_F| + V_{BS}}} \tag{4}$$

As it can be concluded from the above considerations, the transistors $M_{1A,B}$-$M_{2A,B}$ form a truly differential (transconductance) amplifier, with non-linear large signal characteristic given by (3) and the small-signal transconductance which may be approximated as [15]:

$$g_m \approx 2g_{mbp} \tag{5}$$

It is worth mentioning, that both, its noise properties and offset are not worse than observed for the corresponding BD differential pair biased with the same total current [10], [15].

The transistor M_{3B} form a second transconductance stage. Consequently, the equivalent block diagram of the proposed biquad may be presented in the form shown in Fig.2.b where $g_{mn} = g_{m3B}$.

It is worth pointing out, that due to the non-tailed architecture of the first transconductor in Fig. 2, the minimum supply voltage of the proposed biquad filter is as low as $2V_{DSsat}$, where V_{DSsat} is the saturation voltage of an MOS transistor (3-4 U_T in weak inversion region). The input/output swing is limited by the output characteristics of M_{1B} and M_{3B}. Because of the negative feedback loop, the maximum (minimum) output voltage can be very close to supply rails.

B. TRANSFER FUNCTION

The transfer function of the biquad filter in Fig. 2b can be expressed as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{g_{mbp}g_{mn}}{C_1C_2}}{s^2 + s\left(\frac{g_{mn}}{C_2}\right) + \frac{g_{mbp}g_{mn}}{C_1C_2}} \tag{6}$$

thus, it is transmittance of a low-pass filter, where its dc voltage gain (A_{DC}), natural frequency (ω_o), and quality factor (Q), are respectively given by:

$$A_{DC} = 1 \tag{7}$$

$$\omega_o = \sqrt{\frac{g_{mbp}g_{mn}}{C_1C_2}} \tag{8}$$

$$Q = \sqrt{\frac{g_{mbp}C_2}{g_{mn}C_1}} \tag{9}$$

Assuming $g_{mn} = I_B/n_nU_T$ and $g_{mbp} = \eta I_B/n_pU_T$, the natural frequency and the quality factor may be expressed in the form:

$$\omega_o = \frac{I_B}{U_T}\sqrt{\frac{\eta}{n_nn_pC_1C_2}} \tag{10}$$

$$Q = \sqrt{\eta\frac{n_nC_2}{n_pC_1}} \tag{11}$$

As it is easy to note, the natural frequency of the biquad filter is proportional to the biasing current I_B and can be easily tuned with this current. On the other hand, variations of I_B will not affect the quality factor Q. Both quantities (ω_o and Q) will depend slightly on the process, supply voltage and temperature (PVT) variations, because the PVT variations will affect the slope factors n_n, n_p, the coefficient η and U_T. However, one can expect that the variations will be on acceptable level.

The tuning range of ω_o is limited by the acceptable range of $|V_{GS}/V_{DS}|$ voltage drops across MOS transistors in this circuit, that provide operation of all transistors in saturation.

TABLE 1. Transistors aspect ratios and filter capacitances.

Device	W/L [µm/µm]	Device	C [pF]
$M_{1A,B}$	5/4.5	C_1	4.83
$M_{2A,B}$	5/4.5	C_2	9.80
$M_{3A,B}$	5/4.5	C_3	5.00
$M_{4A,B}$, M_B	5/4.5	C_4	5.60

C. NOISE PERFORMANCE

The thermal $\overline{v_t^2}$, and flicker $\overline{v_{1/f}^2}$, noise spectral densities of a MOS transistor can be expressed as follows:

$$\overline{v_t^2} = \frac{8kT}{3g_m} \tag{12}$$

$$\overline{v_{1/f}^2} = \frac{Kg_m^2}{fC_{ox}WL} \tag{13}$$

where k is the Boltzmann constant, T is the absolute temperature, g_m is the transconductance, C_{ox} is the gate oxide capacitance per unit area and K is the flicker noise constant.

Assuming the above noise model, and neglecting the second order effects, the low frequency ($f \ll f_c$) input referred noise of the considered biquad in a weak inversion region can be expressed as:

$$\overline{v_{tb}^2} = 2\frac{8kT}{3\eta g_{mbp}}\left(1 + \frac{n_p}{n_n}\right) \tag{14}$$

$$\overline{v_{1/fb}^2} = \frac{2}{fC_{ox}\eta^2}\left[\frac{K_p}{WL_{1,2}} + \frac{K_n}{WL_{3,5}}\left(\frac{n_p}{n_n}\right)^2\right] \tag{15}$$

Usually, the thermal noise will be dominant, because of very low biasing currents (transconductances) and relatively large sizes of MOS transistors, required in ULV environment. Note, that the noise performance of the biquad filter will be deteriorated by the BD approach ($\eta \ll 1$), which is a well known disadvantage of all BD circuits.

III. BIOPOTENTIAL FILTER

The biopotential filter can be realized as a cascade connection of two biquad filters described in the previous section. Its transistor-level schematic is shown in Fig. 3. Transistor M_B is used for biasing purposes. Note, that transistor sizes and biasing currents in both sections were assumed to be identical.

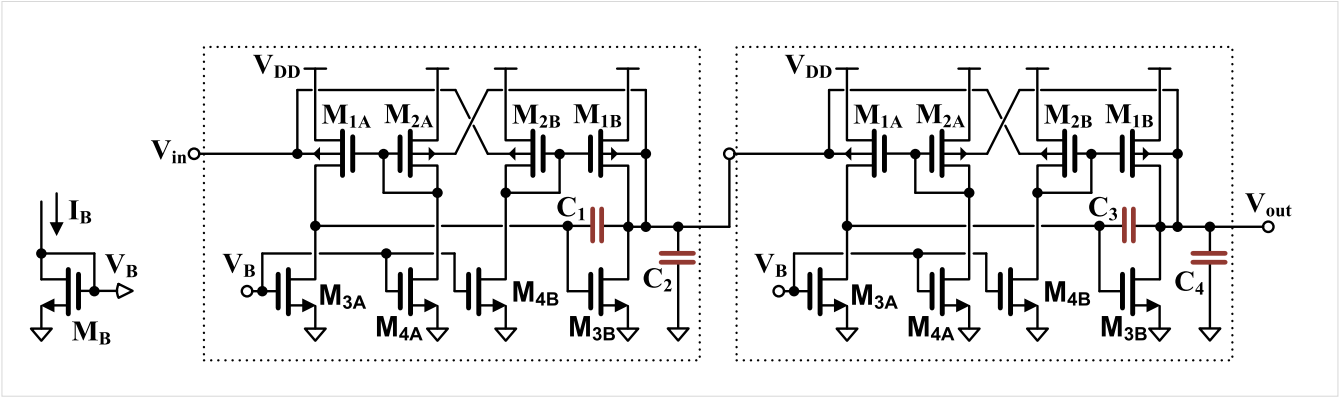

FIGURE 3. CMOS schematic of the proposed biopotential filter.

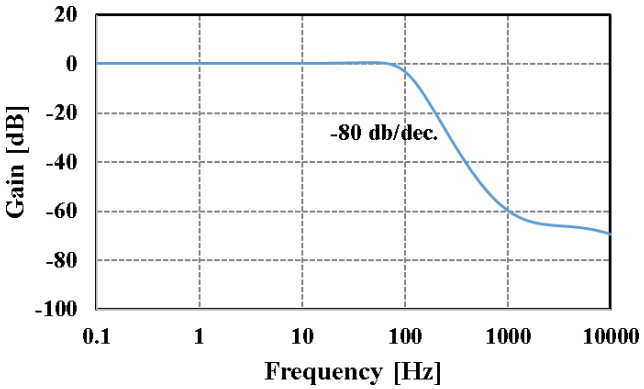

FIGURE 4. AC response of the filter for IB = 0.25nA, fc = 100Hz.

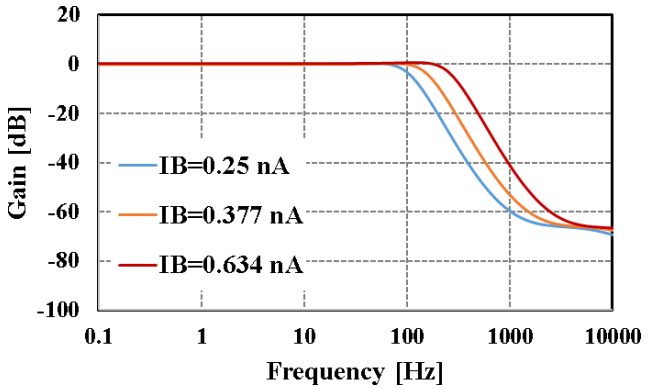

FIGURE 5. AC response of the filter for (IB = 0.25nA, fc = 100Hz), (IB = 0.377nA, fc = 150Hz), (IB = 0.634nA, fc = 200Hz).

In order to obtain a fourth order maximally flat characteristic with 3-dB frequency of 100-Hz, for the assumed I_B = 0.25 nA (g_{mbp} = 2.63 nS g_{mn} = 7.0 nS), the used capacitances were calculated as shown in Table 1. This results in f_o/Q equal to 99.3 Hz/0.87 for the first and 129 Hz/0.65 for the second section of the filter respectively.

The channel lengths of all transistors were chosen relatively large to maximize their g_m/g_{ds} ratios (intrinsic voltage gains). On the other hand, their channel widths were fine tuned during the simulation phase to achieve $|V_{GS}| \approx V_{DD}/2$ at the operating point, that provides maximum voltage headroom for possible PVT variations and signal swing in an ULV environment. The transistor aspect ratios for the design are also provided in Table 1.

IV. SIMULATED RESULTS

A. MAIN CHARACTERISTICS

The circuit has been implemented in a 0.18 μm CMOS process from TSMC, with threshold voltages of around +/− 0.5 V. Its performance was validated using Cadence/Spectre platform. The assumed supply voltage was 0.3 V (+/− 0.15 V for the purpose of simulations).

Fig. 4 shows the magnitude characteristic of the filter for I_B = 0.25 nA. The characteristic agree well with theory. The dc voltage gain was 0.144 dB, while the cutoff frequency was exactly 100 Hz. The attenuation in the stop band exceeded 60 dB, which is sufficient for the considered application.

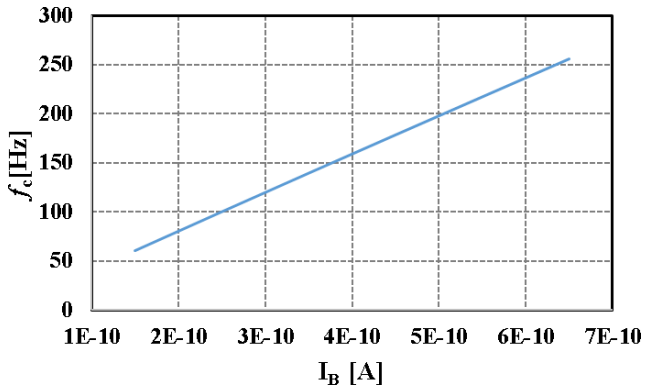

FIGURE 6. Frequency fc versus bias current IB.

Fig. 5 shows variations of the magnitude characteristic with the biasing current I_B. For I_B ranging from 0.25 nA to 0.634 nA, the 3-dB frequency (f_c) of the filter is tuned from 100 Hz to 250 Hz. Note, that variations of the dc voltage gain and shape of the characteristic (quality factors of both sections) are negligible, that agrees well with theory.

Fig. 6. shows the cutoff frequency of the filter against the biasing current I_B. As it is seen, the 3-dB frequency can be linearly tuned for I_B ranging from 0.15 nA to 0.65nA, which

TABLE 2. Effect of PVT variation on the cutoff frequency.

T [°C]	0			27			60		
	f_c [Hz]			f_c [Hz]			f_c [Hz]		
V_{DD} [V]	SS	TT	FF	SS	TT	FF	SS	TT	FF
0.28	113.7	109.4	106.1	102.7	99.71	96.24	92.47	88.3	76.18
0.3	112.5	109.5	106.3	102.9	100	96.58	92.67	88.51	76.51
0.32	112.6	109.7	106.6	103.3	100.3	96.92	92.8	88.64	76.73

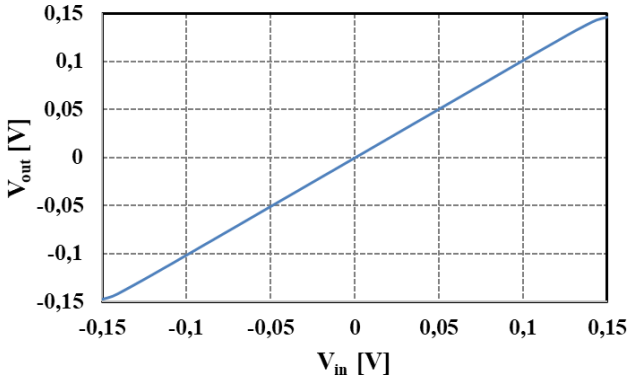

FIGURE 7. DC transfer characteristic of the filter showing rail-to-rail voltage range.

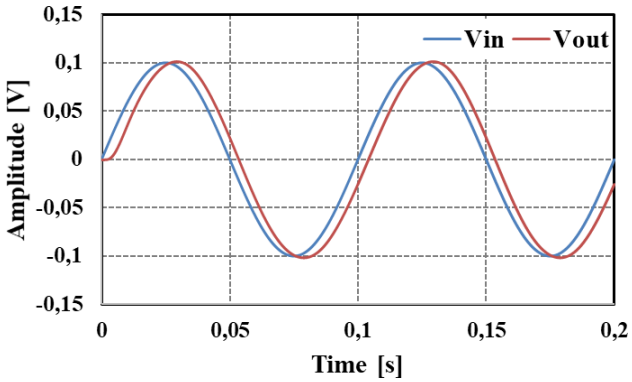

FIGURE 8. Transient response of the filter for input sine wave with Vinpp = 200mV and 10 Hz. THD = 1%.

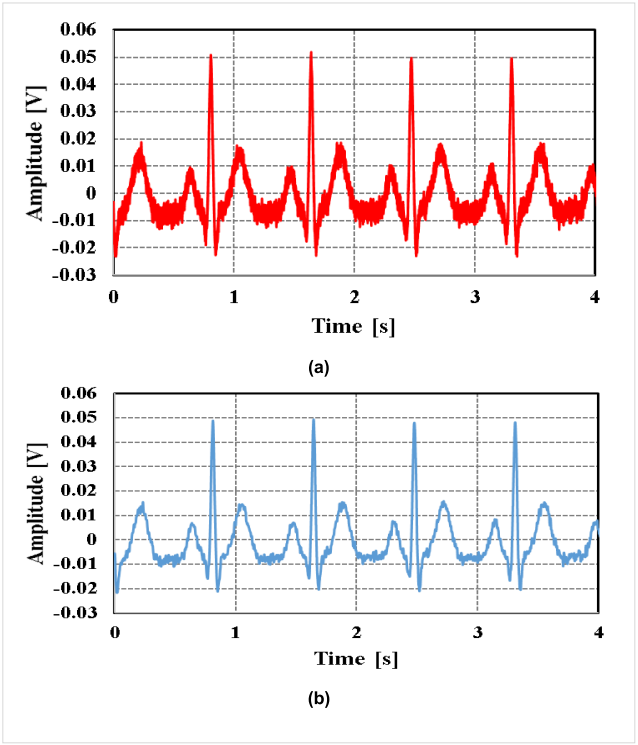

FIGURE 9. Transient response of the filter for noisy ECG signal, (a) input, (b) output.

corresponds to f_c ranging from 60 Hz to 260 Hz. This linear range is limited by the $|V_{GS}/V_{DS}|$ voltage drops across MOS transistors and can be extended for larger V_{DD}.

Fig. 7 shows the static transfer characteristic of the filter. It is worth pointing out a very good linearity of this characteristic, for nearly rail-to-rail voltage swing. The large voltage swing in an ULV environment is obtained thanks to the BD approach applied in this design.

The good linearity of the filter is confirmed also by its sine wave response shown in Fig. 8. For the sine wave of 200 mV_{pp} and 10-Hz frequency, the total harmonic distortion (THD) was 1 %. The phase shift between input and output signals in Fig.8 is caused by the phase characteristic of the filter. The ability of the proposed filter to attenuate noise is shown in Fig. 9. In Fig. 9a we can see an input ECG signal with an amplitude of 50 mV_p, interfered with a parasitic noise modeled as a 500-Hz sinusoidal signal with amplitude of 5mV_p. Fig. 9b shows the resulting signal at the output of the filter, which confirms its proper operation in this case.

B. IMPACT OF PVT VARIATIONS AND MISMATCH

In order to investigate the filter sensitivity to PVT variations and transistor mismatch, both, the corner analysis as well as the Monte Carlo (MC) analysis have been performed. The results of corner analysis are shown in Table 2, where the impact of PVT variations on the cutoff frequency of the filter are shown and in Table 3, where its dc gain is examined. Both parameters show relatively low variations under the assumed range of PVT variations.

The impact of transistor mismatch on f_c and dc gain of the filter is shown in Figs. 10 and 11 respectively. The figures show histograms, being the results of MC analysis (200 runs). The observed standard deviations of f_c (3.19 Hz) and dc gain (0.034 dB) prove a relatively low sensitivity of the filter to transistor mismatch.

The input referred offset of the filter varied from −2.9 mV to 1.8 mV, as a result of PVT variations, while the MC

TABLE 3. Effect of PVT variation on the DC gain.

T [°C]	0			27			60		
	DC gain [dB]			DC gain [dB]			DC gain [dB]		
V_{DD} [V]	SS	TT	FF	SS	TT	FF	SS	TT	FF
0.28	0.852	0.274	0.166	0.239	0.166	0.142	0.168	0.174	0.275
0.3	0.305	0.179	0.138	0.174	0.144	0.134	0.156	0.178	0.342
0.32	0.191	0.145	0.123	0.148	0.132	0.130	0.149	0.187	0.433

TABLE 4. Performance comparison of nanopower 4th-order LP filters.

Parameter	This work (single ended)	TCAS-I (fully-differential) (2019) [6]	TCAS-I (fully-differential) (2018) [4]	TVLSI (fully-differential) (2018) [5]	MJ (fully-differential) (2019) [16]
V_{DD} [V]	0.3	1.5	0.9	0.6	0.3
Technology [µm]	0.18	0.35	0.35	0.35	0.18
Filter order	4	4	4	4	4
f_c [Hz]	100	100	100	101	100
Power [nW]	0.676	5.25	4.26	0.9	4.8
DR [dB]	58.1	56.9	48.2	47	56
DC gain [dB]	0.144	-0.09	-0.05	-2.77	0
C_{total} [pF]	25.2	47.14	38.5	60.56	8.8
IRN [µVrms]	87	39.38	80.5	46.27	73.5
Area [mm^2]	-	0.1	0.11	0.168	0.03
FoM [J]	2.91E-14	2.31E-13	2.21E-13	4.74E-14	2.14E-13
Obtained results	Simulation	Measured	Measured	Measured	Simulation

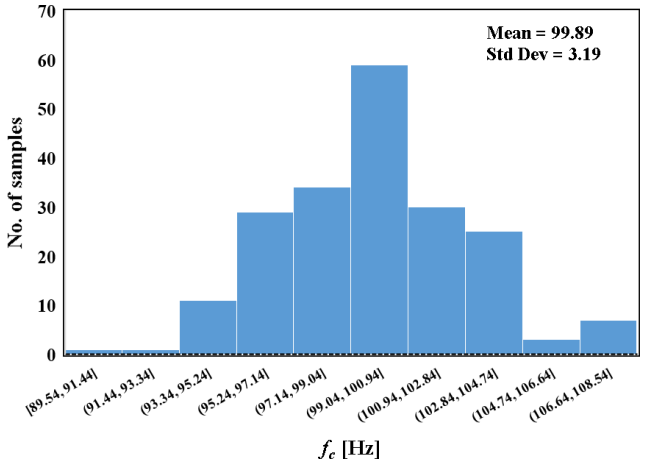

FIGURE 10. The histogram of the frequency fc with 200 MC runs.

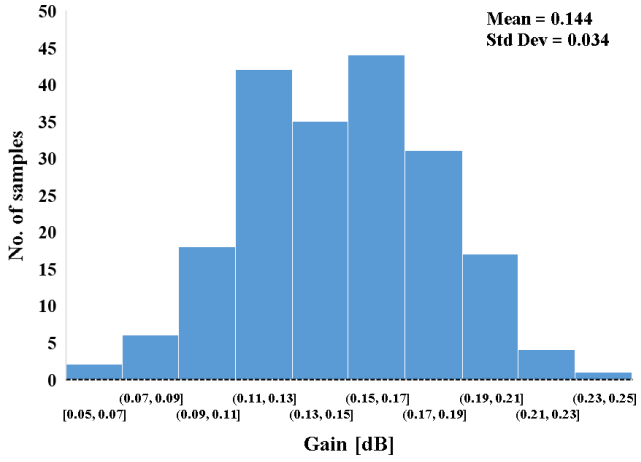

FIGURE 11. The histogram of the DC gain with 200 MC runs.

mismatch analysis showed a mean value of −0.291 mV and standard deviation of 4.91 mV.

The above results show, that the filter is robust under PVT variations and transistor mismatch. Note, that the impact of transistor mismatch could be further lowered, applying larger transistor channel sizes, at the cost of silicon area of the filter.

C. COMPARISON

Table 4 presents a comparison of the proposed filter with other similar designs of biopotential filters, published in recent years. First of all is worth noting, that the proposed filter can operate with much lower V_{DD} than other filters in Table 4, except [16]. Despite its single-ended architecture and ULV supply, the filter offers the best dynamic range among all the compared filters. This property is achieved thanks to the non-tailed BD architectures of the main blocks used in this design. Note, that the DR could be further improved with a fully-differential version of the proposed circuit. In order to facilitate the comparison, the following

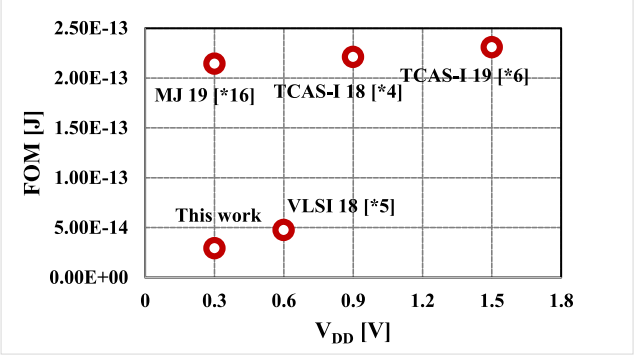

FIGURE 12. Comparison of FOMs and supply voltages.

standard FOM has been used:

$$\text{FOM} = \frac{P_{diss}}{Nf_cDR} \tag{16}$$

where N is the filter order and the other symbols were defined earlier.

As it can be concluded from (16), the above FOM takes into account the power effectiveness of the filter, and refers it to the achieved DR. Lower value of this FOM means better performance of the filter.

The values of the calculated FOMs are shown in Table 4 and in a graphical form in Fig. 12. As it is easy to note, the proposed filter offers the best FOM, which is approximately one order of magnitude better than achieved for the design in [16], which was supplied with the same V_{DD}. The most similar FOM was reported for the filter in [5], however, that circuit was supplied with much larger V_{DD}.

V. CONCLUSION

A new design for an ULV, fourth-order, biopotential (ECG) filter was presented. The filter is a cascade connection of two newly-proposed second-order (biquad) filters, developed from a compact current re-use CMOS buffers [4], [14]. Thanks to the application of BD non-tailed differential pairs, instead of traditional gate-driven pairs, a new ULV biquad filter was obtained, with very low supply voltage (0.3 V) and rail-to-rail input/output range. The simulated results showed, that the circuit outperforms all other designs in terms of standard FOMs, and operates well also in the presence of PVT variations and transistor mismatch. The filter performance can be further improved with a fully-differential version of this design.

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