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Novel Floating and Grounded Memory Interface Circuits for Constructing Mem-Elements and Their Applications

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ABSTRACT Memory elements (known as mem-elements) include memristor, memcapacitor and meminductor. They are considered the keys to developing the new generation of intelligent and neuromorphic devices. However, the complicated nano-scale manufacturing technique makes them difficult to produce, impeding the research and commercialization activities of mem-element devices. The emerging independent/universal emulators is considered one of the most promising candidates for mem-elements research. In this paper, for the completeness of circuit theory, the mathematical representations, classification, concept of unfolding with the extended formulation of three mem-elements are described, respectively. Then, a newly proposed floating and grounded memory interface circuits with wide frequency range are presented, together with the mathematical model and fingerprints. We also discuss the main affecting factors of frequency and demonstrate that the frequency of memristor is as high as 900kHz, and the highest frequency of memcapacitor also exceeds 500kHz. Finally, we explore a potential application based on the proposed interface circuit, i.e., a simple chaotic circuit. Also, the models, strange attractors, and Lyapunov exponents of three chaotic systems with mem-element are obtained, respectively. There is no doubt that the good agreement among theoretical analysis, simulation and experimental results verifies the practicability and flexibility of these interface circuits.

INDEX TERMS Memory interface circuit, floating and grounded, memristor, memcapacitor, meminductor.

I. INTRODUCTION

All along, as the three fundamental two-terminal passive elements: the resistor, the capacitor and the inductor are mainly capable of dissipating or storing energy - but not of generating it. Their behavior represents the constitutive relationship between two of the four variables (current i, voltage v, charge q, and magnetic flux φ, see Fig.1). For the sake of the logical completeness of circuit theory, in 1971, Leon Chua suggested that memristor (MR, abbreviation from 'memory resistor') should be the fourth two-terminal fundamental circuit element, which represents the relationship between q and φ [1]. Later, he expanded the notion of the MR to encompass 'memristive systems' [2] and pointed out the existence of fingerprint (known as 'pinched hysteresis loop') is the sufficient condition of a memory system [3], [4]. Subsequently, in 1978, memcapaci-tor (MC, abbreviation from 'memory capacitor' that repre-sents the relationship between σ and φ, and σ is proportional to the time integral of q) and meminductor (ML, known as 'memory inductor' that represents the relationship between q and ρ, and ρ is proportional to the time integral of φ) were also postulated - but they are not consider as new fundamental circuit elements. In 2008, Stanley Williams and his team at HP Laboratories fabricated the first physical MR, which is based on TiO_2 material [5]. The same year, Di Ventra and co-workers formally proposed the concepts of MC and ML, as well as their mathematical models [6]. However, their solid state implementation are not commercially available until now. It can be said that the study and application of nonlinear memory circuits are still in their infancy.

As well as we know, mem-elements are nano-devices. The study of solid-state storage devices based on them would break the Moore's Law and the monopoly of von Neumann computer system, accelerating the growth rate

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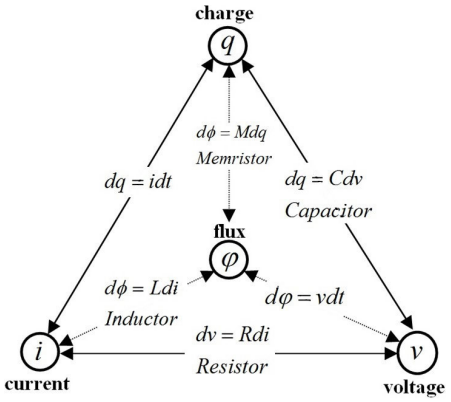

FIGURE 1. The relationship between current i, voltage v, charge q, and flux φ.

of the information technology market. Meanwhile, some scholars found that the continuously tunable memristive behavior have became the new paradigm for nonvolatile, high density, high frequency and adaptive electronic circuit elements. Also, it would open up new realms for circuit investigations, intelligent devices and applications in a range of areas, including oscillators [7]–[13], low-power computation [14], nonvolatile memories [15], [16], neuro-morphic [17]–[21], synchronization systems [22]–[27], neural networks [22]–[25], chaotic masking [28], image encryption [29]–[31], and so on [32]–[37].

For few decades, due to the fact that the mem-elements are still not commercially available, a large number of MR, MC or ML emulators and universal emulators are proposed and considered one of the most potentially candidates for developing the new generation of intelligent and neuromorphic devices. For example, Zdenek Kolka and co-workers analyzed the model of the HP TiO_2 memristor and proposed a new behavioral approximation of static I-V characteristics [8]. Yu D and *et al*. proposed a coupled MC emulator-based relaxation oscillator for mimicking the dynamic behaviors of flux coupled memca-pacitors [9]. Wang G and his fellows designed a new chaotic oscillator based on the realistic model of the HP TiO2 memristor and Chua's circuit [10]. Subsequently, the fellows of the same research group also designed smooth curve models of MC and ML and a new five-dimensional chaotic oscillator [11]. Pershin Y. V and Ventra M. Di proposed two kinds of emulator circuits with MR for constructing other mem-elements [36]. Sah M. P and his fellows proposed an efficient method to build the expand-able circuits of MC emulator in various configurations using an expandable MR emulator [37]. Khalifa Z. J. and Abuelma'atti M. T. presented a floating memristor and applied to an FM-to-AM converter circuit [14]. Sánchez-López C and Aguila-Cuapio L. E. proposed a grounded memristor emulator circuit operating from 16 Hz to 860 kHz [16]. Mohammad S. F. and his fellows utilized the emulators to evaluate the feasibility of these elements in the implementation of adaptive neurons [18], just to name a few. However, some of them belong to the independent emulator and the others are unidirectional circuits with MR for constructing other mem-elements. There are many restrictions that make them impractical and flexibility for prototyping.

Subsequently, the design of universal emulators became a new perspective. By taking minor changes, the transformations among MR, MC and ML could be realized simply and flexibly. For example, in 2014, Yu D and *et al*. designed a bidirectional universal emulator based on active device [38]. Nevertheless, one of the major limitation of one terminal emulators is that they must be grounded in order to function correctly. In 2019, Zheng C and her co-workers proposed a novel universal emulator with the varactor diode [39]. However, it can only be operated under the floating condition whose mathematical model is a quadratic function. The reverse voltage across the varactor diode was fitted by a quadratic polynomial function leading to some truncation errors. Moreover, the prototype has a limited operating frequency range (about dozens *kHz*). Undoubtedly, these existing emulators and related circuits assisted scholars in understanding the nonvolatile behaviors and explored potential applications, but the weakness is that they are incapable to generalize beyond their range of terminal voltages and frequency. Meanwhile, with the help of these emulators, there are also substantial results in the dynamics study and applications of memory systems, such as a meminductor-based chaotic system with nonlinear dynamics [41], co-existing attractors and antimonotonicity [42], [43], [59], coupled [44], [45], bi-stability [25], [28], [46]–[48], synchron-ization [49], infinite chaotic attractors [50], memory neural network circuits [51]–[54], nano-programmable logics [55], multi-stability [56], image encryption [57].

Furthermore, in order to accelerate the development of future memory circuits and nonlinear theory, it is important and necessary to design an analog memory interface circuit that well frequency characteristics and does not depend on any type of memory component and curve fitting substitute, which is also one of the motivations of this paper. Therefore, we propose such novel floating and grounded interface circuits for constructing mem-elements whose mathematical model is similar to the HP memrisor - but not a quadratic function. They would facilitate the manufacture of prototypes and applications, with a wide frequency range. The outline of the remainder of this paper is follows: In Section II, similar to MR, the mathematical model, classification, concept of unfolding with the extended formulation of other memory elements are described. In Section III, a novel floating and grounded memory interface circuits are proposed, as well as the models, fingerprints and frequency characteristics of MR, MC and ML, respectively. In Section IV, the application with mem-element is explored. The simplest chaotic circuit is designed. Also, three chaotic system based on MR, MC and ML are given and the dynamics, including strange attractor, Lyapunov exponents and Hausdroff dimension are also analyzed. Finally, the paper is summarized in Section V.

TABLE 1. Mathematical model of memristors.

MR	Current-controlled	Voltage-controlled
Ideal MR	$\varphi=\hat{\varphi}(q)$ or $u(t)=R_M(q)i(t)$ where $i(t)=\frac{dq(t)}{dt}$, $R_M(q)\overset{\Delta}{=}\frac{d\hat{\varphi}(q)}{dq}$ is called the memristance in Ohm (Ω). The constitutive relation could be recovered to within an arbitrary initial flux value φ_0 from $R_M(q)$ via $\hat{\varphi}(q)=\varphi_0+\int_{-\infty}^{q}R(q)dq$	$q=\hat{q}(\varphi)$ or $i(t)=G_M(\varphi)u(t)$ where $u(t)=\frac{d\varphi(t)}{dt}$, $G_M(\varphi)\overset{\Delta}{=}\frac{d\hat{q}(\varphi)}{d\varphi}$ is called the memductance in Siemens (S). The constitutive relation could be recovered to within an arbitrary initial charge value q_0 from $G_M(\varphi)$ via $\hat{q}(\varphi)=q_0+\int_{-\infty}^{\varphi}G_M(\varphi)d\varphi$
Generic MR	$u=R_M(x)i$, $f_M(x,i)=\frac{dx(t)}{dt}$	$G_M(x,u)=\frac{dx(t)}{dt}$, $g_M(x,u)=\frac{dx(t)}{dt}$
Extended MR	$u=R_M(x,i)i$, $R_M(x,0)\neq\infty$, $f_M(x,i)=\frac{dx(t)}{dt}$	$G_M(x,0)\neq\infty$, $G_M(x,u)=\frac{dx(t)}{dt}$, $g_M(x,u)=\frac{dx(t)}{dt}$

II. MATHEMATICAL MODEL, CLASSIFICATION AND CONCEPT OF MEM-ELEMENTS

The MR has been obtained in detail [4]. The concept of MC and ML, as well as their mathematical models, were proposed by Di Ventra and his co-workers [6], but they are not specifies like MR. For the sake of the completeness of the memory system and circuit theory, in this section, the basics of mem-elements theories are revisited, such as the their mathematical models, classifications, and the concept of unfolding with extended formulations.

A. MEMRISTOR

As shown in Table 1, the mathematical model of a MR can be written in three different representations [4], i.e. the ideal MR, generic MR and extended MR. Each representation can further be divided into the current-controlled and the voltage-controlled forms, depending on whether a current source or a voltage source is used as the input signal [35].

In order to design a more precise quantitative model, the mathematical concept of unfolding of the extended MR [35] is introduced as follows

$$\begin{cases} u=R_M(x,i)\,i \\ R_M(x,0)\neq 0 \\ f_{RM}(x,i)=\dfrac{dx(t)}{dt}=a_{1R}x+a_{2R}x^2+\cdots+a_{mR}x^m \\ +b_{1R}i+b_{2R}i^2+\cdots+b_{nR}i^n+\sum_{j,k=1}^{p,r}c_{jkR}x^j i^k \end{cases} \quad (1)$$

where a_{jR}, b_{kR}, c_{jkR} are unfolding parameters of the MR. Different unfolding parameters can show different but similar fingerprint and frequency characteristics. Several examples are listed in Table 2.

TABLE 2. Several examples of MR unfolding parameters.

Example	MR Unfolding Parameters	Remarks
Ideal MR	$a_j=0, j=1,2,\cdots,m$; $b_1=1$, $b_k=0,k=2,3,\cdots,n$; $c_{jk}=0,j=1,2,\cdots,p$; $k=1,2,\cdots,r$	$u=R_M(x)i$, $i(t)=\frac{dq(t)}{dt}$
HP MR	$a_j=0,j=1,2,\cdots,m$; $b_1=\mu_v\left[\frac{R_{on}}{D}\right]$, $b_k=0,k=2,3,\cdots,n$; $c_{jk}=0,j=1,2,\cdots,p$; $k=1,2,\cdots,r$	Titanium-Dioxide (T_iO_2)
Generic MR	$a_j=0,j=1,2,\cdots,m$; $c_{jk}=0,j=1,2,\cdots,p$; $k=1,2,\cdots,r$	$u=R_M(x)i$, $f_M(x,i)=\frac{dx(t)}{dt}$
Extended MR	$c_{jk}=0,j=1,2,\cdots,p$; $k=1,2,\cdots,r$	$u=R_M(x,i)i$, $R_M(x,0)\neq\infty$, $f_M(x,i)=\frac{dx(t)}{dt}$

Notably HP memristor is an ideal MR. We can take its extended form as an example.

TABLE 3. Mamthematical model of memcapacitor.

MC	Flux-controlled	σ-controlled
Ideal MC	$\sigma=\hat{\sigma}(\varphi)$ or $q(t)=C_M(\varphi)u(t)$ where $u(t)=\frac{d\varphi(t)}{dt}$, $C_M(\varphi)\overset{\Delta}{=}\frac{d\hat{\sigma}(\varphi)}{d\varphi}$ is called the memcapacitance in Farad (F). The constitutive relation could be recovered to within an arbitrary initial charge value σ_0 from $C_M(\varphi)$ via $\hat{\sigma}(\varphi)=\sigma_0+\int_{-\infty}^{\varphi}C_M(\varphi)d\varphi$	$\varphi=\hat{\varphi}(\sigma)$ or $u(t)=g_{C_M}(\sigma)q(t)$ Where $q(t)=\frac{d\sigma(t)}{dt}$, $g_{C_M}(\sigma)\overset{\Delta}{=}\frac{d\hat{\varphi}(\sigma)}{d\sigma}$ is called the inverse memcapacitance. The constitutive relation could be recovered to within an arbitrary initial flux value φ_0 from $g_{CM}(\sigma)$ via $\hat{\varphi}(\sigma)=\varphi_0+\int_{-\infty}^{\sigma}g_{CM}(\sigma)d\sigma$
Generic MC	$q=C_M(x)u$, $f_M(x,u)=\frac{dx(t)}{dt}$	$u=g_{CM}(x)q$, $g_{C_M}(x,u)=\frac{dx(t)}{dt}$
Extended MC	$q=C_M(x,u)u$, $C_M(x,0)\neq\infty$, $f_M(x,u)=\frac{dx(t)}{dt}$	$u=g_{C_M}(x,u)q$, $g_{C_M}(x,0)\neq\infty$, $g_{C_M}(x,q)=\frac{dx(t)}{dt}$

B. MEMCAPACITOR AND MEMINDUCTOR

Similar to MR, MC and ML can also be written in three mathematical representations, and each one has two forms. Among them, two forms of a MC are the flux-controlled and σ-controlled and three mathematical models are ideal MC, generic MC and extended MC, as follows in Table 3.

TABLE 4. Mamthematical model of meminductor.

ML	charge-controlled	ρ-controlled
Ideal ML	$\rho=\hat{\rho}(q)$ or $\varphi(t)=L_M(q)i(t)$ where $i(t)=\frac{dq(t)}{dt}$, $L_M(q)\triangleq\frac{d\hat{\rho}(q)}{dq}$ is called the meminductance in Henry (H). The constitutive relation could be recovered to within an arbitrary initial flux value ρ_0 from $L_M(q)$ via $\hat{\rho}(q)=\rho_0+\int_{-\infty}^{q}L(q)dq$	$q=\hat{q}(\rho)$ or $i(t)=g_{L_M}(\rho)\varphi(t)$ where $\varphi(t)=\frac{d\rho(t)}{dt}$, $g_{L_M}(\rho)\triangleq\frac{d\hat{q}(\rho)}{d\rho}$ is called the inverse meminductance. The constitutive relation could be recovered to within an arbitrary initial charge value q_0 from $g_{LM}(\rho)$ via $\hat{q}(\rho)=q_0+\int_{-\infty}^{\rho}g_{L_M}(\rho)d\varphi$
Generic ML	$\varphi=L_M(q)i$ $f_M(x,i)=\frac{dx(t)}{dt}$	$i=g_{L_M}(x)\varphi$ $g_{L_M}(x,u)=\frac{dx(t)}{dt}$
Extended ML	$\varphi=L_M(x,i)i$ $L_M(x,0)\neq\infty$ $f_M(x,i)=\frac{dx(t)}{dt}$	$i=g_{L_M}(x,\varphi)\varphi$ $g_{L_M}(x,0)\neq\infty$ $g_{L_M}(x,\varphi)=\frac{dx(t)}{dt}$

Also, different forms of a ML are charge-controlled and ρ-controlled and three mathematical models, which are ideal ML, generic ML and extended ML and presented in Table 4.

Similar MR, the mathematical concept of unfolding of the extended MC is described as follows in (2)

$$\begin{cases} q = C_M(x,u)\,u \\ C_M(x,0)\neq 0 \\ f_{CM}(x,u)=\dfrac{dx(t)}{dt}=a_{1C}x+a_{2C}x^2+\cdots+a_{mC}x^m \\ +b_{1C}u+b_{2C}u^2+\cdots+b_{nC}u^n+\sum_{u,k=1}^{p,r}c_{jkC}x^j u^k \end{cases} \tag{2}$$

where a_{jC}, b_{kC}, c_{jkC} are MC's unfolding parameters. Different but similar fingerprint and frequency could be shown by different parameters.

And, the extended ML is described as follows in (3)

$$\begin{cases} \varphi = L_M(x,i)\,i \\ L_M(x,0)\neq 0 \\ f_M(x,i)=\dfrac{dx(t)}{dt}=a_{1L}x+a_{2L}x^2+\cdots+a_{mL}x^m \\ +b_{1L}u+b_{2L}u^2+\cdots+b_{nL}u^n+\sum_{u,k=1}^{p,r}c_{jkL}x^j u^k \end{cases} \tag{3}$$

where a_{jL}, b_{kL}, c_{jkL} are unfolding parameters of ML.

In order to express three mathematical models of a MC clearly, several examples of unfolding parameters are listed in Table 5. And, the similar examples of a ML are listed in Table 6.

TABLE 5. Several example of MC unfolding parameters.

Example	MC Unfolding Parameters	Remarks
Ideal MC	$a_j=0, j=1,2,\cdots,m$ $b_1=1,$ $b_k=0, k=2,3,\cdots,n$ $c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$q=C_M(\varphi)u$ $i(t)=\frac{dq(t)}{dt}$
Generic MC	$a_j=0, j=1,2,\cdots,m$ $c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$q=C_M(x)u$ $f_M(x,u)=\frac{dx(t)}{dt}$
Extended MC	$c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$q=C_M(x,u)u$ $C_M(x,0)\neq\infty$ $f_M(x,u)=\frac{dx(t)}{dt}$

TABLE 6. Several example of ML unfolding parameters.

Example	ML Unfolding Parameters	Remarks
Ideal ML	$a_j=0, j=1,2,\cdots,m$ $b_1=1,$ $b_k=0, k=2,3,\cdots,n$ $c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$\varphi=L_M(\varphi)i$ $u(t)=\frac{d\varphi(t)}{dt}$
Generic ML	$a_j=0, j=1,2\cdots,m$ $c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$\varphi=L_M(x)i$ $f_M(x,i)=\frac{dx(t)}{dt}$
Extended ML	$c_{jk}=0, j=1,2,\cdots,p;$ $k=1,2,\cdots,r$	$\varphi=L_M(x,i)i$ $L_M(x,0)\neq\infty$ $f_M(x,i)=\frac{dx(t)}{dt}$

III. FLOATING AND GROUNDED INTERFACE CIRCUIT AND CONSTRUCTED MEM-ELEMENTS EMULATORS

According to the mem-element circuit structure, the emulator can be divided into floating and grounded. The frequency characteristics of them are essential in measuring the nonvolatile effect and exploring applications. In this section, a floating novel mem-element interface circuits is proposed, which consists of four second-generation current conveyor operational amplifiers (AD844, U_1~U_4), a comparator (U_5), four resistors (R_1 ~ R_4), a capacitor (C_1), a multiplier, and four reserved ports (P_1~P_4), see Fig.2. Also, the grounded one is given as following in Fig.3. By connecting different parts between P_1-P_2 and P_3-P_4, the transformation among MR, MC, ML can be given simply and flexibly. Then, the fingerprints and frequency characteristics of three kinds of mem-elements are analyzed by computer simulations. The result shows that the proposed interface circuits have a wider frequency range than any existing ones.

The relationship between the current and voltage variables of each port of the AD844 can be expressed as follows:

$$\begin{pmatrix} V_x \\ I_y \\ I_z \\ V_0 \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} I_x \\ V_y \\ V_z \\ I_0 \end{pmatrix} \tag{4}$$

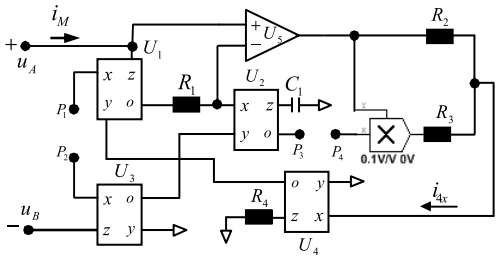

FIGURE 2. The floating mem-elements interface circuit.

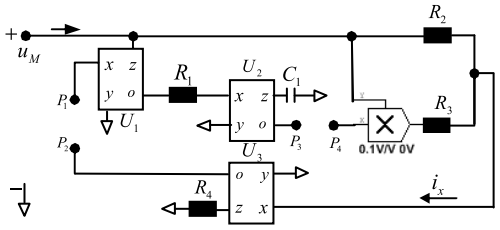

FIGURE 3. The grounded mem-elements interface circuit.

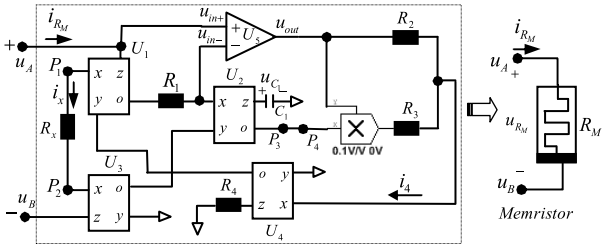

FIGURE 4. The floating MR emulator circuit and symbol.

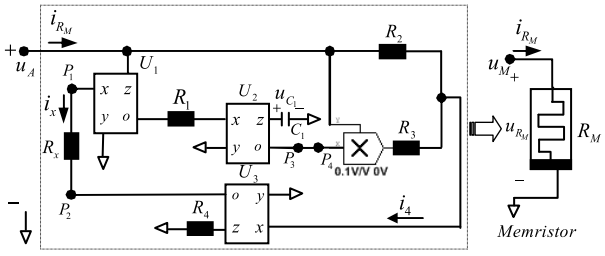

FIGURE 5. The grounded MR emulator circuit and symbol.

where V_x and I_x represent the voltage and current at the x pin, V_y and I_y represent the voltage and current at the y pin, and I_y is equal to zero; V_z and I_z represent the voltage and current at the output z pin, V_o and I_o represents the voltage and current of output o pin, respectively.

A. MEMRISTOR

1) MR EMULATOR AND MATHEMATICAL MODEL

When P_1 and P_2 are connected by a resistor (R_x), and P_3 and P_4 are connected directly, the interface circuit is equivalent to a MR emulator. The floating and grounded circuits are illustrated as shown (see Fig. 4 and Fig. 5). u_{AB} ($u_{AB} = u_{RM}$) is the excitation voltage applied across A and B.

The current i_{AB} ($i_{AB} = i_{RM}$) is flowing into A and flowing out from B. Let q_M and φ_M be the charge and flux of MR, respectively. The flux φ_{AB} is proportional to the time integral of voltage u_{AB} ($\varphi_{AB} = \varphi_M$). And let the q-φ relationship be presented:

$$\begin{cases} q(\varphi) = \alpha_1\varphi + \alpha_2\varphi^2 + \cdots + \alpha_m\varphi^m \\ \varphi(q) = \beta_1 q + \beta_2 q^2 + \cdots + \beta_n q^n \end{cases} \tag{5}$$

where $\alpha_1 \ldots \alpha_m$, and $\beta_1 \ldots \beta_n$ are coefficients of MR, m and n are integers.

$$\begin{cases} R_M = \dfrac{u(t)}{i(t)} = a + bq(t) \\ G_M = \dfrac{i(t)}{u(t)} = c + d\varphi(t) \end{cases} \tag{6}$$

where a represents the initial memristance in Ohm (Ω); c represents the initial memductance in Siemens (S); b and d are parameters; $q(t)$ is the accumulated charge; $\varphi(t)$ is the accumulated flux.

Taking the floating MR emulator as an example, the following shows the derivation process and memductance (G_M). As the relationship between the current and voltage variables of the AD844, the current i_{R1} flowing through R_1 is equal to the current -i_{C1} flowing through C_1, which can be calculated:

$$\begin{cases} u_{1o} = u_{1z} = u_A = u_{in+} \\ u_{2x} = u_{2y} = u_{3o} = u_{3z} = u_B = u_{in-} \end{cases} \tag{7}$$

and

$$\begin{cases} u_{out} = u_{in+} - u_{in-} = u_A - u_B = u_{AB} \\ i_{R1} = \dfrac{u_{1o} - u_{2x}}{R_1} = \dfrac{u_A - u_B}{R_1} = \dfrac{u_{AB}}{R_1} \\ i_{R1} = -i_{C1} \end{cases} \tag{8}$$

where u_{1o} and u_{1z} are the voltages of the o and z pins of U_1; u_{2x} and u_{2y} are the voltages of the x and y pins of U_2; u_{3o} and u_{3z} are the voltages of the o and z pins of U_3, u_{in+}, u_{in-} and u_{out} are the voltages of the input and output pins of U_5, respectively. The voltage u_{C1} across C_1 is proportional to the time integral of u_{AB}, thus u_{C1} can be obtained:

$$u_{C_1}(t) = \frac{1}{C_1}\int i_{C1}(t)\,dt = -\frac{\varphi_{AB}}{R_1 C_1} \tag{9}$$

Also, i_{4x} and i_{4z} are respectively the currents of the x and z pins of U_4, and $i_{4z} = i_{4x}$.

$$\begin{aligned} i_{4x} &= -\frac{1}{R_3}u_{C_1}\cdot u_{AB} - \frac{1}{R_2}u_{AB} \\ &= \frac{1}{R_3 R_1 C_1}\varphi_{AB}\cdot u_{AB} - \frac{1}{R_2}u_{AB} \end{aligned} \tag{10}$$

and

$$\begin{aligned} u_{4z} &= u_{4x} = i_{4x}R_4 \\ &= \frac{R_4}{R_3 R_1 C_1}\varphi_{AB}\cdot u_{AB} - \frac{R_4}{R_2}u_{AB} \end{aligned} \tag{11}$$

As previously mentioned, the current i_{Rx} flowing through R_x is equal to the current -i_{RM} flowing through R_M, and can be calculated as:

$$\begin{cases} u_{1x} = u_{1y} = u_{4o} = u_{4z} \\ i_{Rx} = -\dfrac{u_{1x} - u_{3x}}{R_x} = -\dfrac{u_{1x}}{R_x} \\ i_{R_M} = -i_{Rx} \end{cases} \tag{12}$$

TABLE 7. List of components used in this experimental testing of MR.

Components	Frequency
R_1 =320 $k\Omega$; R_2 =80 $k\Omega$; R_3 =12 $k\Omega$; R_4 =15 $k\Omega$; R_x =100 $k\Omega$;C_1 =80pF.	20 kHz ~ 130 kHz
R_1 =220 $k\Omega$; R_2 =100 $k\Omega$; R_3 =12 $k\Omega$; R_4 =15 $k\Omega$; R_x =100 $k\Omega$;C_1 =80pF.	10 kHz ~ 580 kHz
R_1 =100 $k\Omega$; R_2 =200 $k\Omega$; R_3 =12 $k\Omega$; R_4 =15 $k\Omega$; R_x =100 $k\Omega$;C_1 =80pF.	10 kHz ~ 900 kHz

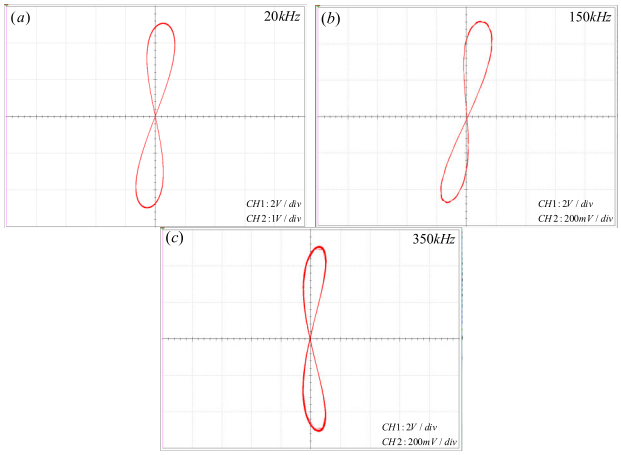

FIGURE 6. The experimentally measured curves of MR: (a) $v_{Rx} - v_{AB}$ under f =20kHz; (b) $v_{Rx} - v_{AB}$ under f = 150kHz; (c)$v_{Rx} - v_{AB}$ under f = 350kHz.

By substituting (9)-(11) into (12), i_{RM} can be calculated:

$$\begin{cases} i_{R_M} = \dfrac{R_4}{10R_xR_3R_1C_1}\varphi_{AB} \cdot u_{AB} - \dfrac{R_4}{R_xR_2}u_{AB} \\ u_M = u_{AB} \end{cases} \tag{13}$$

Finally, the memductance can be obtained:

$$G_M = \frac{i_{R_M}}{u_M} = \frac{R_4}{10R_xR_3R_1C_1}\varphi_M - \frac{R_4}{R_xR_2} \tag{14}$$

2) FINGERPRINT AND FREQUENCY

As we all know, the 'pinched hysteresis loop' is the only fingerprint of MR in the $v - i$ plane [3], [4], [35]. Here, the fingerprints are tested with a bipolar periodic input voltage signals which result in a periodic current response at the same frequency. Initial values of the excitation voltages $u(t) = \pm Usin(2\pi ft)$, U=5V and bias U_b=0.05V. The components used in this simulation are shown in Table 7. The fingerprints are shown in Fig.6.

It can be seen from Table 7 that resistors R_1 and R_2 are the key factors that affect the output frequency. When R_1 decreases and R_2 increases, we could obtain a wider frequency range, and vice versa. The result is that for G_M (see (6)), the frequency range of a MR is wider with a bigger parameter d and smaller c. Nevertheless, bias U_b is necessary in order to ensure the emulator operates correctly. The frequency range [10 kHz, 900 kHz] is the widest among the existing emulators and the highest frequency reaches 900kHz.

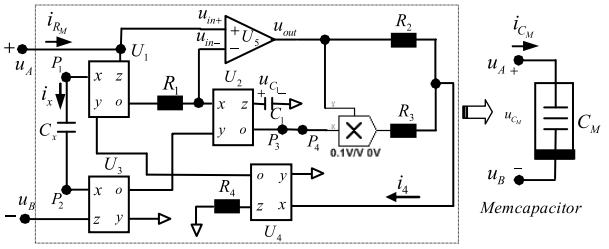

FIGURE 7. The floating MC emulator circuit and symbol.

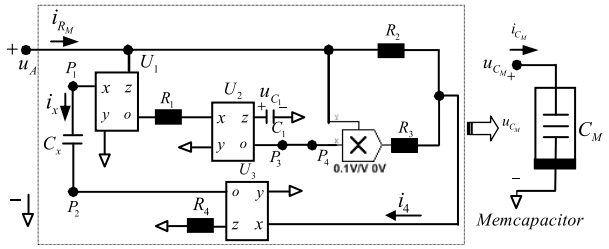

FIGURE 8. The grounded MC emulator circuit and symbol.

B. MEMCAPACITOR

1) mC EMULATOR AND MATHEMATICAL MODEL

When a capacitors (C_x) is connected cross P_1 and P_2, and P_3 and P_4 are tied together, the interface circuit is equivalent to a MC emulator. The floating and grounded MC emulators are illustrated in Fig. 7 and Fig. 8 with the excitation voltage $u_{AB} = u_{CM}$.

The current i_{AB} is flowing from A to B is equivalent to i_{CM} is flowing through the MC. The flux $\varphi_{AB} = \varphi_{CM}$ is proportional to the time integral of u_{CM}; q_{CM} and σ_M is proportional to the time integral of i_{CM} and q_{CM}, respectively. And Let the σ-φ relationship be presented:

$$\begin{cases} \sigma(\varphi) = \gamma_1\varphi + \gamma_2\varphi^2 + \cdots + \gamma_m\varphi^m \\ \varphi(\sigma) = \lambda_1\sigma + \lambda_2\sigma^2 + \cdots + \lambda_n\sigma^n \end{cases} \tag{15}$$

where $\gamma_1 \ldots \gamma_m$, and $\lambda_1 \ldots \lambda_n$ are coefficients, m and n are integers.

$$\begin{cases} C_M = \dfrac{q(t)}{u(t)} = a + b\varphi(t) \\ g_{C_M} = \dfrac{u(t)}{q(t)} = c + d\sigma(t) \end{cases} \tag{16}$$

where a represents the initial memcapacitance in Farad (F); c represents the initial inverse memcapacitance; c and d are coefficients; $\sigma(t)$ is proportional to the time integral of accumulated charge; $\varphi(t)$ is the accumulated flux.

Taking the floating MC emulator as an example, the following shows the derivation process and g_{MC}.

As previously mentioned, the accumulated q_{Cx} through C_x is equal to the accumulated charge -q_{CM} through C_M, and can be calculated as:

$$\begin{cases} i_{Cx} = -C_x\dfrac{d(u_{1x} - u_{3x})}{dt} = -C_x\dfrac{du_{1x}}{dt} \\ q(t) = \int i_{Cx}dt \\ i_{C_M} = -i_{Cx} \end{cases} \tag{17}$$

TABLE 8. List of components used in this experimental testing of MC.

Components	Frequency
R_1 =170 kΩ; R_3 =30 kΩ; R_2 =200 kΩ; R_4=30 kΩ; C_x =20pF;C_1=5pF; U_b=0V.	10 kHz ~ 200 kHz
R_1 =100 kΩ; R_3 =20 kΩ; R_2 =300 kΩ; R_4=30 kΩ; C_x =20pF;C_1 =5pF; U_b=0.09V	10 kHz ~ 300 kHz
R_1 =50 kΩ; R_3 =10 kΩ; R_2 =400 kΩ; R_4=30 kΩ; C_x =20pF;C_1 =5pF; U_b=0.2V	10 kHz ~ 540 kHz

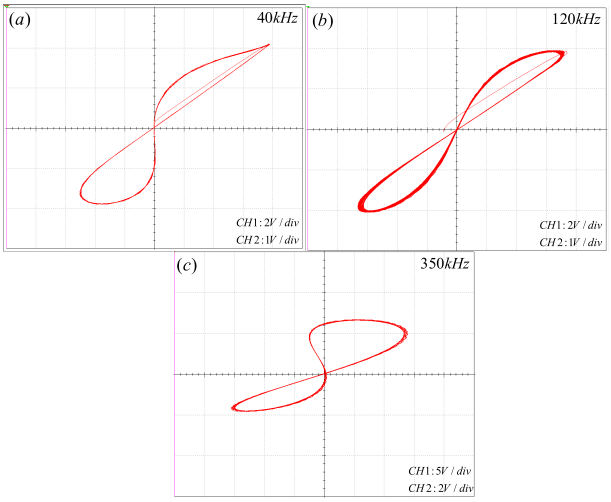

FIGURE 9. The experimentally measured curves of MR: (a)$v_{Cx} - v_{AB}$ under f =40kHz; (b)$v_{Cx} - v_{AB}$ under f = 120kHz; (c)$v_{Cx} - v_{AB}$ under f = 350kHz.

By substituting (9)-(11) into (17), q_{CM} can be calculated:

$$\begin{cases} q_{C_M} = C_x u_{1x} \\ = \dfrac{R_4 C_x}{10 R_3 R_1 C_1} \varphi_{AB} \cdot u_{AB} - \dfrac{R_4 C_x}{R_2} u_{AB} \\ u_M = u_{AB} \end{cases} \tag{18}$$

Finally, the memcapacitance can be obtained:

$$C_M = \frac{q_{C_M}}{u_M} = \frac{R_4 C_x}{10 R_3 R_1 C_1} \varphi_M - \frac{R_4 C_x}{R_2} \tag{19}$$

2) FINGERPRINT AND FREQUENCY

The excitation voltages $u(t)= \pm Usin(2\pi ft)$, U=4V and bias U_b are applied. The fingerprints and frequencies are tested. The components are shown in Table 8. And, fingerprints are shown in Fig.9.

It can be seen that resistors R_1, R_2 and R_3 are the important factors that affect the frequency characteristics. When R_1 and R_3 decreases and R_2 increases, we could obtain wider frequency range, and vice versa. The result is that for C_M (see (16)), the frequency range of a MC is wider with a bigger parameter b and smaller a. Nevertheless, bias U_b is necessary to make sure the emulator operates correctly. So far, the frequency range is the much wider than the existing emulators and the frequency is as high as 540kHz.

C. MEMINDUCTOR

1) ML EMULATOR AND MATHEMATICAL MODEL

When P_1 and P_2 are connected by R_x, and P_3 and P_4 are connected by an integrating circuit, the interface circuit is

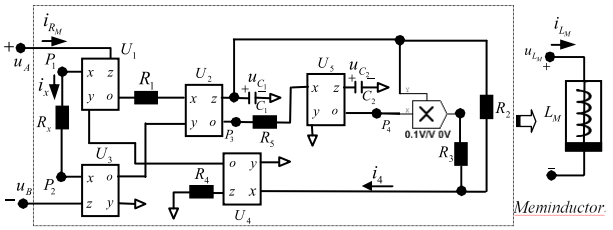

FIGURE 10. The floating MC emulator circuit and symbol.

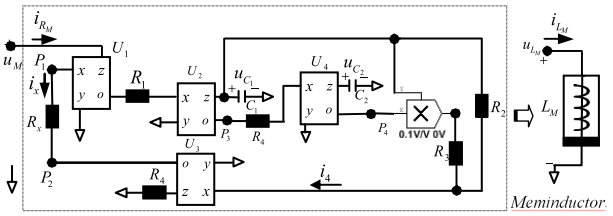

FIGURE 11. The grounded MC emulator circuit and symbol.

equivalent to a ML emulator. As shown in Fig. 10 and Fig. 11, the floating and grounded emulators can be illustrated.

The voltage $u_{AB} = u_{CM}$ is applied and the current i_{AB} ($i_{AB} = i_{LM}$) is obtained. The charge $q_{AB} = q_{LM}$ is proportional to the time integral of i_{LM}; φ_{LM} and ρ_M is proportional to the time integral of u_{LM} and φ_{LM}, respectively. And Let the q-ρ relationship be presented:

$$\begin{cases} q(\rho) = \omega_1 \rho + \omega_2 \rho^2 + \cdots + \omega_m \rho^m \\ \rho(q) = \mu_1 q + \mu_2 q^2 + \cdots + \mu_n q^n \end{cases} \tag{20}$$

where $\omega_1 \ldots \omega_m$, and $\mu_1 \ldots \mu_n$ are coefficients, m and n are integers.

$$\begin{cases} L_M = \dfrac{\varphi(t)}{i(t)} = a + bq(t) \\ g_{L_M} = \dfrac{i(t)}{\varphi(t)} = c + d\rho(t) \end{cases} \tag{21}$$

where a represents the initial meminductance in Henry (H); c represents the initial inverse meminductance; c and d are coefficients; $\rho(t)$ is proportional to the time integral of accumulated flux.

Taking the floating ML emulator as an example, the following shows the process and g_{ML}.

As previously mentioned, voltage u_{C2} across C_2 is proportional to the time integral of u_{C1}, and can be calculated as:

$$u_{C_2}(t) = -\frac{1}{C_2} \int \frac{u_{C1}(t)}{R_5} dt = \frac{\rho_{AB}}{R_1 R_5 C_1 C_2} \tag{22}$$

By substituting (9)-(11) and (22)into (12), i_{LM} can be calculated:

$$\begin{cases} i_{L_M} = i_x = -\dfrac{R_4}{R_x R_1 R_2 C_1} \varphi_{AB} \\ -\dfrac{R_4}{10 R_x R_1^2 R_3 R_5 C_1^2 C_2} \rho_{AB} \cdot \varphi_{AB} \\ \varphi_{AB} = \int u_{AB} dt \\ u_M = u_{AB} \end{cases} \tag{23}$$

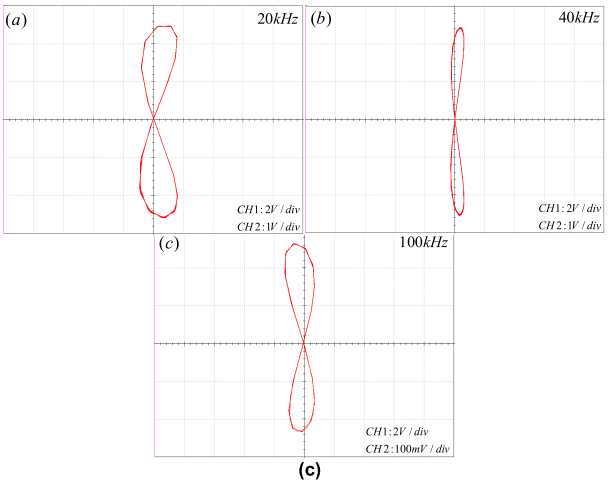

FIGURE 12. The experimentally measured curves of MR: (a)$v_{Rx} - v_{AB}$ under $f = 20kHz$; (b) $v_{Rx} - v_{AB}$ under $f = 40$kHz; (c)$v_{Rx} - v_{AB}$ under $f = 100kHz$.

TABLE 9. List of components used in this experimental testing of ML.

Components	Frequency
$R_3 = R_4 = 20\ k\Omega$; $C_1 = C_2 = 20$pF; $R_2 = 300\ k\Omega$; $R_1 = 300\ k\Omega$; $R_5 = 300\ k\Omega$; $R_x = 100\ k\Omega$; $U_b = -0.08V$	$9kHz \sim 35\ kHz$
$R_3 = R_4 = 15\ k\Omega$; $C_1 = C_2 = 10$pF; $R_2 = 200\ k\Omega$; $R_1 = 300\ k\Omega$; $R_5 = 300\ k\Omega$; $R_x = 100\ k\Omega$; $U_b = -0.1V$	$10\ kHz \sim 70\ kHz$
$R_3 = R_4 = 10\ k\Omega$; $C_1 = C_2 = 5$pF; $R_2 = 200\ k\Omega$; $R_1 = 300\ k\Omega$; $R_5 = 300\ k\Omega$; $R_x = 100\ k\Omega$; $U_b = -0.1V$	$15\ kHz \sim 130\ kHz$

Finally, the inverse meminductance can be obtained:

$$g_{L_M} = \frac{i_{L_M}}{\varphi_M} = \frac{R_4}{10R_xR_1^2R_3R_5C_1^2C_2}\rho_M + \frac{R_4}{R_xR_1R_2C_1} \quad (24)$$

2) FINGERPRINT AND FREQUENCY

When an excitation voltages $u(t) = \pm Usin(2\pi ft)$, $U=4.5V$ and bias U_b are applied, the tested fingerprints are shown in Fig.12. The components used and frequency obtained in this simulation are shown in Table 9.

From Table 9, there are more factors that affect the output frequency of ML than MR/MC, i.e. resistors $R_2 \sim R_4$, C_1 and C_2. When they decreases, we could obtain wider frequency range, and vice versa. The result is that for g_{LM} (see (21)), the bigger parameter c and d are, the wider the ML's frequency range is. Nevertheless, bias U_b is also necessary to ensure the emulator operates correctly. Although the circuit configuration of a ML is the most complex among mem-elements, there are still frequencies range from 9 kHz to $130\ kHz$, which is the widest one among existing single and bidirectional universal emulators.

IV. THE CHAOTIC SYSTEMSAND CIRCUITS

In the nonlinear circuits, frequency is considered to be the necessary condition for system oscillation and oscillators generation, and the oscillation is necessary for strange attractors. Therefore, studying on chaotic and hyper chaotic systems based on mem-elements is one of their important application fields. In this section, we designed the simplest

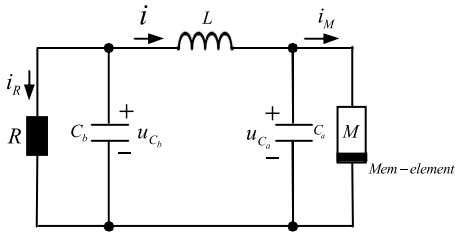

FIGURE 13. The simplest chaotic system based on the novel memory interface circuit.

chaotic circuit based on the proposed novel memory interface circuit as shown in Fig.13. When a MR / MC / ML is connected the block, strange attractors would be generated, and chaotic system model can be obtained.

The unified chaotic system with mem-element is shown as follows

$$\begin{cases} C_a\dfrac{du_{Ca}(t)}{dt} = i(t) - i_M(t) \\ C_b\dfrac{du_{Cb}(t)}{dt} = \dfrac{1}{R}u_{Cb}(t) - i(t) \\ L\dfrac{di(t)}{dt} = u_{Cb}(t) - u_{Ca}(t) \\ \dfrac{d\varphi(t)}{dt} = u_{Ca}(t)\ or \dfrac{dq(t)}{dt} = i_M(t) \\ \dfrac{d\rho(t)}{dt} = \varphi(t)\ \ or\ \ \dfrac{d\sigma(t)}{dt} = q(t) \end{cases} \quad (25)$$

where u_{Ca}, u_{Cb} represent the voltage of u_{Ca} and u_{Cb}; i_M represents the current of mem-element; $\varphi(t)$, $\rho(t)$, $q(t)$ and $\sigma(t)$ are proportional to the time integral of $u(t)$, $\varphi(t)$, $i(t)$ and $q(t)$, respectively.

A. MR HYPERCHAOTIC CIRCUIT AND MODEL

When the floating/grounded MR is implemented, the model is obtained as follows.

$$\begin{cases} \dfrac{du_{Ca}(t)}{dt} = \dfrac{1}{C_a}i(t) - \dfrac{G_M}{C_a}u_{Ca}(t) \\ \dfrac{du_{Cb}(t)}{dt} = \dfrac{1}{RC_b}u_{Cb}(t) - \dfrac{1}{C_b}i(t) \\ \dfrac{di(t)}{dt} = \dfrac{1}{L}\left[u_{Cb}(t) - u_{Ca}(t)\right] \\ \dfrac{d\varphi(t)}{dt} = u_{Ca}(t) \end{cases} \quad (26)$$

Let $u_{Ca} = x$, $u_{Cb} = y$, $i = z$, $\varphi = \omega$, $a = 1/C_a$, $b = 1/C_b$, $c = 1/RC_b$, $e = 1/L$, $m = R_4/(10R_xR_3R_1C_1C_a)$ and $n = R_4/(R_xR_2C_a)$, the time scale transformation is carried out. The generalized mathematical model can be simplified to

$$\begin{cases} \dfrac{dx}{dt} = az - (m\omega - n)x \\ \dfrac{dy}{dt} = cy - bz \\ \dfrac{dz}{dt} = e(y - x) \\ \dfrac{d\omega}{dt} = x \end{cases} \quad (27)$$

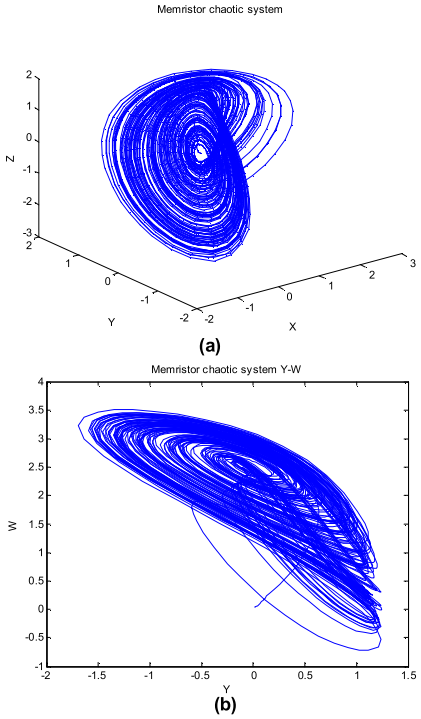

FIGURE 14. Strange attractor: (a) x-y-z; (b) y-w.

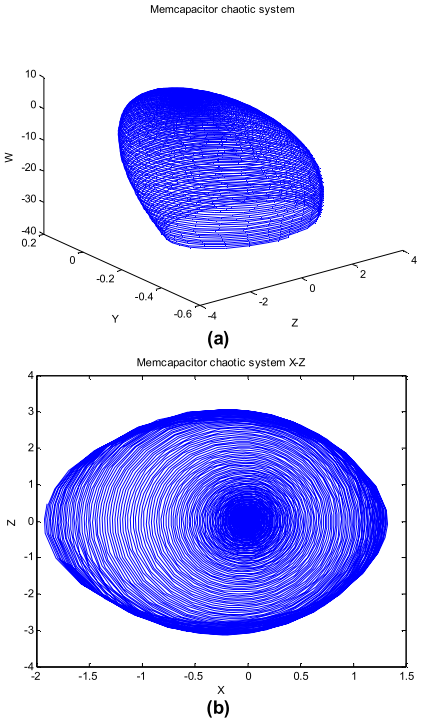

FIGURE 15. Strange attractor: (a) y-z-w; (b) x-z.

If $a = 1.5, b = e = 1, c = 0.95, n = 0.4, m = 0.8$, the initial condition is $[x, y, z, \omega] = [0.05, 0, 0.05, 0.05]$, a strange attractor is obtained as Fig.14.

The dynamics of the system is classified using its Lyapunov Exponents (*LEs*): (1) for stable state LE_1, LE_2, LE_3, $LE_4 < 0$; (2) for chaotic attractors $LE_1 > 0$, $LE_2 = 0$, LE_3, $LE_4 < 0$; (3) for hyper chaotic attractors $LE_1, LE_2 > 0, LE_3$, $LE_4 \leq 0$. And, the sign of the largest LE_{max} determines the relationship between all small perturbations and the state of the system. The *LEs* of system (27) are as follows: $LE_1 = 0.5211$, $LE_2 = 0.0472$, $LE_3 = 0$, $LE_4 = -0.0481$. Within the time interval, the system shows the hyper chaotic behavior quickly. It is a hyper chaotic system.

Based on the *LEs*, we also can calculate the Hausdroff (Lyapunov) dimension $D_L = 5.04$.

As can be seen from the above figure, this model exhibits unique dynamic characteristics. This phenomenon is not the same as other existing chaotic systems. Even if only one memristor is added in a traditional circuit, the experimental results are completely different from the original circuit.

B. MC HYPERCHAOTIC CIRCUIT AND MODEL

When floating/grounded MC is implemented, the model of this system is obtained as follows.

$$\begin{cases} \dfrac{du_{Ca}(t)}{dt} = \left(\dfrac{1}{C_a + C_M}\right) i(t) \\ \dfrac{du_{Cb}(t)}{dt} = \dfrac{1}{RC_b} u_{Cb}(t) - \dfrac{1}{C_b} i(t) \\ \dfrac{di(t)}{dt} = \dfrac{1}{L} \left[u_{Cb}(t) - u_{Ca}(t)\right] \\ \dfrac{d\varphi(t)}{dt} = u_{Ca}(t) \end{cases} \tag{28}$$

Let $u_{Ca} = x$, $u_{Cb} = y$, $i = z$, $\varphi = \omega$, $a = C_a$, $b = 1/C_b$, $c = 1/RC_b$, $e = 1/L$, $m = (R_4 C_x)/(10 R_3 R_1 C_1)$ and $n = (R_4 C_x)/R_2$, the time scale transformation is carried out. The generalized mathematical model can be written as

$$\begin{cases} \dfrac{dx}{dt} = \dfrac{1}{a + (m\omega - n)} z \\ \dfrac{dy}{dt} = cy - bz \\ \dfrac{dz}{dt} = e(y - x) \\ \dfrac{d\omega}{dt} = x \end{cases} \tag{29}$$

If $a = 2, b = 0.2, e = 6, c = 0.03, n = 0.2$, $m = 0.4$, the initial condition is $[x, y, z, \omega] = [0.015, 0, 0.015, 0.015]$, a "Hat-shaped" strange attractor of system (29) is given as Fig.15. Also, the *LEs* are as follows: $LE_1 = 0.1771$, $LE_2 = 0.0476$, $LE_3 = -0.031$, $LE_4 = -0.2216$. Within the time interval, the system shows the hyper chaotic behavior quickly. It is also a hyper chaotic system.

Based on the *LEs*, we also can calculate the Hausdroff (Lyapunov) dimension $D_L = 3.874$.

It can be seen from the above figure that if the memory element in Fig.13 is replaced with a MC, this model also has a unique chaotic phenomenon, which is different from the model (26). It can be said that, in the memory system, MCs are mainly used for storing energy similar to the traditional capacitor, but when it is added to a circuit, it gets completely different characteristics from the traditional energy storage circuit.

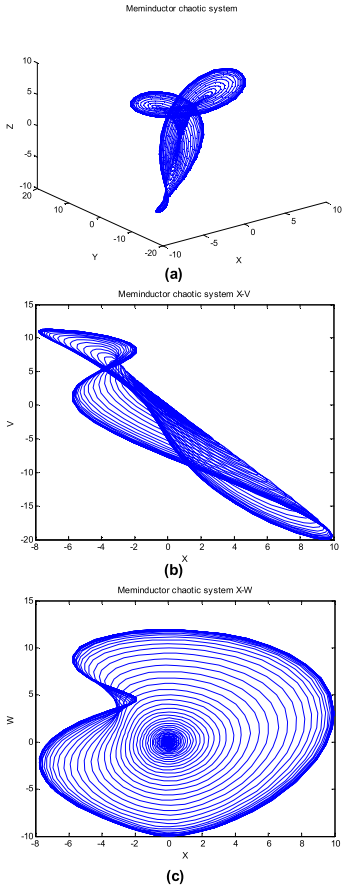

FIGURE 16. Strange attractor: (a) x-y-z; (b) x-v;(c) x-w.

C. ML HYPERCHAOTIC CIRCUIT AND MODEL

When floating/grounded ML is implemented, the model system is obtained as follows.

$$\begin{cases} \dfrac{du_{Ca}(t)}{dt} = \dfrac{1}{C_a} i(t) - g_{L_M} u_{Ca}(t) \\ \dfrac{du_{Cb}(t)}{dt} = \dfrac{1}{RC_b} u_{Cb}(t) - \dfrac{1}{C_b} i(t) \\ \dfrac{di(t)}{dt} = \dfrac{1}{L} \left[u_{Cb}(t) - u_{Ca}(t) \right] \\ \dfrac{d\varphi(t)}{dt} = u_{Ca}(t) \\ \dfrac{d\rho(t)}{dt} = \varphi(t) \end{cases} \tag{30}$$

Let $u_{Ca} = x$, $u_{Cb} = y$, $i = z$, $\varphi = \omega$, $\rho = v$, $a = 1/C_a$, $b = 1/C_b$, $c = 1/RC_b$, $e = 1/L$, $m = R_4/(10R_xR_1^2R_3R_5C_1^2C_2C_a)$ and $n = R_4/(R_xR_1R_2C_1C_a)$, the time scale transformation is carried out. The following generalized mathematics model can be obtained,

$$\begin{cases} \dfrac{dx}{dt} = az - (mv + n)\omega \\ \dfrac{dy}{dt} = cy - bz \\ \dfrac{dz}{dt} = e(y - x) \\ \dfrac{d\omega}{dt} = x \\ \dfrac{dv}{dt} = \omega \end{cases} \tag{31}$$

If $a = 2, b = 1.2, c = 0.18, e = 1, n = 2, m = 0.1$, the initial condition is $[x, y, z, \omega, v] = [0.01, 0.01, 0.01, 0.01, 0.01]$, a strange attractor is obtained as Fig.14. Also, the *LEs* are calculated as shown as the following: LE_1=*0.8675*, LE_2= *0.0054*, LE_3 = − *0.0439*, LE_4 = − *0.0556*, LE_5 = − *1.3525*. Within the time interval, the system shows the hyper chaotic behavior quickly. It is a hyper chaotic system.

Based on the *LEs*, we also can calculate the Hausdroff (Lyapunov) dimension D_L=*4.428*.

As can be seen that if a ML is substituted for the memory element in Fig. 13, the dynamics of this model is completely different from models (26) and (28). As a memory element, although the meminductor also has the ability to store energy similar to traditional inductors, when it is added to a circuit, it will also obtain completely different results from the characteristics of traditional circuits and other memory circuits.

V. CONCLUSION

In summary, an excellent quality emulator or related circuit is helpful to understand the nonvolatile and memory behaviors and explore potential applications. The memory interface circuit with a wide frequency range, less limitation, and high flexibility could provide convenience for this field.

In this paper, firstly, similar to MR, some information of MC and ML are been introduced, such as the mathematical model, classification and concept of unfolding with the extended formulation. Secondly, newly proposed floating and grounded memory interface circuits are presented, together with the mathematical model, fingerprints and frequency characteristics. In addition, we discuss the trends of several important components that affect the output frequency of mem-element circuits. Finally, we explore the application based on proposed interface circuits, i.e., the simplest chaotic circuit is designed. Also, the mathematics models, strange attractors, and Lyapunov exponents of MR/ MC/ ML chaotic system are given, respectively. There is no doubt that the good agreement among theoretical analysis, simulation and experimental results verifies the practicability and flexibility of these interface circuits. The proposed novel memory interface circuits could find potentials in electronic circuit engineering design in future.

Also, some limitations or challenges are involved in the proposed memory interface circuits, such as: i) extensive simulations are tested with NI Multisim and the circuit parameters are listed in detail but have not implemented in the actual circuit; ii) whether this circuits can be further optimized. Next, based on the parameters of memory interface circuits, the actual hardware platform should be built to overcome the above shortcomings. In addition, the compatibility of hardware devices will be comprehensively considered, the frequency range of the proposed interface circuit and the existence of bias voltage will also be verified.

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REFERENCES

[1] L. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.

[2] L. O. Chua and S. Mo Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[3] L. O. Chua, "Nonlinear circuit foundations for nanodevices. I. The four-element torus," *Proc. IEEE*, vol. 9, no. 11, pp. 1830–1859, Nov. 2003.

[4] L. O. Chua, "If it's pinched it's a memristor," *Semicond. Sci. Technol.*, vol. 29, no. 10, p. 104001, Sep. 2014.

[5] J. M. Tour and T. He, "The fourth element," *Nature*, vol. 453, no. 7191, pp. 42–43, Apr. 2008.

[6] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors," *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, Oct. 2009.

[7] M. Itoh and L. O. Chua, "Memristor Oscillators," *Int. J. Bifurcation Chaos*, vol. 18, no. 11, pp. 3183–3206, Nov. 2008.

[8] Z. Biolek, D. Biolek, and V. Biolkova, "Improved model of TiO_2 memristor," *Radioengineering*, vol. 24, no. 2, pp. 378–383, Jun. 2015.

[9] D. Yu, Z. Zhou, H. H.-C. Iu, T. Fernando, and Y. Hu, "A coupled memcapacitor emulator-based relaxation oscillator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 12, pp. 1101–1105, Dec. 2016.

[10] G. Y. Wang, J. L. He, F. Yuan, and C. J. Peng, "Dynamical behaviors of a TiO_2 memristor oscillator," *Chin. Phys. Lett.*, vol. 30, no. 11, Nov. 2013, Art. no. 110506.

[11] F. Yuan, G. Wang, and X. Wang, "Chaotic oscillator containing memcapacitor and meminductor and its dimensionality reduction analysis," *Chaos, Interdiscipl. J. Nonlinear Sci.*, vol. 27, no. 3, Mar. 2017, Art. no. 033103.

[12] J. Kengne, "On the dynamics of Chua's oscillator with a smooth cubic nonlinearity: Occurrence of multiple attractors," *Nonlinear Dyn.*, vol. 87, no. 1, pp. 363–375, Jan. 2017.

[13] C. Li, W. J.-C. Thio, H. H.-C. Iu, and T. Lu, "A memristive chaotic oscillator with increasing amplitude and frequency," *IEEE Access*, vol. 6, pp. 12945–12950, 2018.

[14] M. T. Abuelma'atti and Z. J. Khalifa, "A new floating memristor emulator and its application in frequency-to-voltage conversion," *Anal. Integr. Circuits Signal Process.*, vol. 86, no. 1, pp. 141–147, Jan. 2016.

[15] K. Rajagopal, J. R. Mboupda Pone, S. T. Kingni, S. Arun, and A. Karthikeyan, "Analysis and electronic implementation of an absolute memristor autonomous van der pol-duffing circuit," *Eur. Phys. J. Special Topics*, vol. 228, no. 10, pp. 2287–2299, Oct. 2019.

[16] C. Sánchez-López and L. E. Aguila-Cuapio, "A 860 kHz grounded memristor emulator circuit," *AEU-Int. J. Electron. Commun.*, vol. 73, pp. 23–33, Mar. 2017.

[17] W. Huang, Y.-W. Fang, Y. Yin, B. Tian, W. Zhao, C. Hou, C. Ma, Q. Li, E. Y. Tsymbal, C.-G. Duan, and X. Li, "Solid-state synapse based on magnetoelectrically coupled memristor," *ACS Appl. Mater. Interfaces*, vol. 10, no. 6, pp. 5649–5656, Feb. 2018.

[18] M. S. Feali, A. Ahmadi, and M. Hayati, "Implementation of adaptive neuron based on memristor and memcapacitor emulators," *Neurocomputing*, vol. 309, pp. 157–167, Oct. 2018.

[19] G. Ren, Y. Xu, and C. Wang, "Synchronization behavior of coupled neuron circuits composed of memristors," *Nonlinear Dyn.*, vol. 88, no. 2, pp. 893–901, Jan. 2017.

[20] J. K. Eshraghian, K. Cho, C. Zheng, M. Nam, H. H.-C. Iu, W. Lei, and K. Eshraghian, "Neuromorphic vision hybrid RRAM-CMOS architecture," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 12, pp. 2816–2829, Dec. 2018.

[21] M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, and R. W. Linderman, "Memristor crossbar-based neuromorphic computing system: A case study," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 25, no. 10, pp. 1864–1878, Oct. 2014.

[22] C. Chen, L. Li, H. Peng, Y. Yang, and T. Li, "Synchronization control of coupled memristor-based neural networks with mixed delays and stochastic perturbations," *Neural Process. Lett.*, vol. 42, no. 2, pp. 679–696, Jul. 2017.

[23] M. Zheng, L. Li, H. Peng, J. Xiao, Y. Yang, Y. Zhang, and H. Zhao, "Finite-time stability and synchronization of memristor-based fractional-order fuzzy cellular neural networks," *Commun. Nonlinear Sci. Numer. Simul.*, vol. 59, pp. 272–291, Jun. 2018.

[24] S. Choi, J. H. Shin, J. Lee, P. Sheridan, and W. D. Lu, "Experimental demonstration of feature extraction and dimensionality reduction using memristor networks," *Nano Lett.*, vol. 17, no. 5, pp. 3113–3118, May 2017.

[25] Y. Fan, X. Huang, Z. Wang, and Y. Li, "Nonlinear dynamics and chaos in a simplified memristor-based fractional-order neural network with discontinuous memductance function," *Nonlinear Dyn.*, vol. 93, no. 2, pp. 611–627, Mar. 2018.

[26] L. V. Gambuzza, M. Frasca, L. Fortuna, V. Ntinas, I. Vourkas, and G. C. Sirakoulis, "Memristor crossbar for adaptive synchronization," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 8, pp. 2124–2133, Aug. 2017.

[27] P. P. Singh and B. K. Roy, "Memristor-based novel complex-valued chaotic system and its projective synchronisation using nonlinear active control technique," *Eur. Phys. J. Special Topics*, vol. 228, no. 10, pp. 2197–2214, Oct. 2019.

[28] M. T. Abuelma'atti and A. Y. Alnafisa, "A memristor-based chaotic-masking for analog spread-spectrum communication," *Indonesian J. Electr. Eng. Comput. Sci.*, vol. 14, no. 2, pp. 966–971, May 2019.

[29] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves, Z. Li, J. P. Strachan, P. Lin, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, and Q. Xia, "Analogue signal and image processing with large memristor crossbars," *Nature Electron.*, vol. 1, no. 1, pp. 52–59, Jan. 2018.

[30] C.-L. Li, Z.-Y. Li, W. Feng, Y.-N. Tong, J.-R. Du, and D.-Q. Wei, "Dynamical behavior and image encryption application of a memristor-based circuit system," *AEU Int. J. Electron. Commun.*, vol. 110, Oct. 2019, Art. no. 152861.

[31] G. Zhang, J. Ma, A. Alsaedi, B. Ahmad, and F. Alzahrani, "Dynamical behavior and application in josephson junction coupled by memristor," *Appl. Math. Comput.*, vol. 321, pp. 290–299, Mar. 2018.

[32] A. Ascoli, F. Corinto, and R. Tetzlaff, "Generalized boundary condition memristor model," *Int. J. Circuit Theory Appl.*, vol. 44, no. 1, pp. 60–84, Jan. 2016.

[33] D. Yu, C. Zheng, H. H.-C. Iu, T. Fernando, and L. O. Chua, "A new circuit for emulating memristors using inductive coupling," *IEEE Access*, vol. 5, pp. 1284–1295, 2017.

[34] M. Chen, M. Sun, B. Bao, H. Wu, Q. Xu, and J. Wang, "Controlling extreme multistability of memristor emulator-based dynamical circuit in flux–charge domain," *Nonlinear Dyn.*, vol. 91, no. 2, pp. 1395–1412, Jan. 2018.

[35] L. Chua, "Resistance switching memories are memristors," *Appl. Phys. A, Solids Surf.*, vol. 102, no. 4, pp. 765–783, Jan. 2011.

[36] Y. V. Pershin and M. Di Ventra, "Memristive circuits simulate memcapacitors and meminductors," *Electron. Lett.*, vol. 46, no. 7, pp. 517–518, Apr. 2010.

[37] M. P. Sah, R. K. Budhathoki, C. Yang, and H. Kim, "Expandable circuits of mutator-based memcapacitor emulator," *Int. J. Bifurcation Chaos*, vol. 23, no. 05, May 2013, Art. no. 1330017.

[38] D. Yu, Y. Liang, H. H. C. Iu, and L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 10, pp. 758–762, Oct. 2014.

[39] C. Zheng, D. Yu, H. H. C. Iu, T. Fernando, T. Sun, J. K. Eshraghian, and H. Guo, "A novel universal interface for constructing memory elements for circuit applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4793–4806, Dec. 2019.

[40] Y. Liu and H. H. Iu, "Antimonotonicity, chaos and multidirectional scroll attractor in autonomous ODEs chaotic system," *IEEE Access*, vol. 8, pp. 1–8, 2020.

[41] B. Xu, G. Wang, and Y. Shen, "A simple meminductor-based chaotic system with complicated dynamics," *Nonlinear Dyn.*, vol. 88, no. 3, pp. 2071–2089, Feb. 2017.

[42] J. Kengne, A. N. Negou, and Z. T. Njitacke, "Antimonotonicity, chaos and multiple attractors in a novel autonomous jerk circuit," *Int. J. Bifurcation Chaos*, vol. 27, no. 7, Jun. 2017, Art. no. 1750100.

[43] L. Zhou, C. Wang, X. Zhang, and W. Yao, "Various attractors, coexisting attractors and antimonotonicity in a simple fourth-order memristive Twin-T oscillator," *Int. J. Bifurcation Chaos*, vol. 28, no. 04, Apr. 2018, Art. no. 1850050.

[44] C. Zheng, H. H. C. Iu, T. Fernando, D. Yu, H. Guo, and J. K. Eshraghian, "Analysis and generation of chaos using compositely connected coupled memristors," *Chaos, Interdiscipl. J. Nonlinear Sci.*, vol. 28, no. 6, Jun. 2018, Art. no. 063115.
[45] F. Gul, "Circuit implementation of nano-scale TiO_2 memristor using only metal-oxide-semiconductor transistors," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 643–646, Apr. 2019.
[46] H. Bao, N. Wang, H. Wu, Z. Song, and B. Bao, "Bi-stability in an improved memristor-based third-order wien-bridge oscillator," *IETE Tech. Rev.*, vol. 36, no. 2, pp. 109–116, Jan. 2018.
[47] S. Zhang and Y. Zeng, "A simple jerk-like system without equilibrium: Asymmetric coexisting hidden attractors, bursting oscillation and double full feigenbaum remerging trees," *Chaos, Solitons Fractals*, vol. 120, pp. 25–40, Mar. 2019.
[48] J. Vista and A. Ranjan, "A simple floating MOS-memristor for high-frequency applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 5, pp. 1186–1195, May 2019.
[49] J. Sun, Y. Wang, Y. Wang, and Y. Shen, "Finite-time synchronization between two complex-variable chaotic systems with unknown parameters via nonsingular terminal sliding mode control," *Nonlinear Dyn.*, vol. 85, no. 2, pp. 1105–1117, Mar. 2016.
[50] J. Sun, X. Zhao, J. Fang, and Y. Wang, "Autonomous memristor chaotic systems of infinite chaotic attractors and circuitry realization," *Nonlinear Dyn.*, vol. 94, no. 4, pp. 2879–2887, Aug. 2018.
[51] J. Sun, G. Han, Z. Zeng, and Y. Wang, "Memristor-based neural network circuit of full-function pavlov associative memory with time delay and variable learning rate," *IEEE Trans. Cybern.*, vol. 50, no. 7, pp. 2935–2945, Jul. 2019.
[52] G. Zhang, F. Wu, T. Hayat, and J. Ma, "Selection of spatial pattern on resonant network of coupled memristor and josephson junction," *Commun. Nonlinear Sci. Numer. Simul.*, vol. 65, pp. 79–90, Dec. 2018.
[53] C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, and Q. Xia, "Efficient and self-adaptive *in-situ* learning in multilayer memristor neural networks," *Nature Commun.*, vol. 9, no. 1, p. 2385, Jun. 2018.
[54] M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia, and J. P. Strachan, "Memristor-based analog computation and neural network classification with a dot product engine," *Adv. Mater.*, vol. 30, no. 9, Jan. 2018, Art. no. 1705914.
[55] J. Lee, J. K. Eshraghian, M. Jeong, F. Shan, H. H.-C. Iu, and K. Cho, "Nano-programmable logics based on double-layer anti-facing memristors," *J. Nanoscience Nanotechnol.*, vol. 19, no. 3, pp. 1295–1300, Mar. 2019.
[56] Y. Zhang, Z. Liu, H. Wu, S. Chen, and B. Bao, "Two-memristor-based chaotic system and its extreme multistability reconstitution via dimensionality reduction analysis," *Chaos, Solitons Fractals*, vol. 127, pp. 354–363, Oct. 2019.
[57] L. Wang, T. Dong, and M.-F. Ge, "Finite-time synchronization of memristor chaotic systems and its application in image encryption," *Appl. Math. Comput.*, vol. 347, pp. 293–305, Apr. 2019.
[58] M. E. Fouda and A. G. Radwan, "Memristor-less current- and voltage-controlled meminductor emulators," in *Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Marseille, France, Dec. 2014, pp. 279–282.
[59] Q. Lai, P. D. K. Kuate, F. Liu, and H. H.-C. Iu, "An extremely simple chaotic system with infinitely many coexisting attractors," *IEEE Trans. Circ. Syst. II, Exp. Briefs.*, vol. 67, no. 6, pp. 1129–1133, Jun. 2020.

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