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Switched-Capacitor LLC Resonant DC-DC Converter With Switch Peak Voltage of Vin/2

GUILHERME MARTINS LEANDRO[1] AND IVO BARBI[2], (Life Fellow, IEEE)
[1]Brazilian Power Electronics and Renewable Energy Institute (IBEPE), Florianópolis 88056-000, Brazil
[2]Federal University of Santa Catarina (UFSC), Florianópolis 88040-900, Brazil

Corresponding author: Ivo Barbi (ivobarbi@gmail.com)

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ABSTRACT A DC-DC hybrid switched-capacitor LLC resonant converter integrating a ladder cell at the input of the LLC resonant converter using frequency modulation is proposed in this paper. This converter has six switches that are subjected to half the voltage of the input source. All switches commutate at zero voltage over the entire load range, and the diodes of the output rectifier bridge commutate at zero current. The proposed converter has the following characteristics: (a) symmetrical operation, (b) simple frequency modulation, (c) commutation of all switches at zero voltage, (d) all switches subjected to half the input voltage, and (e) static gain practically immune to load variations. Theoretical analysis, design, and experimental results in the laboratory for a prototype of 2 kW, 1000 VDC input, 48 VDC output, and 90 kHz switching frequency are included in this study. The maximum efficiency measured was 97.3%.

INDEX TERMS DC-DC converter, LLC, resonant converter, switched-capacitor, zero voltage switching.

I. INTRODUCTION

Resonant converters are widely used when a high energy density is desired, as they facilitate soft commutation of their switches, which enables the use of high switching frequencies and thereby reductions in the weight and volume of magnetic devices.

The pioneer device among resonant converters was the resonant series converter [1] proposed by Schwarz in the 1970s, which has been widely used since then due to its characteristics of a high switching frequency, a high power density, low switching losses, and sinusoidal currents in the components, which means low EMI emission.

The resonant series converter was used while disregarding the effects of the magnetizing inductance until the 1990s, when Furukawa *et al.* decided not to neglect this effect, giving rise to the LLC resonant converter [2]. This converter has since been widely used in applications such as battery chargers, fuel cells, distribution systems, wireless power transfer systems, space applications, and cell phone chargers [3]–[8].

The LLC converter is widely used due to its main characteristics, such as high power density, high efficiency, possibility of regulating the output voltage through small variations in the switching frequency, ZVS-type soft commutation over the entire operating range in primary MOSFETs and ZCS-type soft switching of output diodes operating below resonance, and all of the parasitic elements being used to achieve ZVS commutation of switches [9]–[14].

Despite these advantages of the LLC converter over other isolated DC-DC converters, the switches are subjected to the input voltage, which makes its use difficult in applications where this voltage is high, for example, when the voltage comes from the output of a three-phase PWM rectifier with active power factor correction or in PV generation and direct current microgrid applications.

In [15], a topological variation of the three-level LLC converter is presented, in which two input capacitors associated in series are used to divide the input voltage into equal parts. For the converter to work correctly, the voltages across the two input capacitors must be the same. However, in the proposed converter, voltage equalization does not occur naturally, requiring additional voltage and control sensors, which increases the complexity of the converter proposed by the authors. This topic is not discussed in the publication.

In [16], a three-level LLC converter is studied. Despite the proposed topology preserving all the advantages of the original full bridge LLC converter and reducing the voltages on the switches, it also requires the use of two capacitors associated in series at the input, whose voltages must

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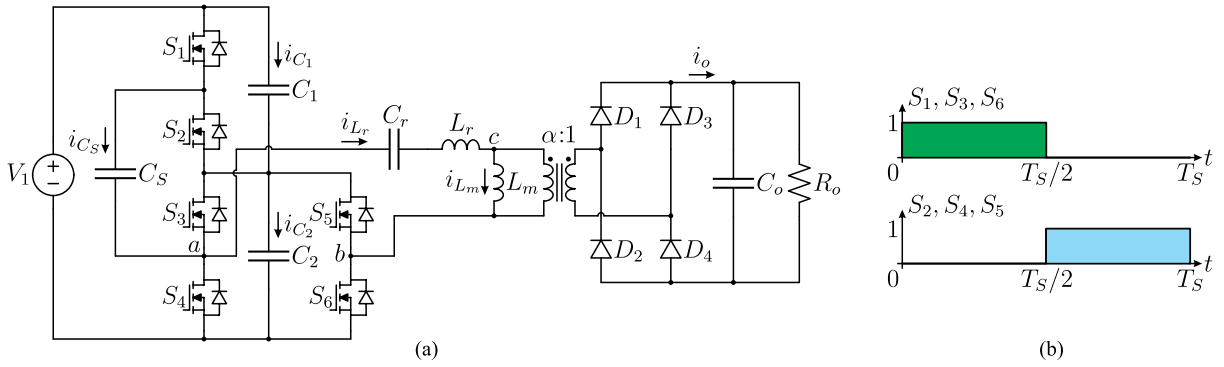

FIGURE 1. (a) DC-DC hybrid switched-capacitor LLC resonant converter, and (b) gate signals.

be equalized. This disadvantage is not mentioned or discussed in the publication.

In the topology presented in [17], the switches are subjected to half the voltage of the input power supply. However, this topology requires two isolation transformers, two resonant capacitors and an unusual configuration of the output rectifier. In addition, the analysis and design are more complex than those for the conventional LLC converter.

So-called hybrid converters are designed to encompass the characteristics of two or more distinct converters in one converter. Therefore, the integration of converters and technologies already existing in the literature is widely used to improve the topologies already consolidated [18], [19]. In the 1990s, the first study that used the ladder switched-capacitor cell also appeared in the literature [20]. This cell proved to be easy to integrate with other topologies, and it has been widely used since then as a way to reduce voltage stress on components [18], [21].

This paper aims to investigate the integration of the ladder switched-capacitor cell with the LLC resonant converter. We will demonstrate that the proposed converter has the main characteristics of the LLC converter, such as soft commutation (ZVS) of all switches, high immunity of the static gain to load variations, and symmetrical operation of the isolation transformer, with the advantage of semiconductors being subjected to half the voltage of the input source, which allows the use of low-voltage switches. The commutation of rectifier diodes occurs at zero current, further contributing to the converter efficiency.

Another important advantage of the proposed solution, regarding the solutions employing the three-level technique, is the natural equalization of the voltages across the capacitors associated in series, without the need for voltage sensors or control of individual voltages.

In Section II, the operation of the proposed converter is described, while the theoretical analysis is presented in Section III. Section IV addresses commutation analysis. Section V discusses the converter design and the experimental results obtained from the prototype in the laboratory.

II. PROPOSED CONVERTER AND OPERATION

The proposed DC-DC hybrid switched-capacitor LLC resonant converter and its gate signals are shown in Fig. 1. This converter consists of an LLC converter with a switched-capacitor cell integrated into its input, formed by divider capacitors C_1 and C_2 and switched capacitor C_S, in addition to the insertion of two new switches into the LLC converter (S_1 and S_2).

The ladder cell integration aims to reduce voltage stresses on the switches to half the input voltage, preserving the main characteristics of the LLC resonant converter.

Considering that the ladder cell always works in the incomplete charge/discharge mode [22], the proposed converter has three modes of operation, i.e., below the resonant frequency, above the resonant frequency, and at the resonant frequency. It is not recommended to work above the resonant frequency, as commutation in rectifier bridge diodes becomes forced, which increases commutation losses, thus affecting the converter efficiency. For the commutation of the rectifying diodes of the output stage to be soft ZCS type, it is necessary that the converter operate at a frequency lower than, but close to, the resonance frequency, where there is a region that provides soft commutation of the ZVS type for the active switches of the converter.

The converter operating below the resonant frequency presents eight topological states throughout the commutation period, which are represented in Fig. 2, while their main waveforms are shown in Fig. 3. Since the converter is symmetrical, the first four topological stages are described below, and as simplifications, ideal power semiconductors are considered, while dead time is disregarded.

A. $t_0 \le t \le t_1$ [SEE FIG. 2(a)]

At time t_0, switches S_2, S_4 and S_5 are blocked, while switches S_1, S_3 and S_6 are turned on. Voltages v_{ab} and v_{cb} are positive, and $V_o' > V_{C2}$. The resonant and magnetizing currents are both negative, i_{Lr} increases sinusoidally, and i_{Lm} increases linearly. This stage ends at t_1 when the resonant current is zero.

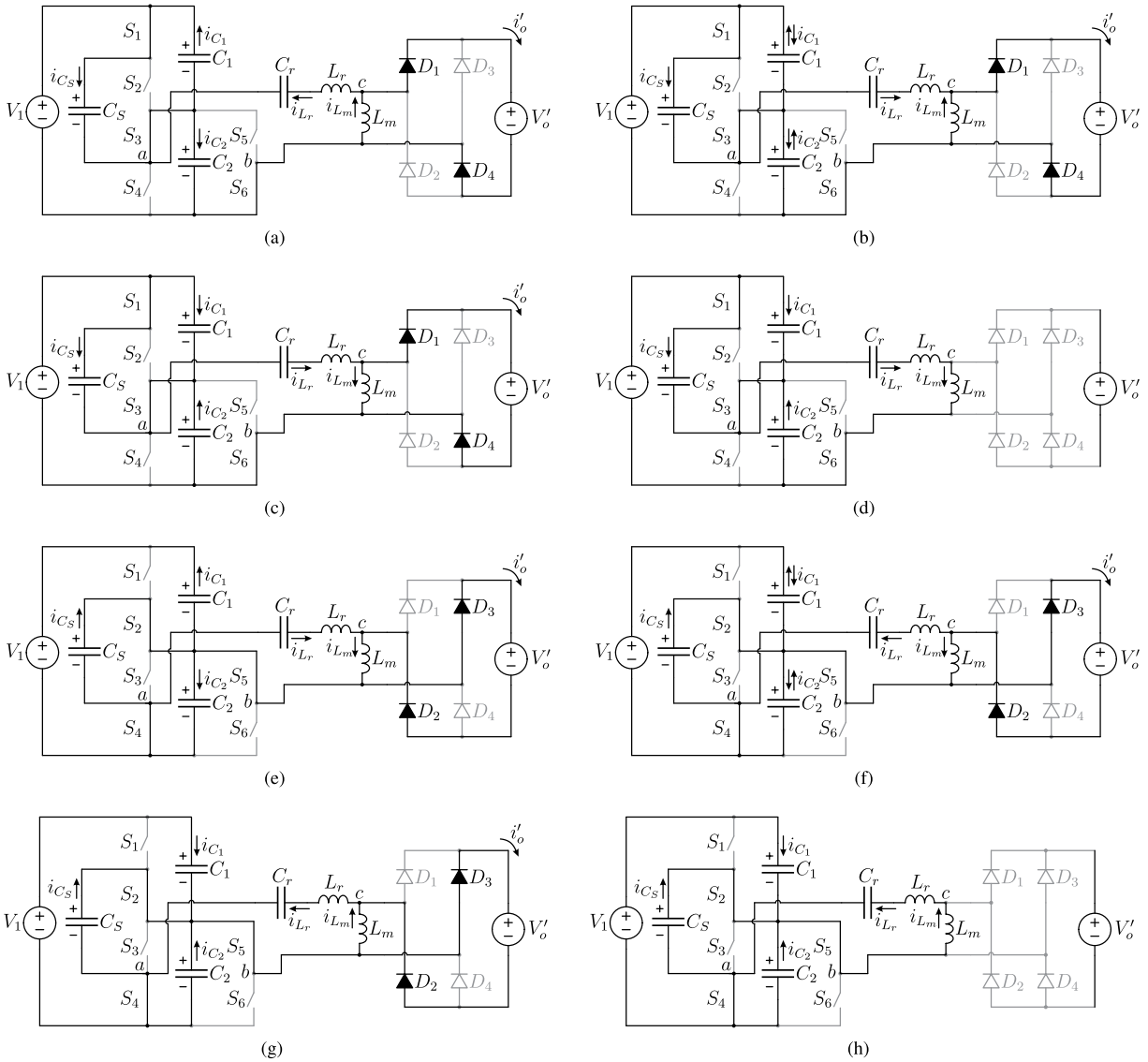

FIGURE 2. Topological stages of the proposed DC-DC hybrid switched-capacitor LLC resonant converter. (a) First, (b) second, (c) third, (d) fourth, (e) fifth, (f) sixth, (g) seventh, and (h) eighth.

B. $t_1 \le t \le t_2$ [SEE FIG. 2(b)]

At time t_1, the resonant current becomes positive and still increases sinusoidally, while i_{Lm} is negative and increases linearly. This stage ends at t_2, when the magnetizing current is zero.

C. $t_2 \le t \le t_3$ [SEE FIG. 2(c)]

At time t_2, the magnetizing current becomes positive. The resonant and magnetizing currents are now both positive. This stage ends at t_3, when the resonant current equals the magnetizing current, implying that the current in the transformer secondary winding is zero, which means that the diodes of the output rectifier commutate with no losses.

D. $t_3 \le t \le t_4$ [SEE FIG. 2(d)]

At time t_3, the resonant and magnetizing currents are equal and remain the same until the end of this stage, which occurs in $T_S/2$. The current in the transformer secondary winding remains zero, allowing rectifier bridge diodes to start conducting with zero current in the next stage; then, the phenomenon described in the literature as ZCS occurs. At the end of the stage, voltage v_{ab} undergoes polarity inversion when switches S_2, S_4 and S_5 are gated ON and S_1, S_3 and S_6 are turned OFF.

III. THEORETICAL ANALYSIS

A. STEADY STATE ANALYSIS-PART 1

To simplify the steady-state analysis of the proposed converter, it is assumed that the voltage across capacitor C_2, i.e., v_{C_2}, is practically constant throughout the commutation period. Thus, it can be treated as a voltage source, which characterizes a conventional LLC converter considering switches S_3, S_4, S_5 and S_6 onward.

The analysis is based on the first harmonic approximation (FHA) [23], which has been used several times for LLC

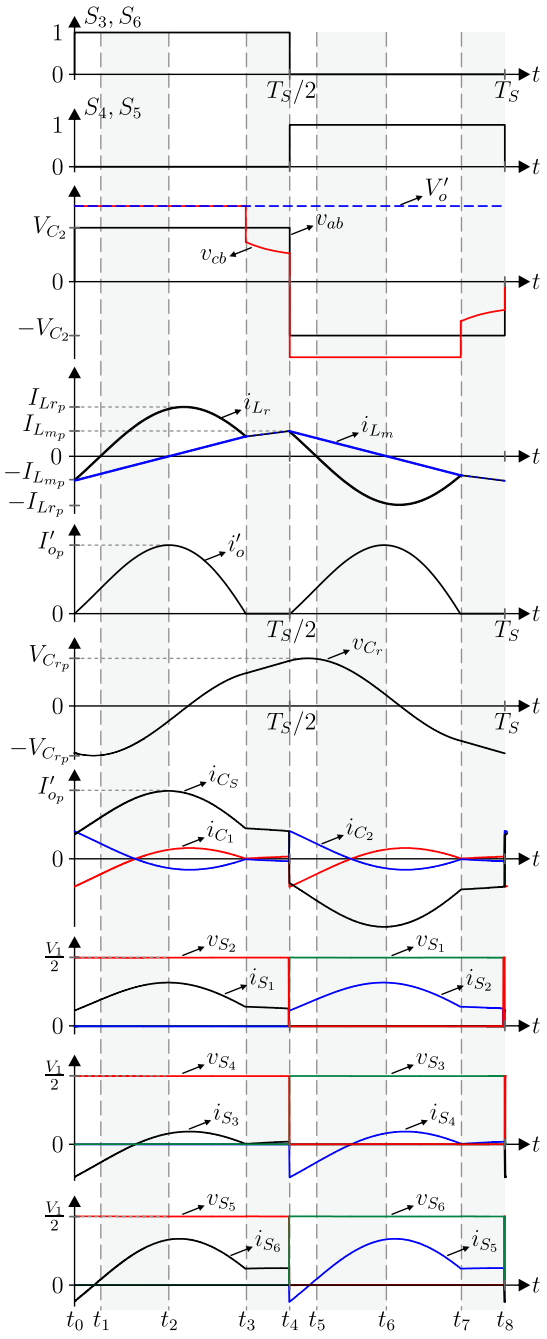

FIGURE 3. Typical theoretical waveforms of the hybrid LLC converter for operation below the resonant frequency.

analysis [14], [24], [25]. The fundamental component of the voltage generated between points a and b is

$$v_{ab1}(t) = \frac{4(V_1/2)}{\pi} sin(\omega_s t) \tag{1}$$

The voltage source (v_{th}) and the impedance (Z_{th}) of the Thevenin equivalent circuit are

$$v_{th1} = v_{ab1} \frac{\omega_s^2 C_r L_m}{\omega_s^2 C_r (L_r + L_m) - 1} \tag{2}$$

$$Z_{th} = j \frac{L_m \left(\omega_s^2 L_r C_r - 1\right)}{\omega_s^2 C_r \left(L_m + L_r\right) - 1} \tag{3}$$

Thus, the static gain is given by

$$q = \frac{f_n^2}{\sqrt{\left[f_n^2(\lambda+1) - \lambda\right]^2 + \left[f_n Q \left(f_n^2 - 1\right)\right]^2}} \tag{4}$$

where

$$\begin{cases} \lambda = \dfrac{L_r}{L_m} \\ f_o = \dfrac{2\pi}{\sqrt{C_r L_r}} \\ f_n = \dfrac{f_s}{f_o} \\ R_{ac} = R'_o \dfrac{8}{\pi^2} \\ Q = \dfrac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \end{cases} \tag{5}$$

The static gain curve as a function of the normalized switching frequency is shown in Fig. 4, where the regions where ZVS and ZCS occur are highlighted.

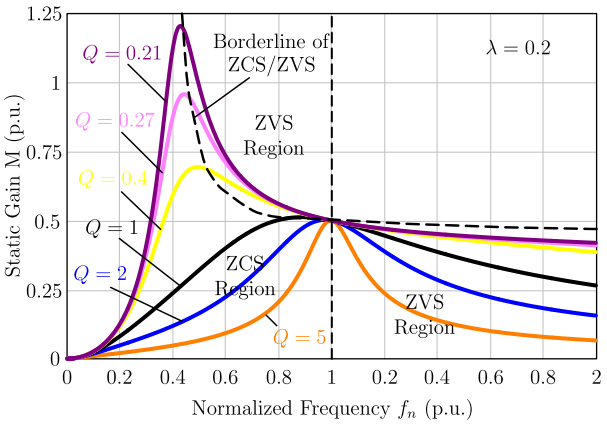

FIGURE 4. Static voltage gain of the hybrid LLC converter as a function of the normalized frequency for different quality factors.

B. STEADY STATE ANALYSIS-PART 2

To simplify the analysis, it is also assumed that the resonant stage can be replaced by a sinusoidal current source at terminals a and b.

Fig. 5 shows the corresponding equivalent circuit, where the current $i_{L_r}(t)$ is given by

$$i_r(t) = I_r sin(\omega_o t + \phi) \tag{6}$$

The capacitances of the switched capacitor stage are the same and defined as

$$C_1 = C_2 = C_S = C \tag{7}$$

Applying Kirchhoff's voltage and current laws yields

$$4R_{DSon} \frac{di_{C_1}}{dt} + \frac{3}{C} i_{C_1} = R_{DSon} \frac{di_r}{dt} + \frac{i_r}{C} \tag{8}$$

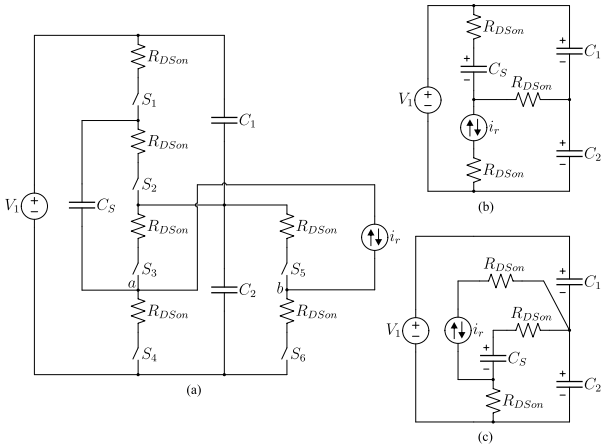

FIGURE 5. (a) Consideration of the LLC converter as a current source, and (b) first and (c) second topological stages.

The solution of (8) allows determination of the currents in the other switched capacitors and therefore their respective voltages. Thus, the equivalent resistance of the switched capacitor stage can be determined as follows:

$$R_{eq} = \frac{\frac{V_1}{2} - V_{C_2 avg}}{I_{avg}} \tag{9}$$

Appropriate substitutions and algebraic manipulation gives

$$\overline{R_{eq}}(\alpha) = \frac{R_{eq}}{R_{DSon}} = K_1 K_2 - K_3 \left(K_4 - K_5\right) \tag{10}$$

where

$$\begin{cases} K_1 = \dfrac{3 + 16\pi^2\alpha^2 + 2\pi\alpha tan\phi}{6\alpha\left(9 + 64\pi^2\alpha^2\right)\left(1 - e^{-\frac{3}{8\alpha}}\right)} \\ K_2 = \left(3 + 16\alpha - (16\alpha - 9)\, e^{-\frac{3}{8\alpha}}\right) \\ K_3 = \dfrac{2\pi}{9 + 64\pi^2\alpha^2} \\ K_4 = \dfrac{4\alpha - 3 - 16\pi^2\alpha^2}{4\pi\alpha} \\ K_5 = \dfrac{12 + 64\pi^2\alpha^2 + 4\pi^2\alpha}{8\pi^2\alpha} tan\phi \end{cases} \tag{11}$$

$$\alpha = R_{DSon} C f_s \tag{12}$$

The normalized value of the equivalent resistance, given by equation (12), is plotted in Fig. 6(b). The value of $\overline{R_{eq}}$ decreases as the normalized frequency α increases. After α reaches a value of appoximately 0.4, the equivalent resistance remains practically constant and equal to 2.

$$\overline{R_{eq}}_{min}(\alpha) = \lim_{\alpha \to \infty} \overline{R_{eq}} = 2 \tag{13}$$

The equivalent steady-state circuit in terms of average values is shown in Fig. 6(a), while the $\overline{R_{eq}}(\alpha)$ curve as a function of α is shown in Fig. 6(b). Thus, the stage already has the minimum equivalent resistance for α greater than approximately 0.4; thus, it is recommended to work with $\alpha > 0.4$.

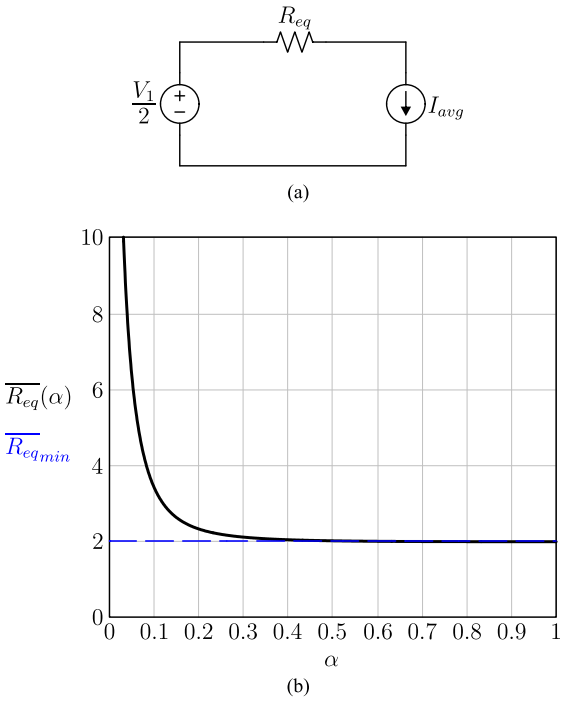

FIGURE 6. (a) Hybrid switched-capacitor equivalent circuit, and (b) parameterized equivalent resistance as a function of α.

IV. COMMUTATION ANALYSIS

At instant $t = t_4$, power semiconductors S_1, S_3 and S_6 are turned OFF, and commutation from S_1, S_3 and S_6 to S_2, S_4 and S_5 is initiated. The topological states for the different time intervals are shown in Fig. 7, while the relevant waveforms are represented in Fig. 8.

Applying Kirchhoff's voltage law, we find

$$\begin{cases} v_{C_{S_1}}(t) + v_{C_{S_2}}(t) = V_{C_1} \\ v_{C_{S_3}}(t) + v_{C_{S_4}}(t) = V_{C_2} \\ v_{C_{S_5}}(t) + v_{C_{S_6}}(t) = V_{C_2} \end{cases} \tag{14}$$

Thus,

$$\begin{cases} \dfrac{d}{dt}\left(\dfrac{q_{C_{S_1}}(t)}{C_{S_1}}\right) + \dfrac{d}{dt}\left(\dfrac{q_{C_{S_2}}(t)}{C_{S_2}}\right) = \dfrac{dV_{C_1}}{dt} \\ \dfrac{d}{dt}\left(\dfrac{q_{C_{S_3}}(t)}{C_{S_3}}\right) + \dfrac{d}{dt}\left(\dfrac{q_{C_{S_4}}(t)}{C_{S_4}}\right) = \dfrac{dV_{C_2}}{dt} \\ \dfrac{d}{dt}\left(\dfrac{q_{C_{S_5}}(t)}{C_{S_5}}\right) + \dfrac{d}{dt}\left(\dfrac{q_{C_{S_6}}(t)}{C_{S_6}}\right) = \dfrac{dV_{C_2}}{dt} \end{cases} \tag{15}$$

After appropriate substitution and algebraic manipulation, we find

$$\begin{cases} i_{C_{S_1}}(t) = -i_{C_{S_2}}(t) \\ i_{C_{S_3}}(t) = -i_{C_{S_4}}(t) \\ i_{C_{S_5}}(t) = -i_{C_{S_6}}(t) \end{cases} \tag{16}$$

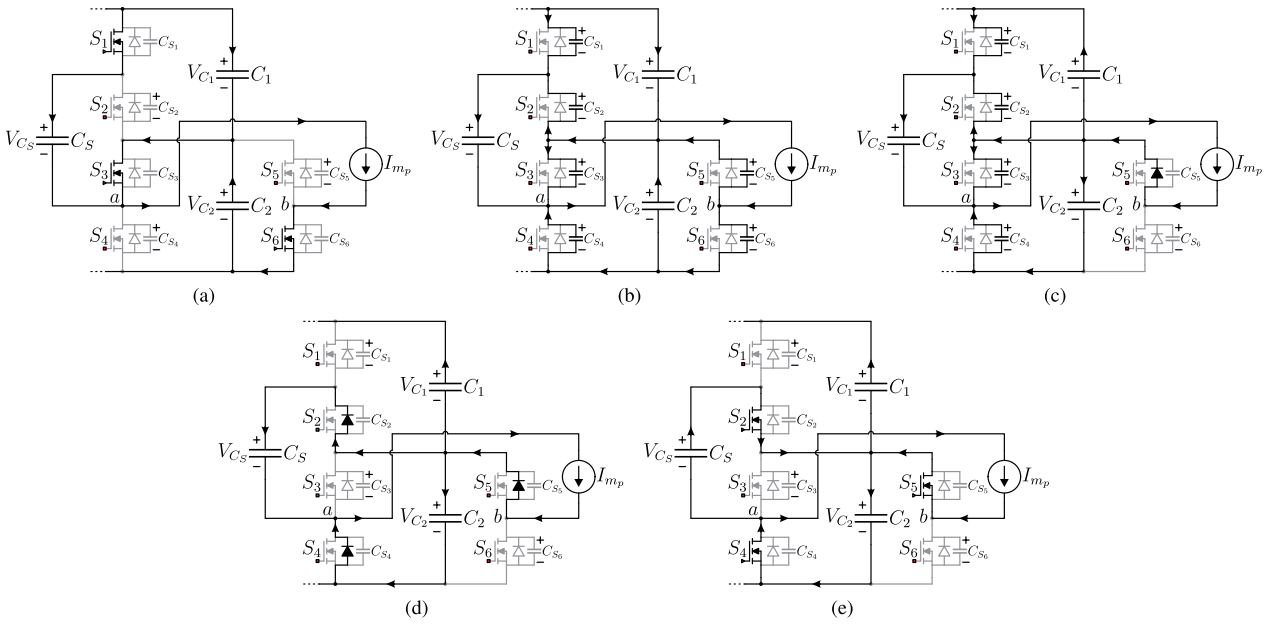

FIGURE 7. Topological stages during the commutation time interval. (a) First, (b) second, (c) third, (d) fourth, and (e) fifth stages.

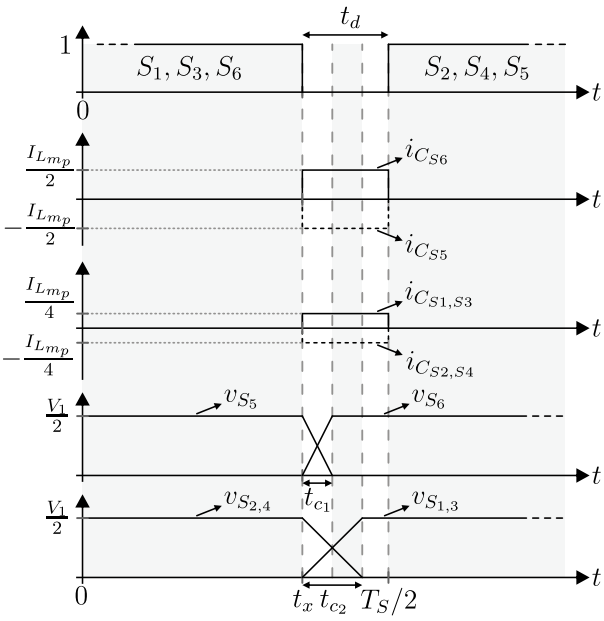

FIGURE 8. Commutation waveforms on switches.

Applying Kirchhoff's current law, we find

$$\begin{cases} i_{C_S}(t) = i_{C_{S_1}}(t) - i_{C_{S_2}}(t) \\ i_{C_{S_3}}(t) - i_{C_{S_4}}(t) + i_{C_S}(t) = I_{m_p} \\ i_{C_{S_6}}(t) - i_{C_{S_5}}(t) = I_{m_p} \end{cases} \tag{17}$$

With appropriate substitution, we find the currents in the power semiconductors at the instant of the commutation, which are given by

$$\begin{cases} i_{C_{S_1}}(t) = i_{C_{S_3}}(t) = \dfrac{I_{m_p}}{4} \\ i_{C_{S_2}}(t) = i_{C_{S_4}}(t) = -\dfrac{I_{m_p}}{4} \\ i_{C_{S_5}}(t) = -\dfrac{I_{m_p}}{2} \\ i_{C_{S_6}}(t) = \dfrac{I_{m_p}}{2} \end{cases} \tag{18}$$

From the previous equations, we obtain the currents in capacitors C_{S_3} and C_{S_6} as

$$\begin{cases} i_{C_{S_3}}(t) = C_{oss}\dfrac{dv_{C_{S_3}}}{dt} = C_{oss}\dfrac{\Delta v_{C_{S_3}}}{\Delta t} \\ i_{C_{S_6}}(t) = C_{oss}\dfrac{dv_{C_{S_6}}}{dt} = C_{oss}\dfrac{\Delta v_{C_{S_6}}}{\Delta t} \end{cases} \tag{19}$$

With appropriate substitutions, we find

$$\begin{cases} \dfrac{I_{m_p}}{4} = C_{oss}\dfrac{V_{C_2}}{t_{c_1}} \\ \dfrac{I_{m_p}}{2} = C_{oss}\dfrac{V_{C_2}}{t_{c_2}} \end{cases} \tag{20}$$

Consequently, the durations of the commutation are given by

$$\begin{cases} t_{c_1} = \dfrac{4C_{oss}V_{C_2}}{I_{m_p}} \\ t_{c_2} = \dfrac{2C_{oss}V_{C_2}}{I_{m_p}} \end{cases} \tag{21}$$

ZVS is achieved provided that the dead time t_d between the gate signals of the switches is larger than the commutation time t_{c_1}. Thus,

$$t_d > t_{c_1} = \frac{4C_{oss}V_{C_2}}{I_{m_p}} \tag{22}$$

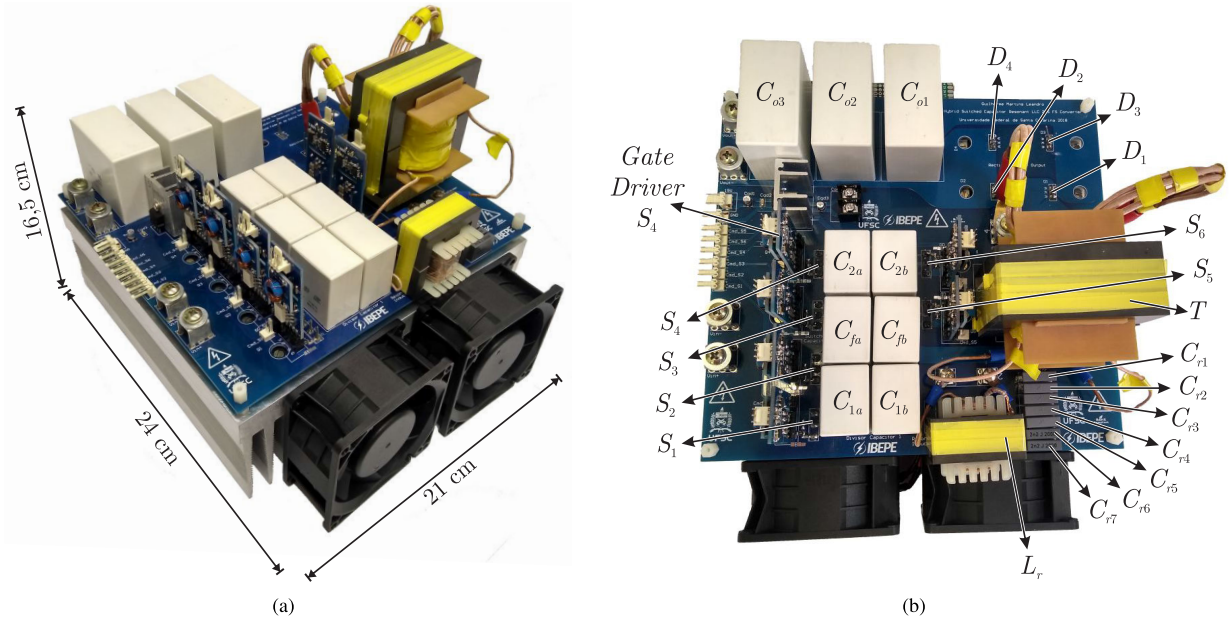

FIGURE 9. Prototype of the proposed hybrid switched-capacitor LLC resonant converter. (a) Perspective view, and (b) top view.

V. PROTOTYPE IMPLEMENTATION AND EXPERIMENTAL RESULTS

An experimental prototype was designed and constructed to validate the theoretical analysis, as shown in Fig. 9. Prototype components were dimensioned with the parameters listed in Table 1. The switching frequency was chosen to be below but in the vicinity of the series resonant frequency to obtain ZCS of the rectifier diodes on the secondary side and ZVS commutation on the primary side power semiconductors.

TABLE 1. Hybrid switched-capacitor LLC resonant DC-DC converter specifications.

Symbol	Parameter	Value (Unit)
P_o	Rated power	2 kW
V_i	Input voltage	1000 V
V_o	Output voltage	48 V
f_s	Switching frequency	90 kHz
f_o	Resonance frequency	100 kHz

The parameters of the experimental laboratory prototype are shown in Table 2.

As seen in Table 2, it was necessary to use a combination of components to achieve the desired specifications. To form the dividing capacitors C_1 and C_2, two capacitors were associated in parallel, C_{1a} with C_{1b} and C_{2a} with C_{2b}, respectively. For the switched capacitor C_S, two capacitors were also used in parallel, C_{Sa} and C_{Sb}. For the resonant capacitor, seven capacitors were associated in parallel, C_{r1}-C_{r7}, and for the output filter capacitor, three capacitors were used in parallel, C_{o1}, C_{o2} and C_{o3}.

TABLE 2. Components used in prototype.

Component	Type	Value/Model
S_1, S_2, S_3, S_4, S_5, S_6	SiC MOSFET	650 V / 21 A / 175mΩ @125ºC SCT3120AL
$C_{1a,b}$, $C_{2a,b}$, $C_{Sa,b}$	Film Capacitor	15 µF / 650 V / 10,5 A / 5,3 mΩ C4AQCBU5150A12J
C_{r1}, C_{r2}, C_{r3}, C_{r4}, C_{r5}	Film Capacitor	4,7 nF / 2 kV R76UI14704040J
C_{r6}, C_{r7}	Film Capacitor	2,2 nF / 2 kV R76UI12204030J
Lr	Ferrite N97	57,328 µH / N = 18 90 x AWG38 / E 42/21/20
T	Ferrite N87	N_p = 22 / 150 x AWG38 N_s = 2 / 1600 x AWG38 L_m = 459,72 µH L_{lk} = 33,785 µH E 70/33/32
D_1, D_2, D_3, D_4	FERD	100 V / 40 A / 0,375 V @175ºC FERD40H100STS
C_{o1}, C_{o2}, C_{o3}	Film Capacitor	55 µF / 800 V / 16,5 A / 4,1 mΩ C4AQIBW5550A3NJ

By substituting the parameters of the conduction resistance of the MOSFETs (R_{DSon}) and the capacitance of the switched capacitors ($C = C_{Sa} + C_{Sb}$) shown in Table 2 and the switching frequency (f_s) shown in Table 1 into equation (12), the value of α was obtained as 0.4725, indicating that the converter operated in the region of lower losses due to the switched capacitor stage.

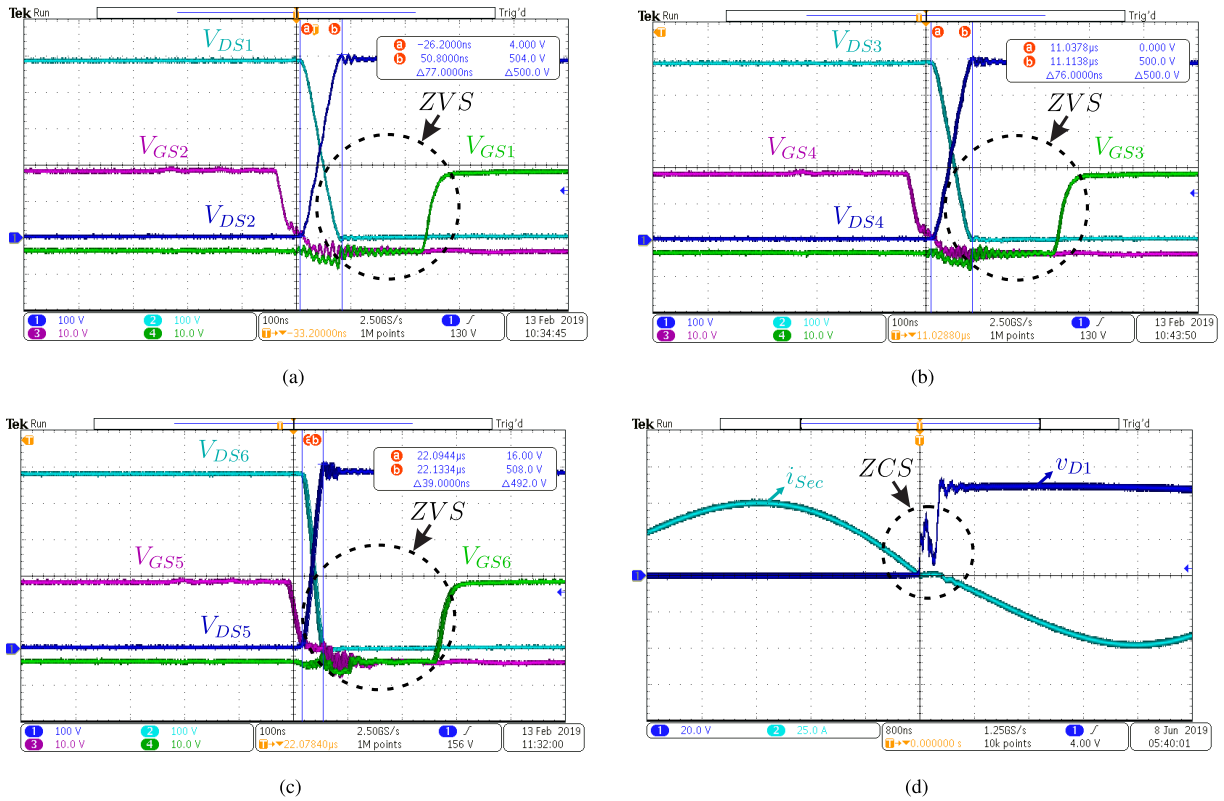

FIGURE 10. Experimental waveform results ($P_o = 1300\ W$). (a) S_1 and S_2 drain-source voltages (100 V/div) and gate-source voltages (10 V/div), with the ZVS performance shown for S_1, (b) S_3 and S_4 drain-source voltages (100 V/div) and gate-source voltages (10 V/div), with the ZVS performance shown for S_3, (c) S_5 and S_6 drain-source voltages (100 V/div) and gate-source voltages (10 V/div), with the ZVS performance shown for S_6, and (d) D_1 cathode anode voltage (20 V/div) and transformer secondary current (25 A/div), with the ZCS performance shown for D_1.

Experimental waveforms of the drain-source voltages of the power semiconductors are shown in Fig. 10(a), Fig. 10(b) and Fig. 10(c). These waveforms show that ZVS-type commutation occurs for all power semiconductors on the primary side of the transformer.

Fig. 10(d) shows the voltage and current in one of the rectifier stage diodes on the secondary side of the transformer, which confirms the existence of soft switching of the ZCS type.

Waveforms of the v_{ab} voltage, resonant current i_{L_r}, and voltage on the resonant capacitor v_{C_r} are shown in Fig. 11.

The efficiency of the proposed converter was measured using a TEKTRONIX PA-1000 power analyzer and is shown in Fig. 12. The maximum efficiency is 97.267% at 594 W. Due to the limitations of the available power analyzer, the efficiency was not measured for power greater than 1.3 kW.

The losses in the converter were calculated and are shown in Fig. 13, where it is possible to observe that the losses in the rectifier diodes (P_D) are the most significant factor decreasing the efficiency of the converter due to the high output current. It is also observed that the losses in the switches (P_S) do not represent a substantial portion of the total losses because the converter works with soft commutation over the entire operating range, which eliminates the switching losses.

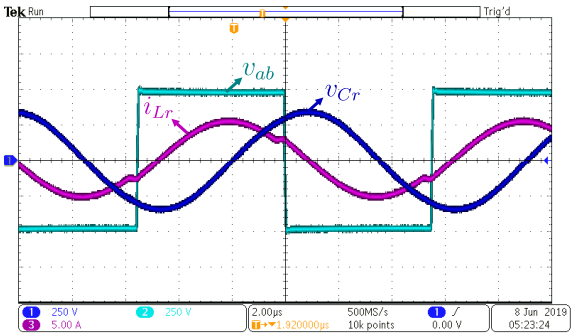

FIGURE 11. Experimental waveform results ($P_o = 1300\ W$): resonant inductor current i_{L_r} (5 A/div), resonant capacitor voltage v_{C_r} (250 V/div), and voltage between the a and b terminals v_{ab} (250 V/div).

The experimental static gain as a function of the normalized load current is depicted in Fig. 14 for resonant and switching frequencies equal to 100 kHz and 90 kHz, respectively.

VI. COMPARISON OF CONVERTER TOPOLOGIES

In Table 3, a succinct comparison of the proposed topology with the topologies presented in [15]–[17] and [26] is made. All topologies are resonant LLC topologies and subject the

TABLE 3. Comparison of LLC resonant converter topologies.

Topologies	[15]	[16]	[17]	[26]	Proposed Converter
Number of switches	4	4	4	4	6
Number of capacitors	2	2	2	4	3
Voltage stress across the switches	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$
Capacitor voltage equalization	Control	Control	Control	Control	Natural equalization
Soft commutation	Primary: ZVS Secondary: ZCS	Primary: ZVS Secondary: ZCS	Primary: ZVS Secondary: ZCS	Primary: ZVS Secondary: -	Primary: ZVS Secondary: ZCS
Modulation	FM		FM	PS	FM
Power flow	Unidirectional	Unidirectional	Unidirectional	Unidirectional	Unidirectional
Maximum measured efficiency	95.1%	95.3%	95.08%	95.25%	97.3%
Output power	48 V/20 A	54 V/10 A	48 V/10 A	50 V/20 A	48 V/41.7 A

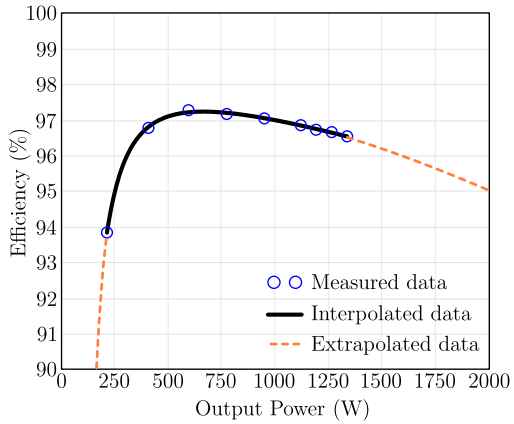

FIGURE 12. Measured efficiency versus load power of the proposed converter.

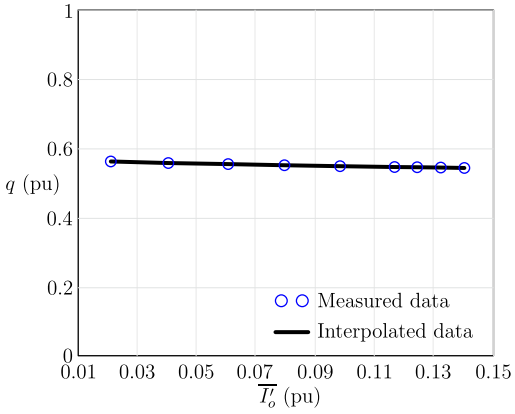

FIGURE 14. Measured external characteristic versus parameterized output current.

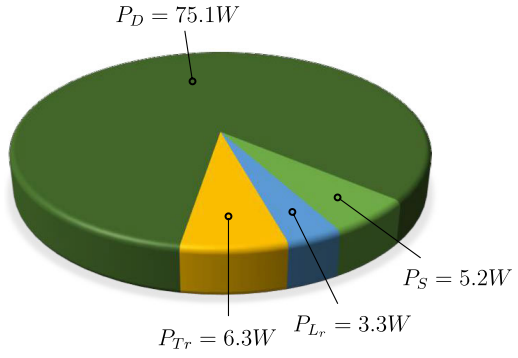

FIGURE 13. Calculated power loss distribution at the rated load.

semiconductors and capacitors on the primary side of the transformer to half the value of the input voltage.

In addition, all converters operate with a switching frequency less than the resonance frequency, but in the vicinity of the resonance frequency, to provide ZVS commutation of the high voltage side semiconductors and ZCS commutation of the diodes of the output rectifier stage.

The powers of the converters presented in [16] and [17] are approximately 500 W. The powers of the converters in references [15] and [26] are equal to 1 kW, while the proposed converter was designed to operate with 2 kW.

A comparison criterion is the number of semiconductors used. All the topologies chosen for the comparison are based on the three-level cell and therefore employ four semiconductors, while the proposed converter, which is based on the switched-capacitor ladder cell, uses six semiconductors.

However, the maximum efficiencies presented in [15], [16], [17] and [26] are 95%, while the maximum value obtained for the proposed converter is 97.3%. In addition, in the proposed converter, equalization of the voltages in the input voltage dividing capacitors occurs naturally, while the three-level topologies require control of these voltages to ensure equalization, which increases the complexity of the circuits.

VII. CONCLUSION

A DC-DC hybrid switched-capacitor LLC resonant converter was proposed, designed, constructed, and analyzed in the laboratory. The analysis and experimental results showed that the converter maintains the LLC characteristics, including soft commutation of all ZVS switches, ZCS-type soft commutation of output diodes, a small variation in the static gain

with load variation, and high efficiency. Voltage stresses of half the input voltage on switches and natural equalization of capacitor voltages without the need for control were obtained with ladder cell incorporation.

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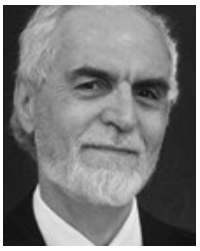
GUILHERME MARTINS LEANDRO was born in Minas Gerais, Brazil, in 1990. He received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV), Viçosa, Brazil, in 2014, and the M.S. degree in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 2019.

He is currently a Research Engineer with the Brazilian Power Electronics and Renewable Energy Institute (IBEPE). His research interests include soft switching, switched capacitors, resonant converters, solid-state transformers, and high-voltage power supplies.



IVO BARBI (Life Fellow, IEEE) was born in Santa Catarina, Brazil. He received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1973 and 1976, respectively, and the Dr.Ing. degree in electrical engineering from the Institut National Polytechnique de Toulouse (INPT), Toulouse, France, in 1979.

He founded the Brazilian Power Electronics Society (SOBRAEP) and the Brazilian Power Electronics Conference (COBEP), in 1990, and the Brazilian Power Electronics and Renewable Energy Institute (IBEPE), in 2016. He is a Researcher with the Solar Energy Research Center and an Emeritus Professor in electrical engineering with the Federal University of Santa Catarina.

Prof. Barbi received the IEEE William E. Newell Power Electronics Award. He was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON POWER ELECTRONICS, for several years.