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# Analysis and Design of 4-to-1 Capacitor-Stacking Balancer for Stacked Voltage Domain

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**ABSTRACT** This paper presents an alternative method for achieving more efficient and reliable DC-DC conversion and balancing operations for low-power applications in a stacked voltage domain. This work comprehensively analyzes the operating principles and power conversion loss of a proposed capacitor-stacking balancing circuit at the system level. The analysis and design of the capacitor-stacking balancing circuit in the stacked voltage domain, including the time-domain operation, voltage equation, and dead-time effect, are explored and implemented. This study provides an opportunity to achieve a highly optimized system with high efficiency. A comprehensive analysis of efficiency at the system level shows the advantages and limitations according to each stacking method under a given system condition. Considering the redundancy issues of the previous method at system-level analysis, the capacitor-stacking balancing method is a preferable choice for low-power, high-reliability, and high-efficiency applications under light load conditions. This study also provides an analytical efficiency model under current imbalance, which is a notable difference from previous research and case studies concerning power converters. Prototype board with lithium-ion battery power and a core voltage of 0.825 V—a low-power application—was built to verify the proposed model and analysis. The experimental efficiency reached 94.9% at 20% of the maximum workload.

**INDEX TERMS** Balancing circuit, DC-DC converter, stacked voltage domain, switched-capacitor circuit.

## I. INTRODUCTION

Recently, semiconductor technology scaling has accomplished the size reduction of the digital device and lowered the power supply voltage of processor and production cost [1], [2]. Consequently, the high performance of digital circuits including application processor (AP) and graphics processing unit (GPU) has been achieved. However, the performance level of a handheld system with a high-performance processor has been constrained by a thermal budget due to the power consumption. As a result, the study on the power conversion system is getting more and more attention to its importance in increasing system efficiency [3], [4]. For this reason, the power converter is indeed very important for electronic devices such as mobile phones, tablets, laptops, data centers, and automotive electronic systems [5]–[10]. Conventional embedded systems adopt the power conversion techniques such as dynamic voltage scaling (DVS) [11], adaptive body biasing (ABB) [11], clock gating [12], and adiabatic–switching [13] to improve system efficiency significantly for mobile devices. Although the system adopting these techniques achieves power efficiency improvements, these are usually constrained by a given system condition and environment. In other words, it has a system-dependent efficiency limitation.

As shown in Fig. 1, it is shown that the system-level power optimization achieves larger benefits such as power saving and reduced iteration time compared to lower-level design, taking into account system-level metrics and constraints [47]–[51]. Until recently, there has been a lot of research on system-level approaches for many research areas [14]–[17]. The electrical performance or system reliability has been improved by adopting system software [14], black box modeling [15], and system-level strategy [16], [17].

To overcome the limitations of the given power structure, the concept of the stacked voltage domain (SVD) was

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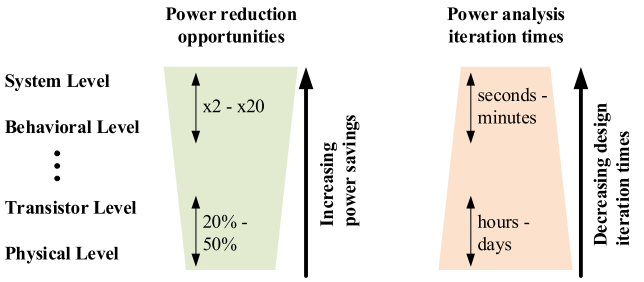



**FIGURE 1.** Benefits of system-level power analysis and optimization [47].

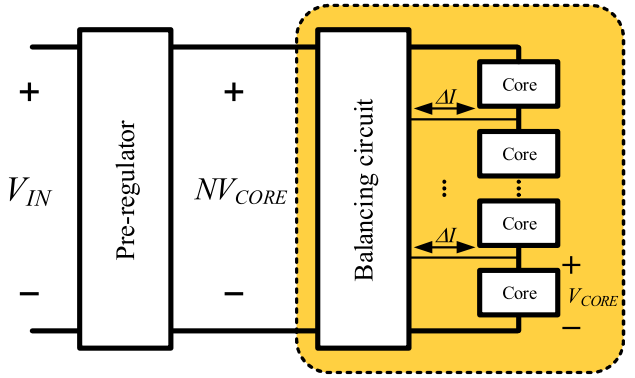



**FIGURE 2.** Principle of *N*-level SVD architecture with balancing circuit and stacked load.

proposed [18], [19] as shown in Fig. 2 with the high-level power design approach. Many studies have been done on the SVD until recently from low power to high power applications [6], [8], [20]–[26]. In the $N$-level SVD system, when the $N$ stacking is performed, the following characteristics related to power conversion are addressed as shown in [18], [22]. The supply voltage generated by the pre-regulator is $N$ times bigger than the parallel structure, and the current is $1/N$ times. Because of the increased voltage and reduced current, the impedance to the load shown by the converter has increased by $N^2$, which reduces the regulation burden of the power converter significantly. One of the important factors in designing a power converter is noise, which is caused by a large current change, $di/dt$ with parasitic capacitance [27], [28]. The SVD system reduces noise due to smaller ground currents, reducing the size and burden of noise filters compared to conventional structures [29]. Also, the burden of conversion ratio caused by low output voltage in high-performance digital circuits is mitigated.

Although the stacked system has the above list of advantages [18], [22], a converter in SVD is required to balance the voltages and currents between cores to operate the stacked system properly. In the case of the differential power processing (DPP) [6], [23], [24], a converter is proposed and analyzed to satisfy the maximum power point tracking (MPPT) of the system in a stacked structure. The structure this study used the most is one in which a step-down converter is chained by using voltage generated from upper and lower adjacent cores. However, because a large number of energy storage components in each stage are required to create DPP, this structure suffers from the burden of size compared to other topologies such as switched-capacitor or hybrid converter topology on which many studies have been recently done. Recent studies [8], [25], [26] using a ladder-type structure, one of the common types of switched-capacitor converters, has implemented for SVD voltage balancing circuit with a smaller area and simple operation. However, the ladder-type power converter has limitations of large voltage ripple and low efficiency due to load imbalance, requires additional circuit technology, and burdens the system [25].

Recently, lithium-ion batteries are required as a power source for many applications such as mobile devices, laptops, and wearable devices [30]. Besides that, in other applications where functional safety issues are critical, such as automotive, aerospace, and medical applications, ensuring high power conversion efficiency and system reliability is also an important requirement [31]. The lockstep applications [32]–[34] with multiple loads by using the properties of the SVD method with the battery input source achieve efficient and reliable operation, and many types of research have been studied recently. The proposed circuit, which is applied to the applications mentioned above with battery input, is shown in Fig. 3. Balancing operation is achieved with a capacitor-stacking balancing (CSB) method for SVD operation with battery input. The proposed circuit consists of bulk capacitors, load capacitors, load currents, and matrix switch set and performs 4-to-1 conversion from the battery input to the load. For low power applications, the supply voltage of load is required around 1V or less, and due to the nominal conversion ratio for step-down conversion in the industry [35], the lithium-ion battery is suitable because of its cell voltage range of around $3\text{V} \sim 4\text{V}$ [30]. Therefore, this study using a 4-to-1 conversion ratio can be applied to general low power applications. At the same time, balancing operation is effectively done using the characteristics that the electrical connection of the load change over time. Detailed descriptions regarding its operation and each component are provided in the next section.

Since few studies have been done on the system-level approach, previous studies on SVD architecture does not spread to industrial systems and remains only at the converter level. The purpose of this study is to analyze the system including the power converter and perform system analysis to maintain the advantages of the converter and overcome the disadvantages. To our best knowledge in the literature, the system-level approach to switching capacitor circuits in the SVD architecture has not been presented. The purpose of this work is to provide a system-level analysis of switched capacitor circuits for low power applications.

This study expands from the previous study [36] in the following research perspectives. In the previous study [36], the introduction of the matrix switch set and its simple modeling are presented. This study furthers the comprehensive analysis in detail between the CSB method and previous topology at

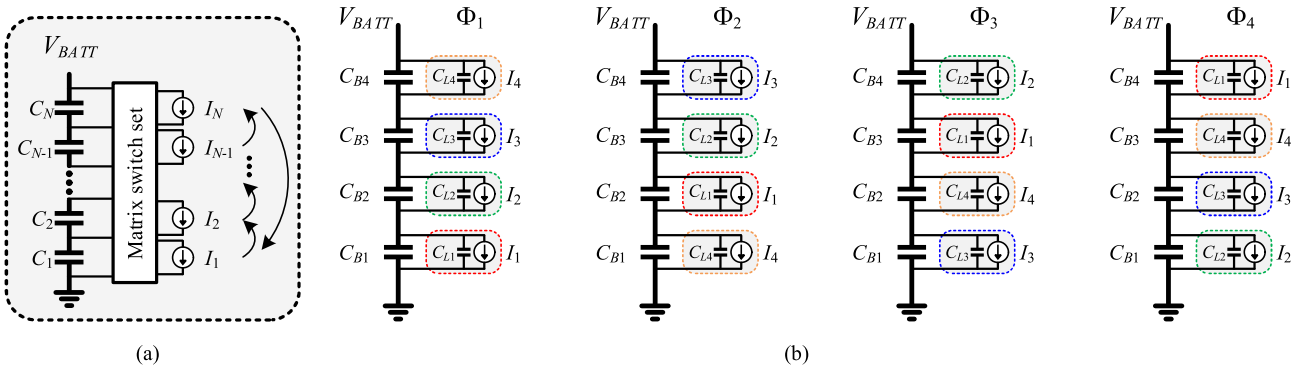



**FIGURE 3.** (a) Block diagram of the *N*-stacked domain of the proposed topology (b) Operating principle of the 4-stacked domain (capacitor–stacking balancer (CSB)).

**TABLE 1.** Comparison with Previous Works.

| | [19] | [23] | [6] | [8] | [34] | [37] | This work |
|---|---|---|---|---|---|---|---|
| Application | Digital circuit | Photovoltaic | Datacenter, server | Digital circuit | Digital circuit | Wearable, IoT | Low power application |
| Topology | Linear regulator | Buck/boost with DPP | Isolated DPP | Buck/boost with DPP | 2, 3 levels cyclic SC | Dual active bridge | CSB method |
| Load voltage | 1.8 V | 10 V | 12 V | 1 V | 1.08~1.32 V | 0.8~1.5 V | 0.825 V |
| Stacked size | 2, 3 | 2 | 4 | 4 | 2,3 | 3 | 4 |
| Efficiency | 93% (2*VDD*) 80% (3*VDD*) | 95% | 99.89% | 98% | 99% | 87.2% | 94.96% |

the system-level perspective [7]. The analysis and design of the CSB including time-domain operation, voltage equation, and the dead-time effect are explored. Note that although the observations on the current imbalance as discussed in the previous works [8], [23], are only partly addressed, this study provides analytical models that predict the results for a generic case. In Table 1, this study is compared with recent previous studies [6], [8], [19], [23], [34], [37]. Many studies based on differential power processing suffer from the size issue due to many inductors and capacitors, while this work is suitable for small area low power high-efficiency applications. As with many cases dealing with digital circuits, this prototype board is implemented with 0.825V of core voltage and compared the results of each. The experimental results are shown to verify the analysis and modeling for the proposed method in Section IV.

## II. OPERATIONAL PRINCIPLE

This section starts with the operational principle and voltage equation of the CSB method, which is fundamental for the following analysis in this study. The generic model of the load voltage associated with the bulk capacitor voltage is derived, and then, a load voltage equation with dead-time yields an analytical model for loss modeling.

### A. MATRIX SWITCH SET

To begin with, the behavioral description of the matrix switch set is introduced. As shown in Fig. 3, the proposed circuit consists of bulk capacitors, load capacitors, load currents, and matrix switch set. In Fig. 3, the bulk capacitors, load capacitors, and load currents are $C_{B1} \sim C_{B4}$, $C_{L1} \sim C_{L4}$, and

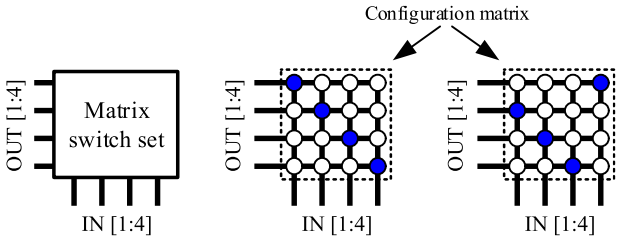



**FIGURE 4.** Description of matrix switch set with configuration matrix and examples of connection for 4-stacked domain.

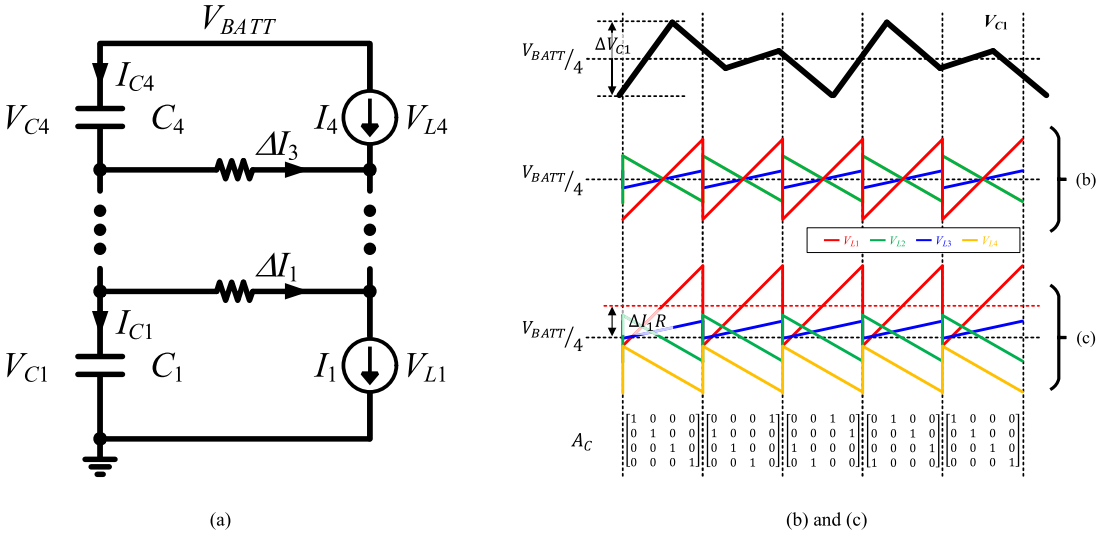
$I_1 \sim I_4$, respectively. The general description of the matrix switch set is studied in [36]. The matrix switch set is illustrated as in Fig. 4 including inputs, outputs, and status of dots. The two examples of Fig. 4 indicate the connection of input and output according to the dots. Therefore, by replacing the set of dots with the configuration matrix, the input-output connection is changed according to the state of the matrix, and the relationship between the input and output, here $V_C$ and $V_L$, for the $k_{th}$ phase are described as

$$\begin{bmatrix} V_{C1}(k) \\ V_{C2}(k) \\ V_{C3}(k) \\ V_{C4}(k) \end{bmatrix} = A_C(k) \cdot \begin{bmatrix} V_{L1}(k) \\ V_{L2}(k) \\ V_{L3}(k) \\ V_{L4}(k) \end{bmatrix}, \tag{1}$$

$$A_C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \cdots, \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}, \tag{2}$$

where $A_C$ is the configuration matrix at the $k_{th}$ phase.

In Fig. 3, the load capacitor is modeled as the sum of the parasitic capacitance, such as decoupling capacitance, and




(a) (b) and (c)

**FIGURE 5. (a) Simplified circuit with capacitors and loads with the differential current. Illustration showing the relationship between the capacitor voltage, $V_{C1}$.**

common–mode capacitance to ground. On the other hand, the bulk capacitor is a filter capacitor for maintaining voltage and has a relatively larger value than the load capacitor. For 4-to-1 CSB operation, which is operating in four phases in this work, the four bulk capacitors are connected in series while each load is rotating with the corresponding state of configuration matrix [36].

### B. VOLTAGE EQUATION

In this section, the voltage equation of the CSB operation is derived. At first, the circuit configuration consists of an equivalent capacitor and load with an arbitrary phase for the steady-state is considered as shown in Fig. 5 (a). The current difference is expressed as $\Delta I_N = I_N - I_{N+1}, N = 1 \sim 3$ for four-level CSB operation in this work as shown in Fig. 5 (a). The switch is modeled to be turned-on with the on-resistance, and the capacitor on the left side, $C_1 \sim C_4$, is the sum of both the bulk and load capacitor at its corresponding phase as shown in Fig. 4, and it is described as

$$\begin{bmatrix} C_1(k) \\ C_2(k) \\ C_3(k) \\ C_4(k) \end{bmatrix} = \begin{bmatrix} C_{B1} \\ C_{B2} \\ C_{B3} \\ C_{B4} \end{bmatrix} + A_C \cdot \begin{bmatrix} C_{L1} \\ C_{L2} \\ C_{L3} \\ C_{L4} \end{bmatrix}. \tag{3}$$

To investigate the voltage of the load capacitor, it is required to define the load voltage. Since the load voltage consists of a DC term and a ripple term, it is expressed as $v_L = V_L + \Delta v_L$. Here $\Delta v_L$ is the ripple that occurs during one phase. Then, the DC term $V_L$ is divided as $V_L = V_C + \Delta IR$, where the desired DC level of the bulk capacitor $V_C$ and resistive drop $\Delta IR$. The average voltage of the bulk capacitor, which is the steady-state voltage of the balancing operation, is done to be $V_{BATT}/N$ in previous study [36]. Due to the capacitance difference, in the normal case $C_L \ll C_B$ as discussed in this section, the voltage characteristic of the load capacitor is dominated by the bulk capacitor due to charge sharing property. When the ripple term is the same for both load and bulk capacitor during one phase, $\Delta v_L = \Delta V_C$, then the load voltage is expressed as $v_L = V_{BATT}/N + \Delta IR + \Delta V_C$. As shown in Fig. 5 (b) and (c), the load voltages and $V_{C1}$ voltage are illustrated with the voltage ripple, the DC term of the bulk capacitor, and the *IR* drop. Each part will be covered in detail in the following.

To explore this behavior in detail, the steady-state waveform with zero on-resistance of the switch throughout four phases of both capacitor and load side are plotted in Fig. 5 (b). The capacitor voltage varies by its corresponding load at each phase. In the four-level SVD operation, the voltage of the capacitor varies over four phases. Under steady-state conditions, the voltage ripple of a capacitor is periodically constant because voltage ripple is a function of the sum of each load current in every phase. Also, theoretically, every bulk capacitor has the same voltage ripple shape due to the phase shift. When the on-resistance of the switch is considered, which means nonzero on-resistance, the load voltages, $V_{L1} \sim V_{L4}$ as shown in Fig. 5 (c), reflect the resistance drop (IR drop) depending on the current direction above or below from the bulk capacitor voltage. The ripple voltage of the bulk capacitor is derived by considering the current flowing through each capacitor with the following analysis. The current differences in each branch are rewritten as

$$\begin{cases} \Delta I_1 = I_1 - I_2 = C_1 \dfrac{dV_{C1}}{dt} - C_2 \dfrac{dV_{C2}}{dt} \\ \Delta I_2 = I_2 - I_3 = C_2 \dfrac{dV_{C2}}{dt} - C_3 \dfrac{dV_{C3}}{dt} \\ \Delta I_3 = I_3 - I_4 = C_3 \dfrac{dV_{C3}}{dt} - C_4 \dfrac{dV_{C4}}{dt}, \end{cases} \tag{4}$$

where $C_i$ is the equivalent capacitor at each layer as shown in Fig. 5 (a), which is the sum of $C_B$ and $C_L$ as shown in Fig. 3. Then, each voltage difference within one phase is derived, assuming that the sum of voltage difference is zero.

$$\frac{d}{dt}(V_{C1} + V_{C2} + V_{C3} + V_{C4}) = 0. \tag{5}$$

Then, the current difference is derived by the following equations (6), shown at the bottom of this page.

It is simplified in a matrix form under the condition that every capacitor is the same, $C_1 = C_2 = C_3 = C_4 = C$, for four-phase CSB operation.

$$C\frac{d}{dt}\begin{bmatrix} v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \end{bmatrix} = \frac{1}{4}\begin{bmatrix} -3 & -2 & -1 \\ 1 & -2 & -1 \\ 1 & 2 & -1 \\ 1 & 2 & 3 \end{bmatrix}\begin{bmatrix} \Delta I_1 \\ \Delta I_2 \\ \Delta I_3 \end{bmatrix}, \quad (7)$$

where negative sign indicates discharging operation, meaning the current is going out of the capacitor, whereas the positive sign indicates charging operation, meaning the current is going into the capacitor.

This behavior associated with voltage ripple in $N$-level SVD operation for other applications is generalized as

$$C\frac{d}{dt}\begin{bmatrix} v_{C(1)} \\ v_{C(2)} \\ \vdots \\ v_{C(N-1)} \\ v_{C(N)} \end{bmatrix} = \frac{1}{N}\begin{bmatrix} -(N-1) & \cdots & -2 & -1 \\ 1 & \ddots & -2 & -1 \\ 1 & 2 & -2 & -1 \\ 1 & 2 & \ddots & -1 \\ 1 & 2 & \cdots & N-1 \end{bmatrix}\begin{bmatrix} \Delta I_1 \\ \Delta I_2 \\ \vdots \\ \Delta I_{N-1} \end{bmatrix}. \quad (8)$$

### C. DEAD-TIME EFFECT ON LOAD VOLTAGE

When considering a practical operation, it is necessary to take into account the effect of the dead-time effect on the load (parasitic) capacitor at the load side. The dead-time is required for the time between the connection and disconnection of the load and bulk capacitors. That is, the load capacitor and the bulk capacitor are separated during the dead-time. In this case, the load capacitor fully handle the load itself, additional voltage ripple occurs in this period, and it is considered as

$$\Delta V_{dt} = \frac{I}{C_L} t_{dt}, \quad (9)$$

where $\Delta V_{dt}$ is the voltage ripple, normally drop, due to its load current at the load capacitor during dead-time, $t_{dt}$ is dead-time, and $C_L$ is the load capacitor.

By combining (7)–(9), the ripple of the load voltage is expressed as

$$\Delta\begin{bmatrix} v_{L1} \\ v_{L2} \\ v_{L3} \\ v_{L4} \end{bmatrix} = \frac{1}{4C}\begin{bmatrix} -3 & -2 & -1 \\ 1 & -2 & -1 \\ 1 & 2 & -1 \\ 1 & 2 & 3 \end{bmatrix}\begin{bmatrix} \Delta I_1 \\ \Delta I_2 \\ \Delta I_3 \end{bmatrix} T_S + \Delta\begin{bmatrix} v_{dt1} \\ v_{dt2} \\ v_{dt3} \\ v_{dt4} \end{bmatrix}. \quad (10)$$

As aforementioned, the average value at the load side reflects the IR drop from the capacitor's, and the voltage ripple is composed of the two terms as shown in (10).

## III. LOSS ANALYSIS

In this section, the loss modeling of the CSB method and the effect of each loss factor on system efficiency are established and discussed. First, the capacitive charge sharing loss due to dead-time and load capacitor selection is discussed. Next, the loss of the CSB circuit itself, based on the operational principle in the previous section, is discussed, and the system-level block diagram, which includes system configuration with considering CSB, is explored, and a high-level estimation of the loss analysis due to the structure is performed. Finally, system efficiency for CSB and the previous method is discussed and compared.

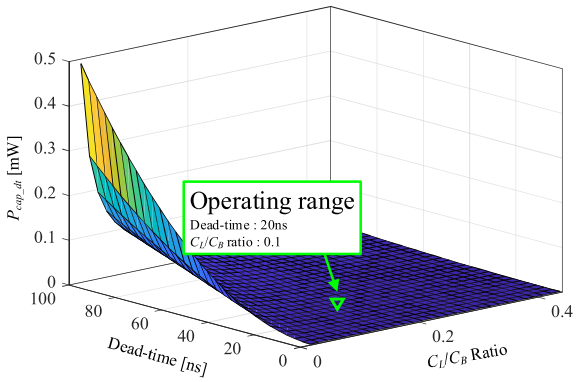



**FIGURE 6.** Capacitive charge sharing loss due to the dead-time and ratio between the load capacitor and the bulk capacitor.

$$\begin{cases} \dfrac{dV_{C1}}{dt} = \dfrac{-\left(\Delta I_1\left(C_3C_4 + C_2C_4 + C_2C_3\right) + \Delta I_2\left(C_2C_4 + C_2C_3\right) + \Delta I_3C_2C_3\right)}{C_1C_2C_3 + C_1C_2C_4 + C_1C_3C_4 + C_2C_3C_4} \\ \dfrac{dV_{C2}}{dt} = \dfrac{\Delta I_1C_3C_4 - \Delta I_2\left(C_1C_4 + C_1C_3\right) - \Delta I_3C_1C_3}{C_1C_2C_3 + C_1C_2C_4 + C_1C_3C_4 + C_2C_3C_4} \\ \dfrac{dV_{C3}}{dt} = \dfrac{\Delta I_1C_2C_4 + \Delta I_2\left(C_1C_4 + C_2C_4\right) - \Delta I_3C_1C_2}{C_1C_2C_3 + C_1C_2C_4 + C_1C_3C_4 + C_2C_3C_4} \\ \dfrac{dV_{C4}}{dt} = \dfrac{\Delta I_1C_2C_3 + \Delta I_2\left(C_1C_3 + C_2C_3\right) + \Delta I_3\left(C_1C_2 + C_1C_3 + C_2C_3\right)}{C_1C_2C_3 + C_1C_2C_4 + C_1C_3C_4 + C_2C_3C_4}. \end{cases} \quad (6)$$

### A. DEAD-TIME EFFECT ON CAPACITIVE CHARGE SHARING LOSS

As discussed in Section. II, during the dead-time, the additional voltage ripple is produced. Due to the voltage difference between the load and the bulk capacitor, the capacitive charge-sharing loss is generated, and it is expressed as [38]

$$P_{cap} = 0.5\left(\frac{C_i C_j}{C_i + C_j}\right)\Delta V^2 F_{SW}, \tag{11}$$

where $C_i$, $C_j$, $\Delta V$ are any two-capacitors $C_i$, $C_j$, and voltage difference $\Delta V$, respectively. Therefore, the capacitive charge sharing loss due to voltage difference (9) is expressed as

$$P_{cap\_dt} = 0.5\left(\frac{C_B C_L}{C_B + C_L}\right)\left(\frac{I}{C_L} t_{dt}\right)^2 F_{SW}, \tag{12}$$

where $P_{cap\_dt}$ refers to the capacitive charge sharing loss during dead-time. Fig. 6 shows the plot of (12) according to the dead-time and the ratio of the load capacitor and the bulk capacitor. As shown in Fig. 6, in the case of dead time, the smaller the value, the less the loss. However, a certain minimum value of dead-time is required to prevent a shoot-through due to mismatches in signals or components in the circuit. For the load capacitor, the larger the value, the smaller the loss. However, since the capacitor allocates most of the area, it is expected that the area of the entire system will be larger [39]–[41]. The operating range as shown in Fig. 6 shows that the designed value of dead-time and the capacitance to make the corresponding losses small enough.

### B. CONVERTER VIEW

The power loss breakdown for a power converter, which operates as a balancing circuit is considered as below

$$P_{loss} = P_{cond} + P_{sw} + P_{cap}, \tag{13}$$

where $P_{cond}$ refers to the resistive conduction loss, $P_{sw}$ refers to the switching loss, and $P_{cap}$ refers to the capacitive charge sharing loss. It is noted that (13) only include the loss terms of the converter. The whole loss model is covered later in this section. With the understanding of the operating principle as described in Section II, the power loss modeling of CSB is expressed as

$$P_{loss\_CS} = P_{cond\_CS} + P_{sw\_CS} + P_{cap\_CS}, \tag{14}$$

$$P_{cond\_CS} = \sum_{k=1}^{N} 4 I_k^2 R_{on}, \tag{15}$$

$$P_{sw\_CS} = \sum_{k=1}^{N} 2 V_k I_k T_{tr} F_{SW}, \tag{16}$$

$$P_{cap\_CS} = \sum_{k=1}^{N} 0.5\left(\frac{C_B C_L}{C_B + C_L}\right)\Delta V_k^2 F_{SW}, \tag{17}$$

where subscript $CS$ means the proposed method, CSB, $I_k$ is the current through the $k_{th}$ core, $V_k$ refers to the voltage of the $k_{th}$ core, $R_{on}$ refers to the on-resistance of the single switch, $T_{tr}$ refers to the transition time of the power switch, $F_{SW}$ refers to the switching frequency, and $\Delta V_k$ refers to the voltage ripple at each core as shown in (7)–(10), respectively. Since each core contains the four switches due to the bi-directional operation as shown in Fig. 7 (a), the conduction loss and switching loss are four times each loss for a single switch set.

Likewise, the previous method named the LS method, which is a typical type of switched-capacitor converter as shown in Fig. 7 (b), is modeled as

$$P_{loss\_LS} = P_{cond\_LS} + P_{sw\_LS} + P_{cap\_LS}, \tag{18}$$

$$P_{cond\_LS} = \sum_{k=1}^{N} 4\Delta I_k^2 R_{on}, \tag{19}$$

$$P_{sw\_LS} = \sum_{k=1}^{N} 2 V_k \Delta I_k T_{tr} F_{SW}, \tag{20}$$

$$P_{cap\_LS} = \sum_{k=1}^{N} 0.5\left(\frac{C_B C_L}{C_B + C_L}\right)\Delta V_k^2 F_{SW}, \tag{21}$$

where subscript $LS$ refers to the load stacking method as shown in Fig. 7 (b) and $\Delta I_k$ refers to the current difference between adjacent core as shown in Fig. 5 (a). It is shown that the loss model of CSB method includes $I_k$, while the loss model of the LS, which is the previous method includes $\Delta I_k$.

### C. SYSTEM VIEW

Many previous studies related to SVD have been done in terms of power converter [6], [8], [20]–[26]. However, if these technologies are not considered thoroughly along with the peripheral circuits required from the system perspective, they are incomplete due to limited applications. Therefore, in this study, the peripheral circuit targeting SVD at the system point of view is considered and compared for both methods at the system-level.

In Fig. 7, the corresponding peripheral circuits are considered for each. In the overall system, the load itself cannot operate without adjacent peripherals especially in a modern embedded system. The peripheral circuits are categorized with one or some of the memory devices, communication devices, sensors, and analog or digital circuits. The biggest difference between the proposed circuit and the previous topology is that the electrical connection between the loads changes over time for the ground. In other words, the changes over time of the electrical position at the load side distinguish both methods. By considering this difference, the system-level configurations with the peripheral circuits are shown in Fig. 7 for both methods.

The following cause additional losses, which decrease power efficiency at the system-level:

1) The I/O related loss: For communication between the load and peripheral circuit, the signal needs to be transferred through the signal path including an I/O pad. There is parasitic capacitance regarding clamp circuit for ESD cell, package, wire for connection, and PCB line, which destroys the high-frequency signal transfer. Since the signal switching is normally faster than the switching frequency of the balancing circuit, it is taken into account in the additional switching loss with higher switching frequency than the frequency of the balancing circuit. In addition to the switching loss at the I/O pad, the leakage current from the supply voltage of the I/O to the ground is also considered.

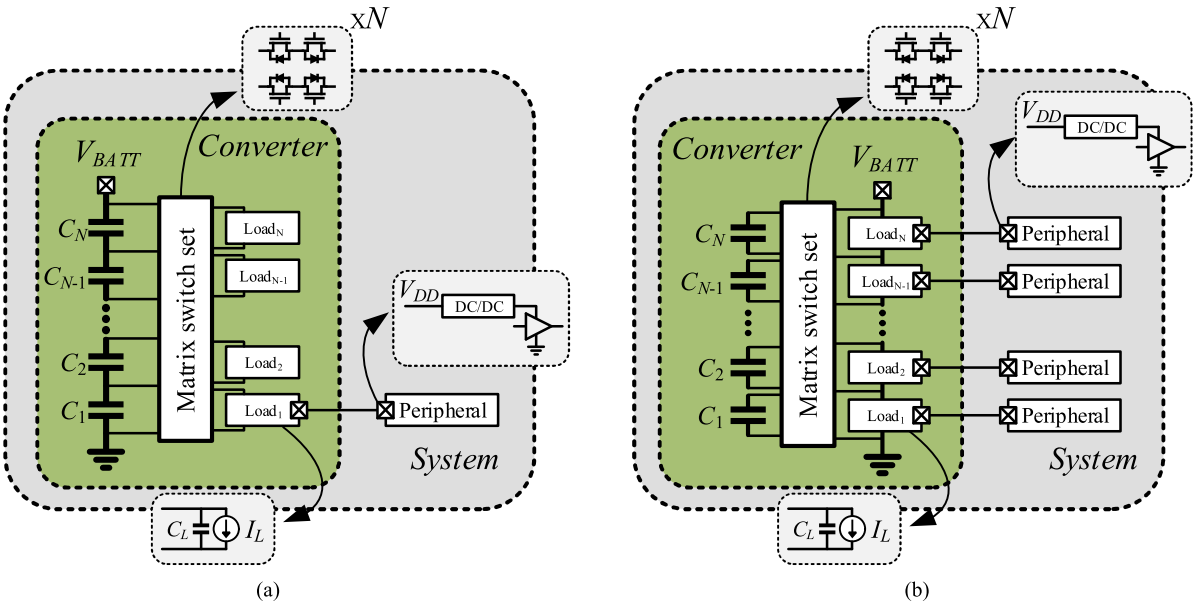



**FIGURE 7.** System-level block diagram of the *N*-level (a) CSB method, (b) conventional method (LS method).

2) Loss of the additional power converter at I/O pad: Each I/O pad requires a dedicated power converter, which provides a certain supply voltage and power sequence for stable operation. In addition to the power loss, the physical area and component cost to implement the power converter is also a significant loss in terms of the overall system design.

The system-level power loss is modeled in consideration discussed above. As shown in Fig. 7 (a), the CSB method communicates through single-channel due to its inherent load rotating property. The loss model including the loss terms of I/O, $P_{sw\_IO}$, additional power converter loss, $P_{add}$, and leakage loss, $P_{leak}$, of CSB method are modeled as

$$P_{loss\_CS} = P_{cond\_CS} + P_{sw\_CS} + P_{cap\_CS} + P_{sw\_IO\_CS} + P_{add\_CS} + P_{leak\_CS}, \quad (22)$$

$$P_{sw\_IO\_CS} = 0.5 C_{IO} V_{IO}^2 F_{IO\_CS}, \quad (23)$$

where $C_{IO}$ is the total equivalent capacitance including all the parasitic capacitance seen at the I/O pad, $V_{IO}$ refers to the voltage of I/O pad, and $F_{IO\_CS}$ refers to the switching frequency at the I/O stage for the proposed circuit.

For the additional power converter loss, $P_{add\_CS}$, which is added to each I/O pad, it is assumed that its efficiency is around 90% with the proper assumption for both methods. The expression for leakage power of CMOS inverter with the supply voltage of $V_{DD}$ and the threshold voltage of $V_{TH}$ is as follows [33]

$$P_{add} = 0.1 P_{sw\_IO}, \quad (24)$$

$$P_{leak} = \gamma exp\left(\frac{V_{DD} - V_{TH}}{s}\right), \quad (25)$$

where $\gamma$ and $S$ are constants that depend on the given technology [33].

Likewise, the loss model of the LS method as shown in Fig. 7 (b) is modeled as

$$P_{loss\_LS} = P_{cond\_LS} + P_{sw\_LS} + P_{cap\_LS} + P_{sw\_IO\_LS} + P_{add\_LS} + P_{leak\_LS}, \quad (26)$$

$$P_{sw\_IO\_LS} = \sum_{k=1}^{N} 0.5 C_{IO} V_k^2 F_{IO\_LS\_k}. \quad (27)$$

It shows that $P_{sw\_IO\_CS}$ has a single component, while $P_{sw\_IO\_LS}$ has the sum of each component with different frequencies.

### D. EFFECTIVE OPERATING FREQUENCY AT I/O STAGE

It is shown that the contribution of switching losses at the I/O stage for both control methods depends on its operating frequency. Since the CSB method needs a single I/O channel as aforementioned in the previous subsection as shown in Fig. 7 (a), only one frequency needs to be determined. If each I/O stage of the LS method has the same frequency as the CSB method, then theoretically $N$ times of the system performance is achieved. In other words, the operating frequency for each core of the CSB method is $1/N$ times of the LS method for the same system performance. However, it is shown that the optimal frequency for stable operation of each core depends on the following characteristics [42], which are affected by the delay of the signal transmission, and the overall characteristic is determined by the lowest frequency

$$delay = k \frac{V_{dd}}{(V_{dd} - V_{th})^2}, \quad (28)$$

where $k$ is constant, $V_{dd}$ is the supply voltage, and $V_{th}$ is the threshold voltage with the given semiconductor process. Normally, the lower supply voltage has a bigger delay, resulting in lower operating frequency.

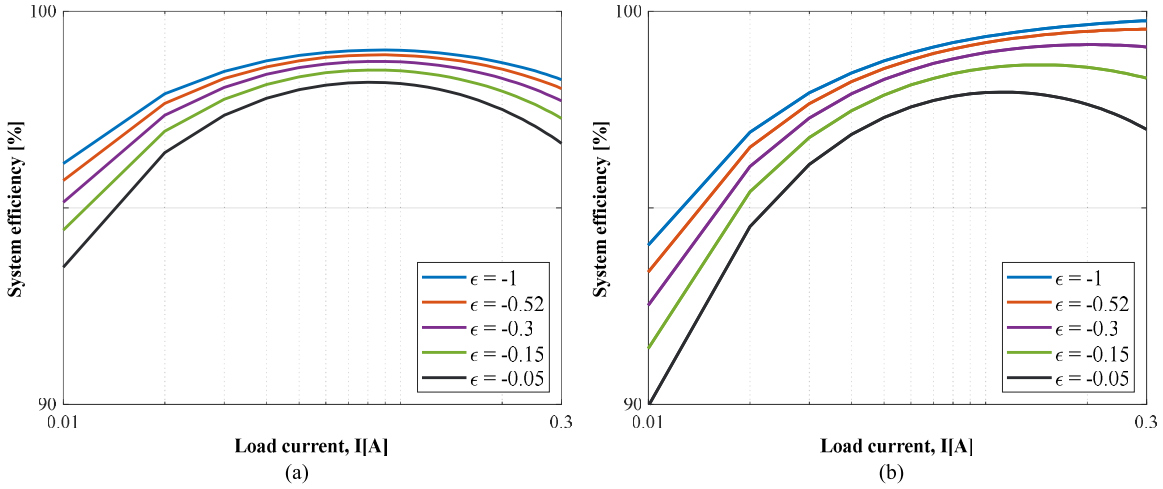



**FIGURE 8.** System efficiency plot with current imbalance of the (a) CSB method and (b) the conventional method (LS method) for 4-level system.

Also, the clock skew, due to the process variations, wire *RC* delay, and clock loading [43]–[46], is considered, which affects the overall characteristics of multichannel signal transmission. Taking this skew characteristic into account, a system implemented with the CSB method has a lower performance than the ideal without clock skew. Thus, the frequency of the LS method at I/O stage is derived as a function of the frequency with CSB operating frequency as follows

$$F_{IO\_LS} = \alpha \frac{min\left(F_{IO\_CS}\right)}{N}, \tag{29}$$

where $\alpha$ refers to the coefficient, $0 < \alpha < 1$. Observe that the total I/O loss for each method is the same with the value of $\alpha = 1$, and the loss for the CSB method is relatively increasing compared to the LS method as $\alpha$ is decreasing.

### E. SYSTEM EFFICIENCY COMPARISON

In this subsection, by combining all the above analysis, the system efficiency of both methods is compared when the current imbalance is applied. Fig. 8 shows the estimated system efficiency versus load current for various current imbalance values for both methods. The error ratio, $\varepsilon$ in Fig. 8 is $log_{10}\left(\Delta I/I\right)$. In both methods, efficiency tends to decrease as the error increases. With these results, based on the loss modeling derived from (22)–(27), this study provides an analytical tendency of system efficiency including the parameters of each control method and system conditions.

Fig. 9 shows the loss breakdown of each control method, which shows the loss contributions under light load and heavy load condition. In light load, the loss of I/O and additional power converters become dominant, so the CSB method is advantageous. On the other hand, for the LS method, as the load current increases, conduction loss of balancing circuit increases, which is more advantageous compared to the CSB method. From this analysis results, it shows that one method

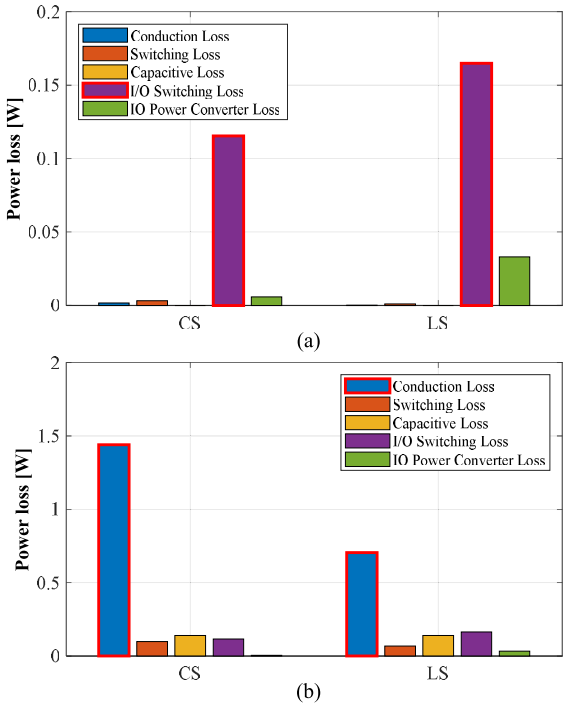



**FIGURE 9.** Power loss breakdown for both methods at (a) light load condition and (b) heavy load condition.

does not always dominate, but has an advantageous region depending on the operating conditions of the system. Therefore, each control method has the appropriate load area and system conditions.

## IV. EXPERIMENTAL RESULTS

The prototype board as shown in Fig. 10, which is designed to be operable for both methods, is implemented. All power switches are used with bi-directional switches for both methods as shown in Fig. 7. A unit switch of the bi-directional

**TABLE 2. Overview of the Components in the Prototype Board.**

| Description | Component | Value |
|---|---|---|
| Input Voltage | $V_{DD}$ | 2.5 V~4 V (Typ:3.3 V) |
| Load (Core) Voltage | $V_{L1} \sim V_{L4}$ | 0.825 V |
| Bulk capacitor | $C_{B1} \sim C_{B4}$ | 47 uF |
| Load capacitor | $C_{L1} \sim C_{L4}$ | 4.7 uF |
| Load resistor | $R_{L1} \sim R_{L4}$ | 1~4 ohm |
| Switching frequency | $f_{sw}$ | 100 kHz |
| Power switch | AON7810 | 2N-CH 30 V 6 A MOSFET |
| Gate driver | 2EDF7235K | - |

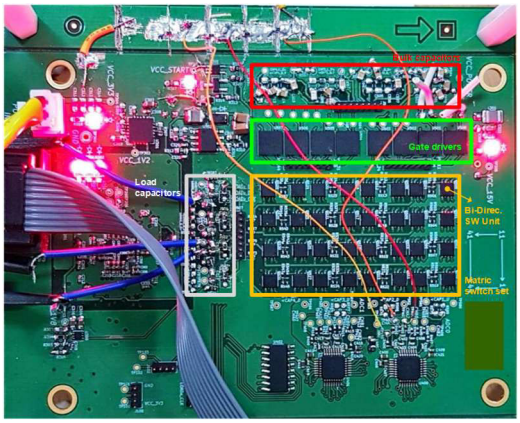



**FIGURE 10. Prototype board, which is designed to be operable for both methods and its experimental setup.**

switch is implemented with the device listed in Table 2. Gate driver is implemented with 2EDF7235K to control each power switch unit. Bulk capacitors, load capacitors, and load resistors are located on both sides of the matrix switch set and the board is configured to be operable for both methods. Detailed information about the prototype board is listed in Table 2.

Fig. 11 shows the measured voltage waveforms with 47uF of the bulk capacitor and 4.7uF of load capacitor for CSB operation. As shown in (9), Fig. 12 (a) shows the simulation results of additional voltage ripple of load voltage waveforms for various dead-time. It is shown that as the dead-time increases, the additional voltage ripple increases as shown in (9). According to the analysis regarding charge sharing loss, the smaller the dead-time or the larger the load capacitor, the smaller the corresponding loss. However, in practical design, the capacitance affects the system area, so it is recommended to have an allowable smaller dead-time smaller to effectively minimize losses and sizes. The experimental result for the voltage ripple of dead-time and load capacitors that do not significantly affect the overall ripple is shown in Fig. 12 (b). The overall ripple tendency due to (9) is verified as shown in Fig. 12 (c). Compared to the simulation results, in real component of the ceramic capacitor, as the DC bias of the capacitor increases, the capacitance decreases, resulting in a bit bigger voltage ripple, up to 15% of the initial capacitance.

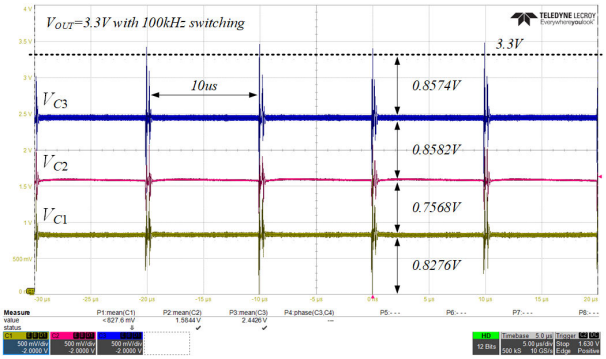



**FIGURE 11. Experimental result of voltage waveform with 100kHz switching frequency of CSB method (4-level SVD, 0.825 of nominal core voltage, 47uF of the bulk capacitor, and 4.7uF of load capacitor).**

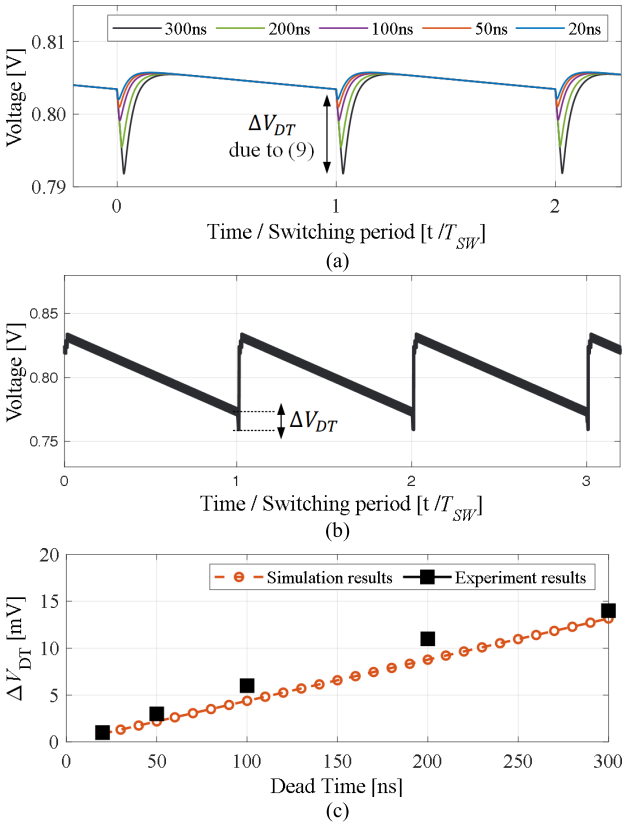



**FIGURE 12. (a) Simulated result of voltage waveforms for various dead-time values (b) Experimental result of voltage waveform with 20ns of dead-time with maximum load current and 4.7uF of load capacitor (c) simulation results and experiment results of voltage ripple due to (9).**

Fig. 13 and Fig. 14 shows the measured voltage waveforms with the same capacitances for both methods. The input is assigned with the battery, and the target core voltage is 0.825V, which is one-fourth of the input voltage. Initially, each load is equally assigned with 4 ohms of resistance and then the $V_{L3}$ is assigned a heavy load of 1 ohm for both control methods.

In the prototype board, various workloads are assigned to evaluate the efficiency performance as described in Section III. In this work, the efficiency of the 4-level system

**TABLE 3.** Average ($I_1 \sim I_4$) and difference ($\Delta I_1 \sim \Delta I_3$) value of Load Currents of FIG.15 (@ 20% of current imbalance).

| | $I_1$ [A] | $I_2$ [A] | $I_3$ [A] | $I_4$ [A] |
|---|---|---|---|---|
| Load current | *0.176* | 0.209 | 0.166 | 0.199 |
| | $\Delta I_1$ [A] / (% error) | $\Delta I_2$ [A] / (% error) | $\Delta I_3$ [A] / (% error) | |
| Current difference | -0.0336 / -19.1% | 0.043 / 20.5% | -0.0323 / -19.4% | |

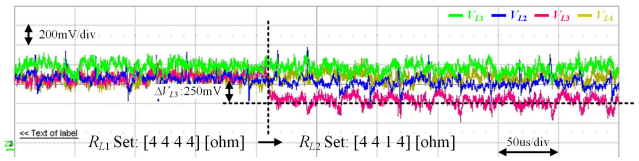



**FIGURE 13.** Experimental result of voltage waveform in load transient with 100kHz switching frequency in CSB method (4-level SVD, 0.825 of nominal core voltage, 47uF of the bulk capacitor, and 4.7uF of load capacitor).

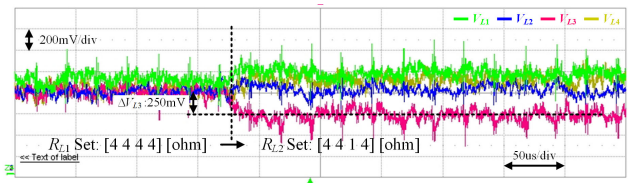



**FIGURE 14.** Experimental result of voltage waveform in load transient with 100kHz switching frequency in LS method (4-level SVD, 0.825 of nominal core voltage, 47uF of the bulk capacitor, and 4.7uF of load capacitor).

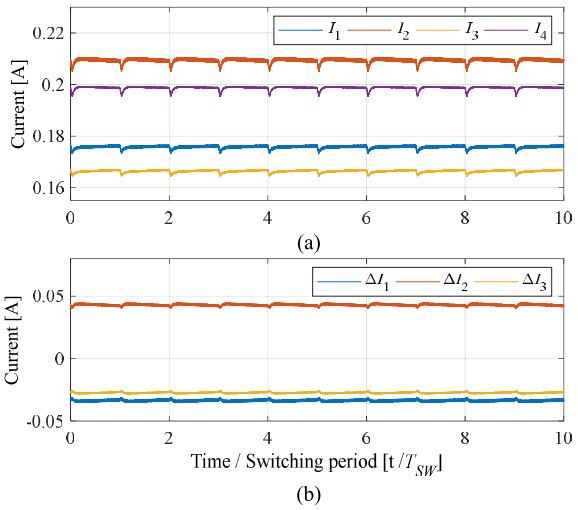



**FIGURE 15.** Experimental result of (a) load current $I_1 \sim I_4$ and (b) current difference $\Delta I_1 \sim \Delta I_3$, the values are summarized in Table 3.

is defined as

$$Efficiency = \frac{\sum_{k=1}^{4} V_k I_K}{V_{IN} I_{IN}}, \tag{30}$$

where $V_k, I_k, V_{IN}, I_{IN}$ are the voltage of $k_{th}$ load, the current of $k_{th}$ load, the input voltage, and the input current, respectively. To verify the measured efficiency and calculated results of loss modeling, the current for each load is measured as shown in Fig. 15. The average and difference values of current are summarized in Table. III for 20% current imbalance. Fig. 16 (a) and (b) show the measured efficiency with 20% and 50% of the current imbalance for both methods, respectively. Each dotted line is the efficiency result including the converter circuit only, and each solid line is the system efficiency, which takes into account the condition in (22)–(27). At 20% of the current imbalance, the CSB and LS methods have light load efficiencies of 90.88% and 88.21%, respectively. The peak efficiency of CSB and LS is 94.96% and 96.72% respectively. Compared with the calculation result of the efficiency shown in Fig. 8, the measured efficiency is slightly lower than that. The main reason is that (a): actual current and current difference are somewhat discontinuous in real operation and (b): gate driver and other circuits (level shifter) related losses are not included. As aforementioned in Section III, the efficiency varies depending on the current imbalance property. Based on the analytical modeling as shown in (22)–(27), these results provide options of proper balancing methods and usable range of loads, in which an engineer can select a topology with given system conditions under SVD structure.

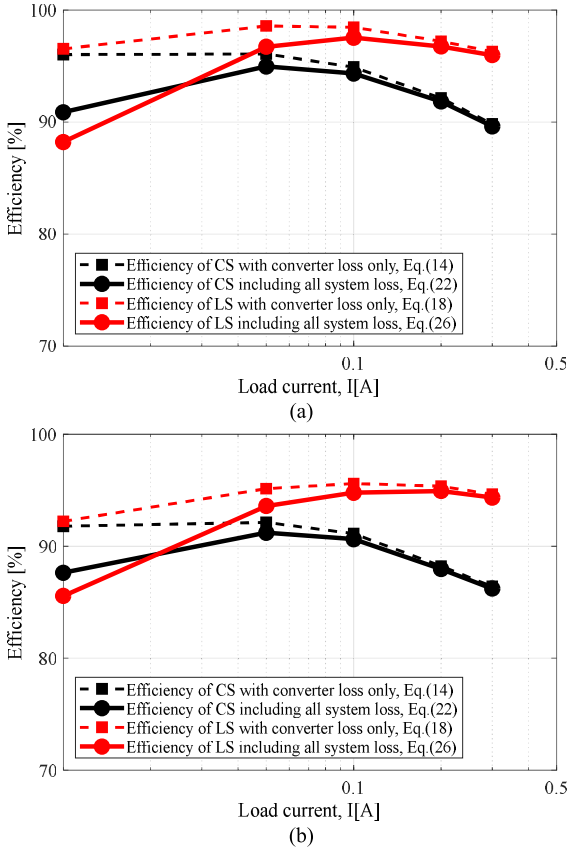



**FIGURE 16.** Experimental result of efficiency for capacitor stacking (CS) and load stacking (LS) method (100kHz switching) (a) 20% of the current imbalance, (b) 50% of the current imbalance.

## V. CONCLUSION

In this paper, the CSB method for SVD is proposed to achieve efficient, reliable DC-DC conversion for low-power applications in a stacked voltage domain. The analysis and design of a capacitor-stacking balancing circuit in the stacked voltage domain, including the time-domain operation, voltage equation, loss modeling, and dead-time effect, are explored and implemented. To validate the analysis, the proposed topology, called the CSB method, is evaluated and compared with a previous method. According to the analysis of system efficiency, the proposed method is preferable for light load current with minimal redundancy, while the load stacking method has higher efficiency for heavy load current than the CSB method due to its differential current property.

The experimental results show the measurement results of the voltage waveform and efficiency of 20% and 50% of the maximum workload, respectively. At 20% of the current imbalance, the CSB and LS methods have light load efficiencies of 90.88% and 88.21%, respectively. The peak efficiencies of CSB and LS are 94.96% and 96.72%, respectively. In this study, analysis and experimental results based on analytical modeling are particularly meaningful compared with previous studies that presented only experimental results without an analytical model. Based on the analytical modeling shown in (22)-(27), these results provide an appropriate balancing method and available load range options that allow an engineer to select a topology with specified system conditions in an SVD structure.

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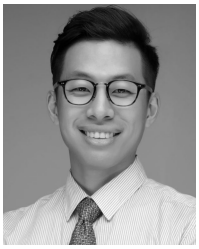

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