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All-Pass-Filter-Based PLL for Single-Phase Grid-Connected Converters Under Distorted Grid Conditions

TAO XIA, XU ZHANG, GUOJUN TAN, (Member, IEEE), AND YEZHAO LIU
School of Electrical and Power Engineering, China University of Mining and Technology, Xuzhou 221116, China

Corresponding author: Guojun Tan (gjtan_cumt@163.com)

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ABSTRACT All-pass-filter-based single-phase phase-locked loop (APF-PLL) is a widely used grid synchronization method in grid-connected power converters. However, the performance of APF-PLL degrades under distorted grid conditions and the estimated phase and frequency will contain low-frequency oscillation terms, which is not conducive to practical application. To deal with this problem, this paper proposes two advanced APF-PLLs, which have good ability to suppress harmonics and dc offset interference without sacrificing the dynamic response of the system. In the first one, a band-pass filter (BPF) is used as the prefilter of APF-PLL to process the input voltage signal, and in the second one, the APF-PLL input signal is processed by using a harmonic decoupling network (HDN) and multiple prefilters. In addition, their parameter design procedure is also described in detail and is easy to follow. The experimental results presented in this paper finally verify the superiority and effectiveness of the two proposed methods.

INDEX TERMS All-pass-filter (APF), phase-locked loop (PLL), dc offset, harmonic.

I. INTRODUCTION

In energy and power applications, such as pulse width modulation (PWM) rectifier, active power filters [1], distributed generation and uninterruptible power supplies (UPS) [2], it is extremely important to estimate grid voltage parameters (i.e., phase, frequency, and amplitude). In recent years, phase-locked loops (PLL) have been widely studied as a technology for grid synchronization.

The single-phase PLL consists of three parts: the phase detector (PD), the loop filter (LF), the voltage-controlled oscillator [3]. The main difference between different PLLs is usually the implementation of the PD module. In view of this, PLLs can be divided into two categories: pPLLs and QSG-PLLs. Compared with pPLLs, QSG-PLLs have attracted more attention. There are many ways to generate quadrature component, such as transfer delay-based PLL (TD-PLL) [4], inverse Park transformation-based PLL (IPT-PLL) [5], second-order generalized integrator-based PLL (SOGI-PLL) [6], Hilbert transformer-based PLL (HT-PLL) [7], the differential elements-based PLL (DE-PLL) [8] and all pass filter-based PLL (APF-PLL) [9].

Among the above PLLs, APF-PLL has been widely recognized because of its simple structure and stable performance. However, in practice, the grid voltage usually contains a dc offset caused by the measurement equipment. DC offset can cause undesired periodic ripples in the estimated phase and frequency. Therefore, in practical applications, the designed PLL must be free from the influence of harmonics and dc offset, which is a very important point.

In order to eliminate the influence of the dc offset on the PLL, [10] proposes the modified first-order filter-based PLL (MFOF-PLL). In this method, a degree of freedom (parameter k) is added to the APF-PLL structure. In addition, the APF-PLL is a special case of the MFOF-PLL with $k = 1$. However, this method reduces the ability of the PLL to resist harmonic interference. [11] eliminates dc offset by adding an LPF to the input signal, but the detailed parameter design is not explained. [12] eliminates the influence of dc offset by using the linear Kalman filter technique. However, this method is quite complicated and is not conducive to actual implementation. [13] adds an additional branch for SRF-PLL to eliminate dc offset, which calculates dc offset by

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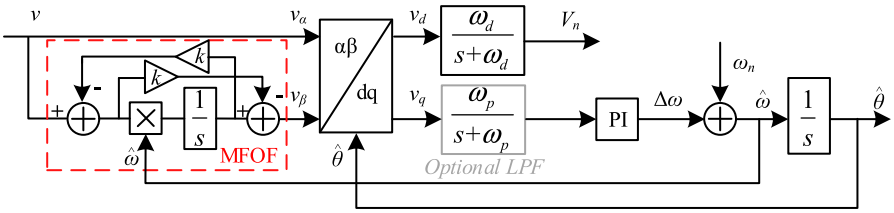

FIGURE 1. Block diagram of the MFOF-PLL.

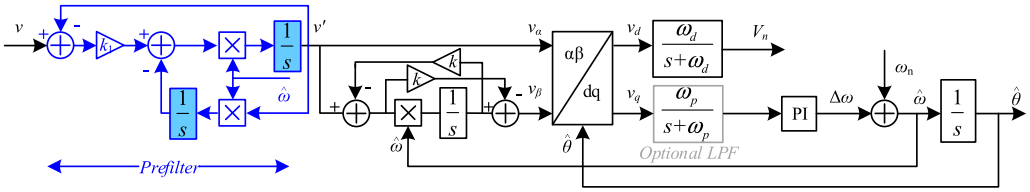

FIGURE 2. Block diagram of the MFOF-PLL-WPF.

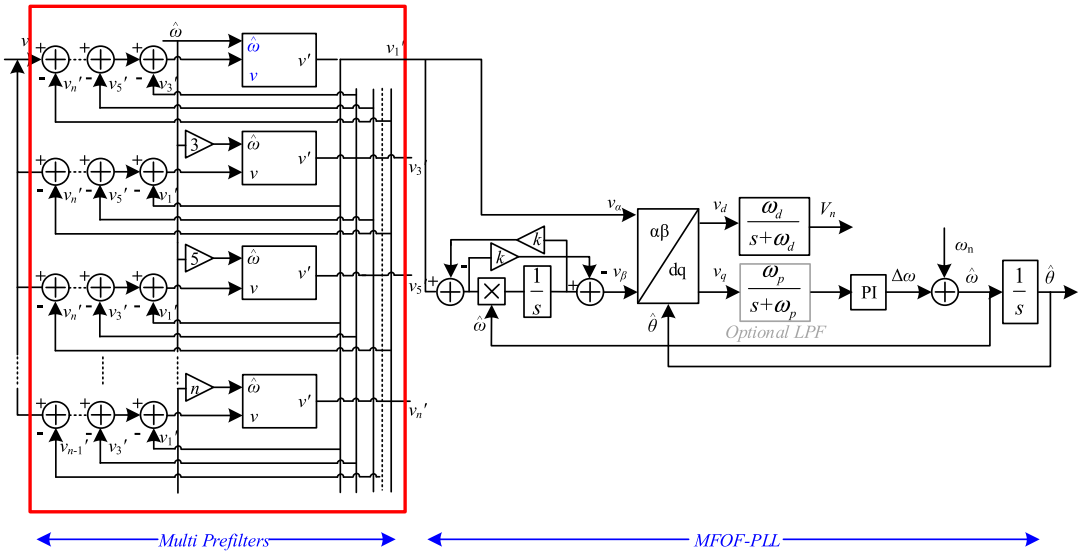

FIGURE 3. Block diagram of the MFOF-PLL-WMPF.

controlling the synchronous d-axis voltage in a PLL system to be zero. However, applying this method to APF-PLL can only ensure that the estimated frequency and phase are not disturbed by the dc offset. The quadrature component of the APF will still have the dc offset, which is not very suitable for the occasion where the input voltage fundamental and quadrature components need to be extracted. [14]–[17] propose a SOGI-FLL with prefilter. By using prefilters, this method enhances the accuracy of standard PLL under harmonic and dc offset conditions. In [18], the SOGI-FLL with in-loop filter is proposed. Both methods improve the performance of SOGI-FLL and can effectively suppress dc offset and harmonic interference.

Within this context, two advanced APF-PLLs, MFOF-PLL with prefilter (MFOF-PLL-WPF) and MFOF-PLL with multi-prefilters (MFOF-PLL-WMPF), are proposed in this paper, both of which use the prefilter to extract the fundamental component of the input signal under distorted grid conditions. Therefore, the dc offset is eliminated before accessing to the APF-PLL and no additional control loop is introduced into the PLL. The dynamic performance and stability of the PLL will not be affected obviously. In this paper, by extending the linear model of MFOF-PLL, we get the model of MFOF-PLL-WPF. Based on the obtained linear model, the parameter tuning of MFOF-PLL-WPF and MFOF-PLL-WMPF are described in detail. Finally, the experimental results show that the performance of the proposed MFOF-PLL-WPF and MFOF-PLL-WMPF are better than MFOF-PLL in the presence of harmonics and dc offset. In addition, MFOF-PLL-WMPF can achieve better results when the input contains a lot of harmonics compared with MFOF-PLL-WPF.

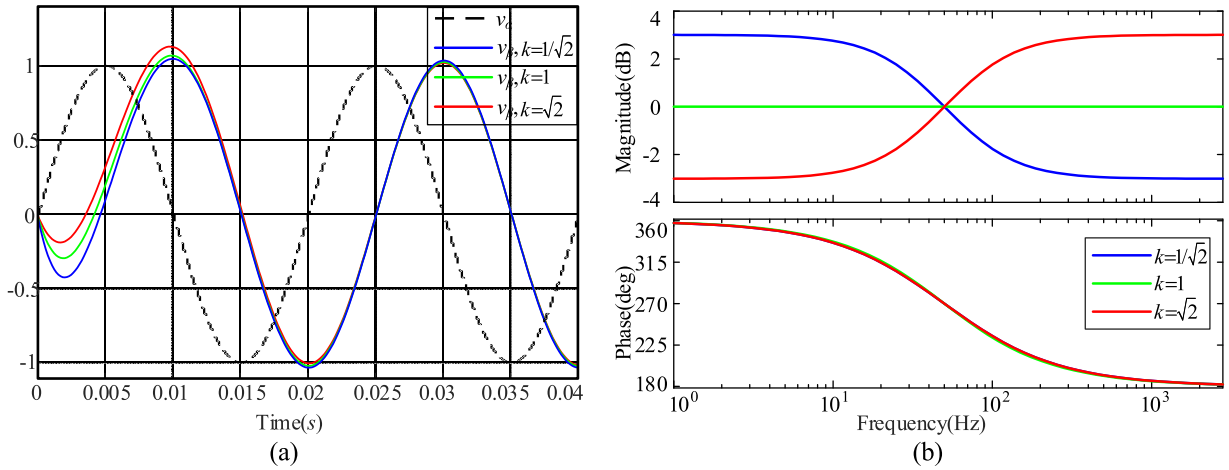

FIGURE 4. The MFOF responses for $\hat{\omega} = 2\pi 50$ rad/s, (a) Time, (b) Frequency.

II. MFOF-PLL

[10] proposes the modified first-order filter-based PLL (MFOF-PLL), by adding a degree of freedom to the APF-PLL structure. The schematic diagram of this approach can be observed in Fig. 2.

The quadrature component are given by

$$v_\alpha(s) = v(s) \tag{1}$$

$$v_\beta(s) = \frac{\hat{\omega} - ks}{k\hat{\omega} + s} v(s) \tag{2}$$

To observe the effect of MFOF after adding a degree of freedom, Fig. 4 shows the MFOF frequency response for three different values of $k = 1/\sqrt{2}$, $k = 1$ and $k = \sqrt{2}$. From this plot and (2), we can obtain the following results:

1. A high value of k makes the ability of the MFOF-PLL to suppress dc offset better, but its ability to suppress harmonics becomes poorer.

2. For different k, the MFOF has 0dB gain and $-90°$ phase shift at the fundamental frequency.

3. We can know from Fig. 4a that for different k, the OSG filter settling time is almost the same.

A. TUNING CONTROL PARAMETERS

Based on the linearized model of the MFOF-PLL in Fig. 5 [9], we can know

$$G_{ol}^{MFOF}(s) = \frac{\hat{\theta}(s)}{\theta(s) - \hat{\theta}(s)} = V_n \frac{0.5(s + \frac{k^2+1}{k}\omega_n)}{s + \frac{k^2+1}{2k}\omega_n} \frac{\omega_p}{s+\omega_p} \frac{k_p s + k_i}{s^2} \tag{3}$$

For the sake of analysis, define ω_n' as follows

$$\omega_n' = \frac{k^2+1}{2k}\omega_n \tag{4}$$

Therefore, (4) can be further written as

$$G_{ol}^{MFOF}(s) = \frac{\hat{\theta}(s)}{\theta(s) - \hat{\theta}(s)} = V_n \frac{0.5(s + 2\omega_n')}{s + \omega_n'} \frac{\omega_p}{s+\omega_p} \frac{k_p s + k_i}{s^2} \tag{5}$$

It is observed that selecting $\omega_p = 2\omega_n'$ results in a pole-zero cancellation and simplifies (5) as

$$G_{ol}^{MFOF}(s) = V_n \frac{\omega_n'}{s+\omega_n'} \frac{k_p s + k_i}{s^2} \tag{6}$$

Through the open-loop transfer function (6), we know that the designed system is a type-2 control system. For this system, we can use the symmetrical optimum method (SOM) to adjust the parameters [19], [20]. Therefore, by using SOM, we can obtain

$$k_p = \frac{\omega_c}{V_n} = \frac{\omega_n'}{V_n b} \tag{7-a}$$

$$k_i = \frac{\omega_c^2}{V_n b} = \frac{\omega_n'^2}{V_n b^3} \tag{7-b}$$

Here, $\omega_c = \sqrt{\omega_n' k_i / k_p}$, which guarantees the maximum phase margin (PM). $b^2 = \omega_n' / (k_i/k_p)$, which determines the PM value as PM $= \tan^{-1}\left(\left(b^2-1\right)/2b\right)$. By considering PM $=45^\circ$, $b = 1+\sqrt{2}$ is achieved. Substituting it into (7), we can get $k_p = 92.0$ and $k_i = 3507.1$. In this paper, based on a trial-and-error procedure, $\omega_d = \omega_n/2 = 157.1$rad/s is selected.

III. PROPOSED PLLS

A. MFOF-PLL-WPF

The transfer function of the prefilter in Fig. 2 is shown below.

$$G(s) = \frac{v'(s)}{v(s)} = \frac{k_1 \hat{\omega} s}{s^2 + k_1 \hat{\omega} s + \hat{\omega}^2} \tag{8}$$

Fig. 6 shows the Bode plots of $G(s)$ with different values of k_1, where $\hat{\omega} = 2\pi 50$ rad/s. It can be clearly known that prefilter is a second-order band-pass filter (BPF). And the prefilter has a gain of 0dB at the fundamental frequency ω_n and a phase shift of 0°. This proves that the use of prefilter does not cause the fundamental signal to lead or lag. The

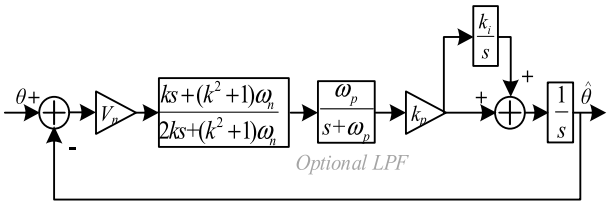

FIGURE 5. Linearized model of the MFOF-PLL.

value of k_1 determines the bandwidth of $G(s)$. A low value for k_1 makes the filtering effect of $G(s)$ better.

First, suppose the input signal $v(t)$ is expressed as follows

$$v(t) = v_{\mathrm{dc}} + V_n \sin(\omega t + \varphi) \tag{9}$$

Here, v_{dc} is the dc offset, V_n is the input signal amplitude, ω is the grid frequency, and φ is the initial phase.

Through the Laplace transform, $v(t)$ can be expressed by the following equation.

$$v(s) = \frac{U_{\mathrm{dc}}}{s} + \frac{V_n(\omega \cos\varphi + s \sin\varphi)}{s^2 + \omega^2} \tag{10}$$

Combining (8) and (10) we can get

$$v'(s) = \frac{k_1\hat{\omega}s}{s^2 + k_1\hat{\omega}s + \hat{\omega}^2}\left(\frac{U_{\mathrm{dc}}}{s} + \frac{V_n(\omega \cos\varphi + s \sin\varphi)}{s^2 + \omega^2}\right) \tag{11}$$

Applying the inverse Laplace transform to (11), we can obtain

$$v'_{\infty}(t) = mV_n \sin(\omega t + \varphi + \varphi_s) \tag{12}$$

$$m = \frac{k_1\hat{\omega}\omega}{\sqrt{k_1^2\hat{\omega}^2\omega^2 + \left(\hat{\omega}^2 - \omega^2\right)^2}} \tag{13}$$

$$\varphi_s = \tan^{-1}\left(\frac{\hat{\omega}^2 - \omega^2}{k_1\hat{\omega}^2\omega}\right) \tag{14}$$

Notice that the estimated frequency $\hat{\omega}$ is fed back to the prefilter for adapting it to the grid frequency changes. When the system is stable, that is $\hat{\omega} = \omega$, (12) can be written as

$$v'_{\infty}(t)\big|_{\hat{\omega}=\omega} = V_n \sin(\omega t + \varphi) \tag{15}$$

Therefore, the MFOF-PLL-WPF can effectively filter out the dc offset from the input signal, which can also be proved by Fig. 6.

1) TUNING CONTROL PARAMETERS

The block diagram of the MFOF-PLL-WPF is shown in Fig. 2. In this paper, we extend the MFOF-PLL model to obtain the linear model of MFOF-PLL-WPF, which is shown in Fig. 7.

Using (6), the closed-loop transfer function of MFOF-PLL may be approximated in the low-frequency range by

$$G_{cl}^{MFOF}(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{\omega'_n\left(V_n k_p s + V_n k_i\right)}{s^3 + \omega'_n s^2 + V_n\omega'_n k_p s + V_n\omega'_n k_i} \approx \frac{\omega'_n\left(V_n k_p s + V_n k_i\right)}{\omega'_n s^2 + V_n\omega'_n k_p s + V_n\omega'_n k_i}$$

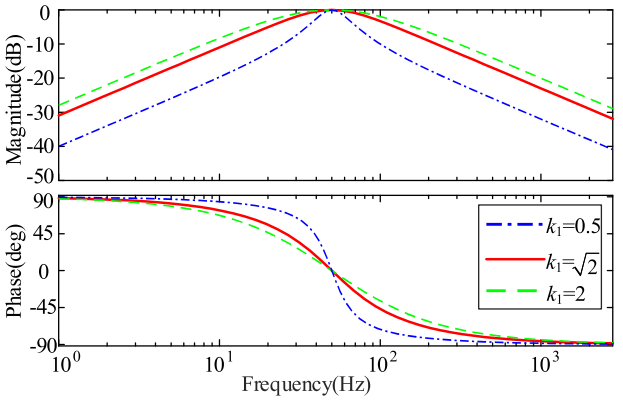

FIGURE 6. Bode plot of $G(s)$ with different k_1 values.

$$= \frac{V_n k_p s + V_n k_i}{s^2 + V_n\omega'_n k_p s + V_n\omega'_n k_i} \tag{16}$$

Therefore, using the same method, the closed-loop transfer function of MFOF-PLL-WPF can be approximated by (17), shown at the bottom of the next page.

By comparing (16) and (17), we can know that in order to make a fair comparison, the parameter selection (k_p and k_i) of MFOF-PLL-WPF should be the same as that of MFOF-PLL. The LPF cutoff frequency ω_d also should be designed to be the same. It is worth noting that in practice, for MFOF-PLL-WPF and MFOF-PLL-WMPF, their PI parameters and LPF cutoff frequency design can be completed in accordance with the MFOF-PLL. Therefore, only the value of k_1 needs to be considered for the proposed MFOF-PLL-WPF.

Assuming that $\hat{\omega}$ is a constant in Fig. 2, we can get

$$v'(s) = \frac{k_1\hat{\omega}s}{s^2 + k_1\hat{\omega}s + \hat{\omega}^2}v(s) \tag{18}$$

Based on (18), we can know that $k_1 = \sqrt{2}$ is the best choice. Under this condition, the corresponding damping factor is equal to $1/\sqrt{2}$. In this way, we can obtain the optimal choice between overshoot and settling time when using the pre-filter to obtain the fundamental component of the input signal.

B. MFOF-PLL-WMPF

The proposed MFOF-PLL-WPF can suppress high-order harmonic components and dc offset well. However, some specific harmonics that are very close to the fundamental frequency, such as the 3rd and 5th harmonics, will affect the stability of the PLL. Therefore, we propose the MFOF-PLL-WMPF.

In Fig. 3, we can see that the multi-prefilters can be understood as n bandwidth filters. By feeding back the estimated frequency $\hat{\omega}$ to the multi-prefilters and multiplying by the corresponding coefficient i, we can filter out the i-th harmonics.

However, some harmonic frequencies are very close, In order to filter out these harmonics, the filter usually needs to set a very narrow bandwidth, which will reduce the dynamic response speed of the system. Therefore, this paper uses the

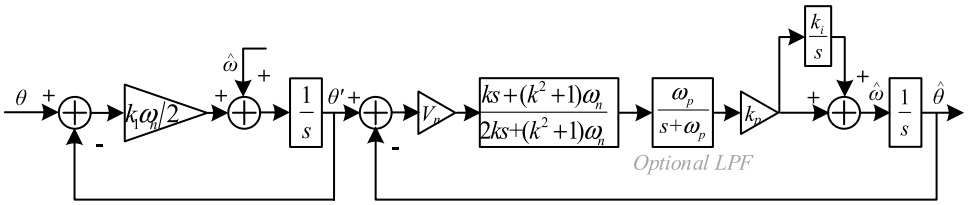

FIGURE 7. Linearized model of the MFOF-PLL-WPF.

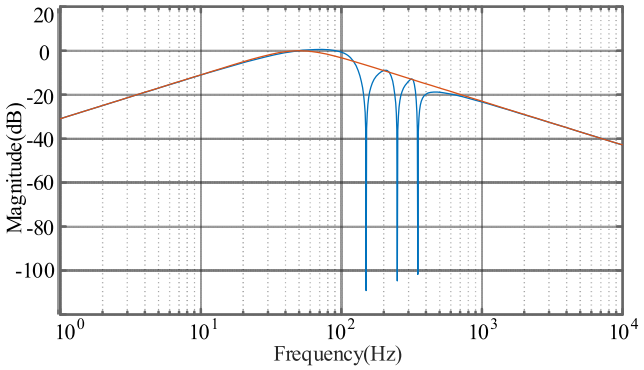

FIGURE 8. Frequency response of the MFOF-PLL-WMPF.

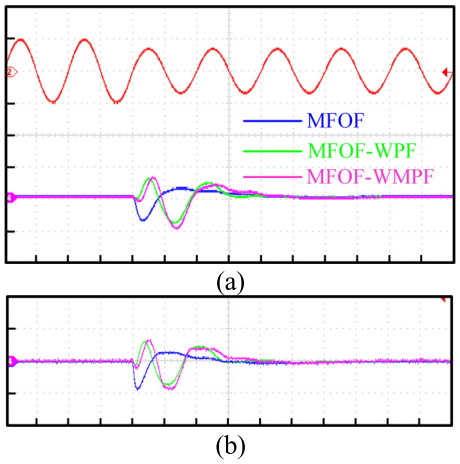

FIGURE 9. Experimental results for Test A. (a) Frequency estimation (1 Hz/div). the input voltage (1 p.u./div). (b)Estimation error of phase angle (0.5 deg/div). Time scale: 10ms/div.

harmonic decoupling network (HDN) to isolate the interaction between different harmonics of the input signal.

Fig. 8 is a Bode diagram of WMPF, where the brown line represents the WPF. We can know that compared with the WPF, the proposed WMPF shows better filtering characteristics at the corresponding resonance frequency.

1) TUNING CONTROL PARAMETERS

In this paper, the parameter k_i of the i-th harmonic is selected as follows

$$k_i = k_1/i \tag{19}$$

In this way, the product $\omega_i k_i$ can be kept constant, ensuring that the bandwidth of all harmonic extraction modules is the same. For a fair comparison, the other parameters of MFOF-PLL-WMPF are the same as those of MFOF-PLL-WPF.

IV. EXPERIMENTAL VALIDATION

An experimental platform based on floating point digital signal processor TMS320C28346 was built, and all input signals in the experiment were provided by the programmable AC power supply. In order to analyze the performance of the proposed MFOF-PLL-WPF and MFOF-PLL-WMPF, the following experiment was conducted with a sampling frequency of 10 kHz.

Five tests are considered.

1) Test A: A 0.3 p.u voltage sag happens.

2) Test B: The grid voltage has a sudden phase change of 20°.

3) Test C: The grid voltage experiences a frequency change from 50 Hz to 55 Hz.

4) Test D: The 10% dc offset is added into the grid voltage.

5) Test E: The grid voltage is considered to be polluted with 5% dc offset, 5% 3rd, 5% 5th and 5% 7th harmonics.

Fig. 9 shows the experimental results of all PLLs in Test A. It can be observed that when estimating the grid voltage parameters, the response speed of all PLLs is very close (about 1.5 cycles of the nominal frequency). Among these three methods, the estimated frequency of the MFOF-PLL has the least overshoot.

$$G_{cl}^{MFOF-WPF}(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{k_1\omega_n'^2\left(V_n k_p s + V_n k_i\right)}{2s^4+\left(2\omega_n'+k_1\omega_n'\right)s^3+k_1\omega_n'2s^2+k_1\omega_n'^2V_n k_p s+k_1\omega_n'^2V_n k_i}$$
$$\approx \frac{k_1\omega_n'^2\left(V_n k_p s + V_n k_i\right)}{k_1\omega_n'2s^2+k_1\omega_n'^2V_n k_p s+k_1\omega_n'^2V_n k_i} = \frac{V_n k_p s + V_n k_i}{s^2+V_n\omega_n' k_p s+V_n\omega_n' k_i} \tag{17}$$

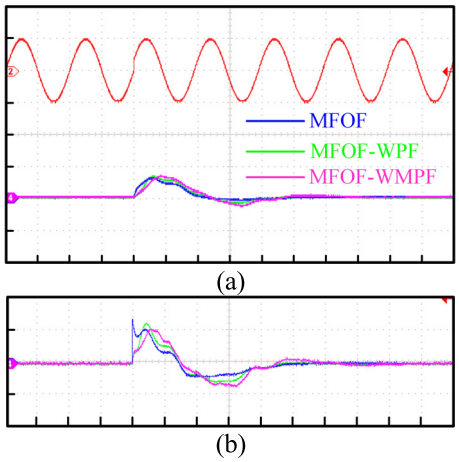

FIGURE 10. Experimental results for Test B. (a) Frequency estimation (1 Hz/div). the input voltage (1 p.u./div). (b)Estimation error of phase angle (20 deg/div). Time scale: 10ms/div.

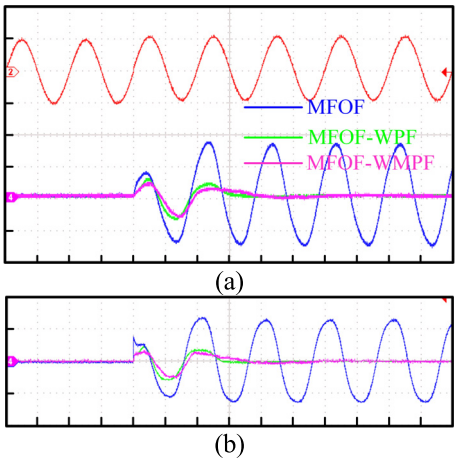

FIGURE 12. Experimental results for Test D. (a) Frequency estimation (1 Hz/div). the input voltage (1 p.u./div). (b)Estimation error of phase angle (2 deg/div). Time scale: 10ms/div.

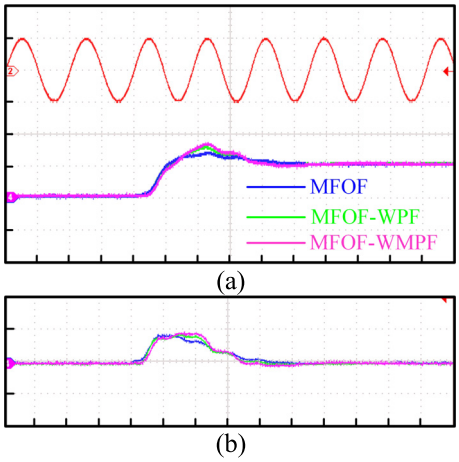

FIGURE 11. Experimental results for Test C. (a) Frequency estimation (5 Hz/div). the input voltage (1 p.u./div). (b)Estimation error of phase angle (0.5 deg/div). Time scale: 10ms/div.

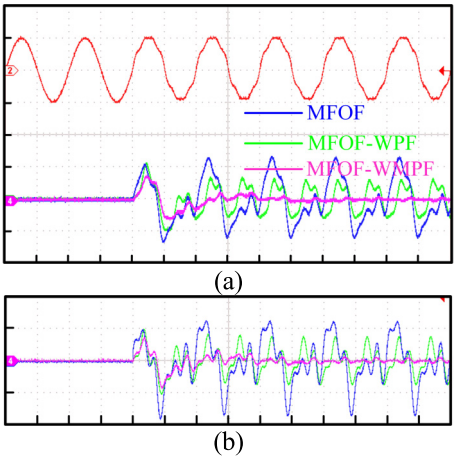

FIGURE 13. Experimental results for Test E. (a) Frequency estimation (1 Hz/div). the input voltage (1 p.u./div). (b)Estimation error of phase angle (2 deg/div). Time scale: 10ms/div.

The grid voltage undergoes a 20° phase jump in Fig. 10. It can be seen from the figure that the settling time of the three PLL algorithms is almost the same.

In Fig. 11, the grid voltage frequency is increased by 5 Hz. We can see that because the proposed PLL algorithms and MFOF-PLL both achieve frequency adaptation through frequency feedback, all PLLs can track the grid frequency change and the settling time is almost the same.

The experimental results under tests D and E are shown in Figs. 12 and 13, respectively. The proposed MFOF-PLL-WPF and MFOF-PLL-WMPF algorithms can effectively reject the interference of dc offset, but the MFOF-PLL will produce oscillation at the output. In addition, compared with the MFOF-PLL, the proposed MFOF-PLL-WPF and MFOF-PLL-WMPF can effectively improve the performance of PLL when the grid voltage contains a lot of harmonics. The MFOF-PLL-WMPF provides a bit higher harmonic filtering capability than the MFOF-PLL-WPF.

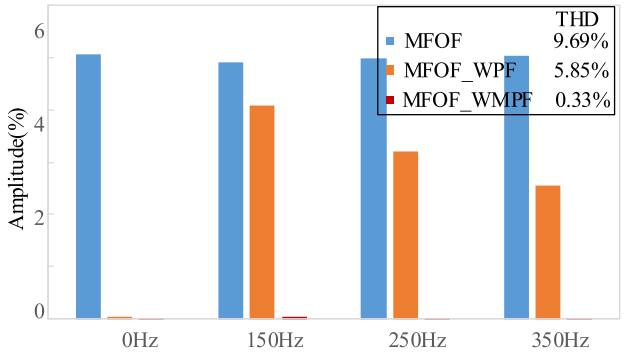

FIGURE 14. Harmonic distortions comparison.

Fig. 14 shows the harmonic distortion generated by the three PLLs under test E. From the figure, we can know that the proposed MFOF-PLL-WPF and MFOF-PLL-WMPF can effectively suppress harmonic interference and dc offset.

TABLE 1. Summary of the results.

	MFOF-PLL	MFOF-WPF	MFOF-WMPF
Voltage sag			
5% settling time	30.5ms	30.7ms	32.0ms
Phase overshoot	0.45°	0.35°	0.47°
Frequency overshoot	0.64Hz	0.78Hz	0.9Hz
Phase jump			
5% settling time	52.7ms	54.1ms	56.0ms
Phase overshoot	25°	24°	20°
Frequency overshoot	0.61Hz	0.72Hz	0.75Hz
Frequency jump			
5% settling time	40.5ms	42.2ms	43.1ms
Phase overshoot	0.41°	0.42°	0.44°
Frequency overshoot	2.14Hz	2.50Hz	3.29Hz
Phase margin	44.8°	44.5°	43.7°
DC offset			
5% settling time	—	42.7ms	43.8ms
Harmonics			
5% settling time	—	—	55ms

TABLE 2. Comparisons of computation load.

PLL Name	×	±	Integrators	TF
MFOF	3	2	1	0
MFOF-WPF	6	4	3	0
MFOF-WMPF	15	22	9	0

The experimental results are shown in Table 1. Frome these experimental results, we can get the following conclusions.

1) The MFOF-PLL suffers from a large oscillation error when the input signal contains the dc offset and harmonics. The proposed MFOF-PLL-WPF and MFOF-PLL-WMPF effectively suppress these interferences.

2) Compared with the MFOF-PLL-WPF, the MFOF-PLL-WMPF offers a higher capability in filtering out the grid voltage harmonics.

3) Under ideal grid conditions, the response speed of these PLLs is almost the same.

In addition, it is worth noting that compared with the MFOF-PLL-WPF, the MFOF-PLL-WMPF has stronger ability to suppress harmonics, but has a higher computational burden and a lower stability margin (see Tables 1 and 2).

V. CONCLUSION

In this paper, we proposes two advanced MFOF-PLLs (MFOF-PLL-WPF and MFOF-PLL-WMPF). By extending the small-signal modeling of the MFOF-PLL, we get the model of MFOF-PLL-WPF. Based on the obtained model, the parameters of these three PLLs are designed in detail. Finally, through experimental verification, the performance comparison of MFOF-PLL, MFOF-PLL-WPF and MFOF-PLL-WMPF was conducted under a fair condition. Experimental results show that the three methods have similar dynamic performance. However, the performance of MFOF-PLL-WPF and MFOF-PLL-WMPF is better than MFOF-PLL in the presence of dc offset and harmonics. In addition, compared with other PLLs, MFOF-PLL-WMPF also provides a method of measuring harmonic components, which has good advantages in some situations where the harmonic component of the input voltage is required. However, the proposed methods do not perform well in the presence of interharmonics. These issues will be considered in future work.

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TAO XIA was born in Gansu, China. He received the B.S. degree in electrical engineering and automation from Jilin University, Jilin, China, in 2014. He is currently pursuing the master's degree in electrical engineering with the School of Electrical and Power Engineering, China University of Mining and Technology. His research interests include grid synchronization technology and power converter control.

XU ZHANG was born in Liaoning, China, in 1990. He received the B.S. and M.S degrees in electrical engineering and automation from the China University of Mining and Technology, Xuzhou, China, in 2014 and 2017, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering with the School of Electrical and Power Engineering. His main research interests include power electronics, multilevel converter, data drive control, intelligent algorithm, and system optimization.

GUOJUN TAN (Member, IEEE) was born in Zunyi, Guizhou, China, in 1962. He received the Ph.D. degree in motor driver and its automation from the China University of Mining and Technology, Xuzhou, China, in 1992. Since 2000, he has been a Professor with the School of Information and Electrical Engineering, China University of Mining and Technology, where he has been the Chief Professor of National Key Discipline on power electronics and motor driver, since 2003. His main research interests include electrical drive, intelligent algorithm, and system optimization.

YEZHAO LIU was born in Yulin, Guangxi, China, in 1996. He received the B.S. degree in electrical engineering and automation from Jilin University, Jilin, China, in 2014. He is currently pursuing the master's degree in electrical engineering with the School of Electrical and Power Engineering, China University of Mining and Technology. His current research interest is mainly about reliability in power electronics and systems, including reliable assessment and multi-physics modeling of power electronic devices and converters.