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A 0.5 V 8–12 Bit 300 KSPS SAR ADC With Adaptive Conversion Time Detection-and-Control for High Immunity to PVT Variations

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ABSTRACT In this paper, a low power asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) involving the process, voltage, and temperature (PVT) compensation is presented. A proposed adaptive conversion time detection-and-control technique enhances the power efficiency, covering wide PVT variations. The proposed detection-and-control technique senses PVT variation in an aspect of conversion time, and adaptively controls the operation speed and power consumption. For PVT compensation, the proposed architecture includes the local supply/ground voltage. The local supply/ground voltage makes high $|V_{GS}|$ for transistors in the comparator and capacitive digital-to-analog converter switches, resulting in enhanced operation speed. However, when PVT condition changes to be favorable for the conversion speed, the $|V_{GS}|$ decreases for low power consumption. 30 chips were measured to verify the proposed ADC. Having the proposed architecture tested with 10 kHz input frequency, SNDR remained higher than 60 dB at unfavorable conditions such as -9 % supply voltage variation, or -20 °C temperature variation. On the other hand, at favorable conditions such as $+9$ % supply voltage variation, or 80 °C temperature variation, the power consumption of SAR ADC decreased without performance degradation.

INDEX TERMS Asynchronous, compensation, low power, process voltage temperature (PVT), successive approximation register (SAR) analog-to-digital converter (ADC).

I. INTRODUCTION

The successive approximation register (SAR) analog-to-digital converters (ADCs) are the most promising candidate for low power applications such as battery-powered sensor nodes and bio-medical systems. SAR ADCs operating at low supply voltage for power efficiency have been reported [1]–[9]. Since using the low supply voltage can cause problems such as leakage current or low signal-to-noise ratio (SNR), many studies mainly have focused on the leakage current or low SNR. However, the low supply voltage SAR ADCs are also vulnerable to process, voltage, and temperature (PVT) variations. Recently, several ADCs involved temperature compensation technique for comparator under the low supply voltage, and PVT-stabilized technique for dynamic amplifiers [9]–[11]. Besides these problems, conversion speed also can be severely affected by PVT variations. Due to the uncertainty of PVT variations, ADCs should have much faster conversion speed than target specifications. However, it causes unnecessary power consumption at the PVT

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conditions that are favorable for the conversion speed. When MOSFET is operating in the subthreshold region, the drain current is

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{TH}}{mU_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{U_T}\right)\right) \quad (1)$$

where $I_0 = \mu_0 C_{ox}(W/L)U_T^2\,(m-1)$, and μ_0, C_{ox}, U_T, and m denote the carrier mobility, gate oxide capacitance, thermodynamic voltage (kT/q), and subthreshold slope factor, respectively [9], [12]–[13]. The high sensitivity of drain current to PVT variations can be inferred by using (1) [13]. Fig. 1. shows a normalized conversion time at the worst-case corner and temperature conditions depending on the supply voltage. The normalized conversion time means that the longest conversion times are divided by the conversion time that is required at the TT, 27 °C. When the supply voltage is 1.2 V, the conversion time becomes longer by 1.28-times at the SS and 80 °C in comparison with the conversion time at the TT and 27 °C. For 0.5 V supply voltage, the conversion time becomes longer by 7.66-times at the SS and −20 °C in comparison with the conversion time at the TT and 27 °C. These variations result in accuracy degradation due to incomplete conversion in asynchronous SAR ADC. In other words, the ADCs having 1.2 V supply voltage should have 1.28-times faster conversion speed than the speed that is required at the TT and 27 °C, which prevents performance degradation at the SS and 80 °C. However, for the ADCs having 0.5 V supply voltage, the conversion speed should be 7.66-times faster, which implies much larger power consumption. Therefore, in this paper, a low-power SAR ADC with full consideration of PVT variations is proposed. The proposed system detects the PVT variation by monitoring the conversion speed and then controls the supply voltage to reduce power consumption. Fig. 2. shows the PVT compensation and reduction in current by controlling the supply voltage depending on PVT condition. As shown in Fig. 2., the conversion time becomes short by increasing the supply voltage to compensate for the PVT variations. In the case of the other PVT conditions, the supply voltage level becomes lower for low power operation, which does not cause performance degradation. Section II will discuss the proposed architecture for sensing and compensating the PVT variation. In sections III and IV, the implementation of the proposed SAR ADC and measurement results will be presented. Lastly, a conclusion will be drawn in sections V.

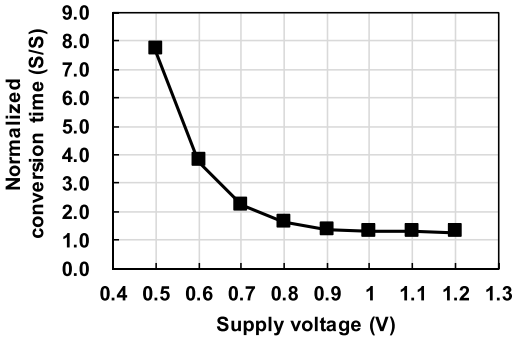


FIGURE 1. Normalized conversion time at the worst-case corner and temperature conditions with various supply voltages from 0.5 V to 1.2 V.

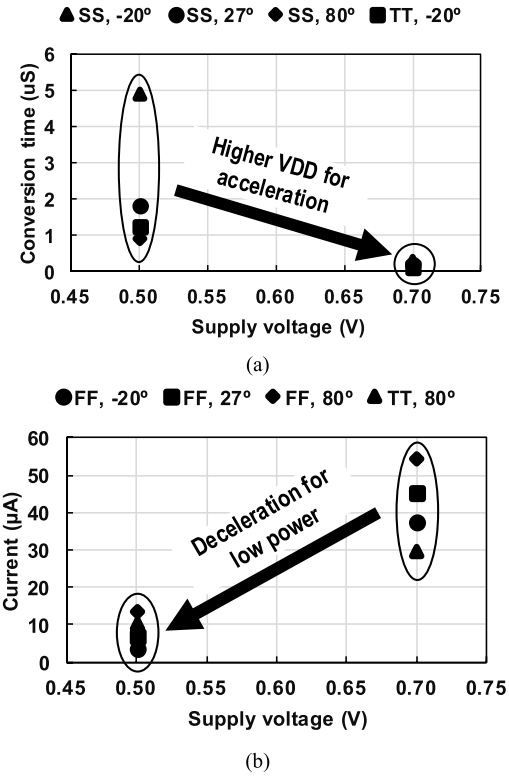


FIGURE 2. (a) The process, voltage, and temperature (PVT) conditions that require acceleration by increasing VDD (supply voltage) and (b) the other PVT conditions that can reduce the current for low power operation.

II. PVT COMPENSATION SYSTEM

Fig. 3. shows the conceptual block diagram of the proposed PVT compensation system. The supply voltage generator supports the ADC's global supply voltage, and the I_{ADC} represents the current. Once the 'PVT SENSING' block gives the information of PVT to the 'Local supply/ground' blocks, local supply/ground voltages of 'comparator' and 'switches' of a capacitive digital-to-analog converter (C-DAC) are adjusted. In the SAR ADC operation, the comparison time of the comparator, and settling time of C-DAC have a large portion of the overall conversion speed. This problem becomes worse when the resolution of ADC increases. Thus, the change in local supply/ground voltages for these blocks can control the conversion speed of ADC, as described in Fig. 2. (a). If PVT changes to be favorable for the conversion speed, local supply/ground voltages become original values like Fig. 2. (b) to reduce the I_{ADC} of Fig. 3, which assuring low power consumption.

A. SENSING THE PVT VARIATIONS

PVT SENSING block senses conversion speed (or conversion time) to sense the PVT variations. Since SAR ADC determines each bit in consecutive order, the least-significant-bit (LSB) decision denotes the end-of-conversion (EOC).

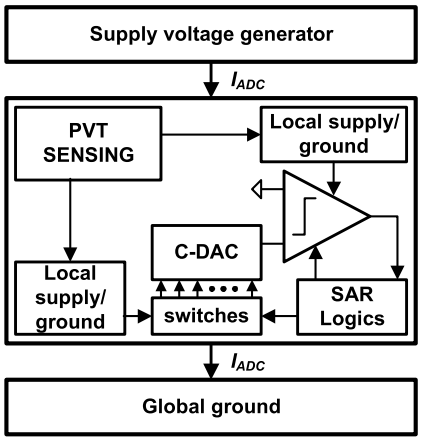


FIGURE 3. The conceptual block diagram of the proposed PVT compensation system.

The detection logic compares the EOC with the next sampling clock that is synchronized by the reference clock to monitor the conversion speed [14]. If conversion speed becomes too slow to complete the conversion, the next sampling clock precedes the EOC. In this case, the PVT SENSING block increases the thermometer code (D_{DNC}) to accelerate the conversion speed. However, at some PVT conditions such as FF corner, higher supply voltage, or 80 °C, the accelerated conversion speed causes large power consumption. Therefore, if the EOC precedes the next sampling clock because of fast conversion speed, the PVT SENSING block decreases the D_{DNC} to decelerate the conversion speed and reduce the power consumption. After several sequences of the tracking PVT, D_{DNC} has two repeated codes in the locking state. Fig. 4. shows a locking state and the criteria to prevent the LSB-missing in the locking state. Since the deceleration of conversion speed can cause LSB-missing, the PVT SENSING block compares the sampling clock with a delayed EOC (DEOC) that is the delayed signal from EOC by T_{delay}. Moreover, if the conversion time variation by changing D_{DNC} (ΔT_{com}) is too large, LSB-missing occurs in the locking state. Therefore, ΔT_{com} should be shorter than T_{delay}, i.e., detection-and-control has the following criteria.

$$T_{delay} > |\Delta T_{com}| \tag{2}$$

B. COMPENSATING PVT VARIATIONS

Local supply/ground voltage can be easily realized by capacitor switching by using a temporal voltage shift because all sub-blocks of SAR ADC are the dynamic circuits. The local supply/ground voltage increases before the operation, and the sub-blocks operate fast with a high $|V_{GS}|$ and $|V_{DS}|$. For convenience, only $|V_{GS}|$ will be mentioned in this paper. After the operation of sub-blocks, the capacitors are charged again during the reset phase. The local supply/ground voltage has a multi-level, and the D_{DNC} determines the voltage level. The number of levels determines the resolution of the control of power consumption. However, increasing the number of levels leads to the burdens of hardware complexity and power consumption, which cancels out the benefits. Moreover, the maximum number of cycles to find the locking state also increases.

III. IMPLEMENTATION

Fig. 5. shows a block diagram of the proposed SAR ADC. It consists of 8-12-bit reconfigurable split-capacitor C-DAC, detection-N-control (DNC), adaptively accelerating C-DAC settling switch (ACS), and adaptively boosting comparator (ABC) blocks. The following sections show each block in detail.

A. DETECTION-N-CONTROL (DNC)

As shown in Fig. 5., the DNC consists of dividers, a phase detector (PD), a delay block, and a thermometer counter. The PD determines whether the SAR operation is fast or not by comparing the DEOC with the next sampling clock. If DEOC rises before the next sampling clock, UP/DOWN becomes LOW. On the contrary, UP/DOWN becomes HIGH if DEOC does not precede the next sampling clock. Depending on the UP/DOWN signal, 4-bit (5 levels) thermometer code (D_{DNC} <3:0>) increases or decreases, and ACS and ABC block uses the value to control the local supply/ground voltage. In this design, after the ADC wakes up, the maximum number of cycles is 4. In the case of increasing D_{DNC} <3:0>, the duration for comparison and C-DAC settling gets shorter. The delay block makes the delay time from EOC to DEOC (T_{delay}) where the time duration of the delay cell is determined by (2). Delay block consists of inverters, and the number of inverters is determined by the worst-case PVT conditions to guarantee the condition of (2). Two T-F/F make the 1/2 divided and 1/4 divided CK_SAM clock (period of each signal is 2× and 4× period of CK_SAM) for PVT detection, and D_{DNC} update, respectively. In other words, the compensation procedure is repeated every four conversion cycles and fully utilizes the given conversion time for low-power operations.

B. VDD-BOOSTER AND VSS-SINKER FOR MULTI-LEVEL SUPPLY/GROUND VOLTAGE

The VDD-Booster and VSS-Sinker blocks generate the multi-level supply/ground voltage adaptively to compensate for the PVT variation. Fig. 6. shows the schematics of VDD-Booster and VSS-Sinker. The VDD-Booster generates a higher voltage than the supply voltage by switching the capacitors. The increased voltages of the VDD_{Boost} node are proportional to the number of switched capacitors among the capacitor bank. D_{ACL} is a synchronized D_{DNC} by CK signal for capacitor switching. In the case of VDD-Booster, when CK is HIGH, the capacitors are charged, and the voltage of VDD_{Boost} becomes VDD. At the falling edge of CK, the gate of M_P becomes HIGH, so that M_P turns off. Then, the bottom of the capacitor switches from the ground to VDD. To prevent the leakage current by high VDD_{Boost} voltage, the gate and body nodes of M_P rise to VDD_{Boost} voltage. Even if the gate and body nodes of M_P do not rise to the VDD_{Boost} voltage,

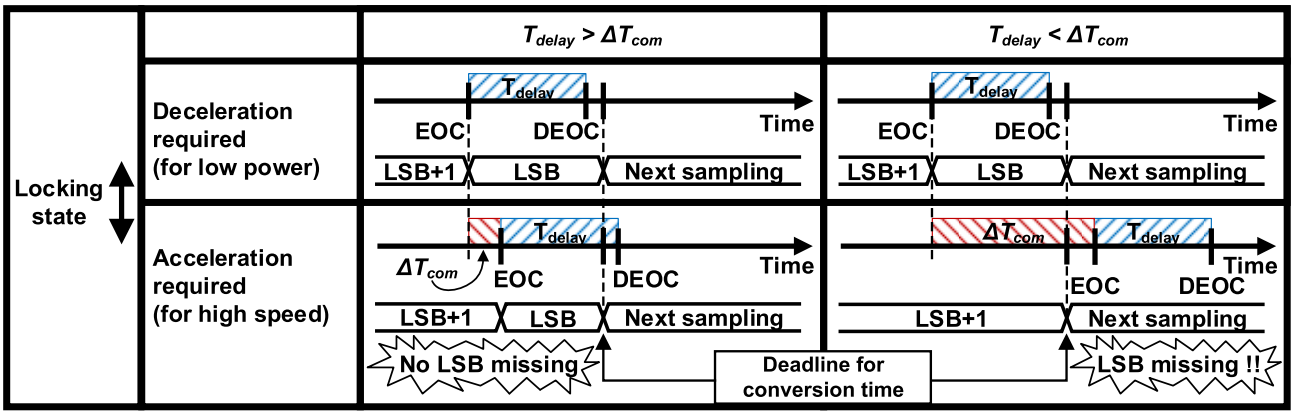
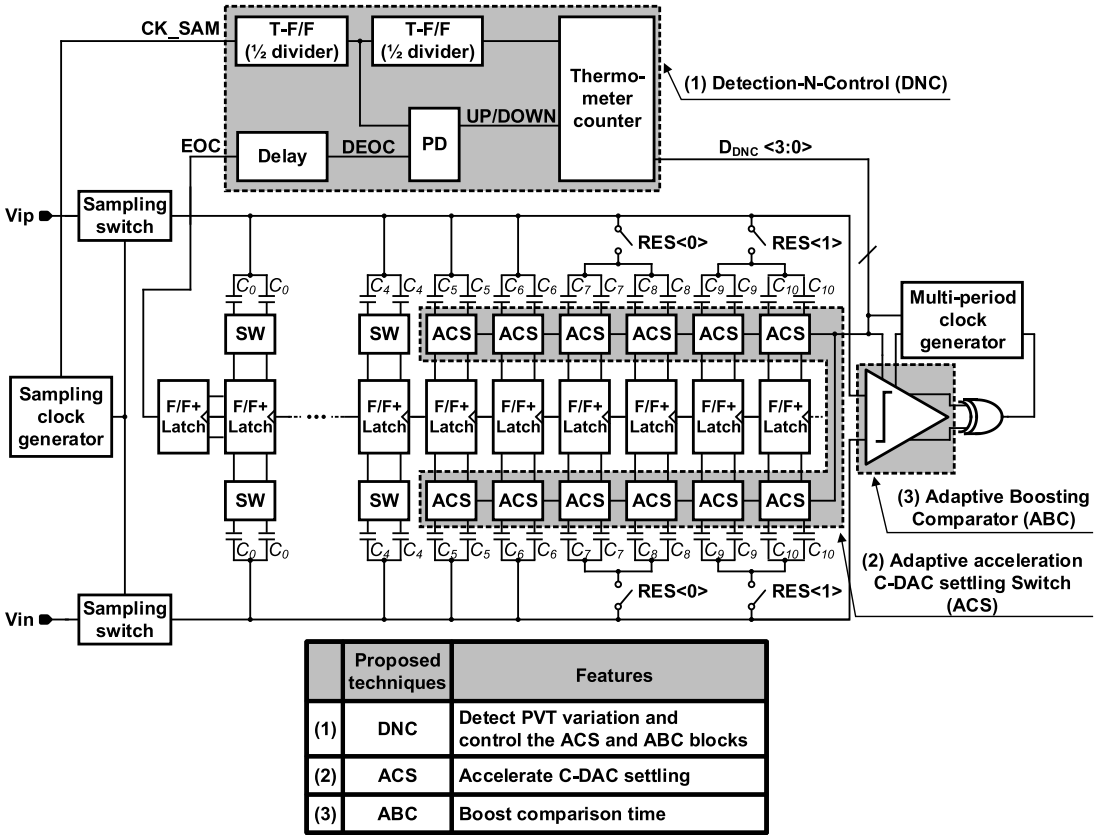


FIGURE 4. A locking state and criteria to prevent the least-significant-bit (LSB) missing.



	Proposed techniques	Features
(1)	DNC	Detect PVT variation and control the ACS and ABC blocks
(2)	ACS	Accelerate C-DAC settling
(3)	ABC	Boost comparison time

FIGURE 5. Block diagram of proposed ADC.

the momentary leakage current can be ignored. When CK becomes HIGH again, the gate of M_P becomes LOW, and the bottom of capacitors switches from VDD to ground. The VSS-Sinker block operates similarly as the VDD-Booster block.

C. ADAPTIVE ACCELERATION C-DAC SETTLING SWITCH (ACS)

Since the capacitance of C-DAC exponentially increases with a resolution of ADC, C-DAC settling time should decrease to speed up the SAR operation. Fig. 7. (a) shows the implementation for adaptively accelerating the C-DAC settling switch (ACS). To enhance the C-DAC settling speed, VDD-Booster and VSS-Sinker are used to S-inverters (small W/L) driving L-inverters (large W/L) which drive the capacitors of C-DAC. In the split capacitor C-DAC [15], COMPX (COMPP or COMPN) nodes and MX (M1 or M2) nodes change from HIGH to LOW and from LOW to HIGH, respectively, during C-DAC switching. In a differential split capacitor C-DAC, four capacitors (C_n) take a role in one bit, and thus, four S-inverters share a single VDD-Booster and VSS-Sinker. The $|V_{GS}|$s of PMOS and NMOS in the S-inverter are

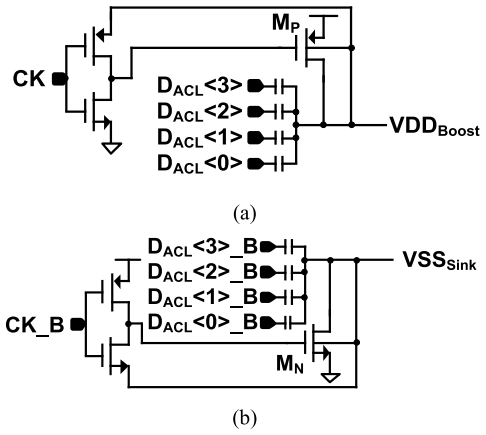


FIGURE 6. Schematic of (a) VDD-Booster and (b) VSS-Sinker for local supply/ground voltages.

increased by VDD-Booster and VSS-Sinker blocks. The temporal changes in source voltages provide a higher $|V_{GS}|$ to the small inverter and help driving L-inverter with higher current. Then, higher $|V_{GS}|$ provided sequentially to L-inverter results in the acceleration for the C-DAC switching. Fig. 7. (b) shows the effect of C-DAC acceleration. At a start of sampling (rising edge of CK_SAM), VDD_{Boost} and VSS_{SINK} nodes change in advance. After sampling and prior-switchings, COMPX signal changes from HIGH to LOW. Because of higher $|V_{GS}|$, the switching of the bottom plate (CBOT) becomes faster. The capacitances of switching capacitors in the VDD-Booster and VSS-Sinker blocks are large enough regarding leakage current and accelerated speed.

The proposed SAR ADC adopts a multi-period clock generator [14]. The multi-period clock generator selects the number of buffers according to D_{DNC}, controlling the period of comparator clocks suitable for the C-DAC switching speed.

D. ADAPTIVE BOOSTING COMPARATOR (ABC)

Fig. 8. shows the schematic of the adaptive boosting comparator (ABC). The ABC comprises of an integrator-based amplifier and the latch [16]. VDD-Booster and VSS-Sinker are used to the second stage and the first stage, respectively. At a reset phase, the voltages of OUT1/OUT2 are VDD, and outputs of the second stage are LOW. During an evaluation phase, the OUT1/OUT2 nodes decrease with different speeds according to the input differences. The second stage uses the difference between OUT1/OUT2 nodes to determine the output of the comparator (OUTN/OUTP). Without acceleration, the discharging for load capacitors of the first stage takes a longer time, and the metastability problem of the second stage can be even worse. With acceleration, D_{Sink} and D_{Boost} signals that are decoded from D_{DNC} and synchronized with clock(Φ) switch the bottom of capacitors of VSS-Sinker and VDD-Booster. Switching capacitors in VSS-Sinker and VDD-Booster blocks increase the $|V_{GS}|$ of input transistors in each stage. Consequentially, the ABC archives fast discharging and the decision. Table. 1. shows the simulation results

TABLE 1. Simulation results and noise budget.

PVT variation	V_Q (nV^2)	V_T (nV^2)	V_C (nV^2)	SNR (dB)	T_{comp} (nS)
TT, 27 ºC W/O boosting	4.97	1.01	22.94	66.36	21.1
SS, -20 ºC W/O boosting		0.85	9.50	69.12	249.37
SS, -20 ºC W boosting			14.43	67.91	59.20

TABLE 2. Summary of dynamic performance at 8 and 10-bit modes.

	Low frequency (10kHz)		Near nyquist frequency	
	SFDR (dBc)	SNDR (dB)	SFDR (dBc)	SNDR (dB)
8-bit	70.37	48.98	71.17	48.92
10-bit	74.81	59.14	72.72	57.07

of the noise and comparison time (T_{comp}) of the ABC. The noise includes quantization noise (V_Q), thermal noise (V_T), and comparator noise (V_C). The simulation results show that the comparison time at SS corner and −20 °C is longer than that of TT and 27 °C without boosting. However, with the boosting, the comparison time decreases without degradation of SNR compared with TT, 27 °C.

E. RECONFIGURABLE C-DAC

The proposed SAR ADC also has the resolution reconfigurable functions [17]. Fig. 9. shows the schematic of the C-DAC with the resolution reconfigurability. External digital codes for the reconfigurable operation connect additional capacitors to 8-bit C-DAC. The switches between CTOP node and $CTOP_{AUX1}$ or $CTOP_{AUX2}$ are 2.5V NMOS transistors (I/O transistor), and the gate voltage swing is 2.5V for the linearity.

IV. MEASUREMENTS

The prototype was fabricated in 65 nm CMOS, and the size is 0.039 mm^2 (0.318 mm × 0.123 mm). Fig. 10. shows the fabricated die micrograph. Even though ADC involves the VDD-Booster, VSS-Sinker, and DNC blocks, there is no extra area for them because the C-DAC area dominates the ADC area. The temperature chamber changed the chip temperature, and the power supply changed the supply voltage. Lastly, 30 chips from 2 wafers were measured to consider process variation. Fig. 11. shows the measured ENOB and current where A, B, and C indicate 'disable the proposed scheme (conventional),' 'enable (ACS + ABC),' and 'enable (ACS + ABC + DNC),' respectively. In these

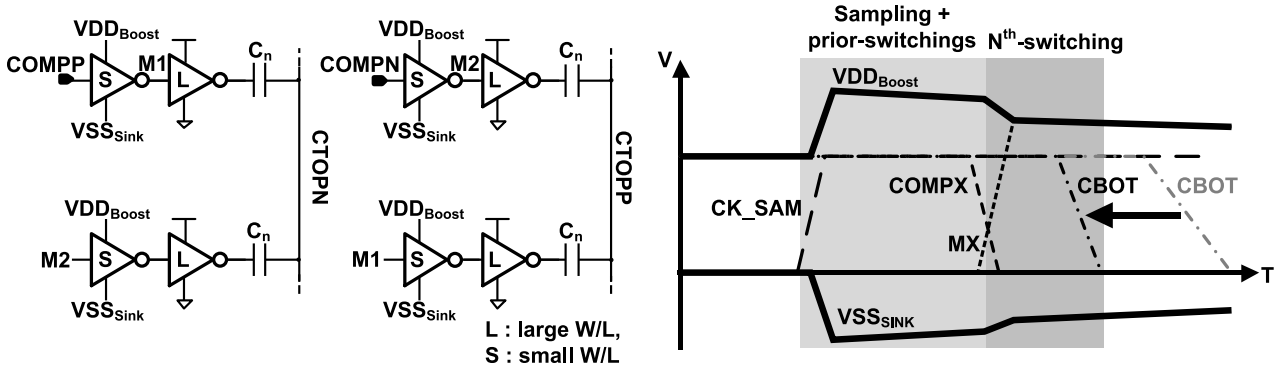


FIGURE 7. The (a) implementation of adaptive acceleration C-DAC settling switch (ACS) and (b) effect of capacitive digital-to-analog converter (C-DAC) acceleration.

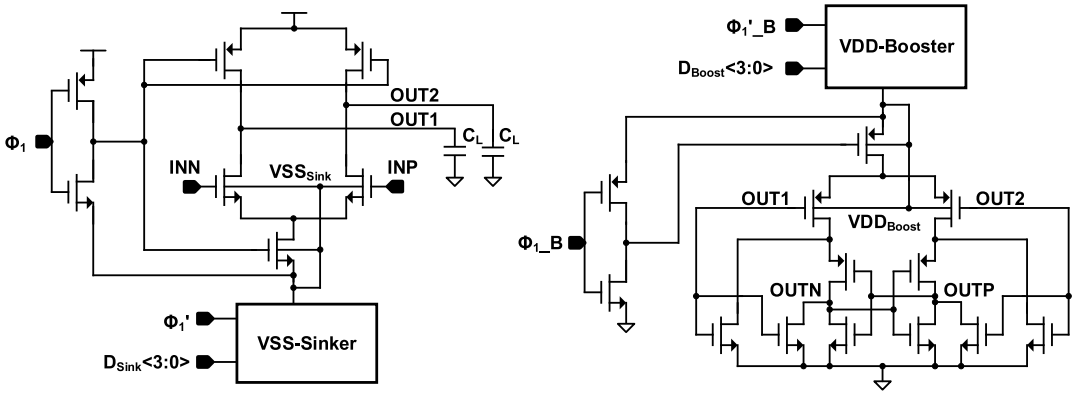


FIGURE 8. The schematic of an adaptive boosting comparator (ABC).

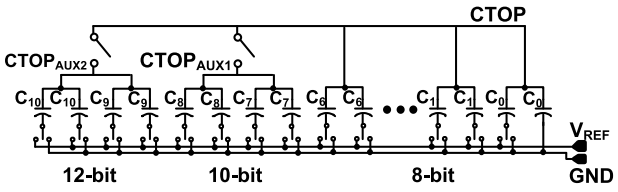
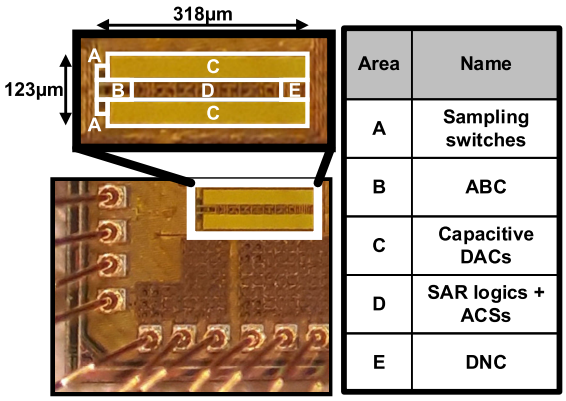


FIGURE 9. Schematic of C-DAC with resolution reconfigurable function.



Area	Name
A	Sampling switches
B	ABC
C	Capacitive DACs
D	SAR logics + ACSs
E	DNC

FIGURE 10. Fabricated die micrograph.

measurements, the PVT variations include the supply voltage variation from 0.46 V to 0.54 V (+/− 9 % variations), temperature variations from −20 °C to 80 °C, and the sampling rates ranging from 100 KSPS to 700 KSPS. At the harsh condition of 700 KSPS, 0.46 V, or −20 °C, ENOB of 'C' (adaptively managing) has the same ENOB with the same in 'B' (continuously accelerating). And, at the favorable situation for ENOB, such as slower sampling rate, higher supply voltage, or higher temperature, the current in 'C' mode is decreased by 27% compared to 'B' mode without ENOB degradation. Unlike 'A' and 'B', 'C' mode has relatively consistent FoM_W in the wide PVT variations. That is, the proposed SAR ADC can adaptively control the power consumption and conversion speed depending on PVT variations. 30 dies from two different wafers of an MPW shuttle were tested to verify the performance over chip-to-chip variations. Measurement results show their ENOBs at 300 KSPS, 500 KSPS, and 700 KSPS as a function of samples. Fig. 12. and 13. shows the measurement results of dynamic performances and DNL/INL of the proposed ADC at 12-bit configuration, respectively. The

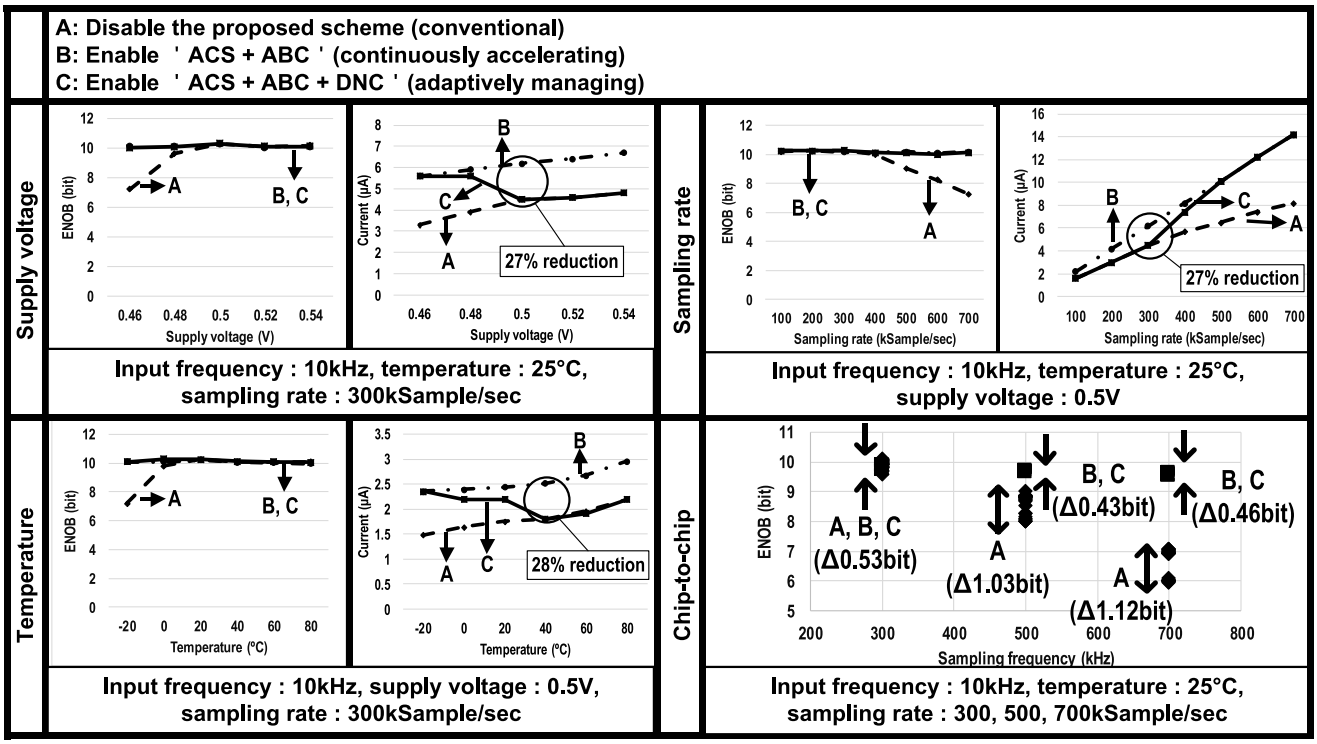


FIGURE 11. The measured ENOB and current (power consumption). In this figure, A, B, and C indicate 'disable the proposed scheme (conventional)', 'enable (ACS + ABC)', and 'enable (ACS + ABC + DNC)'.

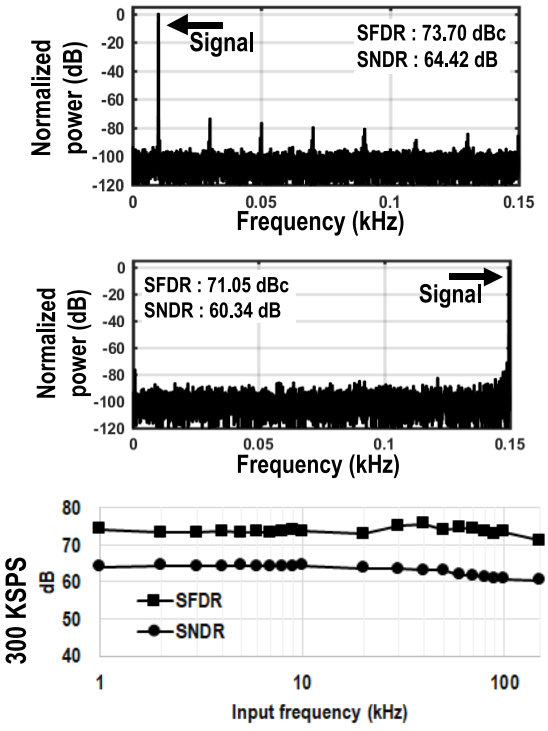


FIGURE 12. The measurement results of dynamic performance.

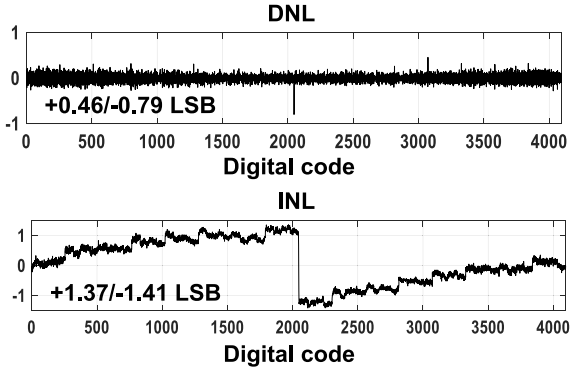


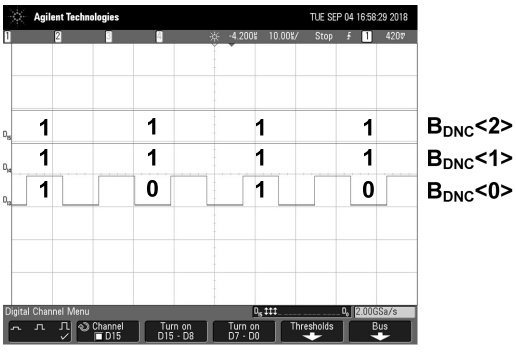
FIGURE 13. The measurement results of static performance.

SNDRs are 64.42 dB and 60.34 dB at low frequency (10kHz) and near the Nyquist rate and DNL and INL are 0.79 LSB and 1.41 LSB. Table 2. shows the dynamic performances of 8 and 10-bit modes. Fig. 14. shows the measured locking status by an oscilloscope. B_{DNC} <2:0> is a binary code of D_{DNC}. In this measurement, B_{DNC} repeat between 111 and 110 after PVT compensation. Table 3. shows the performance summary and comparison table for the state-of-the-art low supply voltage ADCs. Dynamic performances in the table are the measurement results at 300 KSPS with Nyquist input frequency. Recent researches have studied PVT variations on the low supply voltage SAR ADCs [9], [11]. At the various PVT conditions, such as process variation (30 chips), voltage variations (+/− 9 % supply voltage), and temperature variations (from −20 °C to 80 °C), SNDR remains over 60 dB.

TABLE 3. Performance summary and comparison table.

	Tai [2] (ISSCC-2014)	Chen [18] (JSSC-2016)		Hsieh [7] (ISSCC-2018)	Hong [9] (TOCAS I-2019)	Zhang [11] (ISSCC-2019)	This work
Technology	40nm	90nm		90nm	180 nm	65nm	65nm
Supply voltage (V)	0.45	0.4	0.7	0.4	0.225	0.6	0.5
Sampling rate (KSPS)	200	250	4000	270	0.45	20000	300
Resolution (bit)	10	10		13	10	13	12
DNL (LSB)	0.44	0.47		0.45	1.04	0.74	0.79
INL (LSB)	0.45	0.53		0.75	1.04	1.31	1.41
SNDR (dB)	55.63	53.7	54.8	73.57	49.2	71.0	60.34
SFDR (dBc)	76.25	78.5	71.5	89.9	57	89.5	71.05
(Process) The number of measured chips	-	-		-	-	3	30
(Voltage) Supply voltage variation	-	-		-	-	+/-5%	+/-9%
(Temperature) Operating temperature (°C)	-	-		-	0 ~ 40* (over 51.8 dB)	-50 ~ 90	-20 ~ 80
Power (μW)	0.084	0.2	9.25	0.638	0.00085	82	1.8
FoM_W (fJ/conv.-step)	0.85	2.02	5.16	0.606	8	1.4	7.06
Area (mm^2)	0.0065	0.0408		0.059	0.024	0.053	0.039

* Sampling rate : 100 SPS



Measured locking status

FIGURE 14. The measured locking status by oscilloscope.

V. CONCLUSIONS

Low power SAR ADC with adaptive conversion time DNC for high immunity to PVT variation has been presented. The DNC block of the proposed SAR ADC detects the conversion time according to PVT variations, and adaptively controls the conversion speed and power consumption. The prototype ADC with the reconfigurable 8-12-bit resolution was fabricated using the 65nm process. In comparison with the other state-of-the-art low supply voltage ADCs, the proposed work shows the high immunity to PVT variations.

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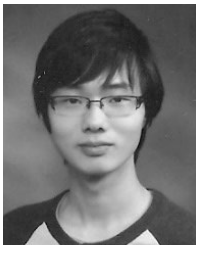

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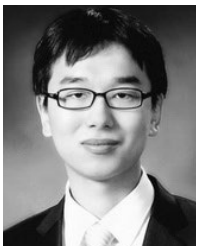

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