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A Passive Soft-Switching Snubber With Energy Active Recovery Circuit for PWM Inverters

ZHI ZHANG, (Student Member, IEEE), XIAOFENG YANG, (Senior Member, IEEE), TRILLION Q. ZHENG, (Senior Member, IEEE), AND JIEPIN ZHANG, (Student Member, IEEE)
School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China

Corresponding author: Xiaofeng Yang (xfyang@bjtu.edu.cn)

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ABSTRACT A passive soft-switching snubber with energy active recovery circuit (PSS-EARC) for pulse width modulation (PWM) inverters is proposed in this paper. The PSS-EARC recovers the buffering energy of the snubber inductors and capacitors back to the input voltage source while achieving passive soft-switching, so as to improve the inverter efficiency. In this paper, the configuration and operation principle of the PSS-EARC are analyzed and studied in detail firstly. Comparing with the traditional energy passive recovery circuit, the PSS-EARC avoids the circulating current issue by employing the auxiliary switches. Because the control of auxiliary switches is simple and independent, it is also benefit to the integration of auxiliary circuits. Moreover, in three-phase inverter application, the EARC is shared by three bridge-legs, which may further simplify the circuit. Finally, a 10kW three-phase inverter with the PSS-EARC is built. The experimental results demonstrate the validity and superiority of the proposed circuit.

INDEX TERMS Energy active recovery, inverter, passive soft-switching, switching loss.

I. INTRODUCTION

To reduce the size, cost, as well as power loss of the magnetic and filter components, it is necessary to increase the switching frequency of inverters. However, higher switching frequency will increase switching loss, which reduces the inverter efficiency a lot. Moreover, the electromagnetic interference (EMI) noise is also increased, which will have negative impact on inverters and reduce the system reliability [1]–[3]. To overcome these drawbacks, many soft-switching circuits for pulse width modulation (PWM) inverters have been proposed. But most of them have their own limitations. For this reason, an improved topology is proposed in this paper.

Some auxiliary resonant circuits were added in DC side of inverters in [4]–[11]. They can provide zero-voltage or zero-current intervals to all switches during switching process with simple structure. But they are more complex in control and it is difficult to realize zero-voltage switching (ZVS) or zero-current switching (ZCS) turn-on and turn-off of all switches at the same time. Therefore, more soft-switching circuits applied in AC side of inverters were proposed. Further, these circuits can be classified into active ones and passive ones.

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Generally, the active soft-switching circuits can achieve ZVS or ZCS of all switches [10], [12]–[17]. But they usually require extra auxiliary switches and passive components, so their circuits and control are more complex, which is detrimental for modularity. Furthermore, by considering the cost of high voltage IGBTs, it is not desirable to add auxiliary switches in the soft-switching circuits for high voltage and high power inverters. Therefore, it is difficult to apply these techniques to high power application. Correspondingly, compared with the active ones, the passive soft-switching circuits realize ZVS or ZCS of all switches without additional auxiliary switches and complex control [18], [19]. The di/dt during turn-on transient and du/dt during turn-off transient can be effectively reduced so as to achieve ZCS turn-on and ZVS turn-off just by passive components. Therefore, the switching loss is greatly reduced. Although it is hard to be completely reduced to zero, the operation environment of switches and the overall efficiency can be greatly improved. Moreover, higher reliability and lower cost can be obtained at the same time.

The resistor-capacitor-diode (RCD) absorption circuit which has been widely used in PWM inverters is the simplest passive soft-switching circuit. It can effectively reduce the electrical stress of switches, switching loss and EMI. But the snubber resistors in the absorption circuit cause inevitable

loss with the increasing of switching frequency in proportion. Therefore, it is not suitable for high frequency high power switching circuits [20]. Many passive lossless soft-switching technologies have been proposed in recent years. The energy captured by the absorption circuit can be transferred to the input side or load side to improve the efficiency. Some lossless passive snubbers have been discussed in DC-DC converters [21]–[23]. But the resonance components of multiple switches may interfere with each other when they are used in inverters. Therefore, they are difficult to be applied to PWM inverters. In [24], [25], a passive lossless turn-on snubber with a soft-clamp turn-off snubber circuit was proposed, which can achieve energy feedback and ZCS turn-on. However, it cannot realize soft-switching when the switches are turned off. Besides, a passive soft-switching snubber with energy passive recovery circuit (PSS-EPRC) was proposed in [20], [26], [27], which can realize soft-switching and energy recovery as well as reduce the voltage and current stress of switches. And it has been applied in small and medium power applications. But the circulating current is inevitable in the energy recovery unit, which may not only affect the inverter efficiency, but also influence its normal operation. On this basis, an improved method was proposed in [28], [29]. It can realize soft-switching, improve the inverter efficiency, and reduce the output harmonics. Nonetheless, the three DC-link capacitors in the input side need to be designed large enough for achieving ZVS turn-off, and the energy recovery circuit cannot be shared by three bridge-legs which will increase the system volume and cost. The circuit proposed in [30] can realize soft-switching and energy active recovery, but the resonant parameters design is more complex. The oscillation caused by parasitic parameters and the reverse recovery of diodes will greatly increase the electrical stress. And its advantage of efficiency on high power occasion has not been verified effectively.

Based on the idea of lossless passive snubber and to avoid the circulating current in the PSS-EPRC, this paper proposes a passive soft-switching snubber with energy active recovery circuit (PSS-EARC) for PWM inverters which is shown in Fig. 1. The PSS-EARC can reduce the du/dt, di/dt and switching loss by the passive soft-switching snubber (PSS). The energy captured in the passive components is transferred into the buffering capacitors. And then it will be recovered to the power supply through the energy active recovery circuit (EARC) so as to improve the efficiency. Although the auxiliary switches are introduced in the EARC, the voltage stress and the rated power of the EARC are far less than the inverters. Therefore, the switching devices with low voltage and low power can be adopted even in high power application. And the control of auxiliary switches is simple and independent, which is benefit to the integration of auxiliary circuits. Moreover, as shown in Fig. 2, the EARC is shared by three bridge-legs in three-phase application. Therefore, the volume and cost of the auxiliary circuit can be further reduced.

The rest of this paper is organized as follows: In section II, the configuration and operation principle of the PSS and

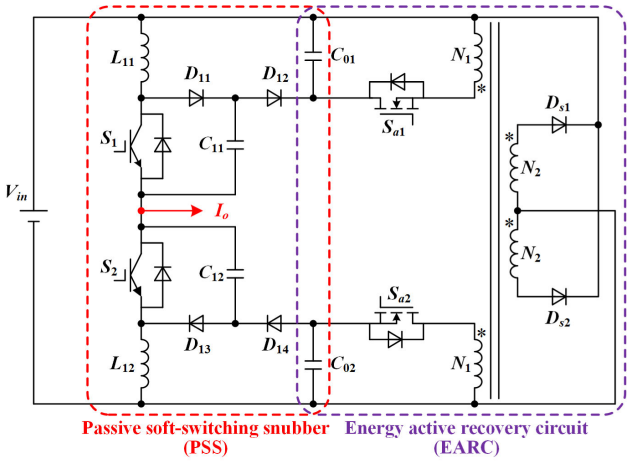

FIGURE 1. Proposed PSS-EARC for inverter phase-leg.

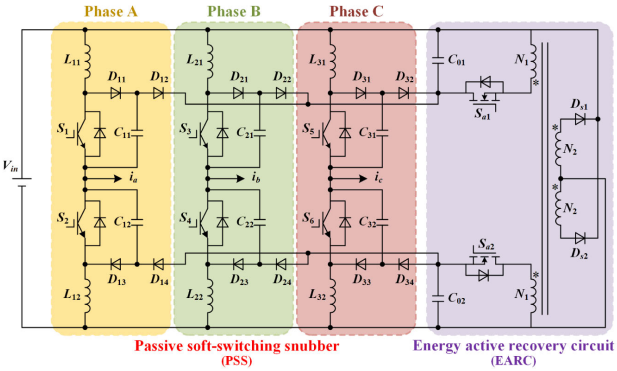

FIGURE 2. Schematic diagram of PSS-EARC used in three-phase inverter.

EARC are presented in detail, respectively. Section III discusses some issues of the PSS-EARC. Moreover, the problem existing in the passive recovery circuit is analyzed in this section. The experimental results and the corresponding comparative analysis are carried out in Section IV. Finally, the conclusions are drawn in Section v.

II. OPERATION PRINCIPLE

The proposed circuit applied for inverter phase-leg shown in Fig. 1 consists of a PSS and an EARC. As for three-phase application, the operation principle of each phase are identical. Without loss of generality, the operation principle of this topology is analyzed in detail based on one bridge-leg of three-phase inverter.

A. CONFIGURATION OF PSS WITH TWO BUFFERING CAPACITORS

The PSS with two buffering capacitors is shown in Fig. 3. The snubber inductors L_{11} and L_{12}, which are in series with the switches S_1 and S_2, are used to reduce the di/dt during turn-on transient. The snubber capacitors C_{11} and C_{12} are in parallel with the switches to reduce the du/dt during turn-off transient. Therefore, the snubber inductors and capacitors

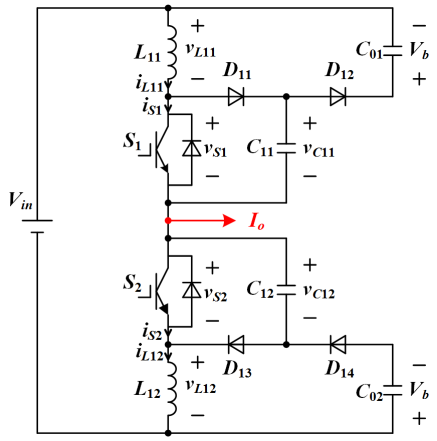

FIGURE 3. Configuration of PSS with two buffering capacitors.

can help suppress the EMI and reduce the switching loss effectively. It is worth mentioning that when the circuit is applied in actual application, the line stray inductance of the inverter can be used to substitute the snubber inductors thereby reduce the volume and cost of the circuit. If the stray inductance is not large enough, it can be increased by winding the wire or putting magnetic cores in the wire. The auxiliary diodes D_{11}, D_{12}, D_{13}, and D_{14} are fast recovery diodes for freewheeling. The buffering capacitors C_{01} and C_{02} absorb the energy captured in the snubber inductors and capacitors, and act as the input of the EARC. Moreover, S_1, L_{11}, C_{11}, D_{11}, D_{12}, and C_{01} constitute the upper leg, whereas the lower leg consists of S_2, L_{12}, C_{12}, D_{13}, D_{14}, and C_{02}.

B. OPERATION PRINCIPLE OF PSS

The output current of inverter is sinusoidal, so it can be positive and negative in a line frequency period. Due to the symmetry property and similarity, the situation with positive load current is analyzed as an example in this section. And in order to simplify the analysis, the circuit is under the following assumption.

1) All switches, inductors, capacitors and diodes are ideal.

2) The switching frequency is much larger than the frequency of load current, so that the output current can be viewed as a constant I_o during a commutation process.

3) The buffering capacitors C_{01} and C_{02} are much larger than the snubber capacitors C_{11} and C_{12}, so that the buffering capacitors voltage v_{C01} and v_{C02} can be seen as constant, with V_b to represent it.

4) Ignore the impact of dead time.

Fig. 4 shows the theoretical waveforms of the PSS when the output current is positive. And Fig. 5 shows the corresponding equivalent circuits under different operating modes.

Assuming the circuit is in the steady state of S_2 on and S_1 off before the switch S_2 is turned off, so the load current flows through S_2, and there are $i_{L11} = i_{S1} = 0$, $i_{L12} = i_{S2} = -I_o$, $v_{C11} = V_{in}$, $v_{C12} = 0$, $v_{C01} = v_{C02} = V_b$.

1) Mode I ($t_0 - t_1$): at t_0, S_1 is turned on and S_2 is turned off, the anti-parallel diode of S_2 is freewheeling, so S_2 is ZVS turn-off. The voltage v_{L12} across L_{12} is changed from zero

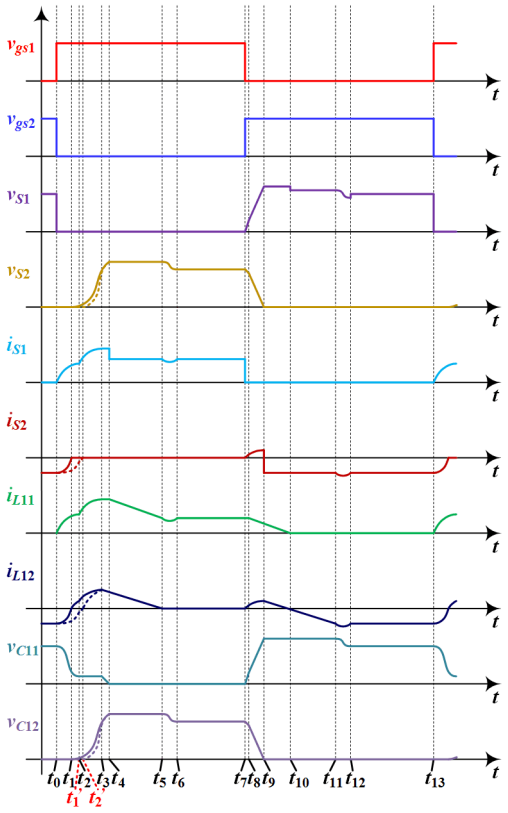

FIGURE 4. Theoretical waveforms of PSS.

to $V_{in}/2$ instantly, so D_{12} starts to conduct and C_{11} starts to discharge through D_{12}, C_{01}, L_{11}, S_1. Meanwhile, with the excitation of input V_{in}, the current i_{L11} through L_{11} increases and the current i_{L12} through L_{12} decreases in resonance, so S_1 is ZCS turn-on. The equivalent circuit in this mode is shown in Fig. 5(a). During this stage,

$$\begin{cases} v_{C11}(t) = -\left(V_b - \dfrac{L_{eq}}{L_{11}} V_{in}\right) \cos\left[\omega_1 (t - t_0)\right] \\ \qquad\qquad + \left(1 - \dfrac{L_{eq}}{L_{11}}\right) V_{in} + V_b \\ i_{L11}(t) = \left(\dfrac{V_{in}}{L_{11} + L_{12}} + \dfrac{V_b}{L_{11}}\right)(t - t_0) \\ \qquad\qquad - \dfrac{V_{in} \sin\left[\omega_1 (t - t_0)\right]}{\omega_1 L_{11}} \\ i_{L12}(t) = \left(\dfrac{V_{in}}{L_{11} + L_{12}} + \dfrac{V_b}{L_{11}}\right)(t - t_0) \\ \qquad\qquad + \left(\dfrac{1}{Z_1} - \dfrac{1}{\omega_1 L_{11}}\right) V_1 \sin\left[\omega_1 (t - t_0)\right] - I_o \end{cases} \tag{1}$$

where $L_{eq} = L_{11}L_{12}/(L_{11} + L_{12})$, $\omega_1 = 1/\sqrt{L_{eq}C_{11}}$, $V_1 = V_b - V_{in}L_{eq}/L_{11}$, $Z_1 = \sqrt{L_{eq}/C_{11}}$.

In this mode, there may be two possible endings. It depends on whether i_{L12} drops to zero firstly or i_{C11} resonates to zero firstly. It takes T_1 of i_{L12} dropping to zero. T_1 can be approximately expressed by

$$T_1 \approx \frac{L_{eq} I_o}{V_b}. \tag{2}$$

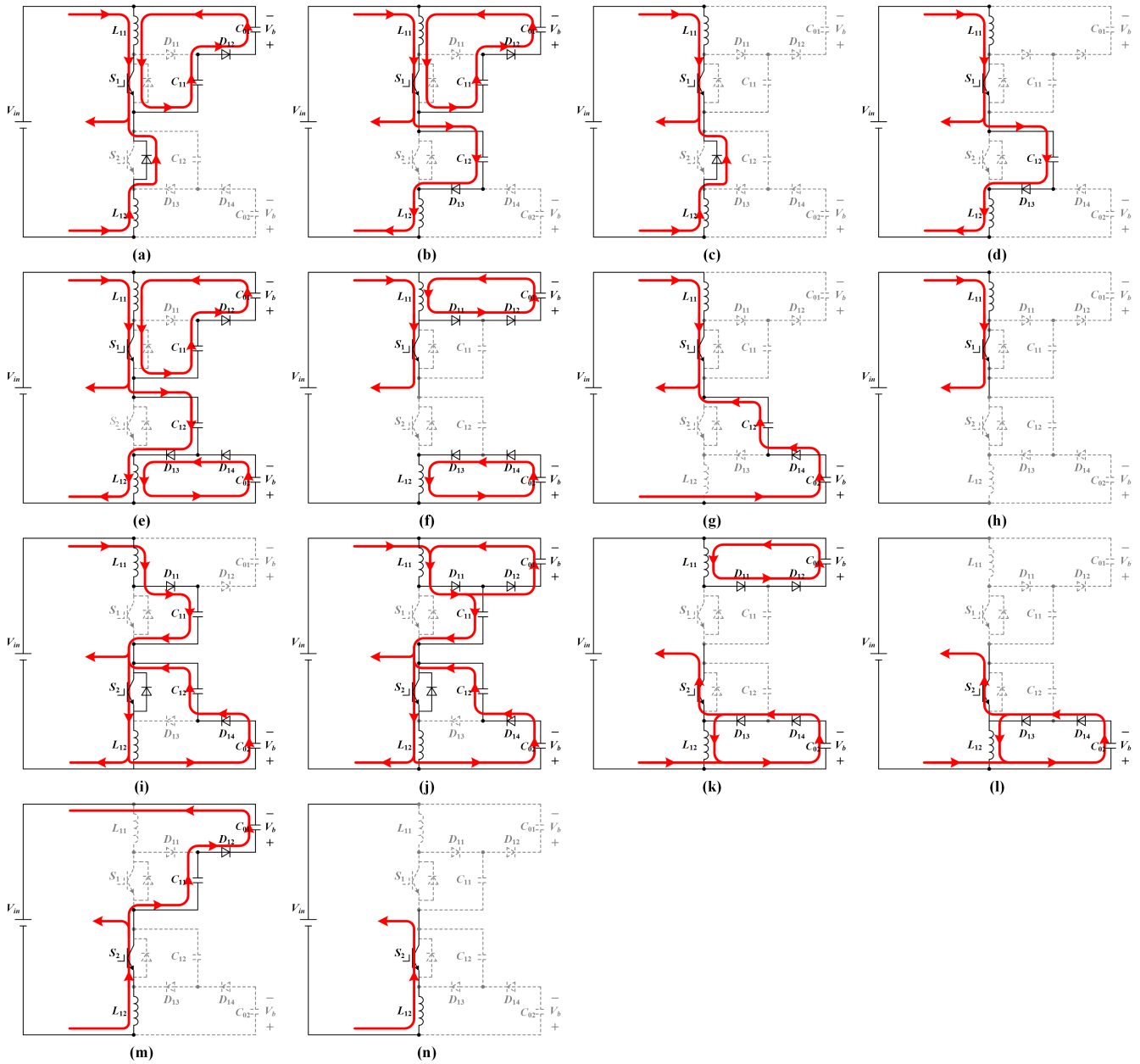

FIGURE 5. Equivalent circuits under different operating modes of PSS. (a) Mode I, (b) Mode II.1, (c) Mode II.2, (d) Mode III, (e) Mode IV, (f) Mode V, (g) Mode VI, (h) Mode VII, (i) Mode VIII, (j) Mode IX, (k) Mode X, (l) Mode XI, (m) Mode XII, (n) Mode XIII.

Whereas the duration T_2 of i_{C11} resonating to zero can be expressed by

$$T_2 = \frac{2\pi}{\omega_1}. \tag{3}$$

If $T_1 < T_2$, the circuit will go to mode II.1. Otherwise, it will go to mode II.2.

2) Mode II.1 ($t_1 - t_2$): at t_1, i_{L12} drops to zero, the anti-parallel diode of S_2 is turned off. D_{13} starts to conduct, so C_{12} starts to charge and C_{11} continues to discharge. And i_{L11} continues to increases in resonance and i_{L12} starts to increase in positive. The equivalent circuit in this mode is shown in Fig. 5(b). When i_{C11} resonates to zero, D_{12} is turned off and C_{11} stops to discharge. And then it goes into the mode III.

3) Mode II.2 ($t_1' - t_2'$): at t_1', i_{C11} resonates to zero, D_{12} is turned off and C_{11} stops to discharge. At this time, i_{L12} is still negative. Then i_{L11} continues increasing and i_{L12} continues decreasing linearly, respectively. The equivalent circuit in this mode is shown in Fig. 5(c). When i_{L12} is decreased to zero, i_{L11} is increased to I_o, this process ends and it goes to mode III.

4) Mode III (t_2 or $t_2' - t_3$): at t_2 or t_2', both D_{12} and the anti-parallel diode of S_2 are turned off. So the voltage v_{C11} across C_{11} remains unchanged and C_{12} resonates with L_{11},

L_{12}. The equivalent circuit in this mode is shown in Fig. 5(d). This mode ends when the voltage v_{C12} across C_{12} is charged to V_{in}.

At the same time, v_{L11} resonates to nearly V_b and v_{L12} resonates to nearly $-V_b$.

5) Mode IV ($t_3 - t_4$): at t_3, D_{12} is turned on once again and C_{11} continues to discharge. D_{14} starts to conduct, v_{L12} is clamped into $-V_b$ and i_{L12} is decreased linearly. C_{12} continues charging with a decreasing current. The equivalent circuit in this mode is shown in Fig. 5(e). This mode ends once v_{C11} is discharged to zero.

6) Mode V ($t_4 - t_5$): at t_4, v_{L11} resonates to $-V_b$ so D_{11} is turned on. v_{C12} increases to nearly $V_{in} + 2V_b$ and stops charging. In this mode, both v_{L11} and v_{L12} are clamped in V_b, the excessive energy of L_{11} and L_{12} is transferred to the buffering capacitors C_{01} and C_{02}. i_{L11} and i_{L12} are decreased linearly. The equivalent circuit in this mode is shown in Fig. 5(f). When i_{L11} is decreased to I_o and i_{L12} is decreased to zero, this mode ends.

7) Mode VI ($t_5 - t_6$): at t_5, D_{11}, D_{12} and D_{13} are turned off, D_{14} is still turned on. C_{12} starts to resonate with L_{11} and is discharged through S_1, L_{11}, V_{in}, C_{02}, D_{14}. The equivalent circuit in this mode is shown in Fig. 5(g). When v_{C12} resonates to V_{in}, i_{L11} resonates back to I_o and D_{14} is turned off, this mode ends.

8) Mode VII ($t_6 - t_7$): this is the steady state of S_1 on, the load current flows through S_1. There are $i_{L11} = i_{S1} = I_o$, $v_{C11} = 0$, $v_{C12} = V_{in}$, $i_{L12} = i_{S2} = 0$. The equivalent circuit in this mode is shown in Fig. 5(h).

9) Mode VIII ($t_7 - t_8$): at t_7, S_1 is turned off and S_2 is turned on. The current through S_1 transfers to C_{11} instantly, and C_{11} starts to charge in resonance, so S_1 is ZVS turn-off. C_{12} starts to discharge through S_2, L_{12}, C_{02}, D_{14}, i_{L11} is increased in resonance. S_2 is ZCS turn-on. The equivalent circuit in this mode is shown in Fig. 5(i). When v_{L11} resonates to $-V_b$, this mode ends.

10) Mode IX ($t_8 - t_9$): at t_8, D_{12} is turned on, v_{L12} is clamped into $-V_b$ again, and part of the energy of L_{11} is transferred to C_{01}. C_{11} continues charging and C_{12} continues discharging. The equivalent circuit in this mode is shown in Fig. 5(j). When v_{C12} is discharged to zero and v_{C11} is charged to $V_{in} + 2V_b$, this mode ends.

11) Mode X ($t_9 - t_{10}$): at t_9, C_{11} stops charging and C_{12} stops discharging. D_{12} and D_{13} are turned on, both v_{L11} and v_{L12} are clamped in V_b again, the excessive energy of L_{11} and L_{12} is transferred to the buffering capacitors C_{01} and C_{02}. i_{L11} and i_{L12} are decreased linearly. And the load current I_o is freewheeling through C_{02}, D_{14}, D_{13}, S_2. The equivalent circuit in this mode is shown in Fig. 5(k). When i_{L11} drops to zero, this mode ends.

12) Mode XI ($t_{10} - t_{11}$): at t_{10}, D_{12} and D_{13} are turned off, the voltage v_{S1} across S_1 is dropped to $V_{in} + V_b$. i_{L12} continues to decrease linearly. The equivalent circuit in this mode is shown in Fig. 5(l). When i_{L12} is dropped to zero and then rises reversely to I_o, this process ends.

TABLE 1. Soft-switching of the main switches.

Switches	Positive load current		Negative load current	
	ON	OFF	ON	OFF
$S_1(S_3, S_5)$	ZCS	ZVS	ZCS	ZVS
$S_2(S_4, S_6)$	ZCS	ZVS	ZCS	ZVS

13) Mode XII ($t_{11} - t_{12}$): at t_{11}, D_{13} and D_{14} are turned off, and D_{12} is turned on again. C_{11} starts to discharge through D_{12}, C_{01}, V_{in}, L_{12}, S_2 in resonance. The equivalent circuit in this mode is shown in Fig. 5(m). When v_{C11} is discharged to V_{in}, i_{L12} resonates back to $-I_o$, v_{L12} resonates from $-V_b$ to V_b, this mode ends.

14) Mode XIII ($t_{12} - t_{13}$): The circuit enters into the steady state of S_1 off and S_2 on. There are $i_{L11} = i_{S1} = 0$, $v_{C11} = V_{in}$, $v_{C12} = 0$, $i_{L12} = i_{S2} = -I_o$. The equivalent circuit in this mode is shown in Fig. 5(n).

The operation principle analysis of one switching cycle with positive load current is over. Due to the symmetry property of the circuit, the operation principle with negative load current is similar. When the load current is negative, the characteristics of upper leg and lower leg are opposite to those when the load current is positive. According to the analysis, all switches can achieve ZVS or ZCS during turn-on and turn-off transient due to the presence of snubber inductors and capacitors. It's summarized in Table 1. And the reverse recovery effect of the anti-parallel diodes of main switches and auxiliary diodes can be suppressed by the snubber inductors.

C. CONFIGURATION OF EARC

The EARC shown in Fig. 6 includes two buffering capacitors C_{01} and C_{02}, two complementary auxiliary switches S_{a1} and S_{a2}, two current limiting diodes D_{s1} and D_{s2}, and a push-pull transformer. The energy stored in the buffering capacitors can be transferred back to the power supply through the transformer by the complementary conduction of the auxiliary switches. As a result, the inverter efficiency will be improved. And this circuit is shared by three bridge-legs when it is applied in three-phase inverters, which can greatly reduce the volume of the auxiliary circuit. In addition, the operation of the EARC is completely independent of the soft-switching circuit and the inverter, which simplifies the corresponding control.

The push-pull transformer with mutual coupling of the upper and lower windings can realize magnetic reset automatically without any external circuit, thereby further simplify the structure. The transformer turns ratio n is defined as secondary turns N_2 to primary turns N_1. According to (4), the larger n is, the lower the voltage across buffering capacitors will be.

$$V_b \approx V_{in}/n. \tag{4}$$

So MOSFETs which have lower rating voltage, smaller on-resistance and higher switching frequency can be employed in

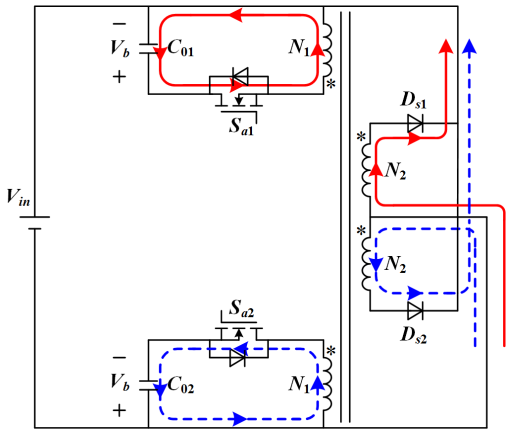

FIGURE 6. Configuration of EARC.

the auxiliary circuit. Correspondingly, the size of transformer can be greatly reduced.

D. OPERATION PRINCIPLE OF EARC

The operation principle of the EARC is analyzed briefly and qualitatively in this section. Assuming the voltage of C_{01} and C_{02} is higher than V_b at the beginning, and the excitation inductance of transformer is large enough. The excitation current will be very small, therefore the impact of the excitation current on the auxiliary switches can be neglected. When S_{a1} is conducted, the energy recovery current is shown as the red solid line in Fig. 6. When S_{a2} is conducted, the energy recovery current is shown as the blue broken line in Fig. 6. As mentioned earlier, the push-pull structure of transformer can realize magnetic reset automatically without adding any external circuit by the symmetric structure.

III. DISCUSSION OF PROPOSED CIRCUIT

A. STRESS ANALYSIS

According to the operation principle analysis, the voltage and current stress of all devices and components are summarized in table 2. Where $I_{o,\max}$ is the maximum value of the output current, D_{sa} is the duty cycle of auxiliary switches, f_{sw} is the switching frequency of main switches, f_{sa} is the switching frequency of auxiliary switches, and L_k represents the total equivalent leakage inductance converted to primary side.

The voltage stress of the devices and components is related to the input voltage V_{in} and turns ratio n. When V_{in} is determined, the larger n is, the lower voltage stress the devices and components will have. But it will also increase the current stress of the auxiliary switches. And if the turns ratio is too large, the efficiency of transformer will be limited, which affects the overall inverter efficiency. Therefore, the turns ratio should be generally kept at 5 to 10 for the concern about the electrical stress of auxiliary switches and the efficiency of transformer.

The peak current of main switches appears at t_4 according to the theoretical analysis. Due to the complexity of theoretical equation, it's unable to get the accurate expression of current stress. The current stress of main switches is related to the

TABLE 2. Stress of the devices and components.

Devices/Components	Voltage stress	Current stress
S_1-S_6	$(n+2)\ V_{in}/n$	$i_{L11}(t_4)$
C_{11}-C_{32}	$(n+2)\ V_{in}/n$	——
D_{11}-D_{34}	V_{in}	$I_{o,\max}$
C_{01}, C_{02}	V_{in}/n	——
S_{a1}, S_{a2}	$2V_{in}/n$	$(V_b\text{-}V_{in}/n)D_{sa}/(f_{sa}L_k)$
D_{s1}, D_{s2}	$2V_{in}$	$(V_b\text{-}V_{in}/n)D_{sa}/(nf_{sa}L_k)$

snubber inductors and capacitors. Lower current stress can be achieved with larger inductance and smaller capacitance. But the current stress will be always larger than the load current according to the analysis. This is one of the main drawbacks of the soft-switching circuit.

On the other hand, the ZCS turn-on and ZVS turn-off of main switches rely on the snubber inductors and capacitors, too. The switching-on loss will decrease with the value increase of snubber inductors. Meanwhile, larger value of snubber capacitors will lead to smaller switching-off loss.

In addition, the average recovery power of the EARC can be approximately expressed as

$$P_{rec} \approx \sum_{i=1}^{3}\sum_{j=1}^{2}\left(\frac{1}{2}L_{ij}I_{rms}^2 + \frac{1}{2}C_{ij}V_{in}^2\right)f_{sw}. \tag{5}$$

As a result, the larger the inductance and capacitance are, the larger the recovery power will be, which would increase the power loss in the EARC so as to decrease the whole efficiency. Therefore, the value of the snubber inductors and capacitors should balance the switching loss, voltage and current stress, and the power loss of the EARC according to the actual situation.

The design of the EARC can be divided into the choice of auxiliary switches and the design of push-pull transformer. Increasing the turns ratio will lower the voltage stress but increase the current stress of auxiliary switches. It is another compromise in engineering application. The specific parameter design method of the PSS-EARC will be further studied in the future.

In order to decrease the voltage stress of auxiliary switches and the volume of transformer, the turns ratio n is set to 10, the switching frequency of auxiliary switches is 50kHz. Considering the dead time, the duty cycle of auxiliary switches is set to 0.45.

For the 10kW three-phase inverter, a high-frequency push-pull transformer whose output power is 300W and operating frequency is 50kHz has been designed by the area product (AP) method [31].

Combining the theoretical analysis, the parameters and devices of the PSS-EARC are summarized in Table 3. It should be noted that the PSS-EARC is proposed for high voltage and high power application. Therefore, IGBTs are adopted for main switches in the inverter. Considering the characteristics of the selected switches in this paper

TABLE 3. Parameters and devices of PSS-EARC.

Parameters	Values	Parameters	Values
f_{sw}	5kHz	f_{sa}	50kHz
L_{i1}	10μH	L_{i2}	10μH
C_{mn}	20nF	C_{01}, C_{02}	680μF
D_{sa}	0.45		
Devices	Types	Devices	Types
S_1-S_6	FF300R17KE3	S_{a1}, S_{a2}	SCT3060AL
D_{11}-D_{34}	C4D20120A	D_{s1}, D_{s2}	DHG20I1200PA
Skeleton	PQ3535	Core material	PC40

and the switching loss, the switching frequency are set to 5kHz.

B. DISCUSSION OF MODE II IN THE PRINCIPLE ANALYSIS OF PSS

As shown in the part B of section II above, there can be two different endings of Mode I of the PSS. It depends on the relationship of T_1 and T_2. Let $T_1 < T_2$,

$$\frac{L_{eq}I_o}{V_b} < \frac{2\pi}{\omega_1} \tag{6}$$

$$I_o < \frac{2\pi V_b}{\omega_1 L_{eq}} = \frac{2\pi V_{in}}{n}\sqrt{\frac{C_{11}\left(L_{11}+L_{12}\right)}{L_{11}L_{12}}}. \tag{7}$$

That is, when the load current I_o meets (7), the current i_{L12} will drop to zero first, and then the circuit will go to mode II.1. If not, it will go to mode II.2.

The parameters can be designed to make that the load current meets (7) all the time, then there will be only II.1 in one line frequency cycle. But this is not necessary, and it will increase the difficulty of parameter design. Therefore, both mode II.1 and mode II.2 will exist under normal circumstances in one line frequency cycle.

C. DEAD TIME IMPACT ON THE PSS

In order to simplify the analysis in the previous, the impact of dead time is ignored. But actually it has a certain influence on the operation process.

Similarly, the situation of positive load current is taken as an example. Firstly, the dead time during S_2 turning off and S_1 turning on will induce an extra mode as shown in Fig. 7(a). The duration of this mode is the dead time T_D and in this mode, the load current will be freewheeling through the anti-parallel diode of S_2. S_2 is still ZVS turn-off. Therefore, the dead time has little effect on this commutation process.

However, the dead time between S_1 turning off and S_2 turning on makes the commutation process more complicated. When S_1 is turned off while S_2 is still off, C_{12} would not discharge. D_{11} is turned on, the current of S_1 transfers to C_{11} instantly. C_{11} starts to charge linearly. The equivalent circuit is shown in Fig.7 (b). When v_{C11} is charged to $2V_b$, this process ends. The duration of this process can be expressed

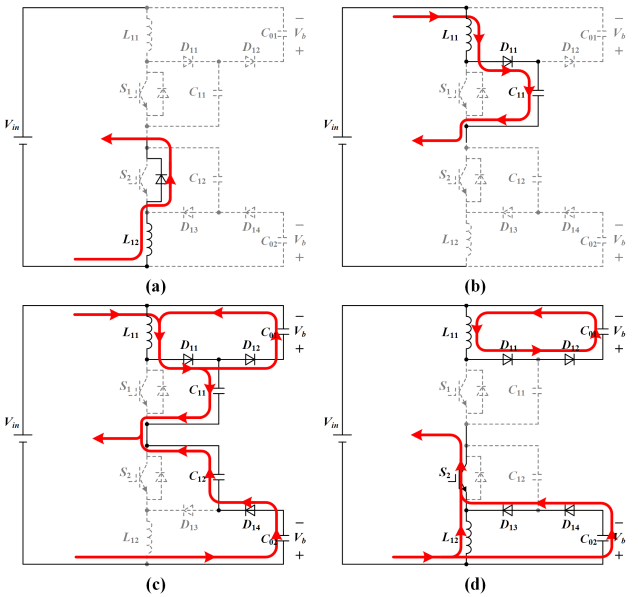

FIGURE 7. Equivalent circuits of PSS under the impact of dead time. (a) Load current is freewheeling through the anti-parallel diode of S_2. (b) C_{11} starts to charge with the load current. (c) C_{12} starts to discharge through the load. (d) Load current flows through S_2.

by

$$T_3 = \frac{2C_{11}V_b}{I_o}. \tag{8}$$

And then if S_2 is still not turned on, D_{12} and D_{14} would be both turned on. C_{12} starts to discharge through C_{02}, D_{14} and the load. C_{11} continues charging and v_{L11} is clamped into $-V_b$ again, a part of the energy of L_{11} is transferred to C_{01}. The equivalent circuit is shown in Fig. 7(c). During this process,

$$\begin{cases} v_{C11}(t) = 2V_b + \dfrac{I_o}{2C_{11}}t \\ v_{C12}(t) = V_{in} - \dfrac{I_o}{2C_{12}}t \\ i_{L11}(t) = I_o - \dfrac{V_b}{L_{11}}t. \end{cases} \tag{9}$$

When v_{C12} is discharged to zero and v_{C11} is charged to $V_{in}+2V_b$, this process ends. Therefore, the maximum duration of this process can be expressed by

$$T_4 = \frac{2C_{12}V_{in}}{I_o}. \tag{10}$$

Then C_{11} stops charging and C_{12} stops discharging. D_{13} are turned on, i_{C12} would be transferred to the anti-parallel diode of S_2. v_{L11} and v_{L12} are both clamped in $-V_b$. i_{L11} is decreased and i_{L12} is increased in reverse linearly. And the load current I_o is freewheeling through L_{12} and C_{02}, D_{13}, D_{13}, S_2. The equivalent circuit is shown in Fig. 7(d). Therefore, if S_2 is turned on after C_{12} is discharged to zero, S_2 can fully achieve ZVS turn-on and no switching-on loss. That is,

$$T_D > T_3 + T_4 = \frac{2C_{11}V_b + 2C_{12}V_{in}}{I_o}. \tag{11}$$

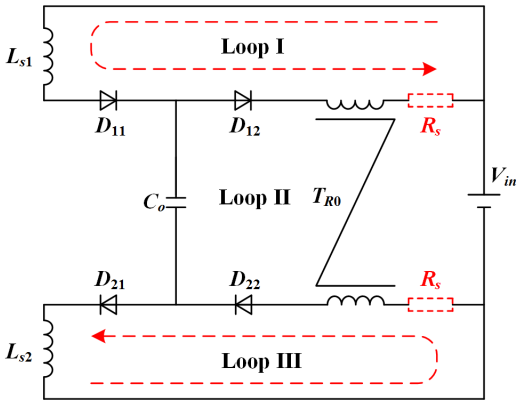

FIGURE 8. Illustration of circulating current.

If the dead time T_D does not meet (11), on this commutation process, S_2 will be ZCS turn-on. Therefore, according to (11), the soft-switching of S_2 depends on the load current I_o. When I_o is relatively large, the appropriate dead time T_D can make S_2 achieve ZVS turn-on and no switching-on loss. But ZVS turn-on of S_2 can be guaranteed when I_o is small because T_D can't be infinite. As a result, both ZVS turn-on and ZCS turn-on of S_2 would happen when the load current is positive. Correspondingly, the dead time has the similar influence to S_1 when the load current is negative and both ZVS turn-on and ZCS turn-on of S_1 would exist.

D. SUPERIORITY OF EARC COMPARED TO PASSIVE RECOVERY

The passive recovery circuit in the similar topologies proposed in [20], [26], [27] exists the Loop I and Loop III as shown in Fig. 8. When the main switches are turned off, part of the energy of inductors L_{s1} and L_{s2} will be transferred to the snubber capacitors, and the excessive energy will be dissipated through the line resistance of Loop I and Loop III. And during this process, the excitation current of transformer will be reduced to zero for magnetic reset. Here, the current in Loop I and Loop III is defined as the circulating current. In the passive recovery circuit, the transformer is connected like a common mode choke and thus presents a large inductance to Loop I and Loop III to minimize the circulating current. But it cannot be eliminated. As the output power increase, the circulating current may not decrease to zero periodically, which affects the normal function of inverter and transformer. Therefore, it's necessary to add suppression resistors R_s in the recovery circuit to suppress the circulating current.

Fig. 9 shows the simulation results of the passive recovery circuit with the same parameters in Table 3. As shown in Fig. 9(a), when the suppression resistors are 5Ω, the current of inductor $L_{s1}i_{Ls1}$ cannot periodically fall to zero in whole power frequency cycle. That will greatly increase the switching-on loss of main switches and lower the reliability of inverter. Therefore, the suppression resistors should be increased. When the suppression resistors are set to nearly 25Ω, i_{Ls1} can periodically fall to zero all the time, which

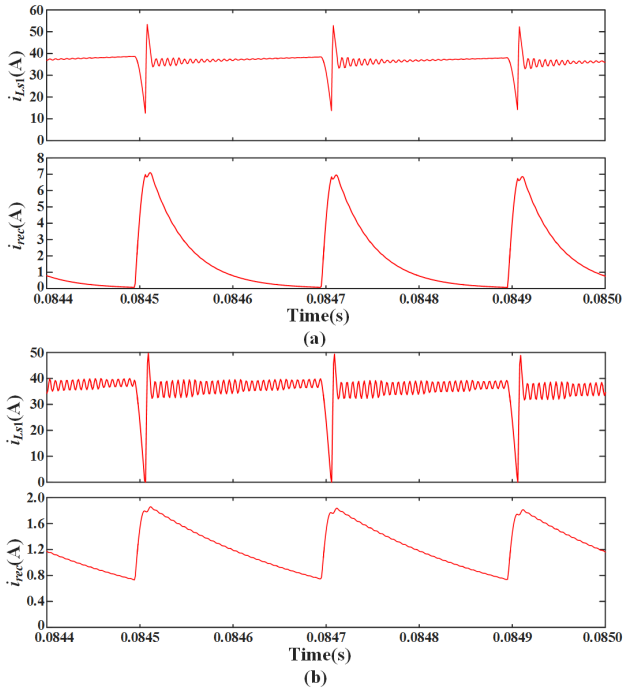

FIGURE 9. Simulation results of passive recovery circuit. (a) $R_S = 5Ω$, (b) $R_S = 25Ω$.

is shown in Fig. 9(b). However, the snubber bus capacitors cannot discharge quickly with too large suppression resistors. The recovery current cannot decrease to zero, which causes the transformer to work with the bias. It will increase the core loss and may cause the core saturation. In conclusion, the suppression resistors is difficult to choose.

In addition, adding suppression resistors results in negative effects while suppressing the circulating current. As the total power increases, so does the loss on the suppression resistors. The volume of resistors will increase and there need to add heat sink on the resistors. Therefore, it results in lower power density, higher cost, and lower system stability. Although the energy recovery circuit will recover the energy absorbed by the buffering circuit, a part of these will still be consumed by the resistors, thereby reduce the efficiency of inverter. And the suppression resistor functions as the resistor of the traditional RCD snubber in a sense.

In the proposed PSS-EARC, the energy of the snubber inductors and capacitors is transferred to the buffering capacitors by the PSS firstly. And then it will be recovered to the power supply through the EARC as shown in Fig.6. The circulating current problem is avoided due to the existence of auxiliary switches. At the same time, with complete independence of the main switches, the control of auxiliary switches is simple. It helps enhance the stability of the circuit and increases efficiency. And it is benefit to the integration of auxiliary circuits.

IV. EXPERIMENTAL RESULSTS

In order to verify the feasibility and validity, a prototype of 10kW three-phase PWM inverter with the PSS-EARC is

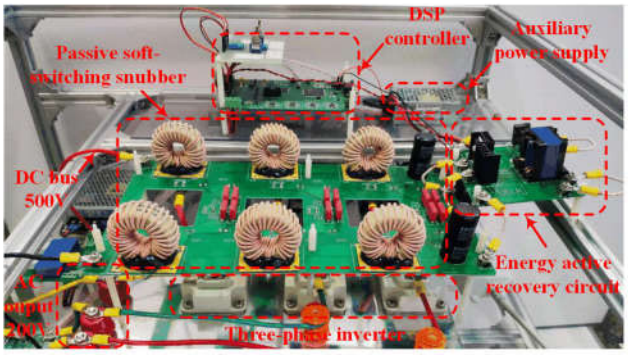

FIGURE 10. Photo of a 10kW three-phase inverter with PSS-EARC.

established. A Chroma DC power supply with the model of 62150H-600 is used as the input and the voltage of DC bus is 500V. Three customized resistors of 6Ω with traditional LC filters are used as loads of the inverter. The output peak voltage is set to 200V. As shown in Fig. 10, the PSS and EARC are placed on the top, and then connected to the corresponding interface of the three-phase inverter. Therefore, the PSS-EARC is integrated into a module, which is beneficial to apply to the existing inverters. Due to that the line stray inductance in the experimental prototype is small, extra inductors are added for the experimental platform. And a Tektronix oscilloscope with the model of DPO4034 is used to record the experimental results.

Fig. 11 and Fig. 12 shows the output voltage of the inverter and the voltage and current waveforms of main switch S_1 under hard-switching and soft-switching conditions, respectively. The turn-on and turn-off characteristics of S_1 are shown in Fig. 11. Under hard-switching, the inrush current is up to 130A and the di/dt reaches to 573A/μs during the turn-on transient. There is obvious overlapping area of the voltage and current. During the turn-off transient, the du/dt reaches to 1047V/μs and the reverse recovery peak current is nearly 102A. Moreover, the voltage starts to increase before the drop of current, which results in large overlapping area of the voltage and current. In addition, the significantly large overlapping area of the voltage and current during the whole switching process brings high switching loss.

Fig. 12 shows the operation waveforms of S_1 under passive soft-switching condition. According to Fig. 12, during the turn-on transient, the current flowing through S_1 rises slowly. The di/dt, the inrush current, and the reverse recovery of S_1 are all suppressed effectively. Furthermore, the du/dt is also suppressed during the turn-off transient. Compared to hard-switching, the di/dt during turn-on transient is reduced to 18A/μs which is only 3.1% of that under hard-switching. The peak current and reverse recovery peak current of S_1 decrease to 53A and 10A, respectively. And the du/dt during the turn-off transient is reduced to 474V/μs which is nearly half of that under hard-switching. Both ZCS turn-on and ZVS turn-off are realized by the snubber inductors and capacitors. Moreover, the voltage starts to increase as the current drop during the turn-off transient. As shown in Fig. 12, the overlapping

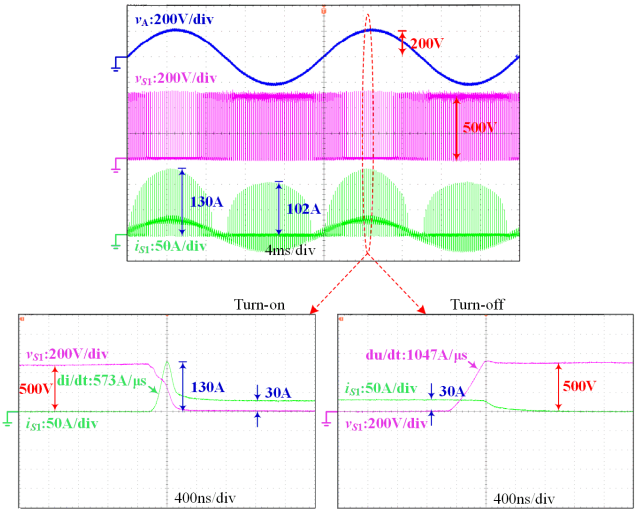

FIGURE 11. Output characteristics of S_1 under hard-switching condition.

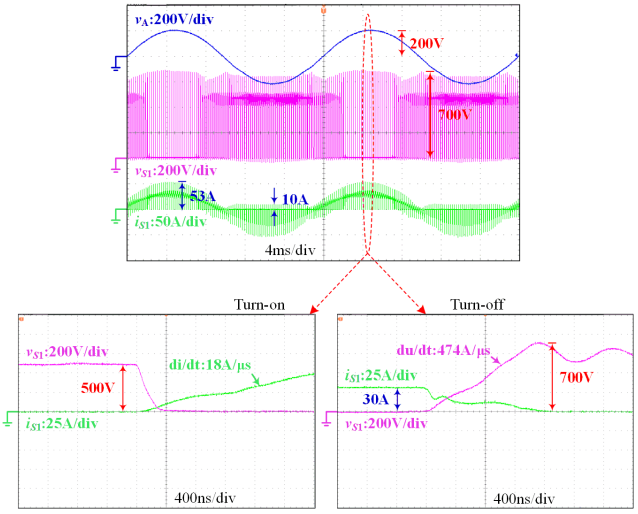

FIGURE 12. Output characteristics of S_1 under soft-switching condition.

area of the voltage and current is greatly reduced compared to that of hard-switching. Therefore, the switching loss of the three-phase inverter is reduced effectively. In addition, the high frequency EMI is also correspondingly suppressed.

Fig. 13 shows the key waveforms of phase A under passive soft-switching when the load current is positive. The experimental results are consistent with the theoretical analysis. The current spike, du/dt, di/dt of main switches and reverse recovery of anti-parallel diodes are well suppressed compared to Fig. 11. Due to the parasitic parameters of the circuit loop, there are some voltage and current oscillations in the voltage and current. Compared to the theoretical voltage stress of main switches according to table 2, which is 600V, the experimental stress resonates to nearly 700V. But it does not affect the normal operation of the circuit and soft-switching.

As discussed before, there are two kinds of Mode II in the PSS. According to (7) and experimental parameters, when the load current is smaller than 19.8A, the current i_{L12}, that is i_{S2} will drop to zero before i_{C11} resonates to zero and go

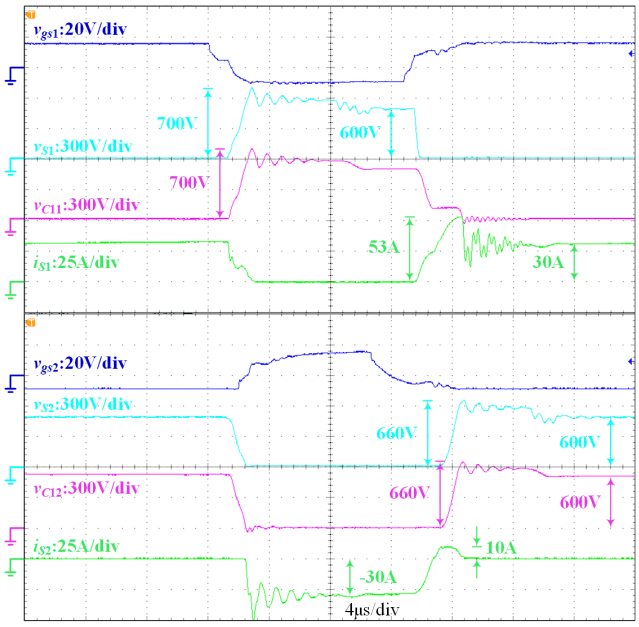

FIGURE 13. Working waveforms of PSS.

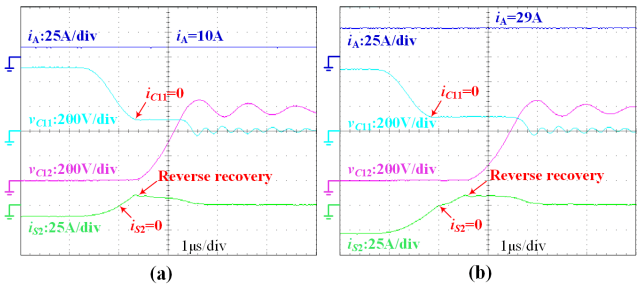

FIGURE 14. Waveforms of S_2 with different load current. (a) $i_A = 10A$. (b) $i_A = 29A$.

to Mode II.1. And when load current is larger than 19.8A, the circuit will go to Mode II.2. Fig. 14 shows two different situations with load current 10A and 29A, and verifies the theoretical analysis. Meanwhile, although the reverse recovery of main switches is suppressed effectively compared to that of hard-switching, it cannot be eliminated.

Similarly, the load current would affect the soft-switching of S_2. Dead time is necessary for voltage-fed inverter to avoid short circuit. In this paper, dead time is set to 2μs. Theoretically, when the load current is larger than 11A according to (11), S_2 can achieve ZVS. As shown in Fig. 15(a), when the load current is 25A, C_{12} is discharged to zero first, so S_2 is fully ZVS-on. And in Fig. 15(b), when the load current is 2A, S_2 is turned on before C_{12} is discharged to zero, so S_2 is ZCS-on with little switching-on loss. Therefore, when the load current is positive, S_2 is almost no switching-on loss.

In the proposed PSS-EARC, most of the energy in the snubber inductors and capacitors would be transferred to the buffering capacitors. And then it will be back to the input voltage source through the EARC. The three bridge-legs share one energy recovery unit so as to decrease volume

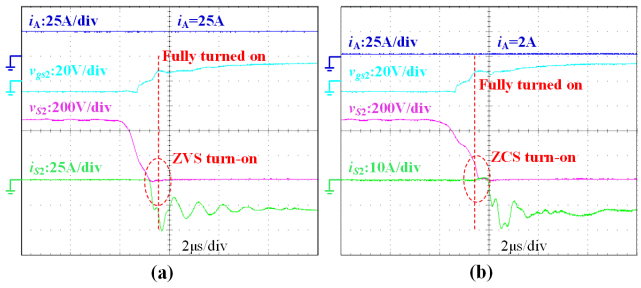

FIGURE 15. Soft-Switching of S_2 under different load current. (a) $i_A = 25A$. (b) $i_A = 2A$.

and increase efficiency. Fig. 16(a) shows the voltage and current waveforms of auxiliary switches. The voltage stress of S_{a1} and S_{a2} is nearly 100V, and the current stress of them is 17A. Because of the parasitic parameters of transformer (distributed capacitance and leakage inductance), when the auxiliary switches are turned on, the transformer current resonates to a large value rapidly and then starts to decrease.

However, according to Fig. 16(b), the auxiliary switches are ZCS turn-off, which not only can eliminate switching-off loss, but also suppress the voltage spike caused by leakage inductance. And owing to the resonance, the auxiliary switches can also achieve quasi-ZCS turn-on. In summary, the loss of the auxiliary switches can be ignored. Therefore, no additional soft-switching circuit is required in the EARC. On the other hand, as shown in Fig. 16(c), thanks to the transformer, the voltage of buffering capacitors C_{01} and C_{02} is maintained at nearly 50V which is 1/10 of the input voltage. And according to the recovery current, the recovery power of EARC is approximately 172W, which is about 1.72% of the input power. Due to that SiC MOSFETs are used, the loss of EARC is very small and can be ignored. Therefore, the overall efficiency of inverter with the PSS-EARC could be much higher than that of the hard-switching inverter.

The power loss distribution and comparison of hard-switching and soft-switching inverters at rated power are summarized in Table 4. Therein, other loss refers to the line stray loss and the loss of filter components. The conduction loss is roughly the same under different conditions. Comparing with the hard-switching (HS) inverter, the soft- switching effect of the PSS-EPRC and the PSS-EARC are basically the same. The switching loss reduced by the passive soft-switching snubber at rated power is about 149W.

However, in order to suppress the circulating current, the extra loss of suppression resistors in the PSS-EPRC is 105W at the rated power. It greatly reduces the PSS-EPRC efficiency to 95.63%. As for the proposed PSS-EARC, the total loss of the auxiliary devices and components including resonant inductors and capacitors, auxiliary switches and transformer is only 57.7W. The reduced loss is much higher than the additional introduced loss, so the three-phase inverter with the PSS-EARC can improve the efficiency effectively.

The efficiency curves of the three-phase hard-switching inverter and soft-switching inverter are shown in Fig. 17.

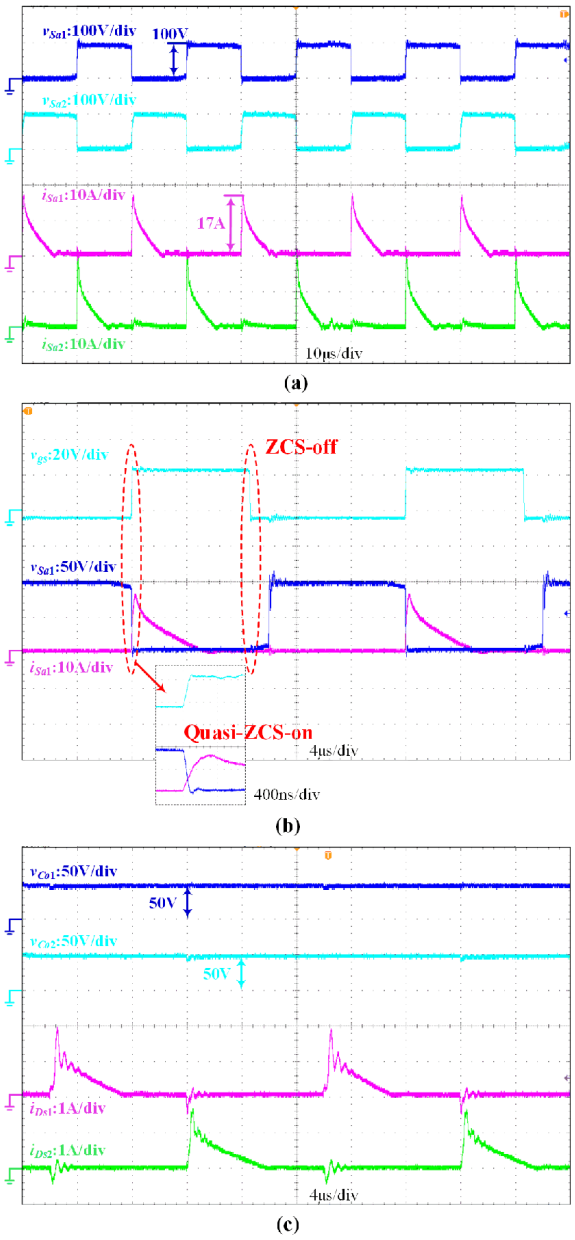

FIGURE 16. Operation waveforms of EARC. (a) Voltage and current waveforms of auxiliary switches. (b) Soft-switching of auxiliary switches. (c) Voltage of buffering capacitors and recovery current.

The overall efficiency under soft-switching is higher than that of the hard-switching all the time. The total efficiency of the three-phase inverter with the PSS-EARC is 96.53% as compared with that of the hard-switching inverter is 95.54% under rated input power. The efficiency of the three-phase inverter with the PSS-EARC is approximately 1.0% higher than the hard-switching inverter at rated load. And the efficiency advantage is greater under light load.

According to above experimental results, the high du/dt, di/dt and current stress of the switches existing in hard-switching inverter is effectively suppressed by the PSS, and all switches in the PSS-EARC realizes soft-switching. Correspondingly, the switching loss is greatly decreased. The

TABLE 4. Power loss distribution and comparison of hard-switching and soft-switching inverter at rated power.

	HS	PSS-EPRC	PSS-EARC
Input power (W)	10029	10212	10132
Output Power (W)	9582	9766	9780
Efficiency (%)	95.54	95.63	96.53
Total loss (W)	447	446	352
Main switches conduction loss (W)	60.5	60.2	59.9
Main switches switching loss(W)	245.8	96.5	97.3
Total loss of auxiliary devices (W)	0	154.1	57.7
Other loss (W)	140.7	135.2	137.1

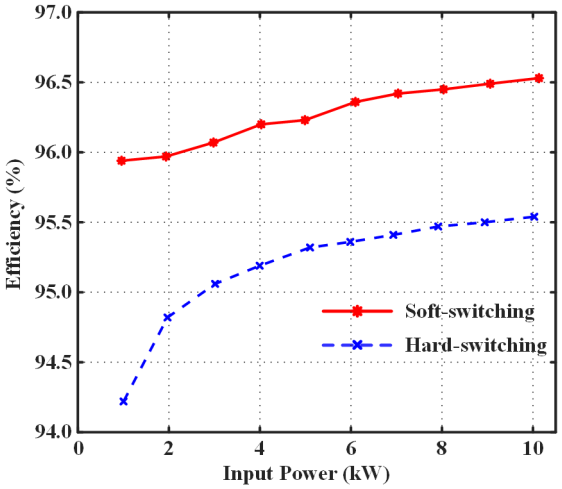

FIGURE 17. Efficiency curves comparison.

energy captured by all resonant inductors and capacitors in three bridge-legs is transferred to the buffering capacitors and further recovered back to the power supply by the EARC. Thanks to the auxiliary switches, there is no circulating current in the energy recovery circuit anymore. Therefore, the efficiency of the inverter is obviously improved.

V. CONCLUSION

In this paper, a passive soft-switching snubber with energy active recovery circuit (PSS-EARC) for PWM inverters is proposed. Both the configuration and operation principle of the PSS-EARC are analyzed in detail. And then some issues of the PSS-EARC are discussed and the analysis of circulating current in the passive recovery circuit are carried out. Finally, based on a 10kW three-phase inverter, the effect of soft-switching and the efficiency advantage of the PSS-EARC are verified. The proposed PSS-EARC employs additional auxiliary devices including inductors diodes, capacitors, switches and the push-pull transformer which will cause extra loss and increase the cost to some extent. But the extra loss is much lower than the saved switching loss, the inverter efficiency and operation environment of

the switches can be improved without complicated control, so the increasing cost is worth it. And in actual application, the line stray inductance of the inverter can be used to substitute the snubber inductors, the volume and cost of the circuit can be further reduced. Correspondingly, the following conclusions can be drawn.

1) The EARC solves the circulating current problem in the traditional energy passive recovery circuit.

2) The PSS reduces the du/dt, di/dt and current stress of the switches effectively during the switching process, as well as suppressing electromagnetic interference.

3) All switches in the PSS-EARC realizes soft-switching, which greatly decreases the switching loss.

4) The control of the auxiliary switches is completely independent of the main switches, so it is simple and reliable.

5) The inverter efficiency is effectively improved by the PSS-EARC.

Moreover, the operation of the PSS-EARC does not depend on load conditions. It is suitable for high power application such as motor driving and interconnection of power system to improve the operation environment of the switches and the efficiency.

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ZHI ZHANG (Student Member, IEEE) was born in Anqing, China, in 1994. He received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2016, where he is currently pursuing the Ph.D. degree in power electronics with the School of Electrical Engineering. His research interests include dc–dc converters, soft-switching technologies, and railway electrification systems.

XIAOFENG YANG (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2003 and 2011, respectively.

From 2003 to 2005, he was a Power Supplier Engineer with the Seventh Research Institute of China Ministry of Information Industry, Guangzhou, Guangdong. From 2012 to 2014, he was a Postdoctoral Fellow with North Carolina State University, Raleigh, NC, USA. He is currently an Associate Professor with Beijing Jiaotong University. His current research interests include high-power energy converters, HVDC, and electrical energy router.

TRILLION Q. ZHENG (Senior Member, IEEE) received the B.S. degree in electrical engineering from Southwest Jiaotong University, Sichuan, China, in 1986, and the M.S. and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China, in 1992 and 2002, respectively.

He is currently a Distinguished Professor with Beijing Jiaotong University. He is also the Director of the Center for Electric Traction, founded by the Ministry of Education, China. His current research interests include the power supplies and ac drives of railway traction systems, high-performance and low-loss power electronics systems, PV-based converters and control, active power filters, and power quality correction.

Dr. Zheng received the Youth Award of Railway Science and Technology of Zhan Tianyou, in 2005, and the Zhongda Scholar for power electronics and motor drive area by the Delta Environmental and Educational Foundation, in 2007.

JIEPIN ZHANG (Student Member, IEEE) was born in Xinxiang, China, in 1991. He received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2014, where he is currently pursuing the Ph.D. degree in power electronics with the School of Electrical Engineering. His research interests include dc/dc converters, stability of cascaded converters, traction drive systems, and power electronic transformers.