IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received April 30, 2020, accepted May 19, 2020, date of publication May 26, 2020, date of current version June 8, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2997826

Broadband Doherty Power Amplifier With Transferable Continuous Mode

DECHENG GAN[1], WEIMIN SHI[2], (Member, IEEE), SONGBAI HE[3], (Senior Member, IEEE), YONG GAO[3], AND GIDEON NAAH[4], (Student Member, IEEE)

[1]School of Electronic Information Engineering, Yangtze Normal University, Chongqing 408100, China
[2]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong
[3]School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China
[4]Electronics Engineering Department, University of Rome Tor Vergata, 00133 Rome, Italy

Corresponding author: Weimin Shi (saiqiuqiu@163.com)

ABSTRACT In this paper, in-band continuous mode transferring (CMT) method is presented for designing broadband Doherty power amplifier (DPA). Specifically, transferable continuous mode, transferring between class-J continuum to class-F^{-1} continuum, is introduced into DPA at output back-off (OBO) power level for improving bandwidth and efficiency. For validation, a broadband DPA with operation mode transferring from continuous class-J to continuous class-F^{-1} is designed, fabricated and measured. Experimental results show the drain efficiencies (DEs) of the fabricated DPA are 46.3%-57.7% and 58.4%-69.1% at 6 dB OBO and peaking power levels over 1.7-2.6 GHz. The saturation power of this DPA is 43.1-45.2 dBm with a gain of 9.1-11.2 dB in the interested band. Furthermore, when the fabricated DPA is stimulated by a 20 MHz wideband signal with a peak-to-average power ratio (PAPR) of 7.05 dB at 2.4 GHz, the measured average power is 36.5 dBm with an average DE of 45.7%, and the measured adjacent channel leakage ratios (ACLRs) are −31.9 dBc and −50.4 dBc before and after DPD technique, respectively.

INDEX TERMS Broadband power amplifier, Doherty, in-band continuous mode transferring.

I. INTRODUCTION

Wireless communication is developing in the direction of network diversification, broadband, integration and intelligence. With the development of wireless communication, everything and everybody at everywhere will be connected to the wireless network [1], [2]. Therefore, the number of smart devices and the data rate will increase rapidly to cover new services and applications. To support high data rate, the bandwidth of transceiver systems and the modulation order of signals need to be further enhanced [2], [3]. Consequently, as an important element in transceiver systems, power amplifier (PA) with wide bandwidth and high output back-off (OBO) efficiency are highly required [3]–[6]. Compared to other efficiency enhancement techniques, Doherty power amplifier (DPA) is the most popular technique due to its simplified architecture and easy realization. And wideband DPAs are expected to continue to play important roles in future communication systems [5], [6].

The bandwidth of DPA is mainly limited by output combiner network, which includes impedance inverter, output matching networks (OMNs) of the carrier and peaking PAs [7]–[10]. Notice that, impedance inverter is an essential element in DPAs. Thus, post-matching network (PMN) DPA was proposed, as post-matching DPA removes the OMNs of the carrier and peaking PAs [11]. As a results, the order of the PMN after the combining point is increased. But this high order PMN would not limit the bandwidth of DPAs [11]–[15]. Furthermore, the impedance inverter can be replaced by a low order network considering the parasitic and package elements of active devices [11], [12].

For DPAs, the drain efficiency (DE) at the OBO power level is more important than at saturation [17], [18]. Thus, to further improve the back-off DE of broadband DPAs, continuous mode DPA (CM-DPA) was proposed and investigated successively [19]–[24]. The CM-DPA works under continuous mode at the OBO power level, leading to high back-off DE and wide bandwidth simultaneously [25], [26]. The CM-DPA designed in [20] obtains a 6 dB back-off DE of 52%-66% across 1.65-2.75 GHz. And in [24], the authors designed a CM-DPA, which works over 2.7-4.3 GHz and achieves a 42%-54% DE at 6 dB OBO power level.

However, all the above CM-DPAs adopted single continuous mode, like class-J continuum [19]–[21] or hybrid continuum [22]. Indeed, the whole combiner of DPA is always a high order network, even in post-matching Doherty

The associate editor coordinating the review of this manuscript and approving it for publication was Rocco Giofré.

architecture. As we all know, with the increase of the order of matching network, the second harmonic impedance trajectory of the matching network becomes more and more divergent. In a high order low-pass network, the second harmonic impedance will be at the edge of the Smith chart. It is hard to maintain the second harmonic impedance at around short-circuited region or open-circuited region across a wide bandwidth.

Therefore, in this paper, in-band continuous mode transferring (CMT) technique is employed to design broadband DPAs. By transferring operation between class-J continuum and class-F^{-1} continuum, the second harmonic space covers the whole edge of the Smith chart [27], [28]. It will be validated in this paper that the in-band CMT technique is suitable to realize broadband DPAs. For validation, a 1.7–2.6 GHz CM-DPA, whose operation mode transfers from class-J continuum to class-F $^{-1}$ continuum, is designed and fabricated. Experimental results indicate the designed DPA obtains a saturation power of 43.1-45.2 dBm, a 6 dB back-off DE of 46.3%-57.7% and a saturation DE of 58.4%-69.1%.

The residual of this paper is as follows. Section II presents the application of the in-band CMT technique to broadband DPAs at the OBO power level. Section III shows the design and simulation of a broadband CM-DPA using in-band CMT. The fabricated DPA is measured in section IV. Finally, the paper is concluded in section V.

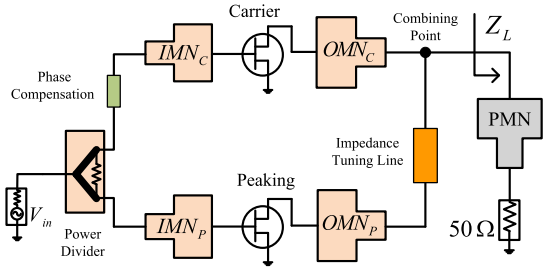


FIGURE 1. The brief architecture of the transferable continuous mode DPA.

II. BROADBAND DPA WITH IN-BAND CMT

In this contribution, the analysis is based on post-matching DPA architecture, as illustrated in Fig. 1. It includes two PAs, the class-B biased carrier PA and class-C biased peaking PA. The peaking PA is switched-on at 6 dB OBO power level. And it is assumed that the same power ability can be achieved by the carrier and peaking PAs. At the input terminal, two input matching networks are inserted to match the optimal source impedance of two transistors. And a power divider equally splits input signal into carrier and peaking paths. At the output terminal, low-order matching networks OMN_C and OMN_P are designed to match the carrier and peaking PA, respectively. Notice that, OMN_C should also play the role of impedance inverter to realize active load-modulation. And these matching networks should take the parasitic and package elements of the utilized transistors into consideration. After OMN_P, an impedance tuning line (ITL) is inserted to tune the output impedance of the peaking PA when it is in the off-state. Finally, a post-matching network (PMN) is implemented to match the Doherty load Z_L to standard 50 Ω. For the whole DPA, a phase compensation line is required to balance the phase difference between the carrier and peaking paths.

A. IN-BAND CMT AT OBO POWER LEVEL

Like in previous single CM-DPA [19]–[24], the carrier and peaking PAs are well matched by OMN_C and OMN_P at saturation power level. This means that CM-DPA can obtain high performance at maximum power level in the interested band. Therefore, the transferable CM-DPA is analyzed at the OBO power level where the peaking PA is in the off-state.

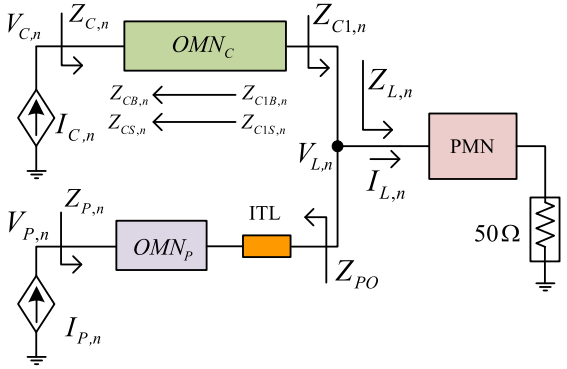


FIGURE 2. The simplified architecture of Doherty power amplifier.

Fig. 2 depicts the simplified Doherty architecture. In 2, the subscript n refers to the nth harmonic. In this paper, only the first three harmonics are taken into consideration. The load impedance of the carrier transistor at OBO power level $Z_{CB,n}$ is related to the whole combiner, which is consist of OMN_C, OMN_P and PMN.

At OBO power level, the whole combiner can be considered as a high-order low-pass network, leading to $Z_{CB,2}$ and $Z_{CB,3}$ are located at the edge of smith chart. Furthermore, It has been demonstrated in [20] and [22] that $Z_{CB,1}$ can be modulated into the impedance space of continuous operation mode. Thus, CM-DPA can be realized if the second and third harmonic are well manipulated.

Normally, continuous mode requires that the second harmonic is located to around the short-circuited or the open-circuited region. Indeed, it is almost impossible to realize this requirements when high-order matching network is utilized. Thus, CMT is introduced into broadband CM-DPA design. Fig. 3 illustrates the CMT technique at the OBO power level of the CM-DPA. The operation mode transfers between class-J continuum and class-F^{-1} continuum.

At the OBO power level, the normalized first three harmonic impedance spaces of class-J continuum can be derived as [20],

$$Z_{J,1} = 2 \cdot (1 + j \cdot \gamma) \tag{1}$$

$$Z_{J,2} = -j \cdot \frac{3 \cdot \pi \gamma}{4} \tag{2}$$

$$Z_{J,3} = 0 \tag{3}$$

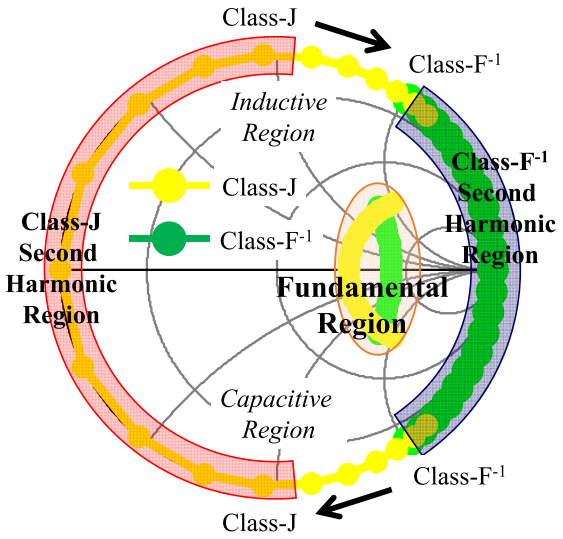


FIGURE 3. The fundamental and second harmonic impedance region of CM-DPA with in-band CMT.

While the first three harmonic impedance spaces of the continuous class-F^{-1} mode can be described as [28],

$$Z_{F^{-1},1} = \frac{\sqrt{2}}{0.43 + j \cdot 0.37 \cdot \gamma} \tag{4}$$

$$Z_{F^{-1},2} = j \cdot \frac{1}{0.49 \cdot \gamma} \tag{5}$$

$$Z_{F^{-1},3} = 0 \tag{6}$$

Here all impedance are normalized to R_{opt}, which is the internal optimal impedance of a class-B biased transistor [27]–[29]. With equations (1)-(6), the fundamental impedance spaces of the class-J and class-F^{-1} can be deduced as the yellow and green lines inside the Smith chart in Fig. 3. And the second harmonic impedance spaces can be deduced as the yellow and green lines at the edge of the Smith chart.

As shown in Fig. 3, The second harmonic impedance spaces of the class-J and class-F^{-1} continuum occupy the whole edge of the Smith chart. Thus, if the trajectory of $Z_{CB,2}$ varies from the short-circuited to open-circuited (or from open-circuited to short-circuited), the operation mode of the CM-DPA will transfer from continuous class-J to continuous class-F^{-1} (or from continuous class-F^{-1} to continuous class-J). With continuous mode transferring, $Z_{CB,1}$ should be matched to the fundamental region, which is formed by $Z_{J,1}$ and $Z_{F^{-1},1}$, as shown in Fig. 3.

Summarily, Fig. 3 shows the fundamental and second harmonic regions of the transferable continuous mode. In this contribution, to perfectly control the second harmonic of CM-DPA, $Z_{CB,1}$ is matched to the fundamental region, and $Z_{CB,2}$ transfers from class-J second harmonic region to class-F^{-1} second harmonic region, or vice verse.

B. SECOND AND THIRD HARMONIC CONSIDERATION

The utilized active transistors in DPAs always possesses parasitic capacitors C_{ds}. In this work, CGH40010F transistor

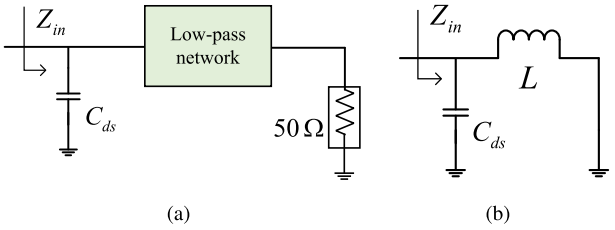


FIGURE 4. The simplified Doherty combiner. (a) C_{ds} paralleled with a high-order low-pass network. (b) Parallel connection between C_{ds} and an inductor.

is utilized. The parasitic capacitor C_{ds} of this kind transistor is approximately equal to 1.2 pF. Thus, the Doherty combiner can be simplified to a parallel structure of C_{ds} and a high-order low-pass network, as show in Fig. 4(a). As demonstrated in [28], the low-pass network can be further simplified to be an inductor at second and third harmonic frequency, as shown in Fig. 4 (b).

The impedance produced by C_{ds} and L can be respectively expressed as,

$$Z_{C_{ds}} = -j \cdot \frac{1}{2 \cdot \pi \cdot f \cdot C_{ds}} \tag{7}$$

$$Z_X = j \cdot 2 \cdot \pi \cdot f \cdot L \tag{8}$$

And the input impedance of the parallel resonant circuit can be deduced as,

$$Z_{in} = j \cdot \frac{2 \cdot \pi \cdot f \cdot L}{1 - (2 \cdot \pi \cdot f)^2 \cdot L \cdot C_{ds}} \tag{9}$$

Fig. 5(a) shows the reactance of $Z_{C_{ds}}$ and Z_X versus frequency. Here, C_{ds} is set to 1.2 pF, and L is set to 0.6, 0.8 and 1 nH. As depicted in Fig. 5(a), C_{ds} dominates the parallel resonant circuit at higher frequency band, while L dominates at lower frequency band. Fig. 5(a) also shows that the reactance of C_{ds} and L have the same magnitude at middle frequency band. And from (7) and (8), the signs of the reactance generated by C_{ds} and L are different. Consequently, the parallel circuit will resonate at middle frequency. Fig. 5(b) depicts the reactance of the whole parallel circuit. Clearly, the parallel circuit resonates at 4.6, 5 and 6 GHz when L equals to 0.6, 0.8 and 1 nH, respectively.

The resonance between C_{ds} and L (high-order combining network) makes sure that the reactance changes from the inductive region to capacitive region in the Smith chart. And finally, the parallel circuit is shorted by C_{ds} at higher frequency band. This is exactly the idea of CMT technique.

C. FUNDAMENTAL CONSIDERATION

At the OBO power level, the non-infinity peaking impedance could modulate $Z_{CB,1}$ to the fundamental impedance space of class-J continuum, as demonstrated in [20] and [29]. However, in the transferable continuous mode DPA, $Z_{CB,1}$ should be located into the fundamental region shown in Fig. 3. And $Z_{CB,1}$ should be close to the fundamental impedance space of class-F^{-1} continuum when $Z_{CB,2}$ approaches to the

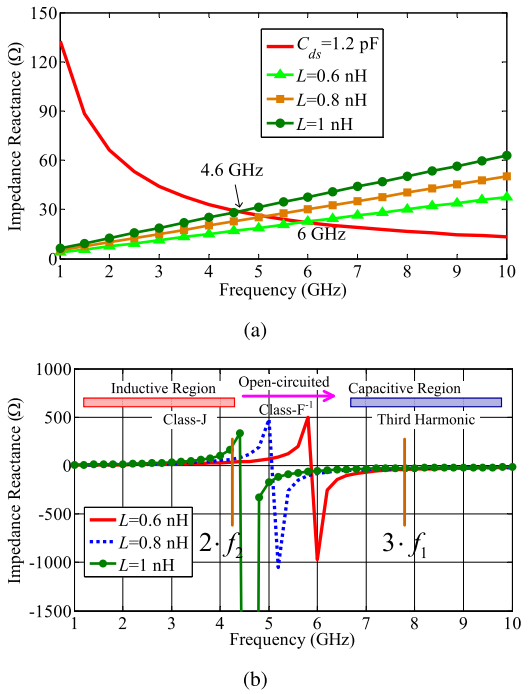


FIGURE 5. (a) The reactance of C_{ds} and L. (b) The resonance between C_{ds} and L.

open-circuited point. Meanwhile, $Z_{CB,1}$ should be close to the fundamental impedance space of class-J continuum when $Z_{CB,2}$ approaches to the short-circuited point.

As shown in Fig. 2, $Z_{CB,1}$ is mainly dependent on OMN_C, and ITL after Z_L is fixed. In single continuous mode DPA, the phase delay of OMN_C is 90° at the center frequency point. And the peaking impedance is tuned to infinity by the ITL at the center frequency point. In this contribution, to realize CMT, the phase delay of the OMN_C is slightly deviated from 90° at the center frequency point, and the peaking impedance is also tuned to slightly deviates from infinity at the center frequency point.

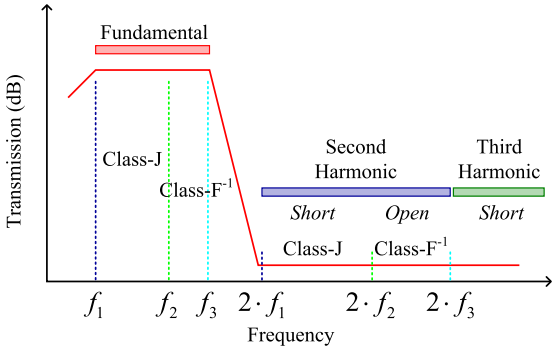


FIGURE 6. The operating principle of the transferable continuous mode DPA.

Finally, the operating principle of the transferable continuous mode DPA can be concluded as in Fig. 6. Assuming that the interested bandwidth is $f_1 - f_3$, and the mode transferring frequency is f_2. Then, the fundamental frequency bands of the class-J and class-F^{-1} continuum are $f_1 - f_2$ and $f_2 - f_3$, respectively. Moreover, the impedance across $2 \cdot f_1 - 2 \cdot f_2$ should be located at around the short-circuited point, and the impedance across $2 \cdot f_2 - 2 \cdot f_3$ should be located at around the open-circuited point. At the third harmonic frequency, short-circuit is provided by C_{ds}.

III. DESIGN AND SIMULATION OF A TRANSFERABLE CONTINUOUS MODE DPA

This section illustrates the design of a symmetrical CM-DPA using in-band CMT. The operation mode of the DPA transfers from continuous class-J mode to continuous class-F^{-1} mode. The targeted frequency band is 1.7-2.6 GHz. The utilized active devices are CGH40010F GaN transistors from Wolfspeed. The optimal impedance of this kind transistor is set to $R_{opt} = 30\ \Omega$ [22]. The gate voltages of the carrier and peaking PAs are -2.9 and -5.5 V, respectively. 28 V voltage is supplied to the drain of the carrier and peaking PAs.

In this section, all simulation results are derived using Advanced Design System (ADS). Across the simulation, Rogers 4350B substrate with thickness of 20 mil is utilized.

A. DPA DESIGN

The design procedure of the transferable CM-DPA is as follows:

Step 1: The Doherty load $Z_{L,1}$ is set to 10 Ω. And a PMN is designed to match 10 Ω to standard 50 Ω.

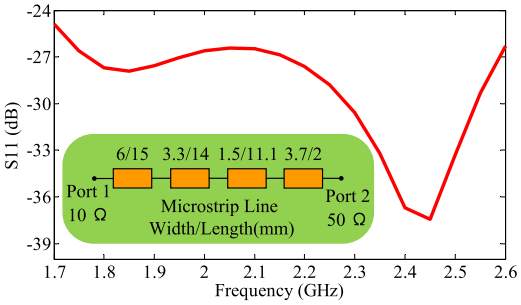


FIGURE 7. The post-matching network and simulation results.

Fig. 7 shows the PMN and its simulation results. The PMN is constructed by four series-connected microstrip lines (see the green colored region in Fig. 7). The simulated S11 is smaller than -24 dB, which means the designed PMN could match 10 Ω to 50 Ω across 1.7-2.6 GHz.

Notice that, considering that $Z_{L,1}$ =10 Ω, the load impedance of the carrier and peaking PAs should be equal to 20 Ω at maximum power level due to the active load modulation.

Step 2: IMN_C and IMN_P are implemented to respectively match the carrier and peaking PAs at their source terminals. And a Wilkinson power divider is designed to equally split input power to the carrier and peaking paths.

Step 3: OMN_P is implemented to match the peaking PA to 20 Ω at maximum input power level.

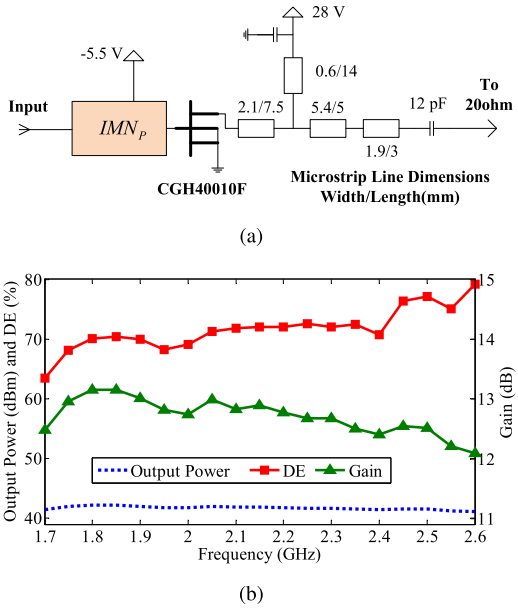


FIGURE 8. The schematic and simulation results of the peaking PA. (a) Schematic. (b) Simulation results.

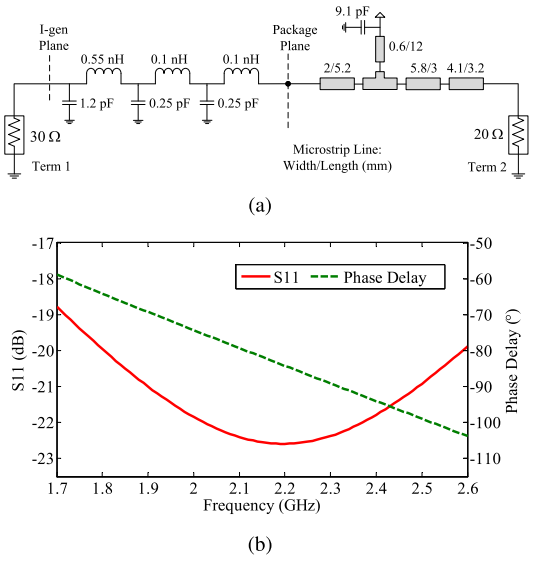


FIGURE 9. The schematic and simulation results of the designed OMN_C. (a) Schematic. (b) Simulation results.

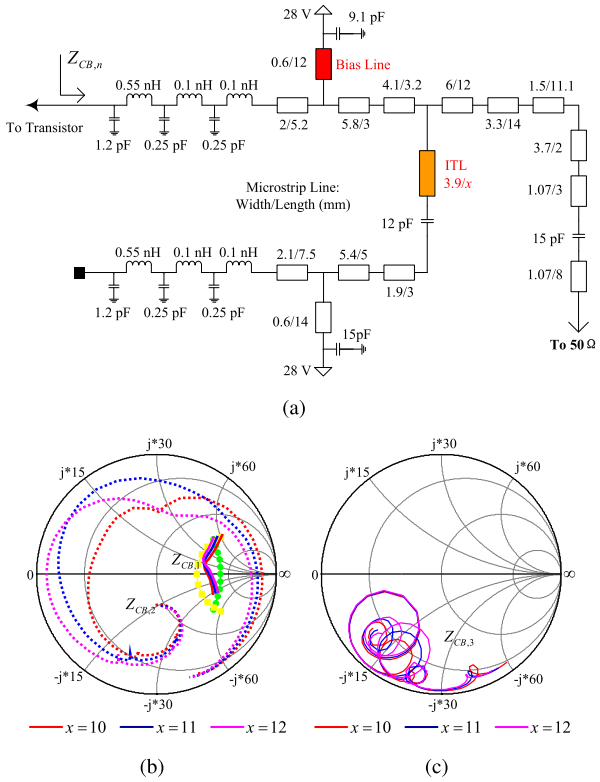


FIGURE 10. The constructed Doherty combiner and its simulation results. (a) Doherty combiner. (b) The simulated fundamental and second harmonic impedance trajectories. (c) The simulated third harmonic impedance trajectories.

OMN_P can be realized easily with the help of ADS optimization. Most importantly is that, OMN_P should be a low-order network, otherwise the achievable bandwidth of the DPA will be limited [11], [12]. The designed OMN_P is illustrated in Fig. 8(a), where depicts the whole schematic of the peaking PA. To validate the designed OMN_P, the simulation results of the peaking PA is shown in Fig. 8(b). The peaking PA delivers a saturation power of 41.1-42.1 dBm with a gain of 12.1-13.2 dB and a DE of 63.4%-79.1%.

Step 4: OMN_C is designed to match 20 Ω to R_{opt} over the interested frequency band. Meanwhile, the OMN_C should also play a role of an impedance inverter.

Fig. 9(a) shows the designed OMN_C, which includes the parasitic and packaged elements of the utilized transistors [22]. The simulation results of the designed OMN_C are depicted in Fig. 9(b). The phase delay of the OMN_C is 90° at 2.3 GHz, which is slightly deviates from the center frequency 2.15 GHz. Meanwhile, the simulated S11 is smaller than -18.8 dB over 1.7-2.6 GHz.

Step 5: The whole combiner is realized by combining OMN_C, OMN_P and PMN. And an 20 Ω ITL should be inserted behind the peaking PA to make sure that the peaking impedance is around the open-circuited point.

The whole combiner is depicted in Fig. 10(a). As stated in Section II, $Z_{CB,1}$ and $Z_{CB,2}$ are determined by the whole combiner, and $Z_{CB,3}$ will be shorted by C_{ds}. Therefore, we can mainly focus on $Z_{CB,1}$ and $Z_{CB,2}$.

Considering the parallel of C_{ds} and other networks, $Z_{CB,2}$ will be resonated to be infinity at middle frequency band (the higher frequency band of second harmonic) as shown in Fig. 5 (b). At the lower frequency band of the second harmonic, we can introduce poles or zeros to the combiner to tune the second harmonic impedance trajectory. Poles and zeros can be introduced by tuning the length of ITL and the drain bias line of the carrier transistor. As shown in Fig. 9 (a) and Fig. 10 (a), the length of the drain bias line is tuned to 12 mm, leading to a pole at 3.6 GHz. Notice that, OMN_C in ***Step 4*** should be re-optimized after tuning the bias line.

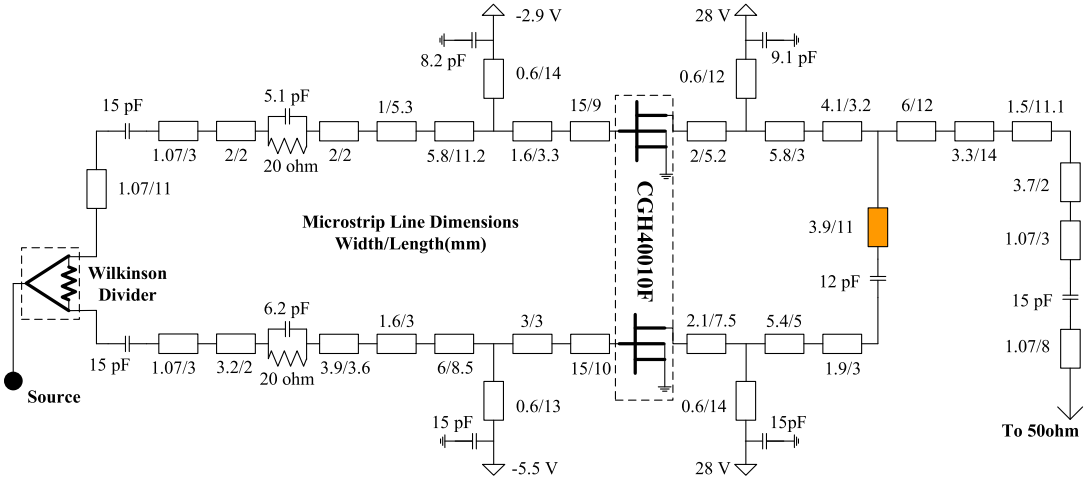


FIGURE 11. The whole schematic of the designed DPA together with the dimensions of elements.

For $Z_{CB,1}$, We have already demonstrated in [20] and [22] that $Z_{CB,1}$ can be modulated to the impedance space of the continuous mode by adjusting the length of ITL. In this design, $Z_{CB,1}$ is also realized by tuning the length of ITL. For simplicity, the length of the ITL is assumed to be x mm, as shown in Fig. 10(a).

As a validation, the simulation results of the combiner are shown in Fig. 10(b) and (c). In the simulation, x is swept from 10 mm to 12 mm with a step of 1 mm. Fig. 10(b) shows that $Z_{CB,1}$ is located into the fundamental impedance region. And $Z_{CB,1}$ changes from the class-J continuum to the class-F^{-1} continuum. Also, Fig. 10(b) shows that $Z_{CB,2}$ changes from the capacitive region to the inductive region passing through the short-circuited point. And finally, $Z_{CB,2}$ reaches to the second harmonic region of continuous class-F^{-1} mode, as shown in Fig. 10(b). The simulated $Z_{CB,3}$ is shown in Fig. 10(c). Though $Z_{CB,3}$ is not perfectly shorted by C_{ds}, it is located at around the short-circuited point.

The simulation results in Fig. 10(b) and (c) validates the designed DPA obtains a transferable continuous mode, transferring from class-J continuum to class-F^{-1} continuum.

B. DPA SIMULATION RESULTS

Based on the above design, the whole schematic of the designed DPA are depicted in Fig. 11. According to the simulation results shown in Fig. 10, the length of ITL is set to 11 mm.

Under the input power level of 20 dBm, the simulated $Z_{CB,1}$, $Z_{CB,2}$ and $Z_{CB,3}$ are depicted in Fig. 12(a) and (b). The simulation results are very close to Fig. 10(b) and (c). This means that the operation mode of the designed DPA transfers from class-J continuum to class-F^{-1} continuum at OBO power level. From Fig. 12(a), $Z_{CB,2}$ transfers from class-J region to class-F^{-1} region at 4.8 GHz. Therefore, continuous class-J DPA and continuous class-F^{-1} DPA can be realized over 1.7-2.4 GHz and 2.4-2.6 GHz, respectively.

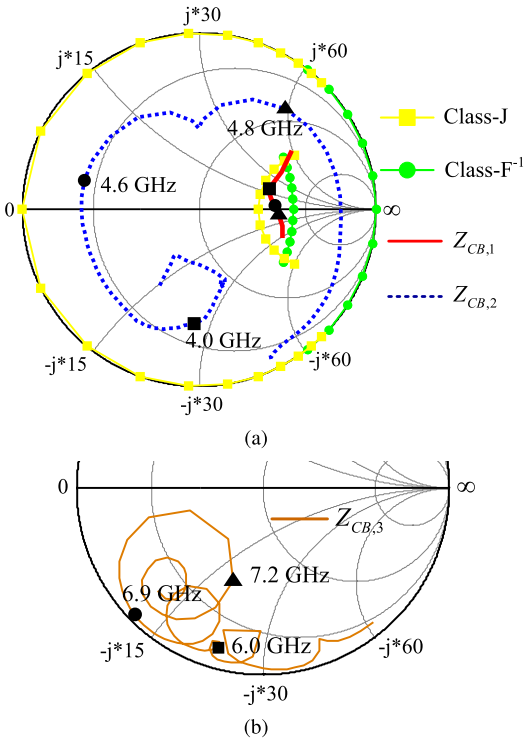


FIGURE 12. The simulated internal load impedance trajectories of the carrier transistors at the low power region. (a) The fundamental and second harmonic load impedance. (b) The third harmonic load impedance.

Like in Fig. 10(c), the simulated $Z_{CB,3}$ is located around the short-circuited point, as shown in Fig. 12(b).

To further validate the proposed theory, Fig. 13(a)-(d) shows the simulated current and voltage waveforms of carrier PA at 1.7, 2.0, 2.3 and 2.6 GHz, respectively. These waveforms are simulated at the I-gen plane of the carrier transistor when the output power is 37.1 dBm. These simulated waveforms demonstrate the operation mode transfers from

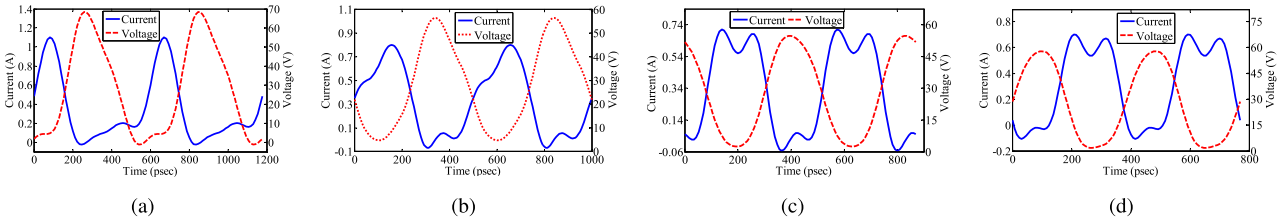


FIGURE 13. The simulated internal current and voltage waveforms of the carrier PA at the output power level of 37.1 dBm. (a) At 1.7 GHz. (b) At 2.0 GHz. (a) At 2.3 GHz. (b) At 2.6 GHz.

class-J continuum to class-F^{-1} continuum in the interested frequency band.

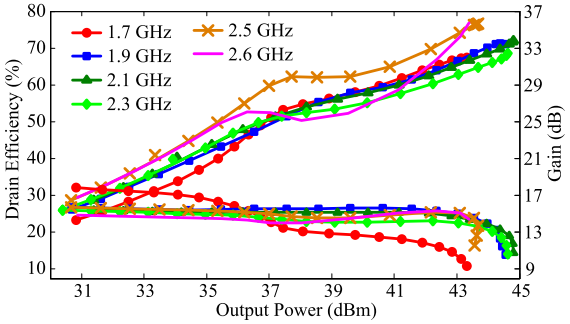


FIGURE 14. The simulated DEs and gains of the designed DPA versus output power.

Finally, the simulated DEs and gains of the designed DPA are shown in Fig. 14. Apparent Doherty behavior is realized across 1.7-2.6 GHz. The saturation output power of the designed DPA is more than 43.3 dBm. And the second efficiency peaks appear at 37-38 dBm. From Fig. 14, the simulated DEs of the designed DPA are better than 50% over 6 dB OBO power region.

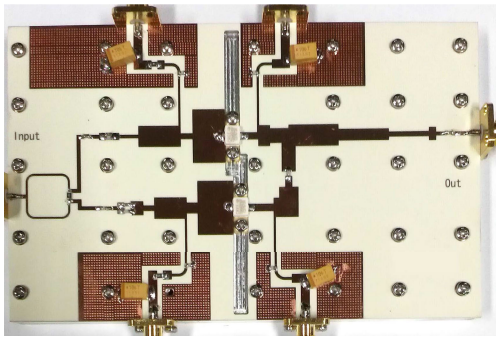


FIGURE 15. The photograph of the fabricated DPA.

IV. EXPERIMENTAL RESULTS

The photograph of the fabricated DPA is shown in Fig. 15. To evaluate the performances of the designed DPA, the fabricated DPA is tested using continuous-wave(CW) and 20-MHz wideband LTE signals, respectively. In the measurement, the drain voltage of the carrier and peaking PAs are 28 V. And the gate voltages of the carrier and peaking PAs are −2.8 V and −5.9 V, respectively.

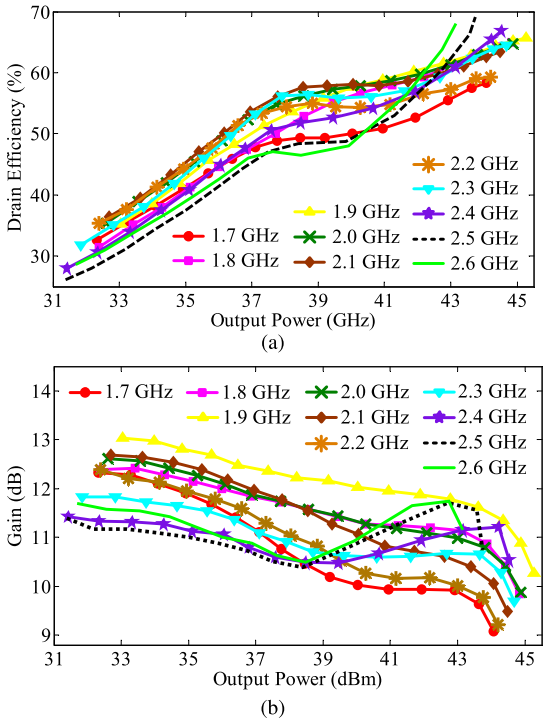


FIGURE 16. The measured DEs and gains of the fabricated CM-DPA versus output power. (a) Measured DEs. (b) Measured gains.

A. CONTINUOUS WAVE SIGNAL EXCITATION

When driven by CW signal, the fabricated DPA is measured over 1.7-2.6 GHz with a step of 100 MHz. The measured DEs and gains versus output power are indicated in Fig. 16(a) and (b), respectively. From Fig. 16(a), apparent Doherty behavior is obtained. Like the simulated DEs, the second efficiency peaks appear at 37-38 dBm power levels. From Fig. 16(b), the measured saturation gains are larger than 9 dB over the whole frequency band. To clearly evaluate the performance of the fabricated DPA, the measured results versus working frequency are shown in Fig. 17(a)-(c).

Fig. 17(a) shows the maximum output power of the fabricated DPA. The fabricated DPA could deliver a saturation output power of 43.2-45.2 dBm with a gain of 9.1-11.2 dB over 1.7-2.6 GHz. For comparison, the simulated saturation output power is also illustrated in Fig. 17(a). The simulated power ability of the designed DPA is 43.3-44.9 dBm in the interested frequency band. Fig. 17(a) indicates that the measured saturation power is similar with the simulation result.

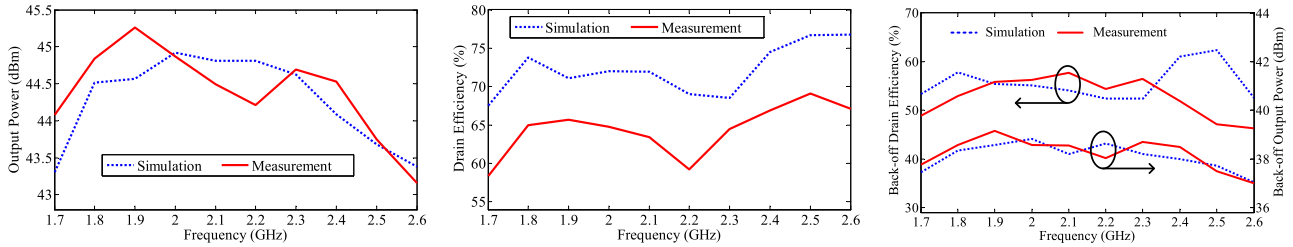


FIGURE 17. The measured output power and DEs of the fabricated CM-DPA versus working frequency (a) Saturation power. (b) DE at maximum power level. (c) Back-off DE and output power.

TABLE 1. Comparison between some recently published CM-DPAs and our work.

Year, Ref.	Frequency (GHz)	BW (GHz)	Power (dBm)	Gain (dB)	DE@Sat (%)	DE@OBO (%)
2016, [19]	1.7–2.8 (49%)	1.1	44–44.5	11–12	57–71	50–55
2018, [20]	1.6–2.7 (51%)	1.1	43.8–45.2	9.4–11.5	56–75.3	46.5–63.5
2019, [22]	1.5–2.6 (53%)	1.1	43.7–45	7.7–9.3	57–75	41.3–55.1
2019, [23]	1.25–2.3 (59.2%)	1.05	41.4–44.6	N/A	56–75.4	45–56.5
2019, [24]	2.7–4.3 (46%)	1.6	38.5–39.2	N/A	48–61	40–43
This Work	1.7–2.6 (42%)	0.9	43.2–45.2	9.1–11.2	58.4–69.1	46.3–57.7

The measured DE versus frequency at saturation power level is shown in Fig. 17(b). Meanwhile, the simulated DE at saturation is also depicted in Fig. 17(b). It indicates that the measured and simulated saturation DEs of the fabricated DPA are 58.4%69.1% and 67.5%-76.8%, respectively. According to Fig. 17(b), the measured DE is a little lower than the simulated DE. This may be caused by the inaccuracy model of the class-C biased transistors and the process error of printed circuit board (PCB).

At 6 dB OBO power level, the measured and simulated DEs and output power with respect to working frequency are illustrated in Fig. 17(c). The measured and simulated 6 dB back-off power is 37-39.2 dBm and 37-38.8 dBm, respectively. From Fig. 17(c), the measured 6 dB back-off DE changes from 46.3% to 57.1% over 1.7-2.6 GHz. And the simulated 6 dB back-off DE of the designed DPA over the whole working band is 52.4%-62.3%.

Under the excitation of CW signal, the experimental results of the fabricated DPA are outlined in Table 1. Furthermore, some recently published CM-DPAs are also given in Table 1 for comparison. Comparable performances are obtained by this work according to Table 1.

B. WIDEBAND SIGNAL EXCITATION

To evaluate the linearity of the fabricated DPA, a 20-MHz LTE signal is utilized to drive the fabricated DPA. The peak to average power ratio (PAPR) of this input signal is 7.05 dB. With the wideband signal excitation, measurement is also performed over 1.7-2.6 GHz with a step of 100 MHz. Across the measurement, the average output power is 36.5 dBm at every frequency points. Fig. 18 shows

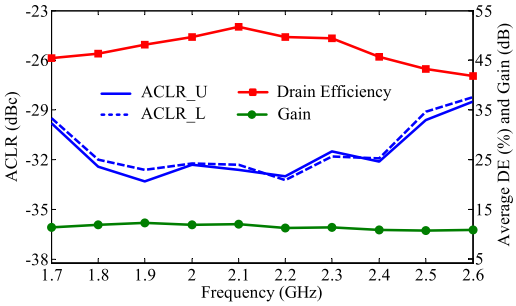


FIGURE 18. The measured ACLRs, average DE and gain of the fabricated DPA versus frequency.

the measured adjacent channel leakage ratios (ACLRs), average DE and gain versus frequency. The measured gain changes from 10.7 dB to 12.3 dB, as shown in Fig. 18. The measured ACLRs at the upper band (ACLR_U) and at the lower band (ACLR_L) change from −33.3 dBc to −28.5 dBc and from −33.2 dBc to −28.2 dBc, respectively. Meanwhile, the measured average DE of the fabricated DPA is 41.8%-51.7% over the whole working frequency band.

Furthermore, digital predistortion (DPD) technique is performed to the fabricated DPA at 2.4 GHz for further improving linearity. At this frequency point, the measured average output power is 36.5 dBm with an average DE of 45.7% as shown in Fig. 18. And the measured ACLRs are −31.9 and −50.4 dBc before and after DPD, respectively. Fig. 19 shows the normalized output spectrums before and after DPD. When performing DPD, indirect learning approach is used to obtain the DPD function. A first-order dynamic deviation

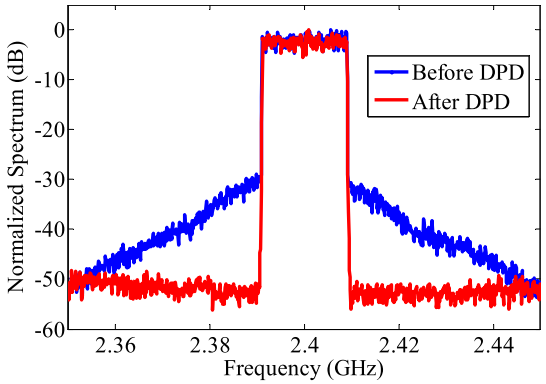


FIGURE 19. The measured output spectrums of the fabricated DPA before and after DPD at 2.4 GHz.

reduction-based Volterra model with non-linear order 4 and memory depth 13 is chosen to build the DPD structure. All the model parameters are estimated through the least square method.

V. CONCLUSION

Doherty power amplifier with transferable continuous mode is presented in this contribution with continuous mode transferring method, the second harmonic impedance of CM-DPA can be perfectly controlled at OBO power level. As a validation, a broadband CM-DPA working over 1.7-2.6 GHz is designed and fabricated. Simulation results indicate that, at the OBO power level, the operation mode of the designed DPA changes from class-J continuum to class-F^{-1} continuum. Experimental results show that the fabricated DPA achieves a 6 dB back-off drain efficiency of 46.3%-57.7% over 1.7-2.6 GHz. The saturation output power of the fabricated DPA is 43.1-45.2 dBm with a drain efficiency of 58.4%-69.1% in the interested band.

REFERENCES

[1] A. Ghosh, A. Maeder, M. Baker, and D. Chandramouli, "5G evolution: A view on 5G cellular technology beyond 3GPP release 15," *IEEE Access*, vol. 7, pp. 127639–127651, 2019.

[2] T. Qi and S. He, "Power up potential power amplifier technologies for 5G applications," *IEEE Microw. Mag.*, vol. 20, no. 6, pp. 89–101, Jun. 2019.

[3] S. Thota, Y. Kamatham, and C. S. Paidimarry, "Analysis of hybrid PAPR reduction methods of OFDM signal for HPA models in wireless communications," *IEEE Access*, vol. 8, pp. 22780–22791, 2020.

[4] Z. Popovic, "Amping up the PA for 5G: Efficient GaN power amplifiers with dynamic supplies," *IEEE Microw. Mag.*, vol. 18, no. 3, pp. 137–149, May 2017.

[5] P. M. Asbeck, "Will Doherty continue to rule for 5G?" in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540208.

[6] R. Pengelly, C. Fager, and M. Ozen, "Doherty's legacy: A history of the Doherty power amplifier from 1936 to the present day," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 41–58, Feb. 2016.

[7] K. Bathich, A. Z. Markos, and G. Boeck, "Frequency response analysis and bandwidth extension of the Doherty amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 934–944, Apr. 2011.

[8] R. Giofre, L. Piazzon, P. Colantonio, and F. Giannini, "A closed-form design technique for ultra-wideband Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3414–3424, Dec. 2014.

[9] R. Darraji, D. Bhaskar, T. Sharma, M. Helaoui, P. Mousavi, and F. M. Ghannouchi, "Generalized theory and design methodology of wideband Doherty amplifiers applied to the realization of an octave-bandwidth prototype," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 3014–3023, Aug. 2017.

[10] G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of GaN MMIC Doherty power amplifiers using broadband transformer-based load modulation network," *IEEE Access*, vol. 7, pp. 119844–119855, 2019.

[11] X. Chen and W. Chen, "A novel broadband Doherty power amplifier with post-matching structure," in *Proc. Asia Pacific Microw. Conf. Proc.*, Kaohsiung, Taiwan, Dec. 2012, pp. 370–372.

[12] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, Dec. 2015.

[13] S. Chen, G. Wang, Z. Cheng, and Q. Xue, "A bandwidth enhanced Doherty power amplifier with a compact output combiner," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 434–436, Jun. 2016.

[14] J. Xia, M. Yang, Y. Guo, and A. Zhu, "A broadband high-efficiency Doherty power amplifier with integrated compensating reactance," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2014–2024, Jul. 2016.

[15] J. Xia, M. Yang, and A. Zhu, "Improved Doherty amplifier design with minimum phase delay in output matching network for wideband application," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 11, pp. 915–917, Nov. 2016.

[16] X. Y. Zhou, S. Y. Zheng, W. S. Chan, S. Chen, and D. Ho, "Broadband efficiency-enhanced mutually coupled harmonic postmatching Doherty power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1758–1771, Jul. 2017.

[17] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 1, pp. 143–152, Jan. 2011.

[18] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2295–2305, Sep. 2011.

[19] X. Chen, W. Chen, F. M. Ghannouchi, Z. Feng, and Y. Liu, "A broadband Doherty power amplifier based on continuous-mode technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4505–4517, Dec. 2016.

[20] W. Shi, S. He, X. Zhu, B. Song, Z. Zhu, G. Naah, and M. Zhang, "Broadband continuous-mode Doherty power amplifiers with noninfinity peaking impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1034–1046, Feb. 2018.

[21] C. Huang, S. He, and F. You, "Design of broadband modified Class-J Doherty power amplifier with specific second harmonic terminations," *IEEE Access*, vol. 6, pp. 2531–2540, 2018.

[22] D. Gan and W. Shi, "Design of a broadband Doherty power amplifier based on hybrid continuous mode," *IEEE Access*, vol. 7, pp. 86194–86204, 2019.

[23] S. Ghosh and K. Rawat, "Hybrid analog/digital continuous class B/J mode for broadband Doherty power amplifiers," *IEEE Access*, vol. 7, pp. 74986–74995, 2019.

[24] Y. Li, X. Fang, A. Jundi, H. Huang, and S. Boumaiza, "Two-port network theory-based design method for broadband class j Doherty amplifiers," *IEEE Access*, vol. 7, pp. 51028–51038, 2019.

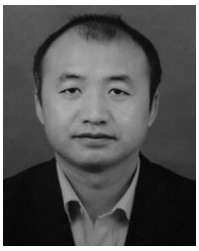
[25] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt, "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 665–667, Oct. 2009.

[26] V. Carubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, S. C. Cripps, and P. J. Tasker, "The continuous inverse class-F mode power amplifier with resistive second-harmonic impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1928–1936, Jun. 2010.

[27] K. Chen and D. Peroulis, "Design of broadband highly efficient harmonic-tuned power amplifier using in-band continuous Class-F^{-1}/F mode transferring," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4107–4116, Dec. 2012.

[28] Y. Sun, X.-W. Zhu, J. Zhai, L. Zhang, and F. Meng, "Highly efficient concurrent power amplifier with controllable modes," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4051–4060, Dec. 2015.

[29] W. Shi, S. He, F. You, H. Xie, G. Naah, Q.-A. Liu, and Q. Li, "The influence of the output impedances of peaking power amplifier on broadband Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 3002–3013, Aug. 2017.



DECHENG GAN received the master's degree from the School of Life Science and Technology, University of Electronic Science and Technology of China, Chengdu, China, in 2007, and the Ph.D. degree from the School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu, in 2018.

In 2019, he joined the School of Electronic Information Engineering, Yangtze Normal University, Chongqing, China, where he is currently an Assistant Professor. His current research interests include passive circuit design and nonlinear active circuits.

WEIMIN SHI (Member, IEEE) received the B.S. degree in electronic information science and technology from the Shandong Institute of Business and Technology, Yantai, China, in 2013, and the Ph.D. degree in circuits and systems from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2019.

He is currently a Postdoctoral Fellow with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong. His current research interests include broadband power amplifiers, load-modulation techniques, and CMOS millimeter-wave IC design.

SONGBAI HE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 1995, 1998, and 2003, respectively.

In 2004, he visited Chiba University, Chiba, Japan, where he was involved with the research of high-efficiency switch-mode power amplifiers. In 2005, he returned to the University of Electronic Science and Technology of China, where he is currently a Professor. His current research plan of broadband high efficiency linear transmitter is supported by the Hi-Tech Research and Development Program of China. His research interests include RF/MW circuits and systems, frequency synthesis, wireless communication, and nonlinear dynamic systems.

YONG GAO received the Ph.D. degree in electromagnetic field and microwave technology from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, 2019.

He is currently working as a Postdoctoral Researcher of electromagnetic fields and microwave technology with UESTC. His research interests include nonlinear dielectric properties of high-power microwave material, interaction mechanism between high power microwave and materials, high-power devices feature parameter extraction, passive intermodulation test technology, design of microwave devices, and microwave integrated circuits.

GIDEON NAAH (Student Member, IEEE) received the bachelor's degree in computer engineering from the All Nations University College, Ghana, in 2011, and the M.S. and Ph.D. degrees in circuits and systems from the University of Electronic Science and Technology of China, Chengdu, China, in 2013 and 2019, respectively.

He is currently a Postdoctoral Fellow with the Electronics Engineering Department, University of Roma Tor Vergata, Rome, Italy. His current research interest includes the design of highly efficient RF PA for broadband wireless systems.