IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 8, 2020, accepted May 17, 2020, date of publication May 26, 2020, date of current version June 16, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.2997809

Carbon Nanotube and Resistive Random Access Memory Based Unbalanced Ternary Logic Gates and Basic Arithmetic Circuits

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This work was supported in part by the Universiti Teknologi PETRONAS, Malaysia, through the Graduate Assistant (GA) Scheme, and in part by the Yayasan Universiti Teknologi PETRONAS (YUTP)-Fundamental Research under Grant 015LC0-245.

ABSTRACT In this paper, the design of ternary logic gates (standard ternary inverter, ternary NAND, ternary NOR) based on carbon nanotube field effect transistor (CNTFET) and resistive random access memory (RRAM) is proposed. Ternary logic has emerged as a very promising alternative to the existing binary logic systems owing to its energy efficiency, operating speed, information density and reduced circuit overheads such as interconnects and chip area. The proposed design employs active load RRAM and CNTFET instead of large resistors to implement ternary logic gates. The proposed ternary logic gates are then utilised to carry out basic arithmetic functions and is extendable to implement additional complex functions. The proposed ternary gates show significant advantages in terms of component count, chip area, power consumption, energy consumption and dense fabrication. The results demonstrate the advantage of the proposed models with a reduction of 50% in transistor count for the STI, TNAND and TNOR logic gates. For THA and THS arithmetic modules 65.11% reduction in transistor count is observed while for TM design, around 38% reduction is observed. In this work, we aim to demonstrate the viability of RRAM in the design of ternary logic systems, thus the focus is mainly on obtaining the proper functionality of the proposed design. Also the proposed logic gates show a very small variation in power consumption and energy consumption with variation in process parameters, temperature, output load, supply voltage and operating frequency. For simulations, HSPICE tool is used to verify the authenticity of the proposed designs. The ternary half adder, ternary half subtractor and ternary multiplier circuits are then implemented utilising the proposed gates and validated through simulations.

INDEX TERMS Multiple valued logic (MVL), ternary logic systems, emerging technologies, carbon nanotube field effect transistor (CNTFET), resistive random access memory (RRAM).

I. INTRODUCTION

Arithmetic operations play a very important role in various digital systems. The design of digital circuits for decades has been associated with binary logic having two possible logical values (0 or 1, true or false). The logic levels in binary systems are represented by two discrete values of current, voltage or charge. For computing systems based on binary logic implementation, one of the critical design issues in the nanoscale range is the interconnect limitation. The interconnect lines used for integrated circuit design contribute to noise, delay and increase in power consumption. The semiconductor devices are being scaled continuously, thus interconnects have become the most important components that determine the performance of integrated circuits [1]. The emergence of multiple valued logic (MVL) is considered as a potential solution to effectively address critical issues (such as delay and parasitic effects) of the interconnects in the

The associate editor coordinating the review of this manuscript and approving it for publication was Chaitanya U. Kshirsagar.

modern circuits. There are significant advantages of implementing MVL circuits over binary logic for design of digital systems. The main advantage of MVL system is that more information can be transmitted by each wire and more than one-bit information can be stored in each memory cell [2]. This is in contrast to binary logic systems wherein we can store only one-bit information per cell. Thus, implementing MVL based systems reduces the complexity of interconnects and enhances the storage capacity. MVL eases the wire routing and packaging of integrated circuits [3] and reduces the huge area and power dissipation overheads related to the interconnects in ultrahigh density field programmable gate arrays (FPGAs) and system on chips (SOCs) [4], [5]. To meet the increasing demands for operating speed and information density, there is a requirement to shift the design paradigm beyond binary logic systems in near future [6]. MVL has emerged as an alternative to binary logic systems for implementation of very high-density logic and information system having higher speed of operation, significantly lesser computational stages and reduced chip area [7]. MVL is also being used extensively for design of various arithmetic and logical applications. MVL circuits utilize more than two levels of logic to carry out the computation. Thus, MVL can be categorized as ternary (base = 3) or quaternary (base = 4) logic system depending on the number of logic levels [8].

Taking into account the issues related to hardware implementation, ternary logic systems with radix of three is the most effective implementation of MVL systems [9]. However, the MVL systems are more susceptible to noise and crosstalk effects [10]. The ternary logic systems were first reported in 1840 by Thomas Fowler [11] of English origin. In 1950's two Russian inventors namely Sergei Sobolev and Nikolay Brusentsov developed a computing machine called "SETUN" [12] based on ternary number logic. Ternary numbers have two main representations [13], first representation is the balanced representation, where ternary numbers are represented by -1, 0 and $+1$ voltage levels. The other representation is called the unbalanced representation which uses 0, 1 and 2 instead. Ternary systems owing to its superior properties have been employed for enhancing computational performance in areas related to fuzzy logic [14], cryptographic systems [15] and artificial intelligence [16]. Ternary logic gates were first implemented based on complementary metal oxide semiconductor (CMOS) logic in 1980's however due to the high sensitivity of logic systems to CMOS transistor dimensions, arithmetic logic design utilizing MVL has faced significant challenges in terms of high leakage power, reduced gate control, parameter variation and short channel effect [17]. To seek improvement in MVL circuit designs various emerging technologies such as Carbon Nanotube Field Effect Transistors (CNTFET) [18], Quantum Dot Cellular Automata (QCA) [19], and Single Electron Transistor (SET) [20] have been introduced. However, amongst these technologies, CNTFET has emerged as the standout technologies for the implementation of MVL based designs. Carbon nanotubes (CNTs) are rolled graphene sheets having a cylindrical structure. Researchers have implemented ternary logic gates based on CNTFET's [21] as CNTFET's are very similar to Metal Oxide Semiconductor Field Effect (MOSFET) devices used in Complementary Metal Oxide Semiconductor (CMOS) logic and thus considered as an alternative to MOSFET's. This makes it easier to transfer the MVL based designs from CMOS to CNTFET. Moreover, the properties of CNTFET's are entirely controlled by the diameter of CNT's which can be changed easily. In addition, the ballistic transport of charge carriers in the channel of CNTFET results in the lesser power consumption as well as the propagation delay [22], [23]. CNTs are categorised as single-walled CNT (SWCNT) and multi-walled CNT (MWCNT), however for implementing ternary logic gates SWCNT is preferred owing to its simpler manufacturing process. SWCNT can act as either a conductor or a semiconductor by changing the angle at which the atoms are arranged along the length of the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m). The diameter of the CNT can be calculated based on the following equation [24]:

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{1}$$

where $a_0 = 0.142$ nm is the interatomic distance between each carbon atom and its neighbour and D_{CNT} is the diameter of the CNT.

The threshold voltage of CNTFET is dependent on diameter of the CNT and is expressed as [24]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a}{e}\frac{V_\pi}{D_{CNT}} \approx \frac{0.436}{D_{CNT}} \tag{2}$$

where E_g is the bandgap, e represents the electron charge, a = 2.49 Å is the atom distance between the carbon atoms, $V_\pi = 3.033$ eV is the carbon π-π bond energy in the tight bonding model.

For realization of ternary logic systems another suitable technology is Resistive Random Access Memory (RRAM) due to its ability to handle multiple resistance states without the need for complex additional circuitry. RRAM consists of a metal insulator metal (MIM) structure and its operation is based on the resistance change upon the application of external electrical inputs to store information in the binary form "0" and "1" [25], [26]. The recent advances in RRAM technology have demonstrated fast switching (about 300ps), excellent miniaturization potential down to 10 nm, low energy operation (about 0.1 pJ), high endurance ($> 10^{12}$ switching cycles) and high CMOS compatibility [27]. RRAM has a simple two terminal metal-insulator-metal (MIM) structure, and its operation depends upon its ability to switch between two resistance states categorised as low resistance state (LRS) and high resistance state (HRS). If a device is in LRS, the RRAM is said to be in the SET or ON state. On the other hand, HRS specifies RRAM to be in the RESET or OFF state. This switching of the resistance states ensures the data bit is stored in the RRAM device. Although,

a number of approaches to explain the switching mechanism of RRAM devices have been proposed but the most widely accepted switching mechanism for RRAM devices is the formation and rupture of conductive filaments caused by drift of oxygen ions/vacancies. Two terminal RRAM devices are used to configure logic circuits such as logic gates in digital systems including field-programmable gate arrays [28] due to their excellent properties such as non-volatility, large on/off ratio, low ON-resistance and excellent scalability. The basic binary logic gates with nanowire RRAM devices have already been proposed [29]. The non-volatility of RRAM device enables low power consumption, non-volatile on-chip data storage, high capacity and simple to fabricate logic circuits. These properties make RRAM highly suitable for use in the design of MVL circuits. Although implementation of RRAM based binary logic gates has been proposed earlier, the design of ternary logic systems utilising RRAM is still in its early stages. Therefore, utilising RRAM for implementing ternary logic functions opens a new domain of opportunities in the design of digital systems.

Ternary logic design utilising CNTFET technology and employing resistive load has been proposed previously [30]. However due to the current requirement of CNTFET's it requires large OFF-chip resistors. In this paper, we present a novel CNTFET-RRAM based design technique which employs active load P-type CNTFET and RRAM for designing ternary gates thus eliminating requirement of large resistors. The main objective of this article is to propose the design of CNTFET-RRAM based ternary logic circuits which have significant advantages in terms of component count, chip area, power consumption, energy consumption, and dense fabrication. In addition, we investigate the effect of variation of process parameters, operating temperature, and output load on power consumption and energy consumption of the proposed designs. The designs of basic ternary gates (Inverter, NAND and NOR) are presented in detail and the ternary half adder, ternary half subtractor and ternary multiplier circuits are simulated and presented as examples of the application of the proposed design technique. To validate the operational performance by performing SPICE simulations, we utilize Stanford University CNTFET model [31] for CNTFET and for RRAM we make use of Stanford University RRAM Model [32].

The paper is organised as follows: Section 2 presents a brief overview of ternary logic systems. A discussion on the proposed CNTFET-RRAM based ternary logic gates in presented in section 3. Section 4 discusses the implementation of basic ternary arithmetic circuits designed using the proposed ternary logic gates. Simulation results and comparative analysis of the proposed ternary designs with the existing designs are presented in Section 5. Finally, in the last section conclusion of the manuscript is presented.

II. TERNARY LOGIC GATES

In a conventional binary system, we have two logical values '0' and '1', which are represented by 0V and V_{dd} respectively. In a ternary logic system, logical values are '0', '1' and '2', which are represented by 0V, $\frac{V_{dd}}{2}$, and V_{dd}, respectively. In MVL systems, the numbers can be represented in either the balanced or the unbalanced mode. However, due to difficulties in implementation of negative voltages, the balanced mode is rarely used for design of ternary logic systems. In this work, focus will be on unbalanced ternary logic representation.

A. TERNARY INVERTER

A ternary inverter in general terms is referred to as a logic gate, having single possible input and three output combinations. In literature, we have three types of ternary inverters: standard ternary inverter (STI), positive ternary inverter (PTI) and negative ternary inverter (NTI). For STI, input and the output have three possible voltage levels describing ternary numbers. For both PTI and NTI, on the other hand the output takes only two voltage levels. The mathematical equations of STI, PTI and NTI [33] are presented in Eq. 3.

$$\begin{aligned} y_0 &= f_0(x) = 2 - x \\ y_1 &= f_1(x) = \begin{cases} 2, & \text{if } x \neq 2 \\ 0, & \text{if } x = 2 \end{cases} \\ y_2 &= f_2(x) = \begin{cases} 2, & \text{if } x = 0 \\ 0, & \text{if } x \neq 0 \end{cases} \end{aligned} \tag{3}$$

The truth table of the ternary inverters in the unbalanced representation is shown in Table 1. Although STI, PTI and NTI logic gates have similar circuit designs, the variation of their behaviour is due to the transistor dimensions. The behaviour of ternary inverters is explained in detail in [34], [35]. The symbols of STI, PTI and NTI circuits are depicted in Fig. 1.

TABLE 1. Truth Table of STI, PTI, NTI.

INPUT	STI(y_0)	PTI(y_1)	NTI(y_2)
0	2	2	2
1	1	2	0
2	0	0	0

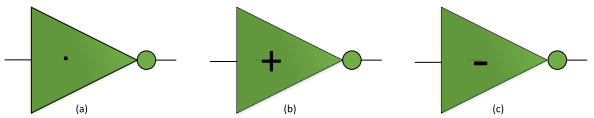

FIGURE 1. Symbols of a) STI b) PTI c) NTI.

B. TERNARY NAND AND NOR

The ternary NAND and the ternary NOR functions for two inputs X_1 and X_2 are represented by the following pair of

TABLE 2. Truth Table of ternary NAND and NOR.

INPUT X_1	INPUT X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

equations [36]:

$$Y_{NAND} = \overline{min\{X_1, X_2\}} \tag{4}$$

$$Y_{NOR} = \overline{max\{X_1, X_2\}} \tag{5}$$

The symbols of the ternary NAND and ternary NOR gates are depicted in Fig. 2.

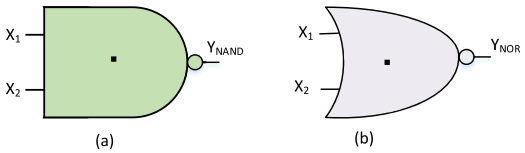

FIGURE 2. Ternary NAND and NOR gates a) Symbol of ternary NAND and b) Symbol of ternary NOR.

III. PROPOSED CNTFET-RRAM BASED TERNARY LOGIC GATES

The proposed ternary logic gate design eliminates the need of large resistors in the existing design by replacing them with active load p-type CNTFETs and RRAM devices. In RRAM, the resistance of the device changes based on the application of the voltage. We utilize this property of RRAM for design of ternary inverter. The benefits of utilizing the resistive behaviour of p-type CNTFET and RRAM are the reduction in component count and minimised area overheads of ternary logic gates. The logic voltage levels for the proposed designs are 0V for logic '0', 0.45 V ($\frac{V_{dd}}{2}$) for logic '1', and 0.9 V (V_{dd}) for logic '2'.

A. CNTFET-RRAM TERNARY INVERTER

The conventional STI schematic in CMOS technology [37] is depicted in Fig. 3 (a). The design consists of two MOS transistors (M_1, M_2) and two resistors (R_1 and R_2). When input applied is 0 (-V_{CC}), the transistor M_2 turns ON while the transistor M_1 is turned OFF. Thus, there is no current flow and output obtained is logic 2 (+V_{CC}). For the case of input being logic 2 (+V_{CC}) M_2 turns OFF while M_1 is turned ON.

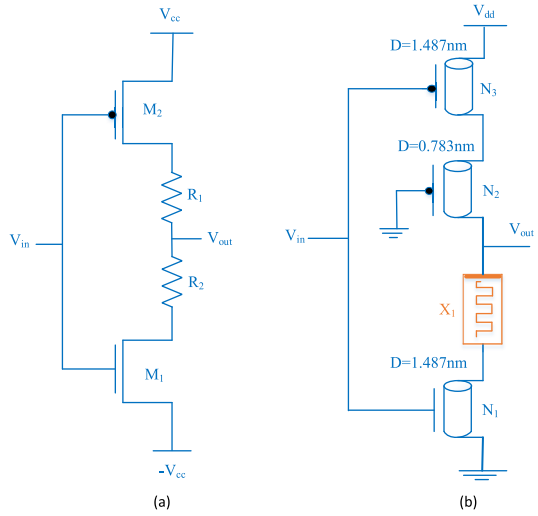

FIGURE 3. a) Existing CMOS standard ternary inverter [37] b) CNTFET-RRAM based ternary inverter.

The output in this case goes down to logic 0 (-V_{CC}) as no current flows through resistors. For logic 1 (0 V) input both the transistors M_1 and M_2 are turned ON, the current flows through both the resistors and due to the large value of the resistors used in the design, the STI output shifts to logic 1.

To eliminate use of resistors, CNTFET-RRAM based ternary inverter design is proposed and its schematic is depicted in Fig. 3 (b). The schematic consists of two CNTFETs (N_1 and N_3) instead of two MOS transistors and the resistors are replaced by grounded-gate p-type CNTFET (N_2) and RRAM device (X_1). The chirality's of the CNTs used in N_1, N_2, and N_3 are (19, 0), (10, 0), and (19, 0) respectively. From eq. (1), the diameters of N_1, N_2, and N_3 are 1.487 nm, 0.783 nm, and 1.487 nm, respectively. Therefore, from eq. (2) threshold voltages of N_1, N_2, and N_3 are 0.293 V, −0.557 V, and −0.293V, respectively. For N_1 and N_3, the tube number is 3 while for N_2 tube number 1 is used for the design. For RRAM device "X_1", the oxide thickness t_{ox} is 12nm, the minimum gap distance (g_{min}) and the maximum gap distance (g_{max}) between the electrodes is 0.2nm and 1.8nm respectively at initial device temperature of 298K and the activation energy for vacancy generation (E_a) is 0.6eV. Moreover, the RRAM device is well capable of handling the input voltages in the range of 0-0.9V used in our design. It is worth mentioning here that we utilize the chirality of the CNTFET and the multibit capacity or multilevel cell (MLC) operation of RRAM for realization of our ternary designs. The CNTFET chirality controls the threshold voltage wherein the MLC capability of RRAM helps in modulating the resistance states with distinguishable resistance ratios for realising the ternary nature of the proposed designs. The change in resistance across the RRAM device due to the variation in the voltage or the current is attributed to modulation of the diameter of the conductive filament (CF) between the top electrode and the bottom electrode of the RRAM.

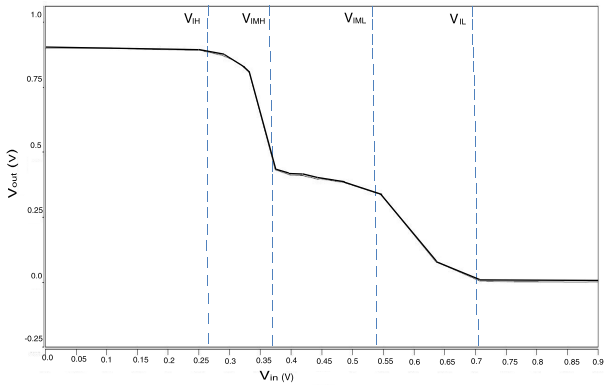

FIGURE 4. Voltage Transfer Characteristics (VTC) of proposed STI.

Initially, for 0V (i.e. logic 0) input voltage, N_1 turns OFF and N_3 is turned ON. As the gate of the P-type CNTFET N_2 is connected directly to the ground it is turned ON, while the RRAM (X_1) in this case is in the high impedance state. Therefore, the output voltage in this case is V_{dd} i.e. 0.9V (logic 2). When the input voltage is changed to $\frac{V_{dd}}{2}$ (i.e. logic 1), both the CNTFETs N_1 and N_3 are turned ON. Also, N_2 is in the ON state, while X_1 is now in the low impedance state. The current flows through the device, while N_2 and X_1 act as equal resistors producing a voltage drop of $\frac{V_{dd}}{2}$. Therefore, the output voltage obtained in this case is $\frac{V_{dd}}{2}$ (i.e. logic 1). Similarly, when the input voltage is changed to 0.9V (i.e. logic 2), N_1 turns ON and N_3 is turned OFF. As a result, the output voltage obtained in this case is 0V (i.e. logic 0). To evaluate the functionality, the voltage transfer characteristics (VTC) for the proposed STI design with supply voltage of 0.9V is simulated and depicted in Fig. 4. The VTC clearly demonstrates the ternary nature of the propsed CNTFET-RRAM based STI.

A very important aspect in design of digital circuits is the noise margin. To ensure full compatibility between the devices, the values of noise margin are carefully specified by the producers. The noise margin for the STI is determined from the VTC curve and the four noise margins (NM_H, NM_{MH}, NM_{ML}, NM_L) are defined at four voltage points (V_{IH}, V_{IMH}, V_{IML}, V_{IL}). The static noise margin (SNM) of the STI is the smallest one among the four noise margins (NM_H, NM_{MH}, NM_{ML}, NM_L). The noise margin values of the proposed and the existing STI circuit are presented in Table 3. Fig. 5 shows the comparison of the voltage transfer characteristic (VTC) curve of STI gate with all CNTFETs, resistive load design and the proposed CNTFET-RRAM based STI design. This curve indicates that the VTC response of the proposed STI is very close to that of the ideal STI.

B. CNTFET-RRAM TERNARY NAND AND NOR

The schematic of CNTFET-RRAM ternary NAND and ternary NOR logic gates are shown in Fig. 6 (a) and (b) respectively.

Both of the logic gates consist of five CNTFETs with two different chirality's. The design of CNTFET-RRAM ternary NAND and NOR gates is identical to existing binary CMOS counterparts except for the transistors of different threshold voltages and different resistive elements. Similar to CNTFET-RRAM based ternary inverter chirality of the

TABLE 3. Noise analysis of STI design.

Parameter	Mahmood et.al [6]	Proposed STI Design
NM_H (mV)	159	170
NM_{MH} (mV)	140	100
NM_{ML} (mV)	141	120
NM_L (mV)	154	150
SNM (mV)	140	100

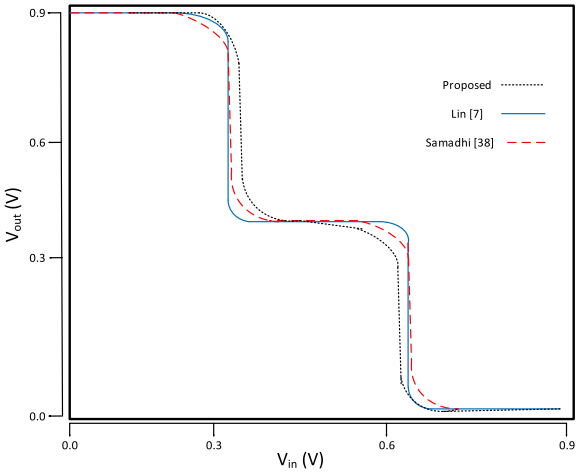

FIGURE 5. Voltage Transfer Characteristics (VTC) related to STI gates with all CNTFETs, resistor load and proposed design.

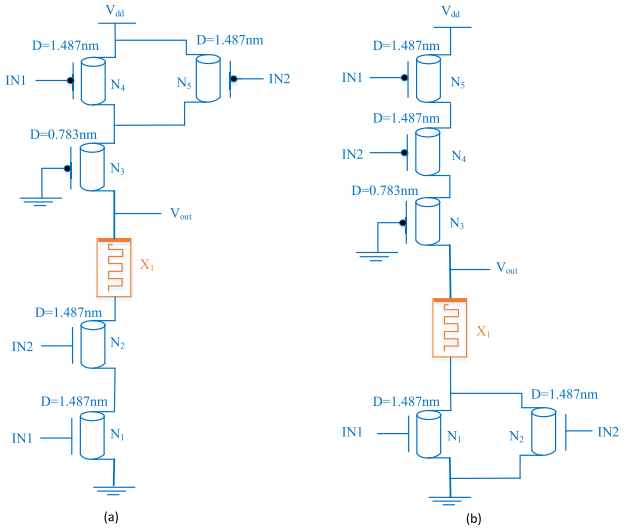

FIGURE 6. Proposed designs for ternary NAND and NOR a) CNTFET-RRAM ternary NAND b) CNTFET-RRAM ternary NOR.

CNTs used in N_1, N_2, N_4, N_5 are (19, 0) while the chirality of CNT used in N_3 is (10, 0) for both the ternary logic gates. The CNTFETs with diameters 1.487 nm and 0.783 nm have threshold voltages of 0.293 V and 0.557 V respectively. For N_1, N_2, N_4, N_5 the tube number is 3 while for N_3 the tube number used is 1. For RRAM (X_1), the parameter values remain the same as used previously in the design of STI. The correctness of the design was confirmed by simulation with HSPICE tool and verifying the obtained results with Table 2.

IV. CNTFET-RRAM TERNARY ARITHMETIC CIRCUITS

The CNTFET-RRAM ternary logic gates can be used as building blocks for constructing various basic ternary arithmetic circuits. The simplest examples that we elaborate in this section are that of the ternary half adder, ternary half subtractor and ternary multiplier circuits. To implement all of these ternary arithmetic circuits, first we need a ternary decoder circuit, the schematic of which is shown in Fig. 7. The ternary decoder is combinational circuit with single input and three outputs. For ternary decoder, the response to excitation 'X' is [38]:

$$X_p = \begin{cases} 2, & \text{if } X = p \\ 0, & \text{if } X \neq p \end{cases} \tag{6}$$

where p takes either one of the logic values 0, 1, or 2. As seen in Fig. 7, the ternary decoder consists of two NTI gates, a PTI gate, and a ternary NOR gate.

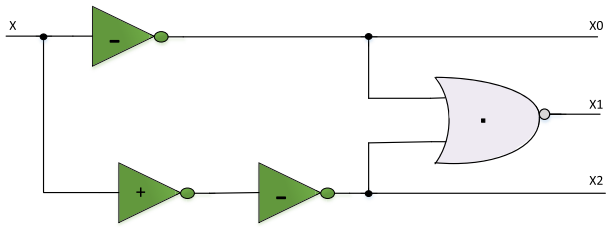

FIGURE 7. Schematic of ternary decoder [38].

In a ternary logic system, each signal can have three different values, therefore the number of digits required in ternary systems is log_3 2 times less than that required in binary logic. To verify the authenticity of the proposed CNTFET-RRAM ternary logic gates, ternary half adder (HA), ternary half subtractor (HS) and ternary multiplier circuits are then simulated using these logic gates. Similar to binary half adder, ternary half adder has two outputs: Sum and Carry. However, the Sum and the Carry outputs take three possible logic values in ternary half adder compared to only two logic levels in binary design. Table 4 represents the truth table of the ternary half adder. Making use of Karnaugh Map, the output equations of HA can be derived from Table 4 and can be acquired as [38]:

$$SUM = A_2B_0 + A_1B_1 + A_0B_2 + 1 \cdot (A_1B_0 + A_0B_1 + A_2B_2) \tag{7}$$

$$CARRY = 1 \cdot (A_2B_1 + A_2B_2 + A_1B_2) \tag{8}$$

TABLE 4. Truth Table of ternary half adder.

INPUT A	INPUT B	SUM	CARRY
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

where A_p and B_p represent the output to A and B inputs from the decoder shown in Fig. 7.

The schematic of ternary half adder proposed in [38] is depicted in Fig. 8. We make use of CNTFET-RRAM based ternary logic gates designed in the previous section to validate the authenticity of our proposed circuits. In this case, the output signal for the inputs A and B are generated by the two decoders (decoder A and decoder B) while to compute the sum and carry functions defined in eq. 7 and eq. 8, ternary logic gates are used.

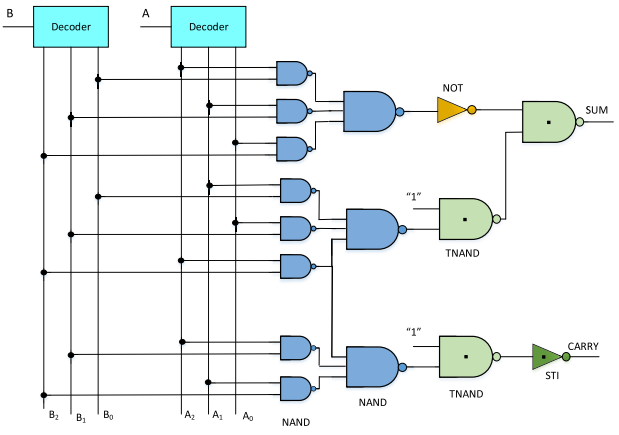

FIGURE 8. Schematic of ternary half adder [38].

Similarly, we utilise the proposed CNTFET-RRAM based ternary logic gates to implement the ternary half subtractor circuit with all possible input and output combinations depicted in Table 5. A ternary half subtractor shown in Fig. 9 is a combinational logic circuit that subtracts one bit from the other and generates two outputs difference and borrow with output equations given by [40]:

$$DIFF = A_0B_1 + A_1B_2 + A_2B_0 + 1 \cdot (A_1B_0 + A_2B_1 + A_0B_2) \tag{9}$$

$$BORROW = 1 \cdot (A_0B_1 + A_0B_2 + A_1B_2) \tag{10}$$

TABLE 5. Truth Table of ternary half subtractor.

INPUT A	INPUT B	DIFF	BORROW
0	0	0	0
0	1	2	1
0	2	1	1
1	0	1	0
1	1	0	0
1	2	2	1
2	0	2	0
2	1	1	0
2	2	0	0

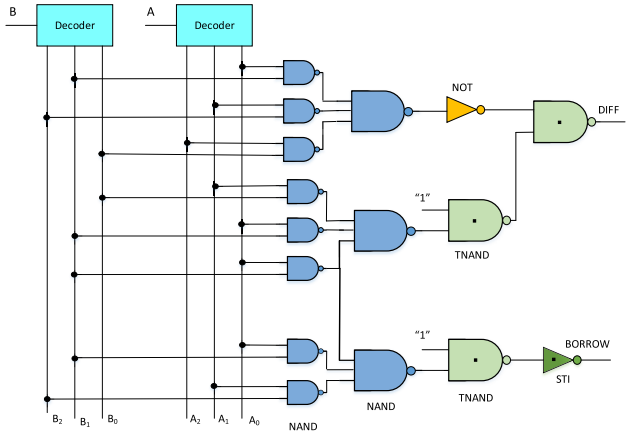

FIGURE 9. Schematic of ternary half subtractor.

where A_p and B_p represent the output to A and B inputs from the decoder shown in Fig. 7.

In both the ternary half adder and half subtractor circuits, the schematic consists of the two proposed ternary decoders, eight 2-inputs binary NAND, three 3-inputs binary NAND, one binary inverter, three proposed TNAND and one proposed STI. The component count including transistors and RRAM of the ternary half adder and the ternary half subtractor circuits is shown in Table 6.

Lastly, for the case of proposed ternary multiplier, we have the product and the carry output. Table 7 represents the truth table of the ternary multiplier. The output equations of ternary multiplier can be derived from Table 7 making use of Karnaugh Map as [38]:

$$Product = A_2B_1 + A_1B_2 + 1\cdot(A_1B_1 + A_2B_2) \quad (11)$$

$$CARRY = 1 \cdot (A_2B_2) \quad (12)$$

where A_p and B_p represent the output to A and B inputs from the decoder shown in Fig. 7. Fig. 10 depicts the schematic of

TABLE 6. Component count of the proposed Ternary Half Adder (THA) and Ternary Half Subtractor (THS).

Design	No. of Devices	No. of Transistors	Sub Total*	No. of RRAM
Proposed TDecoder	2	10	20	2
Binary 2-NAND	8	4	32	-
Binary 3-NAND	3	6	18	-
Binary NOT	1	2	2	-
Proposed TNAND	3	5	15	3
Proposed STI	1	3	3	1
Total			**90 Transistors**	**6**

*Sub Total= No. of Devices x No. of Transistors

TABLE 7. Truth Table of ternary multiplier.

INPUT A	INPUT B	PRODUCT	CARRY
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

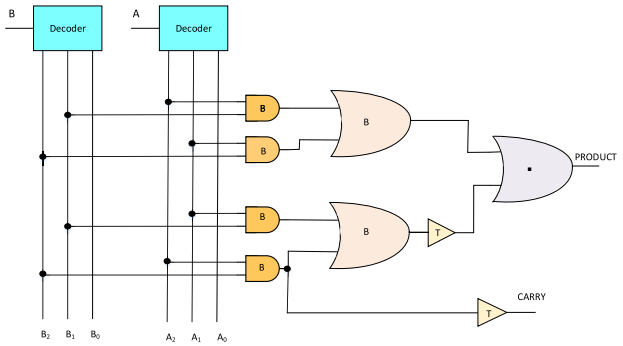

FIGURE 10. Schematic of ternary multiplier [38].

ternary multiplier proposed in [38]. Unlike ternary half adder and ternary half subtractor which were implemented using only ternary logic gates, the ternary multiplier utilises both the binary and the ternary logic gates.

In Fig. 10, T buffer represents a level shifter with logic function as [38]:

$$Out = \begin{cases} 1, & \text{if in} = 1, 2 \\ 0, & \text{if in} = 0 \end{cases} \quad (13)$$

T buffer is basically implemented by utilizing two input ternary NAND gate with one of the inputs of the NAND gate always maintained at logic '1' $\left(\text{i.e. } \frac{V_{dd}}{2}\right)$ voltage level. We utilize the proposed CNTFET-RRAM TNAND for the implementation of the T buffer circuit.

The schematic of ternary multiplier circuit consists of of the two proposed ternary decoders, four 2-inputs binary NAND, two 2-inputs binary OR, one proposed TOR, and three proposed TNAND. The component count of the ternary multiplier is shown in Table 8.

TABLE 8. Component count of the proposed Ternary Multiplier (TM).

Design	No. of Devices	No. of Transistors	Sub Total*	No. of RRAM
Proposed TDecoder	2	10	20	2
Binary 2-NAND	4	4	16	-
Binary 2-OR	2	4	8	-
Proposed TOR	1	8	8	2
T Buffer as proposed TNAND	2	5	10	2
Total			**62 Transistors**	**6**

*Sub Total= No. of Devices x No. of Transistors

V. RESULTS AND DISCUSSION

The circuit simulation of the proposed ternary logic circuits (STI, NAND, NOR, half adder, half subtractor and multiplier) has been done by means of HSPICE software. All the ternary designs have been simulated considering 32-nanometer technology node, and 0.9V power supply voltage at room temperature. To test the operational performance of the ternary designs Stanford University CNTFET model [31] is employed. The Stanford University CNTFET model is a spice compatible compact model describing unipolar MOSFETs with semiconducting single-walled carbon nanotubes as channels. Each device may have one or more carbon nanotubes with user-specified chirality and effects of channel length scaling can be accurately modelled down to 20nm. The parameters of the CNTFET model and their values, with brief description are listed in Table 9. For RRAM, Stanford University RRAM model [32] is employed. Similar to CNTFET model, Stanford University RRAM model is a physics based spice compatible model describing the switching performance of RRAM, with no limitations on the size of the RRAM cell. This model is based on the growth of conductive filament (CF) and includes the effect of critical phenomenon of switching such as Joule heating and temperature change. The CF leaves a gap with the top electrode which is called the filament gap. Thus, the rate of filament growth and filament gap govern the dynamics of this model. This model also takes into account, the effect of electric field as well as the stochastic and temperature dependent filament movement. A brief description of RRAM parameters is presented in Table 10. RRAM devices are CMOS-compatible and can be fabricated with the existing state-of-the-art technology without the need of special equipment and materials. CNTFETs can be built using the traditional silicon-chip fabrication, thus making our designs practically more feasible.

The value of input voltages used for the designs are 0V, 0.45V and 0.9V representing logic levels '0', '1' and '2' respectively. The applied input voltage vector and the corresponding output obtained for the CNTFET-RRAM ternary inverter are shown in Fig. 11. The applied input voltage vector and the corresponding output obtained for the CNTFET-RRAM ternary inverter are depicted clearly. The proposed ternary inverter works in a similar manner to that of the binary inverter for case of inputs being logic 0 and logic 2 levels. In the case of input being logic 1, both the transistors N_1 and N_2 turn on along with the X_1 and N_3 resulting in $\frac{V_{dd}}{2}$ voltage (logic 2) at the output. The simulation results of the proposed ternary NAND and NOR logic gates are depicted in Fig. 12. The applied input signals INPUT A and INPUT B are shown in Fig. 12 (a) and (b). Fig. 12 (c) shows the obtained output logic levels for ternary NAND while the output logic levels for ternary NOR gate are shown in Fig. 12 (d). The obtained output logic levels for ternary NOT, ternary NAND

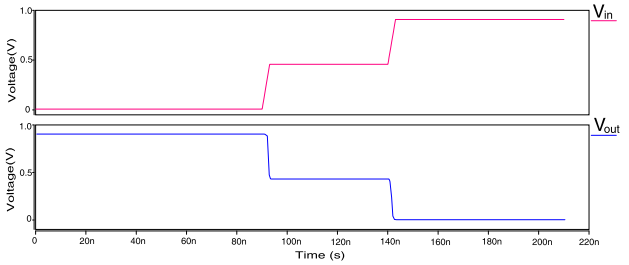

FIGURE 11. Input and output voltages of proposed STI.

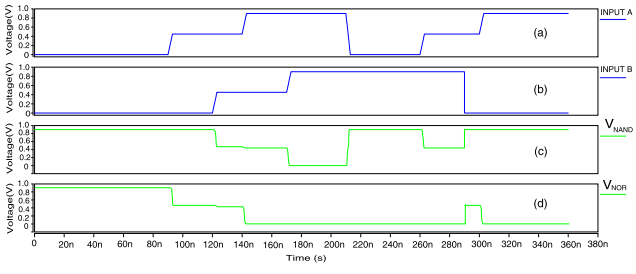

FIGURE 12. (a) Input vector A (b) Input vector B (c) ternary NAND output (d) ternary NOR output.

TABLE 9. Stanford University CNTFET model characteristic parameters.

CNTFET Parameter	Parameter Specification	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
EFI	The Fermi level of the doped S/D tube	6 ev
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m

TABLE 10. Stanford University RRAM model characteristic parameters.

Parameter	Parameter Description	Value
T_ini	Initial Device Temperature	298 K
F_min	Minimum field to enhance gap formation	1.4e9 V/m
t_{ox}	Oxide thickness	12 nm
gap_ini	Initial gap distance	1.8 nm
gap_min	minimum gap distance	0.2 nm
gap_max	maximum gap distance	1.8 nm
E_a	Activation energy for vacancy generation	0.6 eV

and ternary NOR gates are in accordance with their truth tables, therefore verifying the correctness of our proposed ternary logic logic designs.

To validate our ternary logic gate designs, we evaluate the results of the ternary half adder circuit designed using our proposed logic gates. Although, a number of designs for implementing ternary half adder have been proposed we choose the one proposed in [38] for the sake of simplicity. The schematic of the design is shown in Fig. 8 and makes use of two ternary decoders having input signals 'A' and 'B' shown in Fig. 13 (a) and (b), which are decoded to three signals labelled A_0, A_1, A_2 and B_0, B_1 and B_2 respectively. These signals are activated depending upon the logic levels "0", "1" and "2" respectively. The Sum and the Carry outputs of the ternary half adder are then obtained using these signals and are shown in Fig. 13 (c) and (d) respectively. The simulated output voltage levels for the Sum and the Carry outputs are in accordance with the truth table of the ternary half adder.

Similarly, for the case of ternary half subtractor circuit the inputs A and B are shown in Fig. 14 (a) and (b), while the Diff and the Borrow outputs are shown in Fig. 14 (c) and (d)

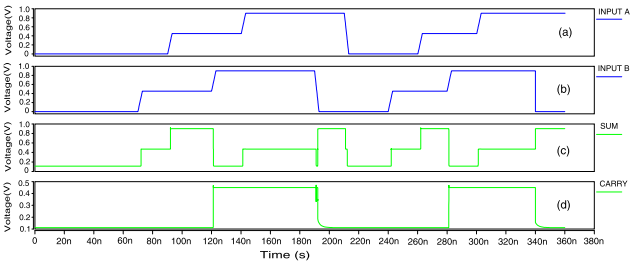

FIGURE 13. (a) Input vector A (b) Input vector B (c) ternary SUM output (d) ternary Carry output.

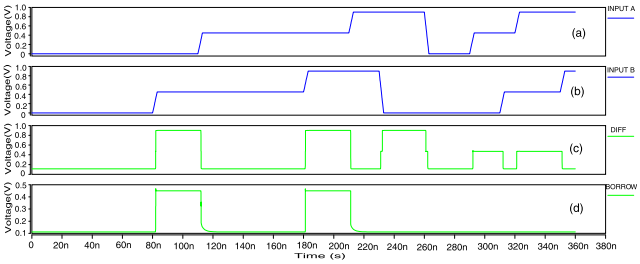

FIGURE 14. (a) Input vector A (b) Input vector B (c) ternary DIFF output (d) ternary BORROW output.

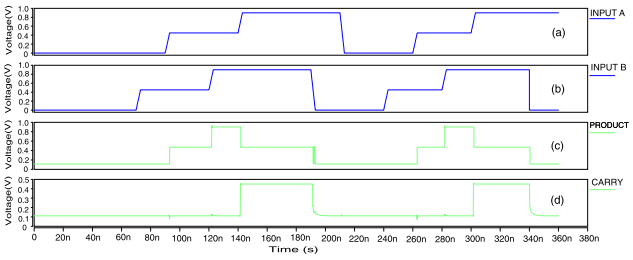

FIGURE 15. (a) Input vector A (b) Input vector B (c) ternary product output (d) ternary carry output.

respectively. The simulated results for the ternary half subtractor are in accordance with the truth table 5. Lastly, the inputs A and B to the ternary multiplier are shown in in Fig. 15 (a) and (b), while the Product and the Carry

outputs are presented in Fig. 15 (c) and (d) respectively. The simulated results for the ternary multiplier are in accordance with the truth table 7.

CNTFET-RRAM based STI, NAND and NOR gates helps minimize the chip area as proposed ternary gates contain lesser number of transistors in comparison to designs previously present in the literature as is depicted in Table 11. The minimization of transistor count is not the only factor that affects the performance of the proposed circuits, but it is an important metric considering the design of digital systems. The transistor count comparison for the proposed STI, TNAND and TNOR with various existing designs demonstrates a notable reduction in the number of transistors. For STI, around 50% reduction in number of transistors is observed compared to STI in [7], [34], [38]–[40] and around 40% compared to STI in [44]. For TNAND, around 50% compared to [7], [34], [38], [40], [44] and around 37.5% compared to [39] is observed. For the case of TNOR, around 50% compared to [7], [34], [38], [40] and around 37.5% compared to [39]. Similarly, for the case of ternary arithmetic circuits the comparison of transistor count is shown in Table 12. The THA implemented using the proposed CNTFET-RRAM ternary logic gates shows a notable reduction in transistor count. Around 33.82%, 19.64%, 65.11%, −5.55%, compared to THA in [7], [38], [40], [44] respectively, while the transistor count compared to [45] remains the same. For THS, the transistor count is reduced by around 65.11% compared to the design in [40]. Lastly for TM design, the reduction by around 38%, 18.42%, and −1.612% is observed compared to [7], [38] and [44] respectively. In addition to the reduced transistor count, the proposed ternary designs have the unique feature of non-voalatility due to the introduction of RRAM making it suitable for in-memory computing applications which is currently an emerging design field for the bio-inspired computing.

TABLE 11. Comparison of ternary logic gates on the basis of transistor count.

Ternary Design	STI	NAND	NOR
Lin et.al [7]	6	10	10
Moaiyeri et.al [34]	6	10	10
Samadi et.al [38]	6	10	10
Gopal et.al [39]	6	8	8
Sridevi et.al [40]	6	10	10
Jaber et.al [44]	5	10	-
Proposed design	**3**	**5**	**5**

TABLE 12. Comparison of ternary arithmetic circuits on the basis of transistor count.

Ternary Design	THA	THS	TM
Lin et.al [7]	136	-	100
Samadi et.al [38]	112	-	76
Sridevi et.al [40]	258	258	-
Jaber et.al [44]	85	-	61
Jaber et.al [45]	90	-	-
Proposed design	**90**	**90**	**62**

For CNTFET-RRAM ternary logic gates, the delay of all input-output transitions are measured, and the maximum value from the measurements is recorded as the propagation delay. Similarly, to measure average power consumption all the possible transitions are considered which guarantees the accurate measurements are recorded. Further to evaluate the performance of the proposed ternary designs, a very important and significant performance metric is the average energy consumption (power delay product), which is obtained by multiplying the average power consumption and the maximum delay. The results obtained from the simulation for average power consumption, worst case delay and the average energy consumption are presented in Table 13. It is evident from the Table 13, that the proposed designs outperform the other designs in terms of the power consumption and energy efficiency. The advantage of proposed CNTFET-RRAM ternary logic gates is that they have the least number of transistor count and the lowest power consumption as well the PDP among all the investigated circuits and as such are more suitable for applications in low-power electronics and embedded systems in order to save battery consumption. Similarly, the comparison of average power consumption, delay and the power delay product of the basic ternary aritmetic designs i.e half adder, half subtractor and multiplier designed utilising the proposed CNTFET-RRAM ternary logic gates is presented in Table 14.

Although ternary logic is highly attractive for design of digital systems, it is highly sensitive to process variations compared to the binary logic. Therefore, finally a set of simulations are carried out to examine the impact of process variations on the functionality of the proposed designs. In this study, we consider the effect of variation of diameter of CNTFET nanotubes and thickness of its gate oxide layer (T_{ox}) on the performance of the proposed designs. Also, the variation of filament gap distance of RRAM is considered. Due to the fact that proposed MVL designs are suitable for low power applications, therefore after evaluating the proper functionality of the proposed designs, the average power consumption and the average energy consumption parameters should be measured in the presence of the process variations. Thus, a Monte-Carlo transient analysis with reasonable number of 100 iterations per simulation is carried out with the help of HSPICE simulator. It is worth mentioning that for each iteration, the calculation is repeated up to 5 times and the largest deviation is saved as a result of that iteration.

TABLE 13. Comparison of power consumption, Delay, and power delay product for the ternary logic gates.

Design	Power Consumption (μW)	Average Delay (ns)	Power Delay Product (PDP) (aJ)
STI			
Lin et al. [7]	1.1310	0.0194	21.94
Moaiyeri et al. [34]	0.4319	0.0156	6.74
Moaiyeri et al. [35]	0.19392	0.0165	3.215
Samadi et al. [38]	0.6908	0.00098	0.68
Proposed	**0.000148**	**0.3295**	**0.049**
TNAND			
Lin et al. [7]	0.7075	0.02672	18.90
Moaiyeri et al. [34]	0.3446	0.01989	6.854
Moaiyeri et al. [35]	0.2273	0.02093	4.758
Samadi et al. [38]	0.000145	29.02	4.22
Proposed	**0.000101**	**18.182**	**1.84**
TNOR			
Lin et al. [7]	0.7359	0.02416	18.21
Moaiyeri et al. [34]	0.32401	0.0171	5.55
Moaiyeri et al. [35]	0.1889	0.0198	3.74
Samadi et al. [38]	0.000315	31.03	9.79
Proposed	**0.000275**	**0.54213**	**0.14**

TABLE 14. Comparison of power consumption, Delay, and power delay product for the basic ternary arithmetic circuits.

Design	Power Consumption (μW)	Average Delay (ns)	Power Delay Product (PDP) (aJ)
Ternary Half Adder			
Lin et al. [7]	4.01	0.11	441.1
Samadi et al. [38]	2.221	0.0999	221
Sridevi et. al. [40]	0.77	0.0052	4.1
Shahrom et al. [42]	0.17	0.016	2.7
Tabrizchi et al. [43]	1.1217	0.03871	43.4
Proposed	**0.001395**	**49.36**	**68.8**
Ternary Half Subtractor			
Sridevi et. al. [40]	0.99	0.0071	6.9
Proposed	**7.098**	**0.1569**	**1114.1**
Ternary Multiplier			
Lin et al. [7]	2.5239	0.0982	248
Samadi et al. [38]	1.462	0.08509	125
Shahrom et al. [42]	0.19	0.014	2.6
Proposed	**0.0012**	**129.4**	**158.77**

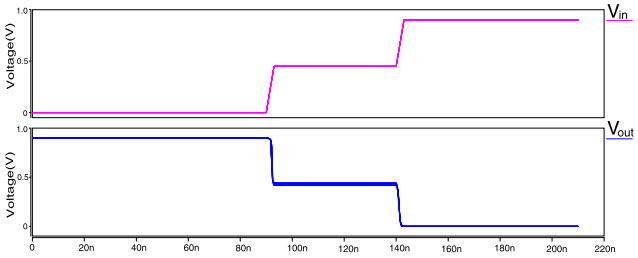

FIGURE 16. Transient response of proposed STI.

For the proposed designs we assume that the diameter and T_{ox} have Gaussian distribution with 8-sigma distribution [41]. The mean value of T_{ox} for all CNTFETs is set to 4nm, while the diameters are set to values demonstrated in Fig. 3 and Fig. 5. For each mean diameter value, a standard deviation in the range of 0.4 nm to 1.6 nm is considered due to the impreciseness of the fabrication techniques. For T_{ox}, 50% deviation from its mean value is taken into account. For RRAM, variation of the filament gap distance in the range of 0.2 to 1.8 nm is considered. The transient response of the proposed STI dcircuit is shown in Fig. 16. From the results, we can infer that a very small variation with mean value of 0.4422 V and standard deviation of 9.7005 mV in the logic '1' level of the proposed STI with the variation of the process parameters is observed. Also, the voltage transfer characteristics (VTC) curve for the proposed STI circuit obtained from the Monte Carlo analysis in the presence of process variations is depicted in Fig. 17. The VTC curve demonstrates minimum variations over 100 iterations, thus confirming the proper functionality of the proposed STI circuit, in addition to the robustness to the process variations. Next the transient response of the proposed ternary NAND and NOR logic circuits is depicted in Fig. 18. A small variation in the logic '1' level of the proposed ternay NAND with mean value of 0.44405V and standard deviation of 6.44024 mV is observed, while for the case of ternary NOR a variation with mean value of 0.44671 V and standard deviation of 4.8758 mV in logic '1' level is observed, thereby confirming the proper functionality of the proposed ternary circuits. Next we investigate the effect of variation of T_{ox} and diameter of CNTFET nanotubes on the power consumption and energy consumption (PDP) of the proposed ternary designs. The results of these variations are depicted in Fig. 19 (a), (b), (c), and (d). The proposed designs demonstrate small variations and thus the process parameter

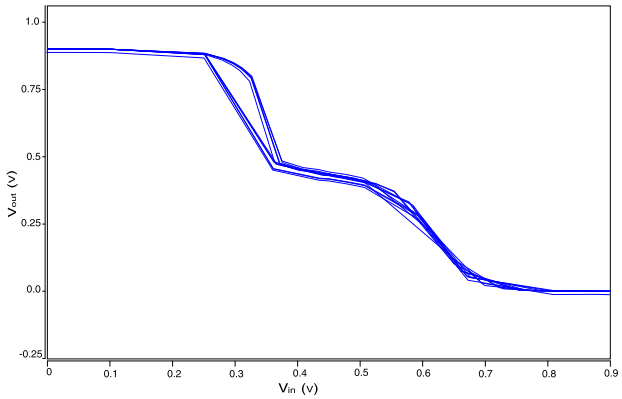

FIGURE 17. Voltage Transfer Characteristics of STI obtained from Monte Carlo Analysis.

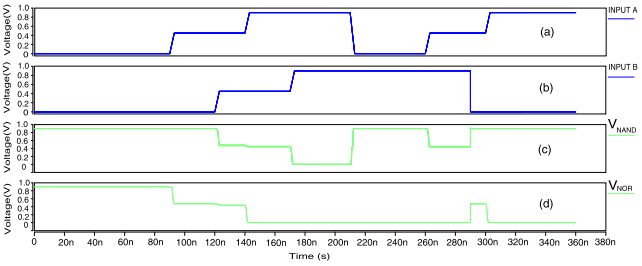

FIGURE 18. Transient response of the proposed ternary NAND and ternary NOR logic gates.

variations have very minimum effect on the functionality, power consumption and energy consumption (PDP) of the proposed ternary designs.

Temperature is one of the most critical issues which negatively affects the performance of the circuit. Therefore, this manuscript also investigates the effect of temperature on the power consumption and power delay product (PDP) of STI, ternary NAND and NOR gates and the same is depicted in Fig. 20 (a) and Fig. 20 (b) respectively. The power consumption and PDP of the ternary logic gates undergoes a very small variation over a wide range of temperature. Therefore, from these observations we infer that there is a negligible effect on circuit performance due to the change in temperature. In the previous simulations, we assumed the output load capacitor to be constant, although the values of the load capacitor may vary in actual circuits. Thus, we investigate the effect of variation of output load capacitor on the power consumption and power delay product (PDP) of the ternary logic gates. From the results depicted in Fig. 20 (c) and Fig. 20 (d), the proposed ternary designs (STI, TNAND, TNOR) show small variation in power consumption as well as the power delay product (PDP) with variation of the output load.

The performance metrics of the proposed CNTFET-RRAM ternary logic gates, with varying supply voltages is also studied. The proper operational performance over various supply voltages is required in such systems, so that they can be used in variety of applications. Fig. 21 (a) and Fig. 21 (b) demonstrates the effect of variation of supply volatge on the power consumption and power delay product of the proposed STI, ternary NAND and NOR logic gates. From the simulation results, we infer that minimum variation in performance

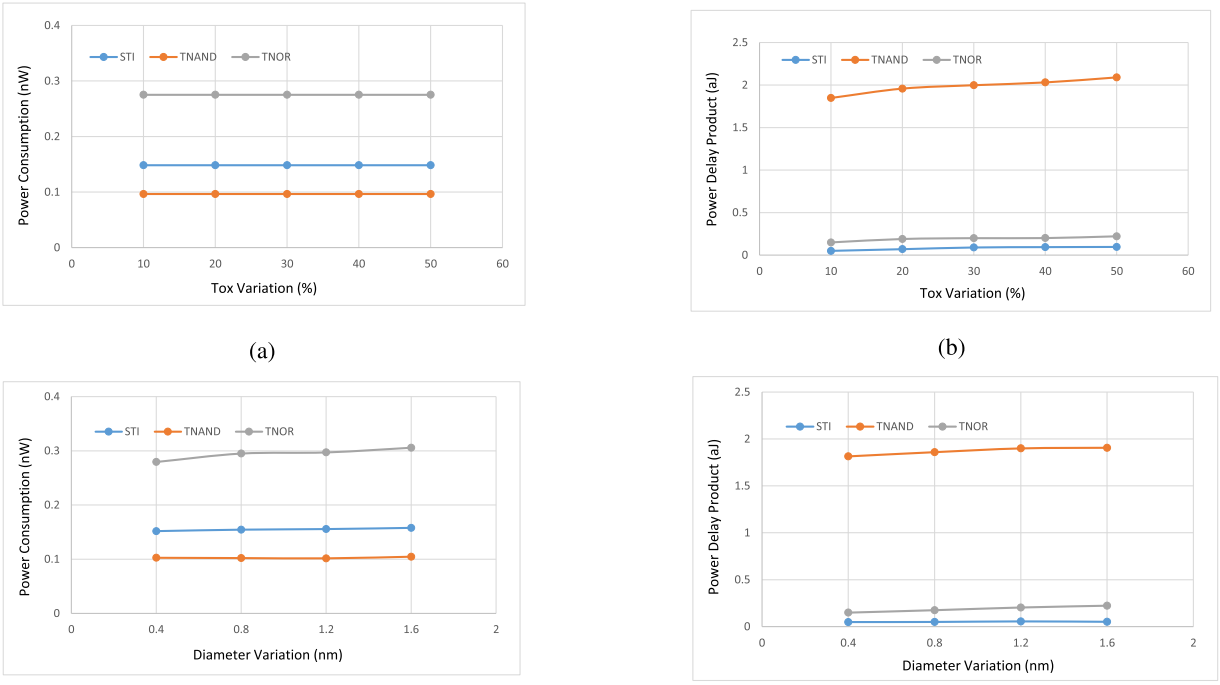

FIGURE 19. Effect of variation of process variations i.e T_{ox} Variation and Diameter Variation on power consumption and PDP of proposed ternary logic gates.

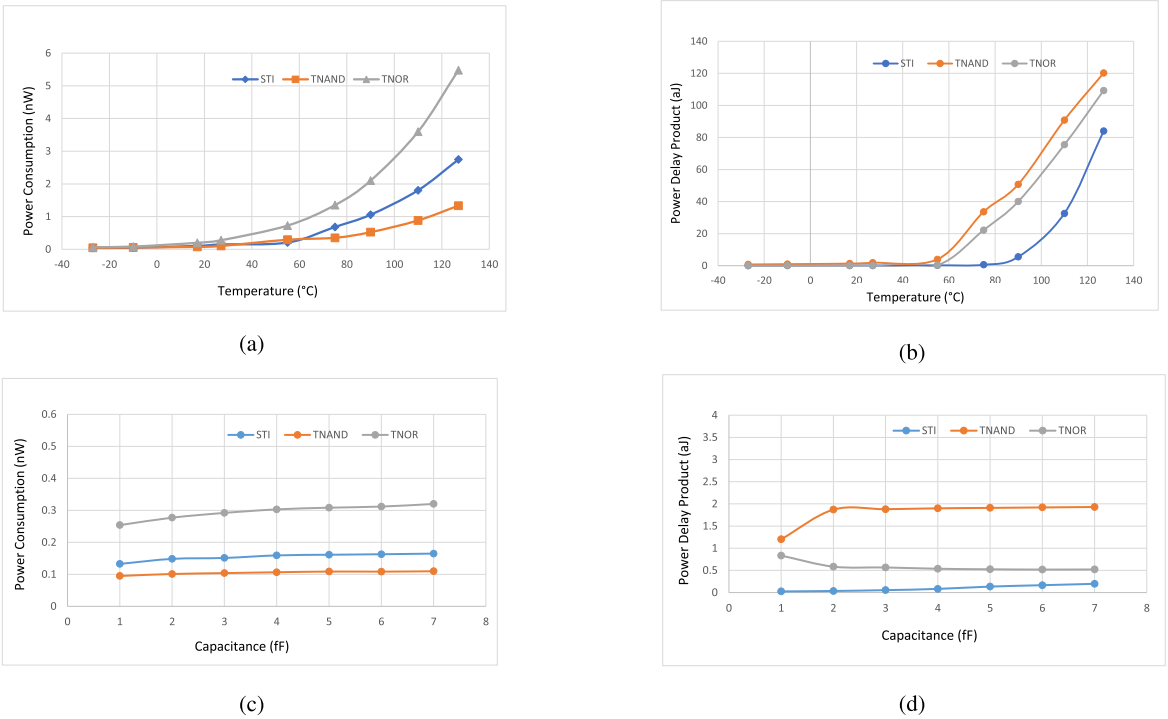

FIGURE 20. Effect of variation of temperature and variation of output load on power consumption and PDP of proposed ternary logic gates.

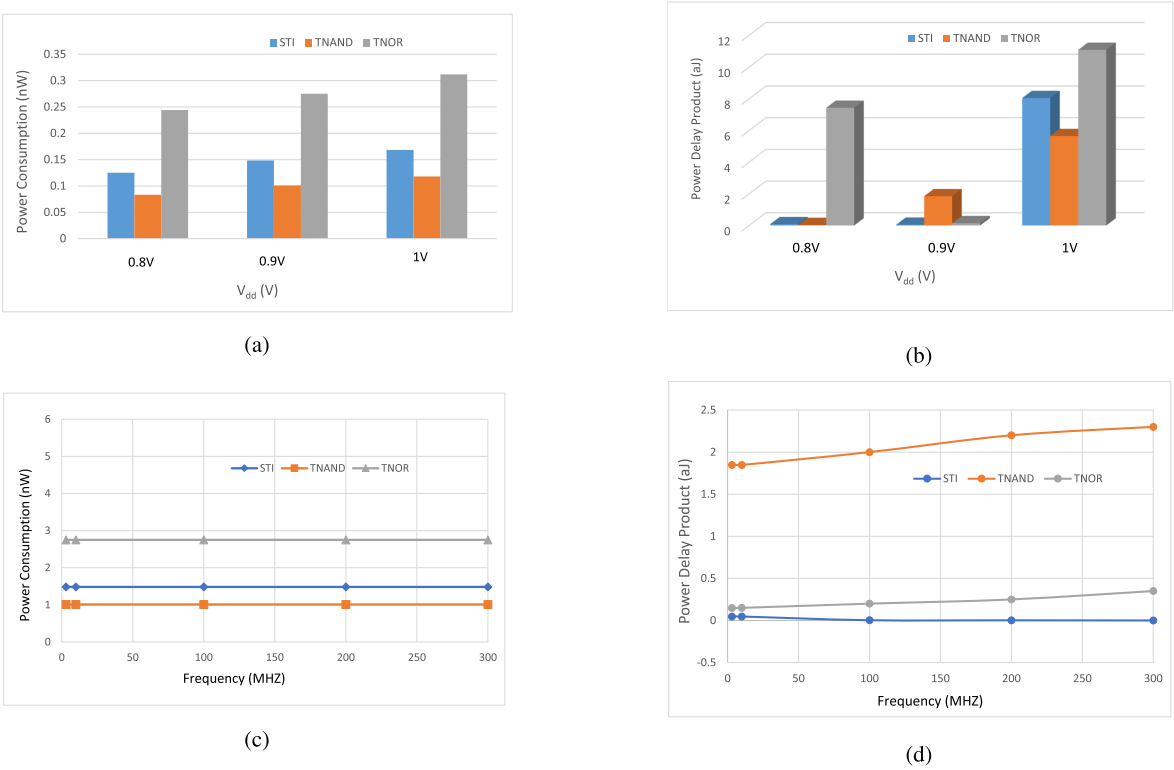

FIGURE 21. Effect of variation of supply voltage and operation frequency on power consumption and PDP of proposed ternary logic gates.

metrics of the proposed ternary logic gates with variation of supply voltage is observed. Electronic circuits behave very differently at high frequencies due to the change in behaviour of the passive components (resistors, inductors and capacitors) and parasitic effects on active components, PCB tracks and grounding patterns at high frequencies. In addition,

TABLE 15. Power consumption and PDP of STI,TNAND and TNOR in various families for varying output load capacitance C_{load}.

Capacitance	[7]	[34]	[38]	Proposed
		STI		
Power (E-6)W				
1f	3.897	0.4753	0.514	0.000148
2f	3.960	0.574	0.593	0.000148
3f	4.024	0.6635	0.6834	0.000149
4f	4.087	0.8529	0.9127	0.000149
PDP (E-15)J				
1f	0.00758	0.00174	0.0154	0.000025
2f	0.1485	0.00271	0.0356	0.000035
3f	0.2279	0.00464	0.0683	0.000054
4f	0.3101	0.00724	0.1278	0.000082
		TNAND		
POWER (E-6)W				
1f	1.210	0.2511	0.511	0.000101
2f	1.251	0.313	0.534	0.000103
3f	1.288	0.37	0.589	0.000104
4f	1.325	0.428	0.635	0.000106
PDP (E-15)J				
1f	0.0047	0.0011	0.01	0.001201
2f	0.009	0.0025	0.037	0.001870
3f	0.013	0.0044	0.058	0.001880
4f	0.018	0.0067	0.0825	0.001902
		TNOR		
Power (E-6)W				
1f	2.6691	0.5428	0.000311	0.000275
2f	2.7636	0.6581	0.00045	0.000278
3f	2.8588	0.7733	0.00056	0.000279
4f	2.952	0.8891	0.00072	0.000285
PDP (E-15)J				
1f	0.1035	0.0238	0.0096	0.000834
2f	0.1978	0.0532	0.0148	0.000584
3f	0.3001	0.0927	0.0191	0.000566
4f	0.4059	0.1418	0.0254	0.000537

TABLE 16. Power consumption and PDP of STI,TNAND and TNOR in various families for wide temperature range.

Temperature	[7]	[34]	[38]	Proposed
		STI		
Power (E-6)W				
20°C	0.3829	0.4451	0.6523	0.000102
40°C	0.3949	0.5352	0.7213	0.000148
60°C	0.403	0.6378	0.7836	0.000206
80°C	0.4111	0.7541	0.8514	0.000683
PDP (E-15)J				
20°C	0.007583	0.001015	0.000641	0.000041
40°C	0.007557	0.001308	0.000681	0.000047
60°C	0.007584	0.001532	0.000731	0.000322
80°C	0.007589	0.00178	0.000800	0.032167
		TNAND		
POWER (E-6)W				
20°C	1.1965	0.2387	0.00014	0.000072
40°C	1.2358	0.2872	0.000148	0.000101
60°C	1.2729	0.3395	0.00016	0.000292
80°C	1.3094	0.4003	0.00017	0.000352
PDP (E-15)J				
20°C	0.00468	0.001	0.004	0.001306
40°C	0.00482	0.00126	0.00422	0.001848
60°C	0.00490	0.00145	0.0045	0.003932
80°C	0.00496	0.00171	0.0047	0.016595
		TNOR		
Power (E-6)W				
20°C	2.669	0.542	0.000321	0.000199
40°C	2.763	0.6581	0.00052	0.000275
60°C	2.858	0.7732	0.00075	0.000726
80°C	2.952	0.8891	0.00089	0.00135
PDP (E-15)J				
20°C	0.1035	0.022	0.00963	0.000128
40°C	0.1978	0.0532	0.0177	0.000149
60°C	0.4059	0.0981	0.0286	0.000248
80°C	2.221	0.1418	0.0365	0.000262

the demand of high frequency operation for electronic devices has grown significantly over time. Therefore, to measure the sensitivity of the proposed ternary logic gates to frequency variation of the input patterns, the frequency is swept from 3MHZ to 300MHZ. According to the simulation results depicted in Fig. 21 (c) and Fig. 21 (d), the effect of frequency variation on the power consumption of the designs is negligible, however the increment of frequency causes slight increase in the power delay product (PDP) of the proposed ternary logic gates.

Finally, a comparative analysis is carried out to investigate the effect of variation of the load capacitance, temperature and supply voltage on the power consumption and energy consumption (PDP) of the proposed CNTFET-RRAM based STI, TNAND and TNOR logic gates with the existing designs in the literature. Firstly, the performance metrics of the proposed STI, TNAND and TNOR are examined against numerous load capacitances. Since the drivability of the basic gates is different for diverse structures, thus appropriate operation over varying load capacitances is vital for the design of basic ternary logic gates. Table 15 demonstrates the power consumption and the PDP values for the STI, TNAND and TNOR logic gates respectively. From the simulation results we can infer that the performance metrics of the proposed STI, TNAND and TNOR outperforms the designs of ternary logic gates presented in [7], [34] and [38] in all the conditions for varying the capacitances. Next, the performance metrics of the proposed basic ternary logic gates is evaluated under various supply voltages and compared to the various families of designs previously proposed. Proper operation

TABLE 17. Power consumption and PDP of STI, TNAND and TNOR in various families for different supply voltage.

Voltage	[7]	[34]	[38]	Proposed
		STI		
Power (E-6)W				
0.8V	0.75	0.15	0.6385	0.00012
0.9V	1.1310	0.4319	0.6908	0.000148
1V	1.98	0.5	0.8008	0.00016
PDP (E-15)J				
0.8V	0.0375	0.0009	0.00056	0.00085
0.9V	0.0197	0.00674	0.00068	0.000049
1V	0.075	0.02	0.00008	0.0008
		TNAND		
POWER (E-6)W				
0.8V	0.653	0.2151	0.000132	0.000075
0.9V	0.707	0.3446	0.00014	0.000101
1V	1.7	0.5231	0.00016	0.00012
PDP (E-15)J				
0.8V	0.0341	0.0.31	0.0039	0.000036
0.9V	0.0189	0.0068	0.0042	0.00184
1V	0.0676	0.0206	0.0045	.00564
		TNOR		
Power (E-6)W				
0.8V	1.3	0.312	0.00029	0.000246
0.9V	0.7359	0.3240	0.00031	0.000275
1V	4.151	0.9921	0.0004	0.000312
PDP (E-15)J				
0.8V	0.0679	0.0186	0.00818	0.00072
0.9V	0.01775	0.0055	0.00979	0.00014
1V	2.221	0.0417	0.014	0.0011

over various voltage supply is required in such systems with power aware architecture. Table 16 demonstrates the power consumption and the PDP values for the STI, TNAND and TNOR logic gates respectively.The simulation results in this experiment indicate that the performance metric of the proposed design outperforms the designs of ternary logic gates proposed previously in [7], [34] and [38] in all the conditions for every gates. Lastly, the simulations of the proposed ternary gates are carried out and the performance metrics of the considered families against a vast range temperature is investigated. Table 17 demonstrates the power consumption and the PDP values for the proposed STI, TNAND and TNOR logic gates respectively. From the simulation results we can infer that the performance metrics of the proposed STI, TNAND and TNOR outperforms the designs of ternary logic gates presented in [7], [34] and [38] in most of the scenarios for variation of operating temperature. Therefore, the proposed designs are robust against a wide range of variations.

VI. CONCLUSION

With the advent of emerging technologies, the realization of ternary computing structures is more than ever possible and a significant amount of research around these subjects have been done in recent years. This paper presents the simple and efficient methodology for design of ternary logic systems based on CNTFETs and RRAM which is a promising alternative to the conventional binary logic design. CNTFET-RRAM logic gates such as STI, ternary NAND and ternary NOR gates have been implemented using HSPICE software and the simulation results confirm the proper functionality and authenticity of the proposed designs. Compared to the existing designs, the proposed ternary gogic gates (STI,TNAND and TNOR) are superior in terms of the power and the energy consumption, in addition to having the reduced transistor count compared to the existing designs. Thus, from the obtained results, we can infer that the proposed design approach is a practical and efficient solution to reduce hardware complexity, number of components, power consumption, energy consumption and cost of the design. Also, ternary half adder, ternary half subtractor and ternary multiplier arithmetic circuits have been implemented using the proposed basic ternary gates to check the effectiveness of the proposed designs. The Monte-Carlo simulation analysis to consider the effects of process variations on the proposed designs have been conducted. The proposed basic ternary logic gates are compared to the various existing families of ternary designs, simulated under various operating conditions with different load capacitances, different operating temperatures and different supply voltages. The results confirm the higher robustness among other designs. Therefore, the proposed circuits can be implemented in applications involving low-power electronics and embedded systems to preserve battery consumption.

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