Investigation of Negative Bias Temperature Instability Effect in Partially Depleted SOI pMOSFET

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ABSTRACT The negative bias temperature instability (NBTI) mechanisms for Core and input/output (I/O) devices from a 130 nm partially-depleted silicon on insulator (PDSOI) technology are investigated. The I/O device degrades more than the Core device under the same stress electric field due to the different gate oxide processes in these two types of devices. Both the oxide trap charge and interface trap lead to the transfer characteristics degradations of the device after NBTI. While the near interfacial traps result in the increase of low frequency noise (LFN). The trap densities near the silicon/gate oxide interface introduced by stress are extracted using the LFN method. NBTI-induced gate current increase is observed for Core device, but not for I/O device. It is result from the enhanced tunneling process, which is induced by the increase of electric field in the gate oxide after charge trapping at or near the channel interface. The gate width and length dependences of NBTI are observed. The enhanced NBTI degradation observed in short channel and narrow channel device is result from the enhanced NBTI effect at channel edge regions. The larger hole concentration is a main cause of the more serious NBTI degradation at the channel edge regions, including the nearby region of STI sidewall along the channel width direction and the gate edge region along the channel length direction. This conclusion is also verified by the TCAD simulations.

INDEX TERMS Low frequency noise, negative bias temperature instability, silicon on insulator, TCAD simulation.

I. INTRODUCTION

Negative bias temperature instability (NBTI) is a major reliability concern for modern CMOS technologies [1]–[3]. It is mainly manifested as the threshold voltage shift, transconductance decrease, saturate current decrease and subthreshold swing increase of the pMOSFET due to the trap charge generated in the gate oxide. The degradations of these parameters may lead to mismatching of high-precision transistor pairs in analog circuits, timing problems and even logic errors in digital logic, reducing of the driving capability and response speed of the drive circuit [4]. As scaling, NBTI is significantly enhanced due to the fact that the gate oxide thickness scales

faster than the power supply voltage, which results in an increasing oxide electric field [5]. The nitride oxide or high-k gate dielectric introduced to reduce gate leakage current has worse hole trapping characteristics than the conventional SiO_2 dielectric layer [6]. These process variations may also change the degradation mechanisms of NBTI. In the past, NBTI degradation is dominated by an increase in the SiO_2/Si interface traps, which origins from the releasing of hydrogen. However, bulk traps have dominated NBTI degradation in sub-1 nm effective oxide thickness (EOT) devices in recent years due to hole trapping [7].

Recently, silicon-on-insulator (SOI) technology has generated great interest because of its major advantages over its bulk counterpart including their latch-up immunity, high speed and density thanks to the complete dielectric isolation

TABLE 1. Two kinds of devices in the 130 nm PDSOI technology.

| Device	Body doping concentration	Operating voltage	Gate oxide thickness	width-length-ratios (W/L)
Core	$\sim 10^{18}$ cm^{-3}	1.2 V	~ 1.8 nm	10µm/0.13µm 0.15µm/0.13µm 10µm/10µm
I/O	$\sim 10^{17}$ cm^{-3}	3.3 V	~ 6.8 nm	10µm/0.3µm

of transistors [8], [9]. Whereas, NBTI reliability research of SOI technology is not as extensive as bulk technology [10], [11]. Moreover, it is generally believed that NBTI is only related to the electric field perpendicular to the channel of MOSFETs, and does not depend on the transverse electric field along the channel direction [1]. So it should not exhibit the gate length and width dependence. However, some researchers have shown that NBTI is enhanced by the decrease of the channel length [12], while some works reported the NBTI degradations decrease with decreasing channel length [13]. Furthermore, the influences of gate width on NBTI is also a controversial issue. The previous works have reported the opposite correlation between channel width of NBTI [14], [15].

In this paper, the NBTI-induced transfer characteristics and gate current degradations and their mechanisms are investigated for a 130 nm partially-depleted (PD) SOI technology. One of our main purposes is to verify the gate length and width dependences of NBTI effects in pMOSFET by experiments and TCAD simulations. Furthermore, the different degradation characteristics of Core logic and input/output (I/O) devices with different gate oxide processes are reported. Low frequency noise is proved to be sensitive to the NBTI-induced oxide traps and is an effective way to extract the trap state.

II. EXPERIMENTAL DETAILS

All the devices used in our experiment were fabricated on a 200 mm diameter UNIBOND®wafer from SOITEC with the top Si film of 100 nm and the buried oxide thickness of 145 nm by a 130 nm PDSOI technology. The Core devices and I/O devices are selected as samples in our experiment and the descriptions for these two kinds of devices are shown in Tab. 1. The gate oxide of Core device is formation in NO at 750°C to a thickness of $\sim$1.8 nm. The gate oxide of I/O device is formation in wet O$_2$ at 800°C to a thickness of $\sim$6.8 nm. All devices have 130 nm thick poly-silicon gates and 65 nm wide spacers. The shallow trench isolation (STI) which connects with the buried oxide (BOX) at the bottom is introduced for field isolation. T-shape gate is used for body contact to suppress the floating-body effect, as shown in Fig. 1.

The NBTI stress experiments were conducted by Agilent B1500 semiconductor parameter analyzer [16] using the voltage step stress (VSS) technique [17]. A step-like V_g waveform used for VSS technique in BTI tests is shown in Fig. 2. The device was stressed at $V_{gst} = V_{gst}(1)$ for a pre-specified time $\Delta t = 1000$ s and then $|V_{gst}|$ was 'stepped up' to $V_{gst}(2) = V_{gst}(1) + \Delta V_{gst}$ for stressing another Δt.
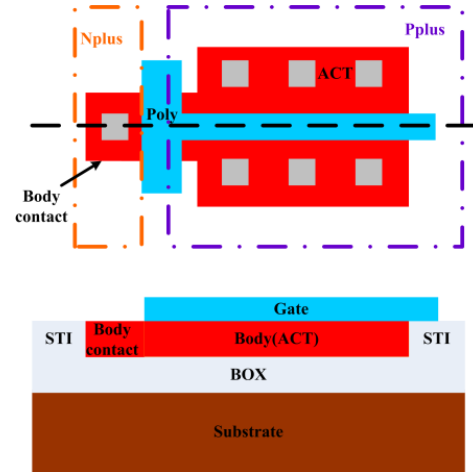
FIGURE 1. Layout and cross-section diagram of pMOS transistor used in our study.
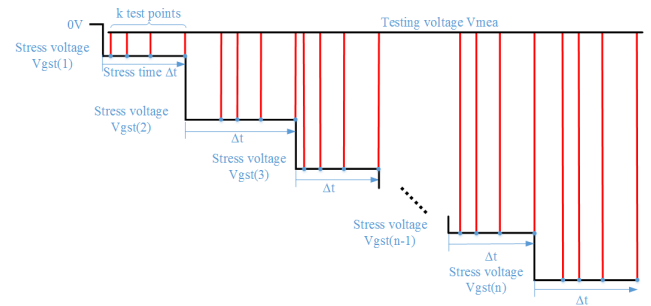
FIGURE 2. Step-like V_g waveform used for VSS technique in NBTI tests.

ΔV_{gst} keeps constant during n steps. This procedure will continue until reaching the pre-set maximum stress voltage $V_{gst}(n)$. The threshold voltage (V_{th}) was measured at pre-defined intervals during each stress step. To minimize the relaxation that could occur between stress and measurement phase, on-the-fly (OTF) method of V_{th} measurement was applied instead of extracting V_{th} through the complete $I_d - V_g$ curve [18], [19]. An intermittent drain current I_d sensing at $V_g = V_{mea}$ is monitored in a preset log-incremental stress time from 5 s to 1000 s to capture the degradation ΔI_d. ΔV_{th} is evaluated by projecting ΔI_d to the fresh transfer characteristics curves. The duration of measurement window for the OTF test is 1 ms [20]. The V_{gst} to be applied on the Core pMOS are from $V_{gst}(1) = -2.1$ V to $V_{gst}(n) = -3.9$ V with $\Delta V_{gst} = -0.3$ V. The V_{gst} to be applied on the I/O pMOS are from $V_{gst}(1) = -4.5$ V to $V_{gst}(n) = -7.5$ V with $\Delta V_{gst} = -0.5$ V. Drain is biased at 0 V during stress phase and $V_d = 0.1$ V during the drain current sensing phase to exclude the self-heating effect and avoid generation of new defects. All the stresses and measurements were performed at T = 30 °C. Since the temperature is not enough high as the usual NBTI experiment, so the obtained effects can be considered as negative bias instability. A complete $I_d - V_g$ curve was measured before and after the stress.

The low frequency noise (LFN) tests were carried out at room temperature before and after NBTI stress. The noise
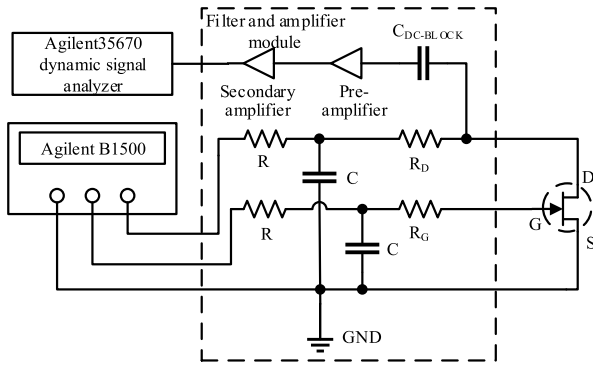
FIGURE 3. Low frequency noise testing system used in this study.

test system mainly consists of Agilent B1500 semiconductor parameter analyzer, Agilent 35670 dynamic signal analyzer, and the filtering and amplification module, as shown in Fig. 3. As a low-noise amplifier, the filter and amplifier module amplifies the small current fluctuation, i.e. current noise. The amplified noise signal is input to Agilent 35670 for spectrum transformation to obtain the current noise power density spectrum.

III. RESULTS ANS DISCUSSIONS
A. DEGRADATION OF I-V CHARACTERISTIC

Fig. 4 (a) shows the transfer characteristics $I_d - V_g$ and transconductance characteristics of a Core pMOS with $W/L = 10$ μm/0.13 μm before and after NBTI stress. Significant negative shift of threshold voltage is observed after stress. The threshold voltages of the MOSFETs are defined as a critical gate voltage, at which the drain current reaches $|(W/L) \times 10^{-7}|$ A in our study. The extracted threshold voltage shift is -116 mV after stress. This response indicates the build-up of the trapped charge in the gate oxide. Since both the oxide trapped charge and the interface traps are positively charged in gate oxide for a pMOS, they contribute to the negative shift of the threshold voltage ΔV_{th}, i.e.

$$\Delta V_{th} = \frac{-q(\Delta N_{ot} + \Delta N_{it})}{C_{ox}} = \frac{-q(\Delta N_{ot} + \Delta N_{it})t_{ox}}{\varepsilon_{ox}} \quad (1)$$

where q is the electron charge, C_{ox} is the gate oxide capacitance per unit area, t_{ox} is the gate oxide thickness, ε_{ox} is the permittivity of the oxide, ΔN_{ot} and ΔN_{it} are the densities of the stress-induced oxide trapped charge and interface traps in the gate oxide, respectively.

Using the method introduced in [21] and combined with (1), ΔN_{it} and ΔN_{ot} can be extracted: $\Delta N_{it} = 1.19 \times 10^{11}$ cm^{-2}, $\Delta N_{ot} = 1.13 \times 10^{12}$ cm^{-2} for Core pMOS after stress. As shown in Fig. 4 (a), the peak value of g_m is 850 μS pre-stress. g_m suffers a noticeable decrease after NBTI stress and the peak value become about 725 μS. This substantial degradation (~14.7%) of the transconductance peak implies the influence of the interface traps or the oxide trapped charges that act like interface traps. The effective Coulombic scattering of the interface traps results in the
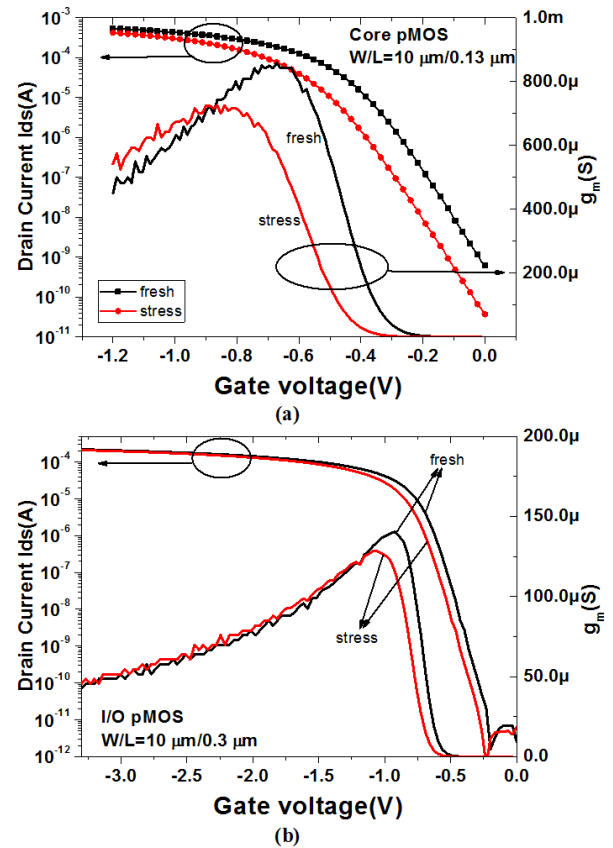

FIGURE 4. (a) Transfer and transconductance characteristics of (a) Core and (b) I/O pMOS before and after NBTI stress. Test condition: $V_{drain} = -0.1V$, $V_{source} = V_{body} = V_{bg} = 0$ V.

degradation of the carrier mobility [22], [23]. It is then depicted as the decrease of the transconductance g_m, since g_m is proportional to the mobility at the linear region. The generation of interface traps also causes an increase of the sub-threshold slope from 81.1 mV/dec to 85.3 mV/dec. A -80.6 mV negative shift of threshold voltage and 8.4% g_m peak degradation are observed for I/O pMOS after stress, as shown in Fig. 4 (b). The sub-threshold slope is increased from 82.4 mV/dec to 84.6 mV/dec. The trap densities can also be extracted: $\Delta N_{it} = 6.53 \times 10^{10}$ cm^{-2}, $\Delta N_{ot} = 1.90 \times 10^{11}$ cm^{-2} for I/O pMOS after stress.

The I/O device shows a larger threshold voltage shift than Core device during stress process, even the equivalent stress electric field in gate oxide is smaller, as shown in Fig. 5. At the stress end, the observed threshold voltage shifts are -178 mV and -224 mV for Core and I/O devices, respectively. NBTI degradation can recover very fast when stress voltage is removed. 34.8% and 64.3% recoveries occur for Core and I/O devices respectively, as soon as the stress voltage is removed. The observed smaller I-V degradations and trap densities for I/O device after stress in Fig. 4 are results from more recovery in I/O device. To compared the degradations of Core and I/O device after the same equivalent electric field stress, the Core device has been stressed from $V_{gst}(1) = -1.3$ V to
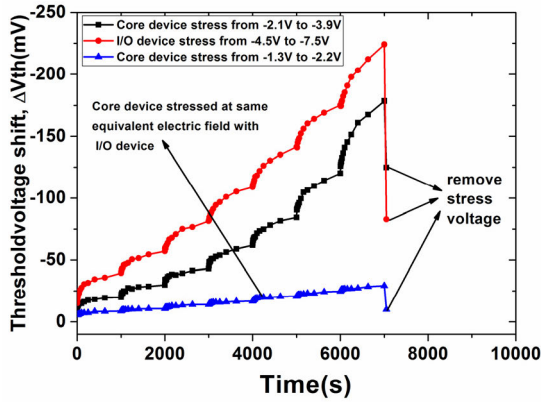
FIGURE 5. Recovery of threshold voltage after removing stress voltage for the Core and I/O pMOS.
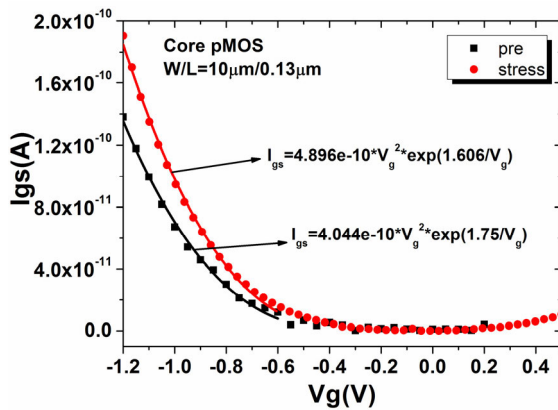

FIGURE 6. Gate current as a function of gate voltage for the Core pMOS before and after NBTI. The solid lines are the gate currents fitted by tunneling mechanism before and after NBTI.

$V_{gst}(n) = -2.2$ V. Obviously, the observed threshold voltage shifts are much smaller than I/O device at this time. The threshold voltage shift is -29.3 mV at stress end and -10.0 mV ($\sim$65.9% recovery) after removing the stress. It seems that the recovery is mainly related to the effective stress electric field in the gate oxide.

Fig. 6 shows the gate current as a function of gate voltage for the Core pMOS before and after NBTI. The gate current from $V_g = -0.6$ V to $V_g = -1.2$ V can be fitted by,

$$Ig = AV_g^2 \exp(\frac{B}{V_g}) \qquad (2)$$

which is the voltage dependence of tunneling conduction process in oxide. So the gate current is confirmed as direct tunneling mechanism before and after NBTI. Then the tunneling current density is expressed as [24]:

$$J \propto E_{ox}^2 \exp[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E_{ox}}] \qquad (3)$$

where E_{ox} is the electric field in the gate oxide, m^* is effective mass, φ_B is tunneling barrier height. The tunneling current is proportional to E_{ox}^2. According to the Gauss's Law, the

effective electric field after NBTI in the gate oxide can be calculated by:

$$E_{ox} = E_{Si}\frac{\varepsilon_{Si}}{\varepsilon_{ox}} + \frac{q(\Delta N_{it} + \Delta N_{ot})}{\varepsilon_{ox}} \approx \frac{|V_{gt}| - \Delta V_{FB}}{t_{ox}} \qquad (4)$$

where E_{Si} is the electric fields in the silicon, ε_{ox} and ε_{Si} are the oxide and silicon permittivities respectively, ΔN_{ot} and ΔN_{it} are the NBTI-induced oxide charge density, $V_{gt} = V_g - V_{th}$ is the overdrive voltage before stress, the flat-band voltage shift $\Delta V_{FB} = \Delta V_{th}$ is negative. Note that E_{ox} becomes larger with positive charge trapping after NBTI. The effective electric field in the gate oxide at $V_g = -1.2$ V can be approximately calculated to be 4.2 MV/cm and 4.9 MV/cm before and after NBT stress, respectively. An increase in E_{ox} produces a larger tunneling current according to (3). This can explain the observed increase of gate current in the range of $V_g = -1.2$ V ~ -0.6 V after NBTI, as shown in Fig. 6. No gate current increase is observed after stress for the I/O pMOS due to the large gate oxide thickness.

B. DEGRADATION OF LOW-FREQUENCY CHARACTERISTIC
LFN is closely related to the quality near the Si/SiO$_2$ interface in semiconductor devices, which can be used as an effective tool to evaluate the reliability of semiconductor devices [25], [26]. To analyze the trap characteristics near the oxide/silicon interface after NBTI, the LFN spectra at linear region under various gate bias voltages are measured. The normalized drain current power spectral density as a function of frequency for the Core and I/O pMOS are shown in Fig. 7 and Fig. 8. The normalized S_{Id}/Id^2 varies with frequency according to a $1/f$ law within the range from 1 Hz to 1 kHz for both Core and I/O pMOS before and after stress. The LFN is slightly increased after NBTI.

The normalized drain current power spectral density taken at 1 Hz is plotted in Fig. 9 versus the drain current for Core and I/O pMOS before and after stress. There is a good correlation between S_{Id}/Id^2 and $(g_m/I_d)^2$ characteristics, which indicates that the front gate noise can be modeled by the carrier number fluctuation (ΔN) model [27], [28] based on trapping and de-trapping of charge in traps near the channel interface. Then S_{Id}/Id^2 can be expressed as,

$$\frac{S_{Id}}{I_d^2} = (\frac{g_m}{I_d})^2 S_{Vfb} \qquad (5)$$

$$S_{Vfb} = \frac{q^2 kT \lambda N_t}{WLfC_{ox}^2} \qquad (6)$$

where S_{Vfb} is the flat-band voltage noise power spectral density, N_t is the trap density near front channel interface, g_m is the transconductance, k is Boltzmann constant, T is temperature, λ is tunneling attenuation coefficient ($\sim$0.1 nm for SiO$_2$), C_{ox} is the gate capacitance per unit area, W and L are the gate width and length, respectively. By fitting $(g_m/I_d)^2$ to S_{Id}/Id^2, S_{Vfb} are extracted to be 4.75×10^{-10} V^2/Hz and 1.24×10^{-9} V^2/Hz for I/O pMOS before and after stress. According to (6), the trap densities N_t for I/O pMOS before and after stress are calculated to be 5.20×10^{17} eV^{-1}cm^{-3}
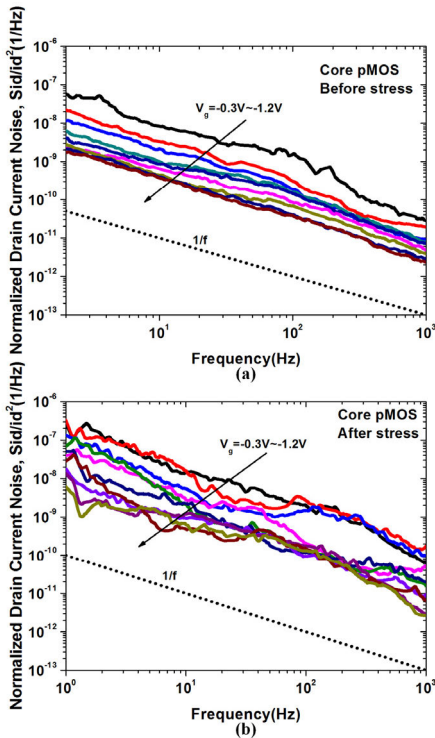
FIGURE 7. Normalized drain current noise power spectral density as a function of frequency for the Core pMOS before and after stress.
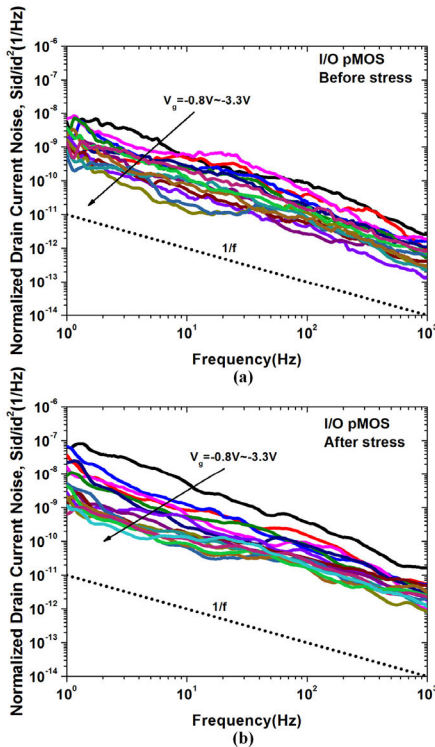

FIGURE 8. Normalized drain current noise power spectral density as a function of frequency for the I/O pMOS before and after stress.

and 1.36×10^{18} eV^{-1}cm^{-3}, respectively. Similarly, the trap densities at the front gate of the Core pMOS before and after stress are 2.16×10^{18} eV^{-1}cm^{-3} and 9.87×10^{18} eV^{-1}cm^{-3}, respectively.
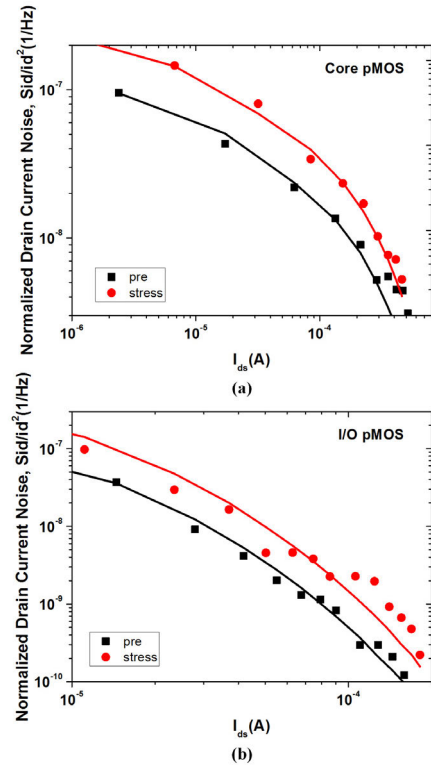

FIGURE 9. Normalized drain current power spectral density taken at 1 Hz versus drain current for (a) Core and (b) I/O pMOS before and after NBTI stress. The scatter is S_{Id}/I_d^2 and the solid line is $S_{Vfb} \times (g_m/I_d)^2$.

The trap density N_t obtained from noise measurements can be converted to the effective sheet charge density of the oxide trapped charge via [29]

$$\Delta N_{ot}(noise) = \int_0^{t_{ox}} \frac{\Delta N_t \cdot (\phi_n + \phi_p) \cdot x}{t_{ox}} dx \qquad (7)$$

where ϕ_n and ϕ_p are the bulk potential energy for nMOS and pMOS with identically processed oxides, $x = 0$ represents the polysilicon/oxide interface and x is the distance from polysilicon/oxide interface in the gate oxide. Low frequency noise is caused by the exchange of charge between the transistor channel and near-interfacial oxide traps (i.e. border trap) with much slower emission and capture times than interface traps in the frequency span range of LFN measurements. The noise power density at a particular frequency f should mainly come from the trapping events with an average time constant around l/f [30]. The relationship between time constant and the tunneling distance of the charge for the border traps can be expressed as [31],

$$\tau = \frac{1}{2\pi f} = \tau_0 \exp\left(\frac{d}{\lambda}\right) \qquad (8)$$

where τ_0 is the time constant of interface trap ($\sim 10^{-10}$ s), d is the distance away from the interface in the gate oxide. The frequency span range of LFN measurements is usually from 1 Hz to <1 MHz [32], then the spatial distribution of
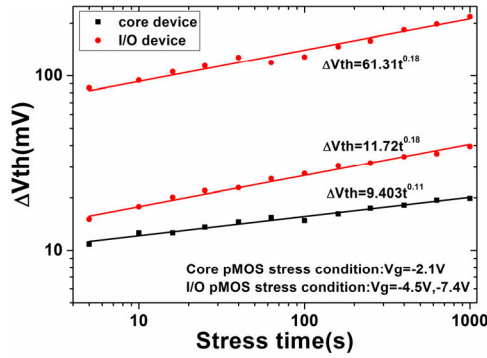
FIGURE 10. NBTI stress-induced threshold voltage shift as a function of stress time for Core and I/O pMOS. The threshold voltages are absolute values.
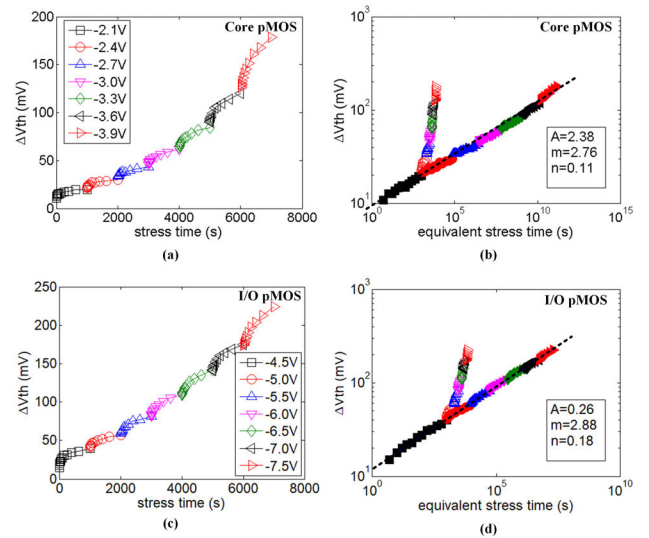

FIGURE 11. Measured results using VSS method for NBTI lifetime prediction in (a) Core and (c) I/O pMOS. Stress time under the increasing stress voltage is transformed with a chosen voltage exponent m for (b) Core and (d) I/O pMOS. Only when the correct m is used, they agree well with the power law predetermined in the first stress step.

oxide traps which are contribute to the low frequency noise (i.e. border traps) is $d = 0.7 \sim 2.1$ nm according to (8). φ_n and φ_p are calculated through TCAD simulations. For I/O device, $\varphi_n \approx 0.447$ eV and $\varphi_p \approx 0.421$ eV; for Core device, $\varphi_n \approx 0.464$ eV and $\varphi_p \approx 0.426$ eV. Suppose the border traps are uniformly distributed in region $d = 0.7 \sim 2.1$ nm, the NBTI stress-induced effective border trap densities can be estimated by LFN to be 2.31×10^{11} cm^{-2} and 8.09×10^{10} cm^{-2} from (7) for Core and I/O pMOS, respectively.

C. INFLUENCE OF GATE OXIDE PROCESS AND DEVICE DIMENSION ON NBTI EFFECTS

Fig. 10 shows NBTI stress-induced threshold voltage shift as a function of stress time for Core and I/O pMOS. The threshold voltage shifts in the figure are absolute values. The threshold voltage shifts vs. stress time follows a perfect time-power law of the form $|\Delta V_{th}| \sim t^n$. This is in agreement with the classic reaction/diffusion theory of the NBTI [33], according to which, the device parameter degradations observed under NBTI stress are the result of interface state and fixed charge generation. Whereas, the Core and I/O devices follow the different power law trends with exponent n values of 0.11 and 0.18, respectively. The I/O device shows a much larger threshold voltage than Core device under the same effective electric field stress, which is corresponding to Core device stressed at -2.1 V and I/O device stressed at -7.4 V.

NBTI degradation can be expressed by a power law against time and voltage [34]:

$$|\Delta V_{th}| = A \cdot V_{gt}^m \cdot t^n \qquad (9)$$

where ΔV_{th} is the threshold voltage shift (mV), A is a fitting parameter, $V_{gt} = V_g - V_{th}$ is the overdrive voltage (V), and m is voltage exponent. According to previous work [1], [35], $m > 1 > n$, which means that increasing stress voltage is more effective than increasing stress time in accelerating NBTI degradation. The ΔV_{th} produced by a higher stress voltage V_{high} in a short time t is equivalent to the degradation produced by another lower stress voltage V_{low} after a long

effective stress time t_{eff}, i.e.

$$A \cdot V_{high}^m \cdot t^n = A \cdot V_{low}^m \cdot t_{eff}^n \qquad (10)$$

$$t_{eff} = \left(\frac{V_{high}}{V_{low}}\right)^{m/n} \cdot t \qquad (11)$$

It is important to note that this is an approximate method, the NBTI degradation in a long time scale may be segmented [36].

Fig. 11 shows the measured results using the VSS method for NBTI lifetime prediction in Core and I/O pMOS. As the stress voltage increase, ΔV_{th} increases more sharply. According to (11), NBTI degradation under multiple gradually increasing stress voltages in VSS test can be equivalent to degradation under a single voltage stress in effective time. The time exponent n has been calculated by using the first stress step data, so the effective time in (11) is only related to m. By guessing different m values, the measured value of ΔV_{th} at increasing stress voltages will give different "effective time exponent" $n\prime$ of the power low. If and only if m value is the real value, $n\prime$ will be equal to the previous calculated time exponent n, as shown in Fig. 11 (b) and (d). The final extracted parameter values are: $A = 2.38$ and $m = 2.76$ for Core pMOS; $A = 0.26$ and $m = 2.88$ for I/O pMOS. Then Lifetime under nominal operating voltage can be predicted by setting the lifetime criterion as $|\Delta V_{th}| = 100$ mV, as shown in Fig. 12. Due to the different gate oxide thickness of Core and I/O pMOS, the lifetime is plotted as effective electric field in gate oxide. It can be seen that the NBTI lifetime of the I/O device is much lower than that of the Core device under the same electric field. This is related to their different gate oxide processes. It is also consistent with the previous conclusion that water in the oxide will enhance NBTI [37].
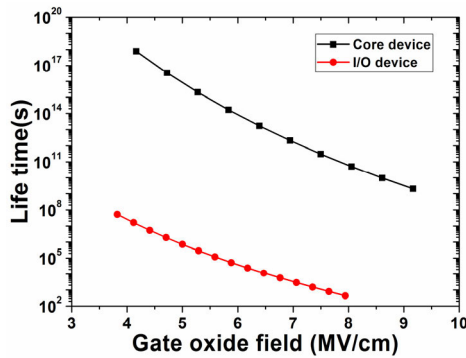
FIGURE 12. Life time as a function of effective gate oxide field for Core and I/O pMOS.
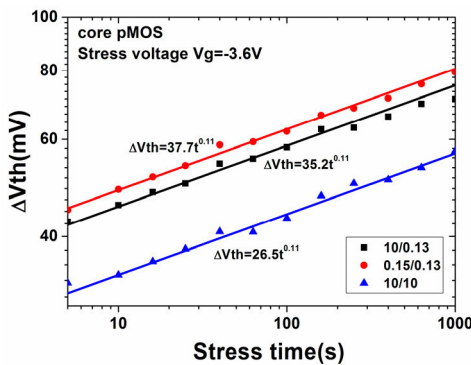

FIGURE 13. NBTI stress-induced threshold voltage shift as a function of stress time for Core pMOS with different dimensions. The threshold voltages are absolute values.
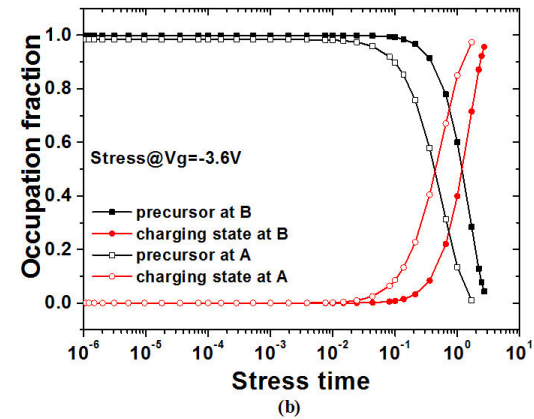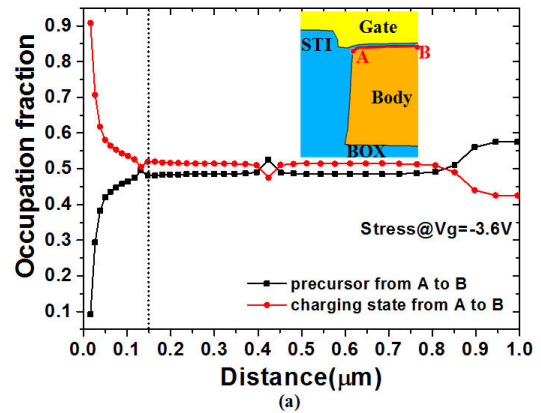

FIGURE 14. (a) Simulated occupation fraction of neutral oxygen vacancy precursors and charging states along the channel width direction of Core pMOS after stressed at $V_g = -3.6$ V for 1 s. (b) Simulated occupation fraction of neutral oxygen vacancy precursors and charging states as a function of time at STI corner region (position A) and the region far away from STI (position B).

Fig. 13 shows NBTI stress-induced threshold voltage shift as a function of stress time for Core pMOS with different dimensions. The devices with different sizes follow the same power law trends, but device with narrow channel and short channel show more significant threshold voltage shift under the same stress condition. It is interesting to note that the total ionizing dose effect of pMOSFET shows the same channel width dependence, which can be explained by the STI-related effect [38]. To verify these phenomena, TCAD simulations are conducted in this paper. The three-dimensional simulations are performed using the Sivaco's device simulator ATLAS. As discussed above, both the generation of positive oxide charges and interface traps in the gate oxide are observed after NBTI. So a two-stage NBTI degradation model [39] is added in the device simulation, which assumes that the NBTI degradation proceeds in a two-stage process. The first stage includes the activation of E' centers from their neutral oxygen vacancy precursors (Si-Si bond near the Si/SiO$_2$ interface) by trapping holes, the charging and discharging of E' centers by exchanging holes with the channel, and the total annealing of E' centers to neutral oxygen vacancy precursors. The second stage considers the activation of poorly recoverable P_b centers (dangling bonds at silicon-oxide interfaces).

The simulated occupation fraction of neutral oxygen vacancy precursors and charging states along the channel width direction of Core pMOS after stressed at $V_g = -3.6$ V are shown in Fig. 14 (a). It can be found that nearly 90% of the neutral oxygen vacancy precursors are transferred into charging state at the STI corner region (position A). While only 42% of the vacancy precursors are activated at the region far away from STI (position B) after the same stress time. The charging state numbers within 0.15 μm from position A is higher than that beyond this region. It implies that the NBTI degradation in the region near STI field oxide is worse than that at the middle region of the Core pMOS under the same stress condition, as shown in Fig. 14 (b).

The enhanced NBTI can be explained by the higher hole concentration near the STI sidewall, as shown in Fig. 15. The hole concentration in the channel at the transition region of gate oxide to STI oxide (position A) is one order of magnitude larger than that at the region far away from STI sidewall (position B). The oxidation-enhanced-diffusion (OED) of phosphorus dopants during the STI liner oxidation lead to the decrease of body doping concentration near STI sidewall. Simultaneously, the non-ideal transition from gate oxide to STI filled oxide can enhance the electric field at the STI corner. All these effects contribute the increase of hole concentration at the channel near STI sidewall, when the gate is biased.
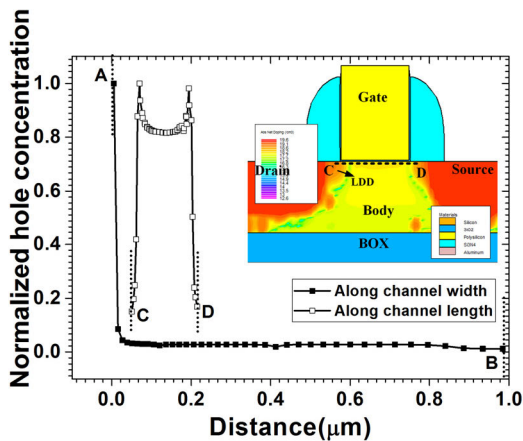
FIGURE 15. Simulated hole concentration in the channel near the gate oxide/body interface along the channel width and channel length direction. The hole concentration is normalized to the maximum value.

Similarly, the channel hole concentration at the gate edge (position C and D) is larger than that at the middle of the channel, which is related to the lightly doped drain (LDD) reducing the net body doping concentration at the overlap region of gate and LDD. Furthermore, more trap states are reported at the gate edge region and STI sidewall region due to low-quality oxide/body interface [14]. The larger hole concentration and trap state density lead to the more serious NBTI degradation at the channel edge regions, including the nearby region of STI sidewall along the channel width direction and the gate edge region along the channel length direction. The enhanced NBTI effect at channel edge regions will increase the degradation of the whole device for 10 μm/0.13 μm and 0.15 μm/0.13 μm device, since the edge regions have the similar dimension with the channel length and width. But it has little influence on the 10 μm/10 μm device due to the large channel length and width. So the minimal degradation is observed in the 10 μm/10 μm device after NBTI.

IV. CONCLUSION

In this work, the NBTI effects of Core and I/O pMOS from a 130 nm PDSOI technology are investigated. Significant negative threshold voltage shifts and transconductance reductions are observed for Core pMOS after NBTI stress, which is result from the generation of trapped charges and interface traps in the gate oxide. The trapped charges at or near the interface can enhance the direct tunneling process in the gate oxide of Core device and lead to the increase of gate current after stress. No gate current increase is observed for I/O device due to the large thickness of gate oxide, where tunneling does not happen. The wet oxidation of gate oxide in I/O pMOS will enhance the NBTI degradations, which is manifested as the lower NBTI lifetime of I/O pMOS at the same effective electric field compared with Core device. The increase of low frequency noise is also observed after NBTI. Using the LFN method, the near interfacial trap densities introduced by stress are extracted to

be 7.71×10^{18} eV^{-1}cm^{-3} and 8.40×10^{17} eV^{-1}cm^{-3} for Core and I/O pMOS, respectively.

A gate length and width dependences of NBTI degradation are observed for the PDSOI pMOSFET. The enhanced NBTI degradations observed in short channel and narrow channel devices are result from the enhanced NBTI effect at channel edge regions. The increase of hole concentration at the channel near STI sidewall and the gate edge are confirmed by TCAD simulations. The larger hole concentration and trap state density lead to the more serious NBTI degradation at the nearby region of STI sidewall along the channel width direction and the gate edge region along the channel length direction.

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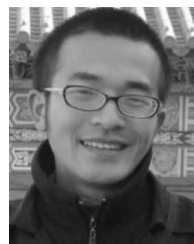
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